# 3-Pin Hotswap, Inrush Current Limiter Controllers (Negative Supply Rail)

## Features

- Pass element is only external part
- No sense resistor required
- Auto-adapt to pass element
- Short circuit protection
- UV & POR supervisory circuits
- 2.5s auto retry
- ±10V to ±72V input voltage range
- 0.6mA typical operating supply current
- Built in clamp for AC path turn-on glitch

## Applications

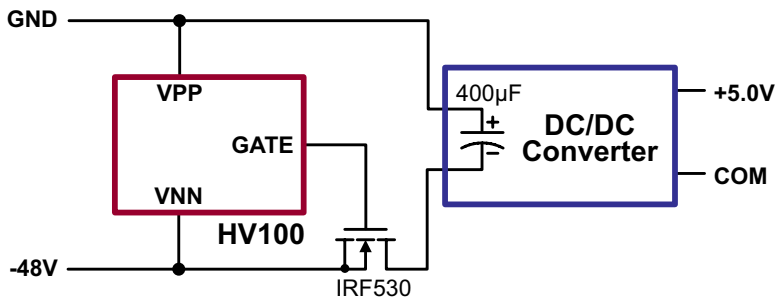
- -48V central office switching (line cards)
- +48V server networks
- +48V storage area networks
- +48V peripherals, routers, switches
- +24V cellular and fixed wireless (bay stations, line cards)
- +24V industrial systems
- +24V UPS systems
- -48V PBX & ADSL systems (line cards)
- Distributed power systems
- Powered ethernet for VoIP

## General Description

The HV100 is a 3-pin hotswap controller available in the SOT-223 package, which requires no external components other than a pass element.

The HV100 contains many of the features found in hotswap controllers with 8 pins or more, and which generally require many external components. These features include undervoltage (UV) detection circuits, power on reset (POR) supervisory circuits, inrush current limiting, short circuit protection, and auto-retry. In addition, the HV100 uses a patent pending mechanism to sample and adapt to any pass element, resulting in consistent hotswap profiles without any programming.

## Typical Application Circuit



## Ordering Information

| Part Number | Package Option | Packing |
|---|---|---|
| HV100K5-G | 3-Lead SOT-223 | 2500/Reel |

*-G denotes a lead (Pb)-free / RoHS compliant package*

## Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| $V_{PP}$ Input voltage | -0.3V to 75.0V |
| Operating ambient temperature range | -40°C to +85°C |
| Operating junction temperature range | -40°C to +125°C |
| Storage temperature range | -65°C to +150°C |

*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

## Typical Thermal Resistance

| Package | $\theta_{ja}$ |
|---|---|
| 3-Lead SOT-223 | 106°C/W |

## Pin Configuration


**3-Lead SOT-223**

## Pin Description

| Pin | Function |
|---|---|
| VPP | Positive voltage power supply to the circuit. |
| VNN | Negative voltage power supply to the circuit. |
| GATE | GATE driver output for the external N-channel MOSFET |

## Product Marking


Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
——— = "Green" Packaging

*Package may or may not include the following marks: Si or*

**3-Lead SOT-223**

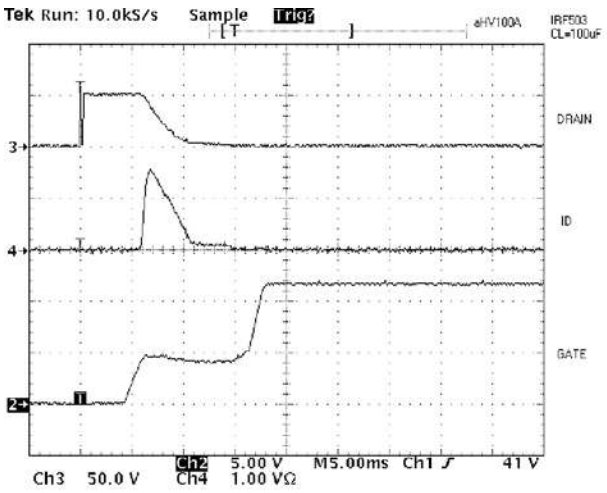
## DC Electrical Characteristics *(-40°C < $T_A$ < +85°C unless otherwise specified)*

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Supply** ***(Referenced to VPP pin)*** | | | | | | |
| $V_{NN}$ | Supply voltage | -72 | - | UV | V | --- |
| $I_{NN}$ | Supply current | - | 0.6 | 1.0 | mA | $V_{NN}$ = -48.0V |
| **UV Control** ***(Referenced to VNN pin)*** | | | | | | |
| $V_{UVL}$ | UV threshold (high to Low) | 30 | 34 | 38 | V | --- |
| $V_{UVH}$ | UV hysteresis | - | 3.0 | - | V | --- |
| **Gate Drive Output** ***(Referenced to VNN pin)*** | | | | | | |
| $V_{GATE}$ | Maximum GATE drive voltage | 10 | 12 | 14 | V | --- |
| $SR_{GATE}$ | Initial slew rate | 1.50 | 2.50 | 3.25 | V/ms | $C_{GATE}$ = 1.0nF |
| $I_{GATEDOWN}$ | GATE drive pull-down current (sinking) | 8.0 | 16 | - | mA | $V_{GATE}$ = 1.0V; $V_{PP}$ = 11.5V |
| $I_{PULLUP}$ | Post hotswap pull-up current | 6.0 | 11 | - | µA | $V_{GATE}$ = 6.0V |
| **Timing Control** ***(Referenced to VNN pin)*** | | | | | | |
| $t_{POR}$ | Insertion POR delay | 1.5 | 3.5 | 5.5 | ms | --- |
| $t_{ARD}$ | Auto restart delay | 1.25 | 2.50 | 3.75 | s | --- |

## DC Electrical Characteristics *(cont.)*

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Example Electrical Results *(Using IRF530)*** | | | | | | |
| $I_{LIM}$ | Max inrush current during hotswap | - | 1.4 | - | A | IRF530 external MOSFET, $C_{LOAD}$ = 100µF |
| $I_{LIM}$ | Max inrush current during hotswap | - | 2.5 | - | A | IRF530 external MOSFET, $C_{LOAD}$ = 200µF |
| $I_{LIM}$ | Max inrush current during hotswap | - | 3.1 | - | A | IRF530 external MOSFET, $C_{LOAD}$ = 300µF |
| $I_{SHORT}$ | Max current Into a short | - | 4.0 | - | A | IRF530 external MOSFET, $R_{LOAD}$ = <<1.0 |
| $t_{SHORT}$ | Shorted load detect time | - | 1.0 | | ms | IRF530 external MOSFET, $R_{LOAD}$ = <<1.0 |
| $\Delta_{GATE}$ | Initial rate of rise of GATE | - | 2.5 | - | V/ms | IRF530 external MOSFET, any $C_{LOAD}$ |
| $t_{HS}$ | Hotswap period to full GATE value | - | 12.5 | - | ms | IRF530 external MOSFET, any $C_{LOAD}$ |

## Typical Waveforms



# Functional Description

## Insertion into Hot Backplanes

Telecom, data network and some computer applications require the ability to insert and remove circuit cards from systems without powering down the entire system. Since all circuit cards have some filter capacitance on the power rails, which is especially true in circuit cards or network terminal equipment utilizing distributed power systems, the insertion can result in high inrush currents that can cause damage to connector and circuit cards and may result in unacceptable disturbances on the system backplane power rails.

The HV100 is designed to facilitate the insertion and removal of these circuit cards or connection of terminal equipment by eliminating these inrush currents and powering up these circuits in a controlled manner after full connector insertion has been achieved. The HV100 is intended to provide this control function on the negative supply rail.

## Description of Operation

On initial power application the high input voltage internal regulator seeks to provide a regulated supply for the internal circuitry. Until the proper internal voltage is achieved all circuits are held reset by the internal UVLO and the GATE to source voltage of the external N-channel MOSFET is held off. Once the internal regulator voltage exceeds the UVLO threshold, the input undervoltage detection circuit (UV) senses the input voltage to confirm that it is above the internally programmed threshold. If at any time the input voltage falls below the UV threshold, all internal circuitry is reset and the GATE output is pulled down to $V_{NN}$. UVLO detection works in conjunction with a power on reset (POR) timer of approximately 3.5ms to overcome contact bounce. Once the UVLO is satisfied, the GATE is held to $V_{NN}$ until a POR timer expires. Should the UV monitor toggle before the POR timer expires, the POR timer will be reset. This process will be repeated each time UVLO is satisfied until a full POR period has been achieved.

After completion of a full POR period, the MOSFET GATE auto-adapt operation begins. A reference current source is turned on which begins to charge an internal capacitor generating a ramp voltage which rises at a slew rate of 2.5V/ms. This reference slew rate is used by a closed loop system to generate a GATE output current to drive the GATE of the external N-channel MOSFET with a slew rate that matches the reference slew rate. Before the GATE crosses a reference voltage, which is well below the $V_{TH}$ of industry standard MOSFETs, the pull-up current value is stored and the auto-adapt loop is opened. This stored pull-up current value is used to drive the GATE during the remainder of the hotswap period. The result is a normalization with $C_{ISS}$ , which for most MOSFETs scales with $C_{RSS}$.

The MOSFET GATE is charged with a current source until it reaches its turn on threshold and starts to charge the load capacitor. At this point the onset of the Miller Effect causes the effective capacitance looking into the GATE to rise, and the current source charging the GATE will have little effect on the GATE voltage. The GATE voltage remains essentially constant until the output capacitor is fully charged. At this point the voltage on the GATE of the MOSFET continues to rise to a voltage level that guarantees full turn on of the MOSFET. It will remain in the full on state until an input under voltage condition is detected.

If the circuit attempts turn on into a shorted load, then the Miller Effect will not occur. The GATE voltage will continue to rise essentially at the same rate as the reference ramp indicating that a short circuit exists. This is detected by the control circuit and results in turning off the MOSFET initiating a 2.5 second delay, after which a normal restart is attempted.

If at any time during the start up cycle or thereafter, the input voltage falls below the UV threshold the GATE output will be pulled down to $V_{NN}$, turning off the N-channel MOSFET and all internal circuitry is reset. A normal restart sequence will be initiated once the input voltage rises above the UVLO threshold plus hysteresis.

# Application Information

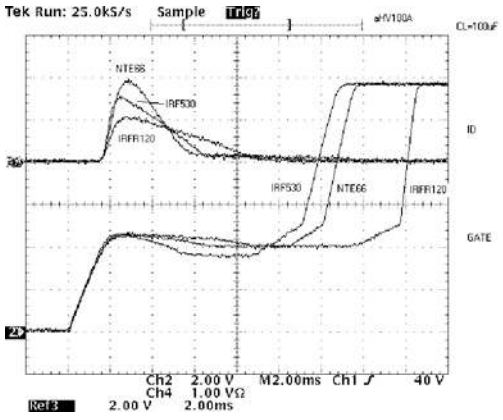
## Turn On Clamp

Hotswap controllers using a MOSFET as the pass element all include a capacitor divider from VPP to VNN through $C_{LOAD}$, $C_{RSS}$ and $C_{GS}$. In most competitive solutions a large external capacitor is added to the GATE of the pass element to limit the voltage on the GATE resulting from this divider. In those instances, if a GATE capacitor is not used the internal circuitry is not available to hold off the GATE, and therefore a fast rising voltage input will cause the pass element to turn on for a moment. This allows current spikes to pass through the MOSFET.

The HV100 includes a built-in clamp to ensure that this spurious current glitch does not occur. The built-in clamp will work for the time constants of most mechanical connectors. There may be applications, however, that have rise times that are much less than 1.0µs (100's of ns). In these instances it may be necessary to add a capacitor from the MOSFET GATE to source to clamp the GATE and suppress this current spike. In these cases the current spike generally contains very little energy and does not cause damage even if a capacitor is not used at the GATE.

## Auto-adapt Operation

The HV100 auto-adapt mechanism provides an important function. It normalizes the hotswap period regardless of pass element or load capacitor for consistent hotswap results. By doing this it allows the novel short circuit mechanism to work because the mechanism requires a known time base.

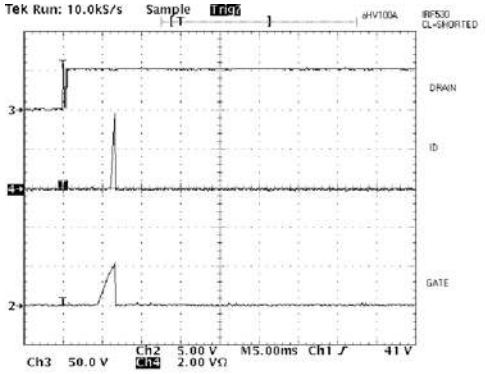



The above diagram illustrates the effectiveness of the auto-adapt mechanism. In this example three MOSFETs with different $C_{ISS}$ and $R_{DSON}$ values are used. The top waveform is the hotswap current, while the bottom waveform is the GATE voltage. As can be seen, the hotswap period is normalized, the initial slope of the GATE voltage is approximately 2.5V/ms regardless of the MOSFET, and the total hotswap period and peak currents are a function of a MOSFET type dependent constant multiplied by $C_{LOAD}$.

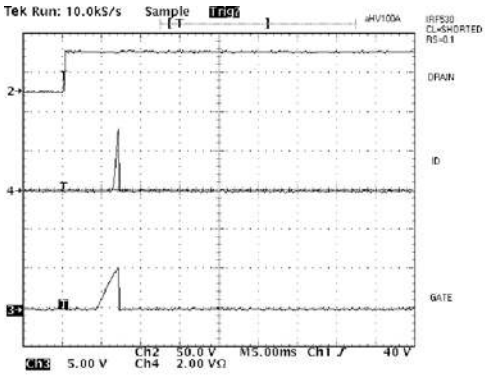
Typically if MOSFETs of the same type are used, the hotswap results will be extremely consistent. If different types are used they will usually exhibit minimal variation.

## Short Circuit Protection

The HV100 provides short circuit protection by shutting down if the Miller Effect associated with hotswap does not occur. Specifically, if the output is shorted then the GATE will rise without exhibiting a "flat response". Due to the fact that we have normalized the hotswap period for any pass element, a timer can be used to detect if the GATE voltage rises above a threshold within that time, indicating that a short exists. The diagram below shows a typical turn on sequence with the load shorted, resulting in a peak current of 4A.



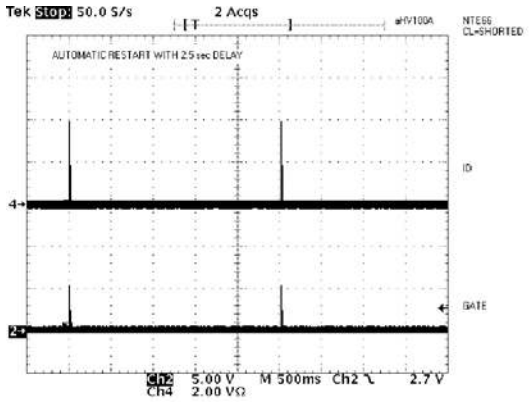

The maximum current that may occur during this period can be controlled by adding a resistor in series with the source of the MOSFET. The lower graph shows the same circuit with a 100mΩ resistor inserted between source and VNN. In this case the maximum current is 25% smaller.



For most applications and pass elements, the HV100 provides adequate limiting of the maximum current to prevent damage without the need for any external components. The 2.5s delay of the auto-retry circuit provides time for the pass element to cool between attempts.

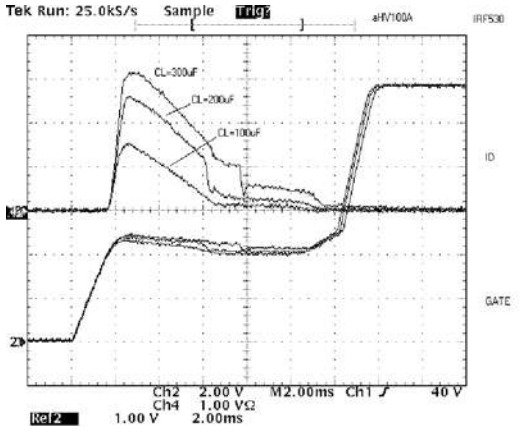
## Auto-Retry

Not only does the HV100 provide short circuit protection in a 3-pin package, they also includes a 2.5s built in auto-restart timer. The HV100 will continuously try to turn on the system every 2.5s, providing sufficient time for the pass element to cool down after each attempt.




## Calculating Inrush Current

As can be seen in the diagram below, for a standard pass element, the HV100 will normalize the hotswap time period against load capacitance. For this reason the current limit will increase with increasing value of the load capacitance.




Inrush can be calculated from the following formula:

$$I_{INRUSH(PEAK)} = (C_{ISS} / C_{RSS}) * 2.5e3 * C_{LOAD}$$

This is a surprisingly consistent result because for most MOSFETs of a particular type the ratio of $C_{ISS}$ / $C_{RSS}$ is relatively constant (though notice from the plot that there is some variation) even while the absolute value of these and other quantities vary. Based on this, the inrush current will vary primarily with $C_{LOAD}$. This makes designing with the HV100 particularly easy because once the pass element is chosen, the period is fixed and the inrush varies with $C_{LOAD}$ only.

## Programming the HV100

The HV100 requires no external components other than a pass element to provide the functionality described thus far. In some applications it may be useful to use external components to adjust the maximum allowable inrush current, adjust UVLO, or to provide additional GATE clamping if the supply rails have rise times below 1.0ms.

All of the above are possible with a minimum number of external components.

i) To adjust inrush current with an external component simply connect a capacitor ($C_{FB}$) from drain to GATE of the MOSFET. The inrush calculation then becomes:

$$I_{INRUSH(PEAK)} = (C_{FB} + C_{ISS})/(C_{RSS} + C_{FB}) * 2.5e3 * C_{LOAD}$$

Note that a resistor (approximately 10KΩ) needs to be added in series with $C_{FB}$ to create a zero in the feedback loop and limit the spurious turn on which is now enhanced by the larger divider element.

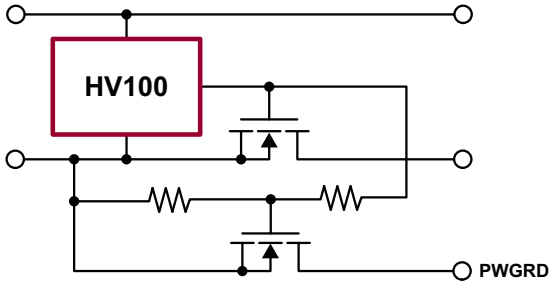
ii) To increase undervoltage lockout simply connect a Zener diode in series with the VPP pin.

iii) If the $V_{PP}$ rises particularly fast (>48e6V/s) then it may be desirable to connect a capacitor from GATE to source of the MOSFET to provide a path for the power application transient spike, which is now too fast for the internal clamping mechanism.

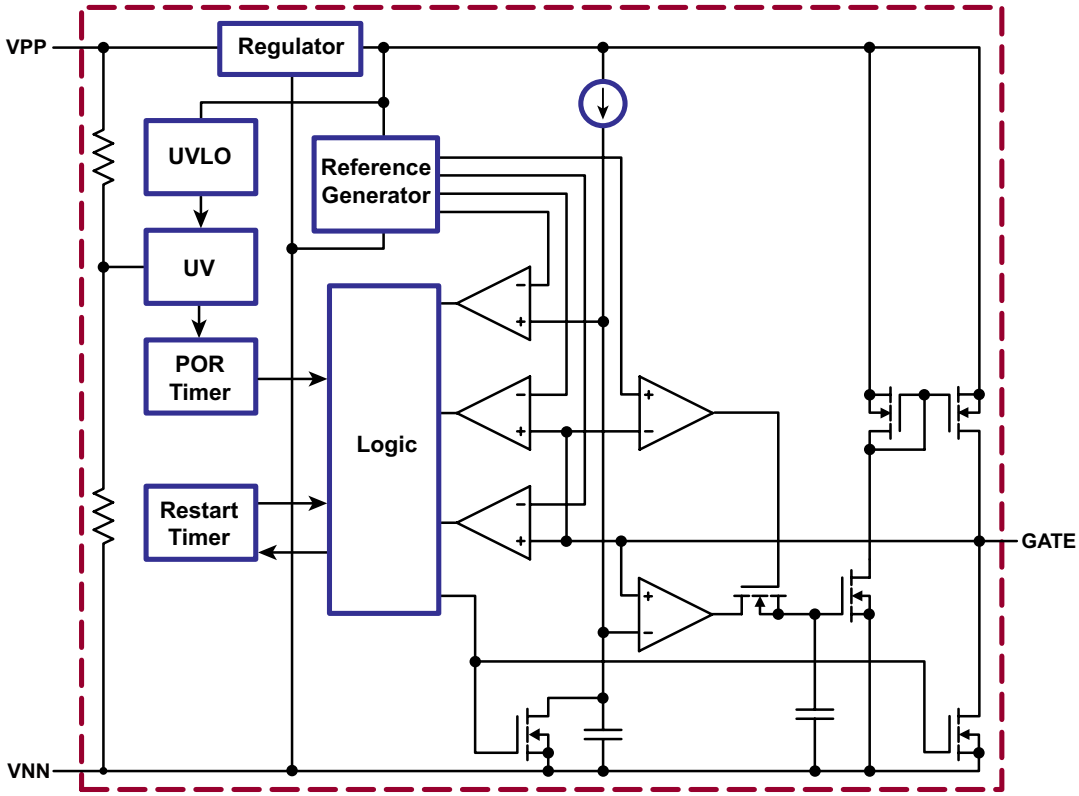
iv) To limit the peak current during a short circuit, a resistor in series with the source of the MOSFET may help.

## Implementing PWRGD Control

Due to the HV100's small footprint, it is possible to create an open drain PWRGD signal using external components and still maintain a size comparable with the smallest hotswap controllers available elsewhere. To accomplish this an external MOSFET may be used in conjunction with the GATE output. Simply use a high impedance divider (10MΩ) sized so that the open drain PWRGD MOSFET threshold will only be reached once the HV100's GATE voltage rises well above the current limit value required by the external MOSFET pass device. Alternatively a Zener diode between the GATE output and the PWRGD MOSFET GATE set at a voltage higher than the maximum pass element $V_t$ will also work.

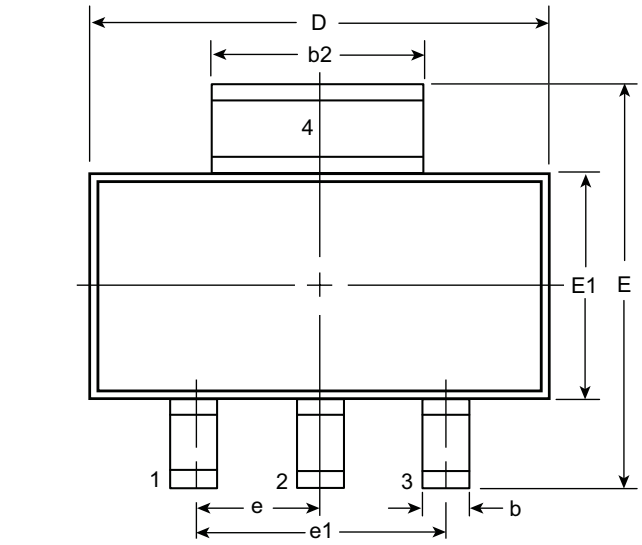



## Functional Block Diagram

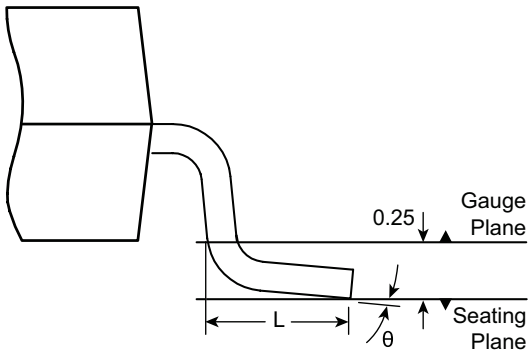


# 3-Lead SOT-223 Package Outline (K5)

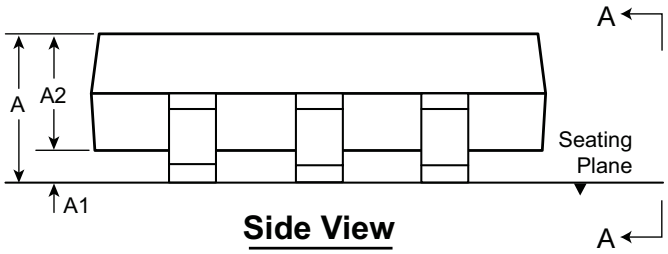
***6.50x3.50mm body, 1.80mm height (max), 2.30mm pitch***



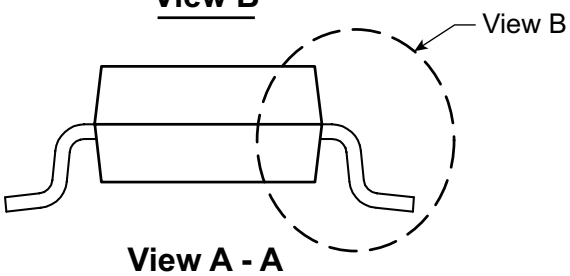

**Top View**




**View B**




**Side View**




**View A - A**

| Symbol | | A | A1 | A2 | b | b2 | D | E | E1 | e | e1 | L | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (mm) | MIN | 1.48* | 0.02 | 1.50 | 0.65† | 2.90 | 6.30 | 6.70 | 3.30 | 2.30 BSC | 4.60 BSC | 0.75 | 0° |
| | NOM | - | - | 1.60 | 0.76 | 3.00 | 6.50 | 7.00 | 3.50 | | | - | - |
| | MAX | 1.80 | 0.10 | 1.70 | 0.85† | 3.15† | 6.70 | 7.30 | 3.70 | | | - | 10° |

*JEDEC Registration TO-261, Variation AA, Issue C, May 2002.*
** This dimension is not specified in the JEDEC drawing.*
*† This dimension differs from the JEDEC drawing.*
***Drawings not to scale.***
***Supertex Doc. #:** DSPD-3SOT223K5, Version A041009.*

*(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)*



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