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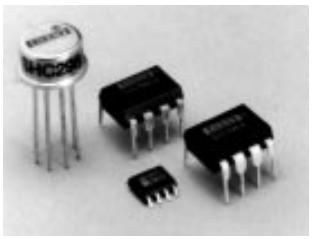
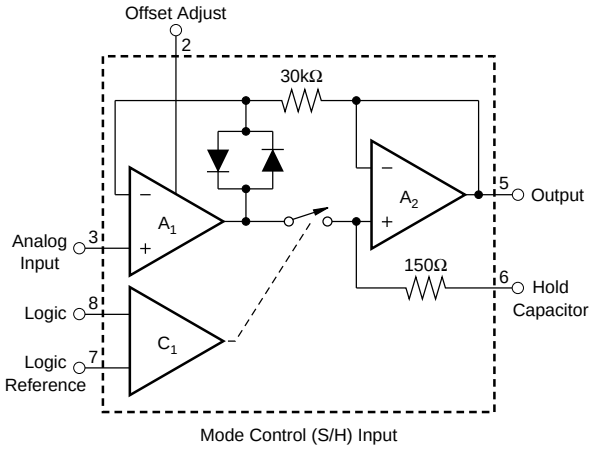


SHC298
SHC298A

Monolithic SAMPLE/HOLD AMPLIFIER

FEATURES

- 12-BIT THROUGHPUT ACCURACY
- LESS THAN 10μs ACQUISITION TIME
- WIDEBAND NOISE LESS THAN 20μVrms
- RELIABLE MONOLITHIC CONSTRUCTION
- $10^{10}\Omega$ INPUT RESISTANCE
- TTL-CMOS-COMPATIBLE LOGIC INPUT



DESCRIPTION

The SHC298 and SHC298A are high-performance monolithic sample/hold amplifiers featuring high DC accuracy with fast acquisition times and a low droop rate. Dynamic performance and holding performance can be optimized with proper selection of the external holding capacitor. With a 1000pF holding capacitor, 12-bit accuracy can be achieved with a 6μs acquisition time. Droop rates less than 5mV/min are possible with a 1μF holding capacitor.

These sample/holds will operate over a wide supply voltage ranging from ±5V to ±18V with very little change in performance. A separate Offset Adjust pin is used to adjust the offset in either the Sample on the Hold modes. The fully differential logic inputs have low input current, and are compatible with TTL, 5V CMOS, and CMOS logic families.

The SHC298AM is available in a hermetically sealed 8-pin TO-99 package and is specified over a temperature range from –25°C to +85°C. The SHC298JP and SHC298JU are 8-pin plastic DIP and SOIC packaged parts specified over 0°C to +70°C.

The SHC298AJP, specified over 0°C to +70°C, is available in an 8-pin plastic DIP. The SHC298A grade features improved gain and offset error, improved drift over temperature, and faster acquisition time.

The SHC298 family is a price-performance bargain. It is well suited for use with several 12-bit A/D converters in data acquisition systems, data distribution systems, and analog delay circuits.

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

ELECTRICAL

At T_J = +25°C, ±15V supplies, 1000pF holding capacitor, –11.5V ≤ V_{IN} ≤ +11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5 V, unless otherwise noted.

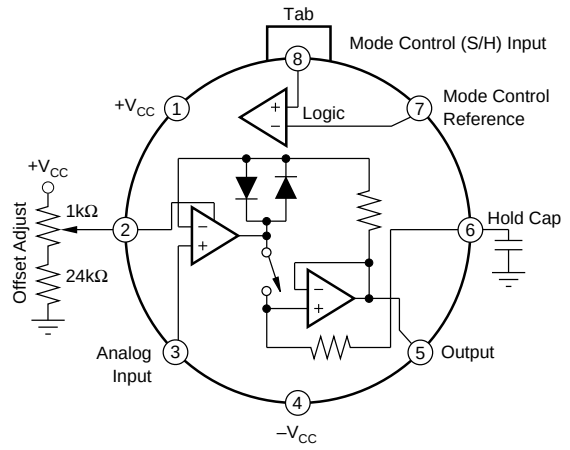
PARAMETER	SHC298AM, JP, JU MIN	SHC298AM, JP, JU TYP	SHC298AM, JP, JU MAX	SHC298AJP MIN	SHC298AJP TYP	SHC298AJP MAX	UNITS
ANALOG INPUT							
Resistance		10^{10}			*		Ω
Bias Current[1]		10	50		*	25	nA
DIGITAL INPUT	Pin 7		Pin 8		Circuit State		
Mode Control Truth Table	0V		+2.4V		Sample (Track)		
	0V		+0.8V		Hold		
	+2.4V		+2.8V		Hold		
	+0.8V		+2.8V		Sample (Track)		
Mode Control and Mode Control Reference Input Current			10				µA
Differential Logic Threshold	0.8	1.4	2.4				V
TRANSFER CHARACTERISTICS							
ACCURACY (+25°C)							
Gain		+1			*		V/V
Gain Error		±0.004	±0.010		±0.001	±0.005	%
Input Voltage Offset (adjust to zero)[1]		±2	±7		±1	±2	mV
Droop Rate[1]		±30			*		µV/ms
Power Supply Rejection		±25	±100		*	*	µV/V
ACCURACY DRIFT							
Gain Drift		3	4		1	2	ppm/°C
Input Offset Drift		15	70		*	25	µV/°C
Droop Rate at T_J = +85°C		10			*		mV/ms
DYNAMIC CHARACTERISTICS							
Aperture Time : Negative Input Step		200			*		ns
Positive Input Step		150			*		ns
Acquisition Time (C = 1000pF): to ±0.1%, 10V Step		5			4	6	µs
Sample/Hold Transient: Peak Amplitude		160			*		mV
Settling to 1mV		1			*		µs
Feedthrough (Response to 10V Input Step)		±0.007			±0.004		% of 20V
OUTPUT							
ANALOG OUTPUT							
Voltage Range	±11.5			*			V
Current Range	±2			*			mA
Impedance (in Hold Mode)	0.5	4		*	*	Ω	
POWER SUPPLY							
Rate Voltage		15			*		VDC
Range	±5		±18	*		*	VDC
Current[1]		±4.5	±6.5		*	*	mA

* Same as specifications for SHC298AM, JP, JU.

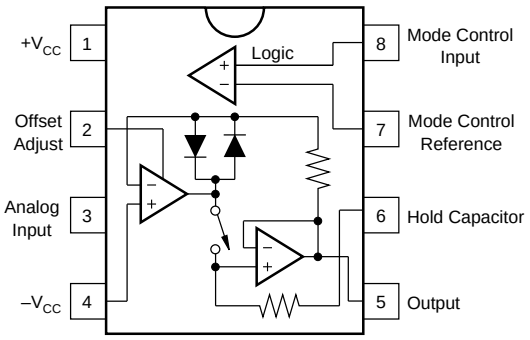
NOTES: (1) These parameters guaranteed over a supply voltage range of ±5V to = ±18V. (2) Charge offset is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01µF hold capacitor. Magnitude of the charge offset is inversely proportional to hold capacitor value.

PIN CONFIGURATIONS

Top View **TO-99**



Top View **Plastic DIP/Small Outline**



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Package Limitation)	500mV
Junction Temperature, $T_{J\ MAX}$	
AM	125°C
JP, JU	100°C
Operating Temperature Range	–25°C to +85°C
Storage Temperature Range	–65°C to +150°C
Input Voltage	Equal to Supply Voltage
Logic-to-Logic Reference Differential Voltage(1)	+7V, –30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10s
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

PACKAGE/ORDERING INFORMATION

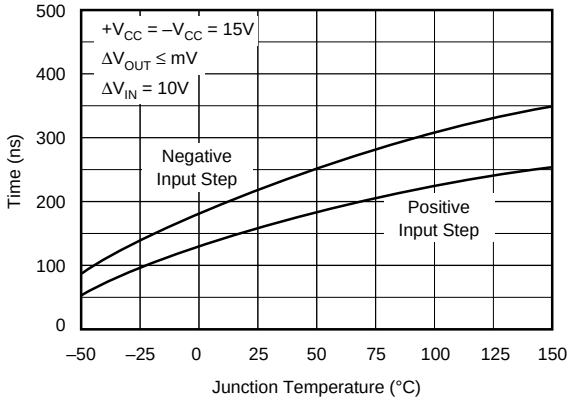
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
SHC298AM	TO-99	001	–25°C to +85°C
SHC298JP	8-Pin Plastic DIP	006	0°C to +70°C
SHC298JU	8-Lead SOIC	182	0°C to +70°C
SHC298AJP	8-Pin Plastic DIP	006	0°C to +70°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

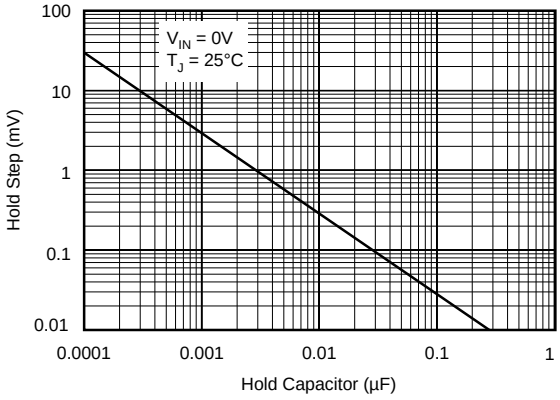
TYPICAL PERFORMANCE CURVES

At T_J = +25°C, ±15V supplies, 1000pF holding capacitor, –11.5V ≤ V_{IN} ≤ +11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5 V, unless otherwise noted.

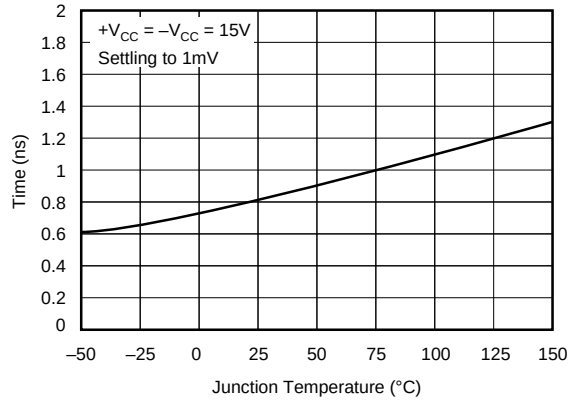
APERTURE TIME



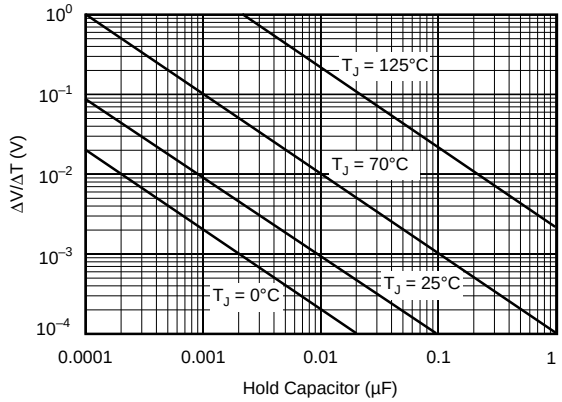
CHARGE OFFSET



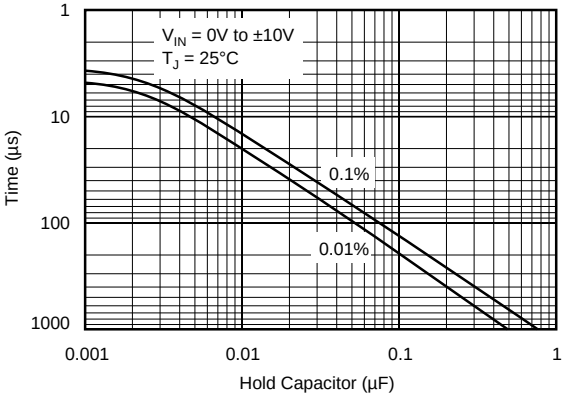
SAMPLE-TO-HOLD TRANSIENT SETTLING TIME



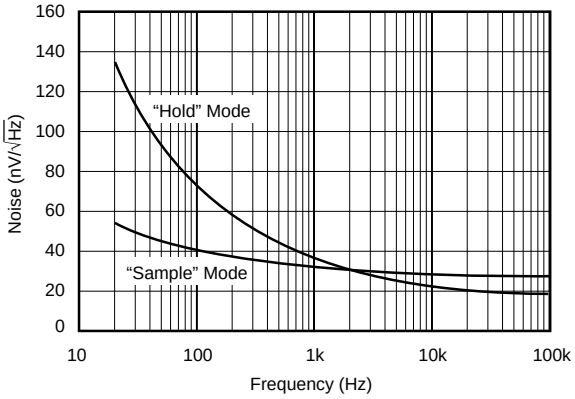
OUTPUT DROOP RATE



ACQUISITION TIME



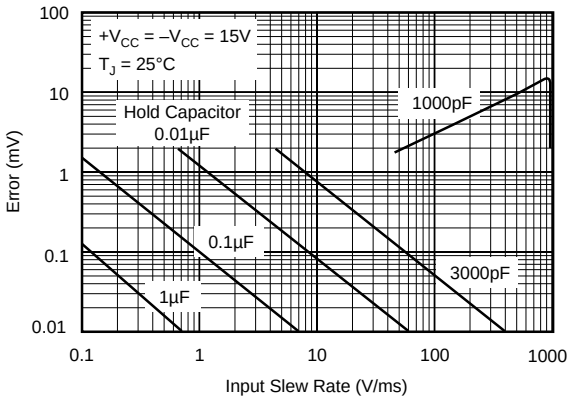
OUTPUT NOISE



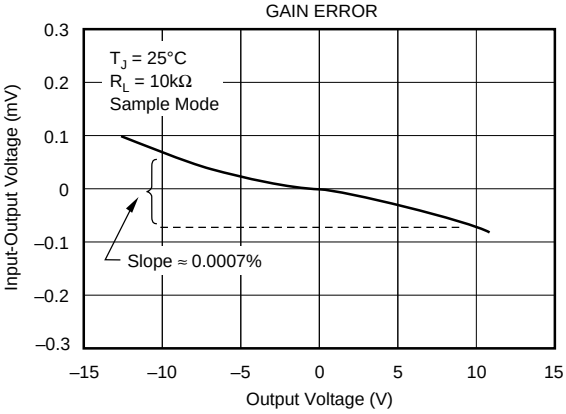
TYPICAL PERFORMANCE CURVES (CONT)

At T_J = +25°C, ±15V supplies, 1000pF holding capacitor, –11.5V ≤ V_{IN} ≤ +11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5 V, unless otherwise noted.

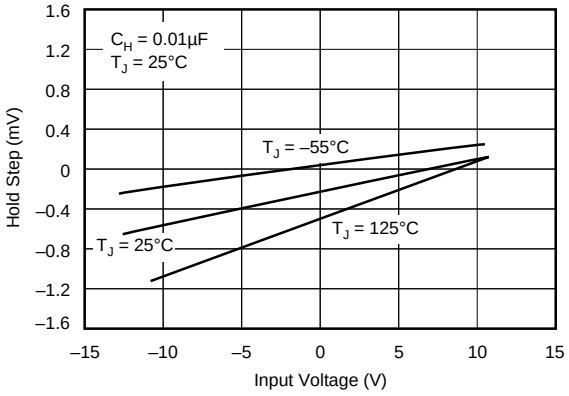
DYNAMIC SAMPLING ERROR



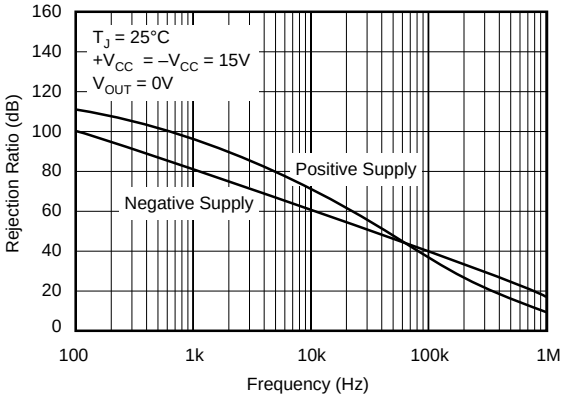
GAIN ERROR



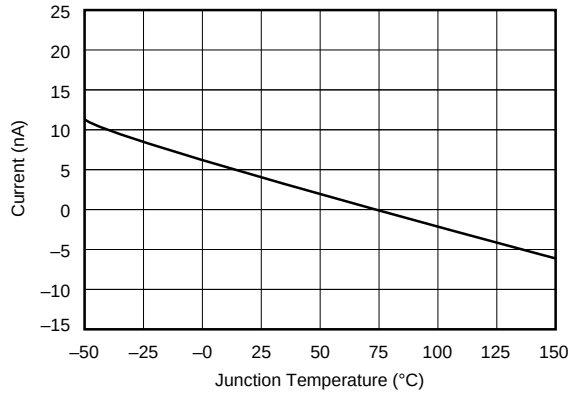
CHARGE OFFSET



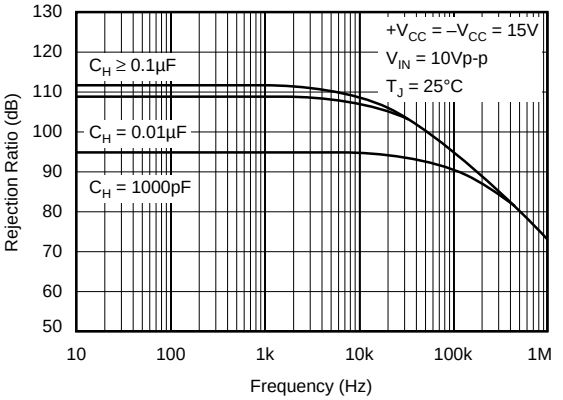
POWER SUPPLY REJECTION



INPUT BIAS CURRENT

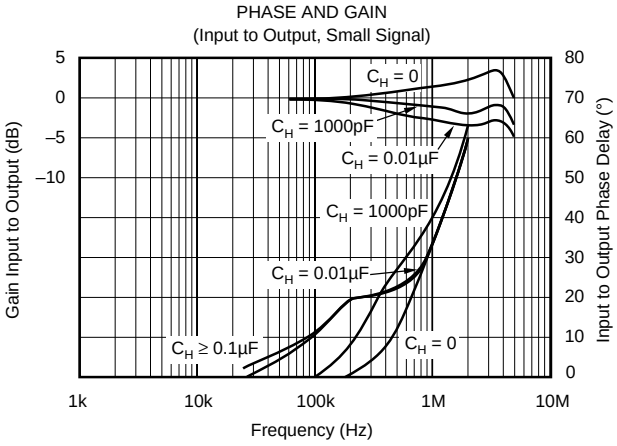


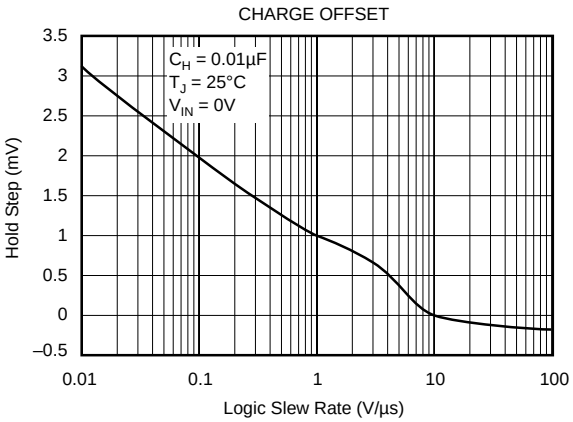
FEEDTHROUGH REJECTION RATIO



TYPICAL PERFORMANCE CURVES (CONT)

At T_J = +25°C, ±15V supplies, 1000pF holding capacitor, –11.5V ≤ V_{IN} ≤ +11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5 V, unless otherwise noted.





DISCUSSION OF SPECIFICATIONS

THROUGHPUT NONLINEARITY

Throughput nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, 1ms of droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by offset and gain adjustments. Throughput nonlinearity is tested with a 1000pF holding capacitor, 10V input changes, 10µs acquisition time, and 1ms Hold time (see Figure 1).

GAIN ACCURACY

Gain Accuracy is the difference between input and output voltage (when in the Sample mode) due to amplifier gain errors.

DROOP RATE

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

Feedthrough is the amount of the input voltage change that appears at the output when the amplifier is in the Hold mode.

APERTURE TIME

Aperture Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

ACQUISITION TIME

Acquisition Time is the time required for the sample/hold output to settle within a given error band of its final value when the mode control is switched from Hold to Sample.

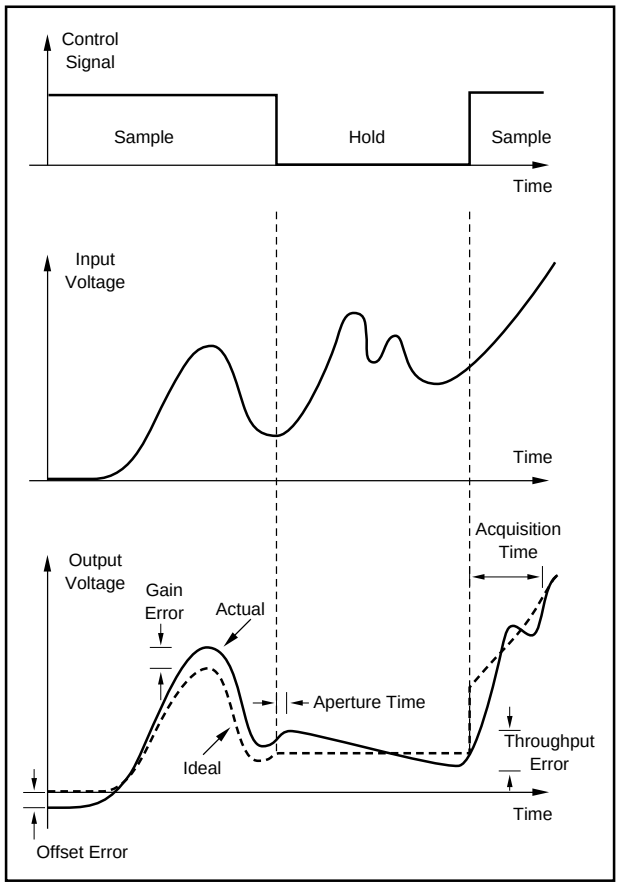


FIGURE 1. Sample/Hold Errors.

CHARGE OFFSET

Charge Offset is the offset that results from the charge coupled through the gate capacitance of the switching FET. This charge is coupled into the storage capacitor when the FET is switched to the "hold" mode.

OPERATING INSTRUCTIONS

EXTERNAL CAPACITOR SELECTION

Capacitors with high insulation resistance and low dielectric absorption, such as Teflon®, polystyrene or polypropylene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize AC and DC leakage currents from the capacitor to reduce charge offset and droop errors.

The value of the external capacitor determines the droop, charge offset and acquisition time of the Sample/Hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table for a 0.001µF capacitor. With a capacitor of 0.01µF, the droop will reduce to approximately 2.5µV/ms and the charge offset to approximately 1.5mV. The behavior of acquisition time with changes in external capacitance is shown in the Typical Performance Curves.

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the Sample and the Hold mode. The error should then be adjusted to zero when the unit is in the Hold mode. In this way, charge offset as well as amplifier offset will be adjusted. When a 0.001µF capacitor is used, it will not be possible to adjust the full offset error at the sample/hold. It should be adjusted elsewhere in the system.

APPLICATIONS

DATA ACQUISITION

The SHC298 may be used to hold data for conversion with an analog-to-digital converter or used to provide Pulse Amplitude Modulation (PAM) data output (see Figures 2 and 3).

DATA DISTRIBUTION

The SHC298 may be used to hold the output of a digital-to-analog converter whose digital inputs are multiplexed (see Figure 4).

TEST SYSTEMS

The SHC298 is also well suited for use in test systems to acquire and hold data transients for human operators or for the other parts of the test system such as comparators, digital voltmeters, etc.

®Teflon, DuPont de Nemours

With a 0.1µF storage capacitor, the output may be held 10 seconds with less than 0.1% error. With a 1µF storage capacitor, the output may be held more than 15 minutes with less than 1% error.

CAPACITIVE LOADING

SHC298 is sensitive to capacitive loading on the output and may oscillate. When driving long lines, a buffer should be used.

HIGH SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the sample/hold plus the conversion time of the analog-to-digital converter. If two or more sample/holds are used with a high-speed multiplexer, the acquisition time of the sample/hold can be virtually eliminated. While the first channel is in hold and switched on to the ADC, the multiplexer may be addressed to the next channel. The second sample/hold will have acquired this data by the time the conversion is complete. Then, the sample/holds reverse roles and another channel is addressed (see Figure 5). For low-level systems, and instrumentation amplifier and double-ended multiplexer may be connected to the sample/hold inputs. The settling time of the multiplexer, instrumentation amplifier, and sample/hold can be eliminated from the channel conversion time as before.

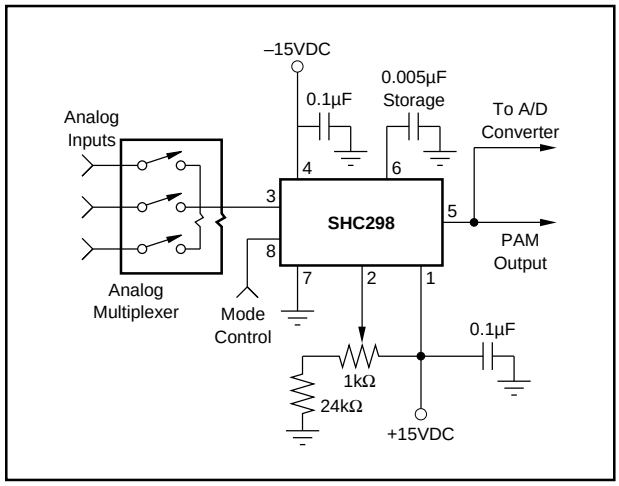


FIGURE 2. Data Acquisition.

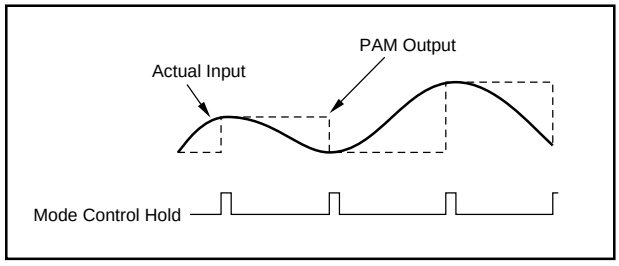


FIGURE 3. PAM Output.

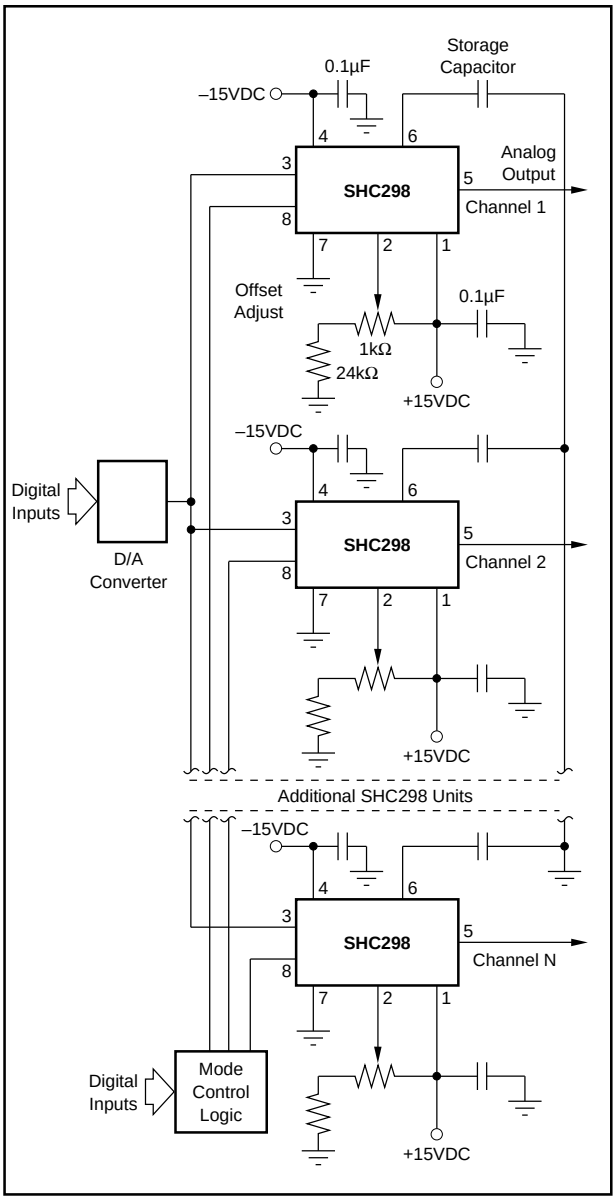


FIGURE 4. Data Distribution.

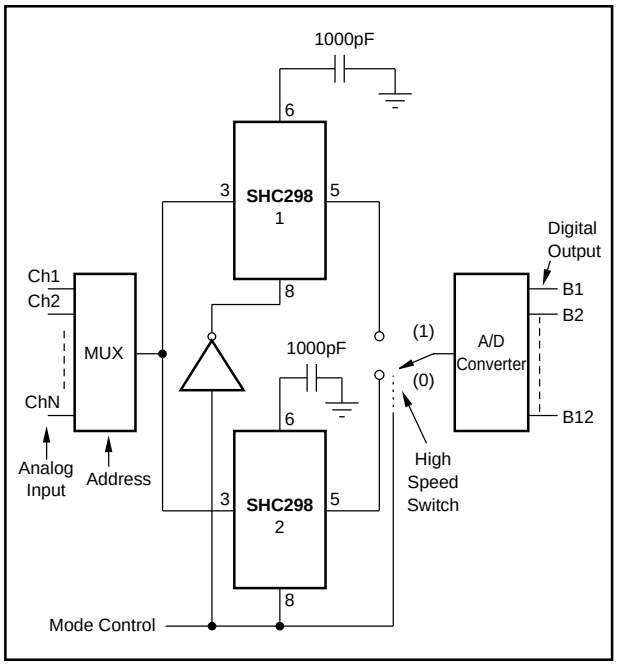


FIGURE 5. “Ping-Pong” Sample Holds.

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