

General Description

- Proprietary α MOS5™ technology
- Low $R_{DS(ON)}$
- Optimized switching parameters for better EMI performance
- Enhanced body diode for robustness and fast reverse recovery

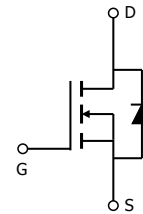
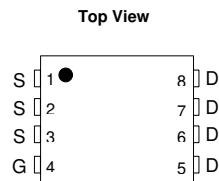
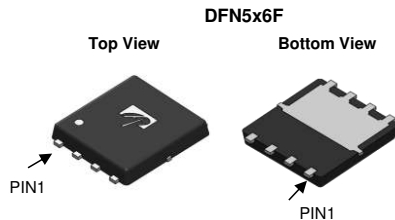
Applications

- Flyback for SMPS
- Charger, Adapter, lighting

Product Summary

$V_{DS} @ T_{j,max}$	800V
I_{DM}	20A
$R_{DS(ON),max}$	< 1.1 Ω
$Q_{g,typ}$	9.4nC
$E_{oss} @ 400V$	1.2 μ J

100% UIS Tested
 100% R_g Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONS1R1A70	DFN5X6F	Tape&Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	700	V
Gate-Source Voltage	V_{GS}	± 20	V
Gate-Source Voltage (dynamic) AC($f > 1\text{Hz}$)	V_{GS}	± 30	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	6.6
		$T_C=100^\circ\text{C}$	4.3
Pulsed Drain Current ^C	I_{DM}	20	A
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	1.3
		$T_A=70^\circ\text{C}$	1.1
Avalanche Current ^C $L=1\text{mH}$	I_{AR}	0.8	A
Repetitive avalanche energy ^C	E_{AR}	0.3	mJ
Single pulsed avalanche energy ^G	E_{AS}	7.5	mJ
MOSFET dv/dt ruggedness	dv/dt	100	V/ns
Peak diode recovery dv/dt	dv/dt	20	V/ns
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	104
		Derate above 25°C	0.8
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	4.2
		$T_A=70^\circ\text{C}$	2.7
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A $t \leq 10\text{s}$	$R_{\theta JA}$	25	30	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient ^{A,D} Steady-State		45	55	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case Steady-State	$R_{\theta JC}$	0.9	1.2	$^\circ\text{C}/\text{W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
STATIC PARAMETERS							
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	700			V	
		I _D =250μA, V _{GS} =0V, T _J =150°C		800			
BV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D =250μA, V _{GS} =0V		0.6		V/°C	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =700V, V _{GS} =0V			1	μA	
		V _{DS} =560V, T _J =125°C			10		
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	2.9	3.5	4.1	V	
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =1A		0.92	1.1	Ω	
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =1A		2.1		S	
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.8	1.2	V	
I _S	Maximum Body-Diode Continuous Current				6.6	A	
I _{SM}	Maximum Body-Diode Pulsed Current ^C				20	A	
DYNAMIC PARAMETERS							
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		461		pF	
C _{oss}	Output Capacitance				15		pF
C _{o(er)}	Effective output capacitance, energy related ^I	V _{GS} =0V, V _{DS} =0 to 480V, f=1MHz		13.3		pF	
C _{o(tr)}	Effective output capacitance, time related ^J				59		pF
C _{rss}	Reverse Transfer Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		1.4		pF	
R _g	Gate resistance	f=1MHz		5.9		Ω	
SWITCHING PARAMETERS							
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =480V, I _D =2.5A		9.4		nC	
Q _{gs}	Gate Source Charge				3.6		nC
Q _{gd}	Gate Drain Charge				2.8		nC
t _{D(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =400V, I _D =2.5A, R _G =5Ω		16		ns	
t _r	Turn-On Rise Time				7		ns
t _{D(off)}	Turn-Off Delay Time				33		ns
t _f	Turn-Off Fall Time				12		ns
t _{rr}	Body Diode Reverse Recovery Time				200		ns
I _{rm}	Peak Reverse Recovery Current	I _F =2.5A, di/dt=100A/μs, V _{DS} =400V		13		A	
Q _{rr}	Body Diode Reverse Recovery Charge			2		μC	

A. The value of R_{qJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{qJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{qJA} is the sum of the thermal impedance from junction to case R_{qJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. L=60mH, I_{AS}=0.5A, R_G=25Ω, Starting T_J=25° C.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

I. C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

J. C_{o(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

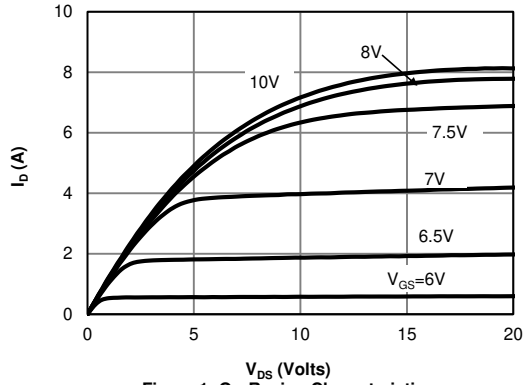


Figure 1: On-Region Characteristics

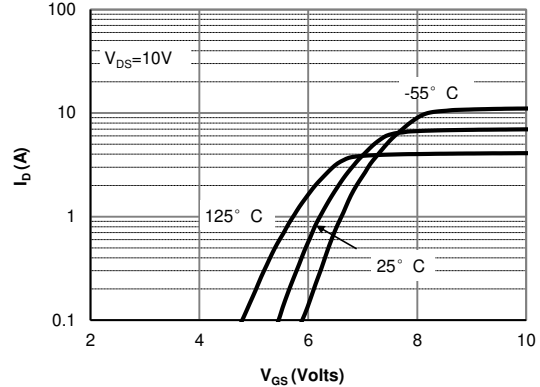


Figure 2: Transfer Characteristics

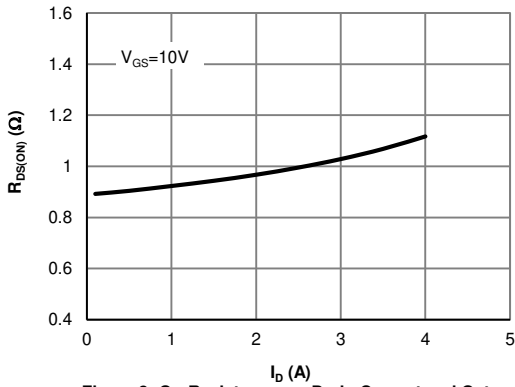


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

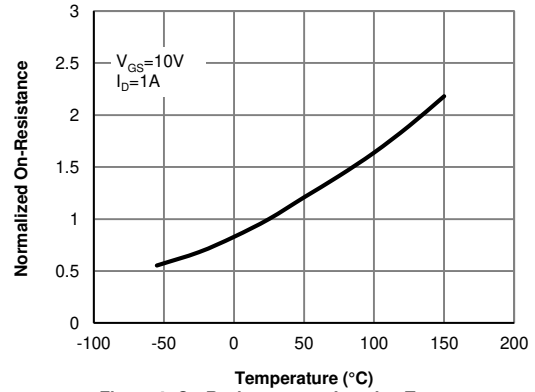


Figure 4: On-Resistance vs. Junction Temperature

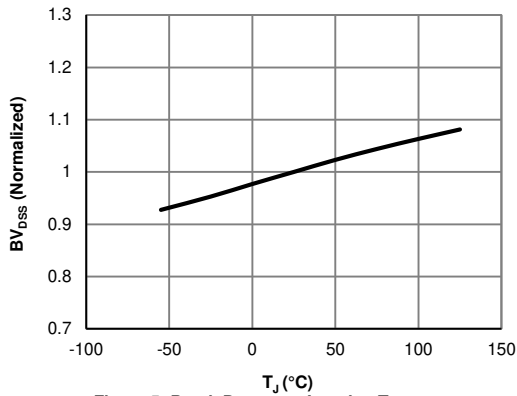


Figure 5: Break Down vs. Junction Temperature

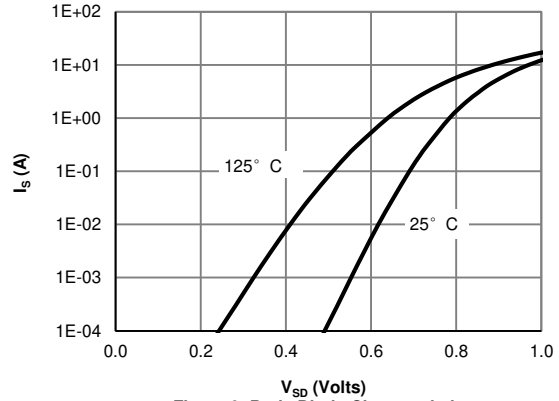


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

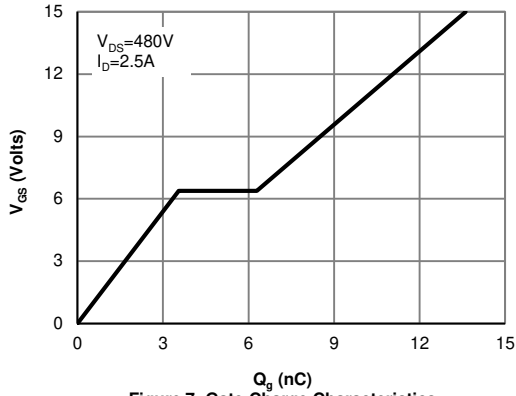


Figure 7: Gate-Charge Characteristics

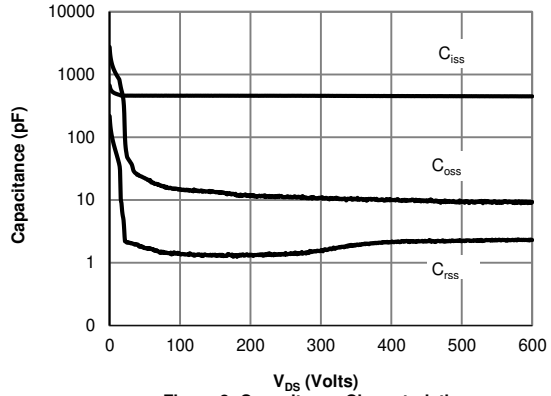


Figure 8: Capacitance Characteristics

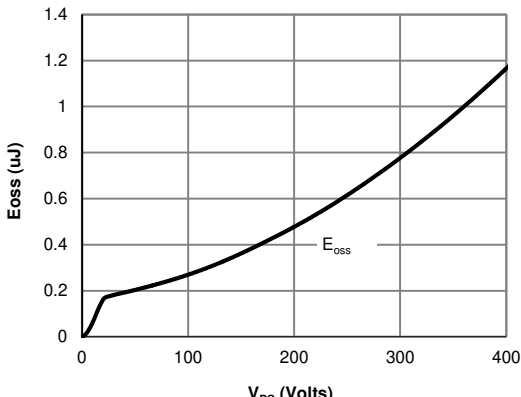


Figure 9: Coss stored Energy

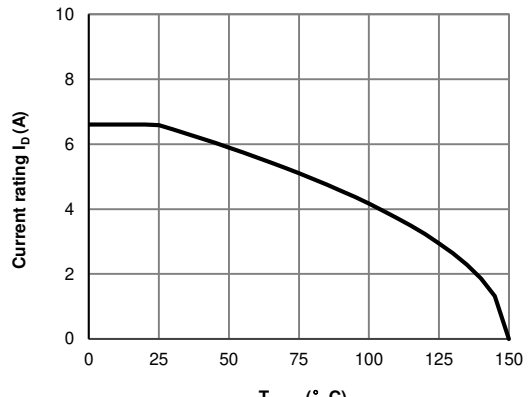


Figure 10: Current De-rating (Note F)

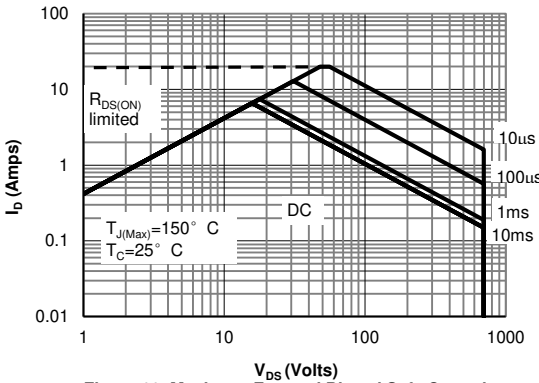


Figure 11: Maximum Forward Biased Safe Operating Area (Note F)

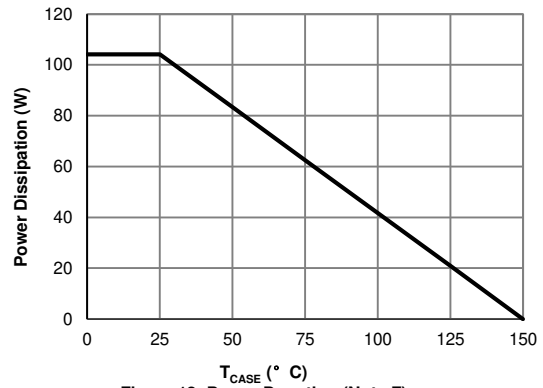


Figure 12: Power De-rating (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

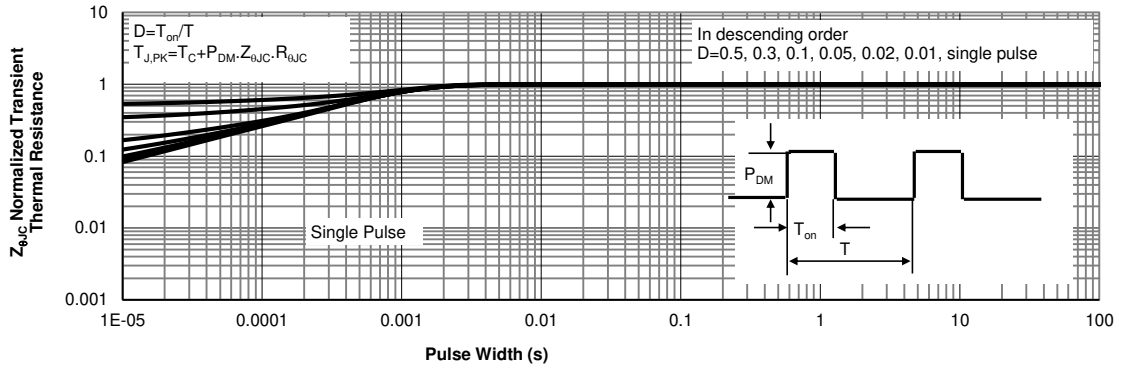


Figure 13: Normalized Maximum Transient Thermal Impedance (Note F)

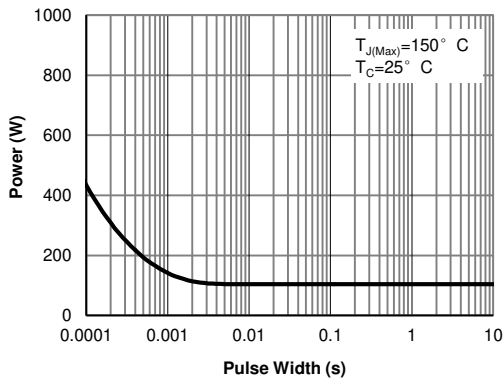


Figure 14: Single Pulse Power Rating Junction-to-Case (Note F)

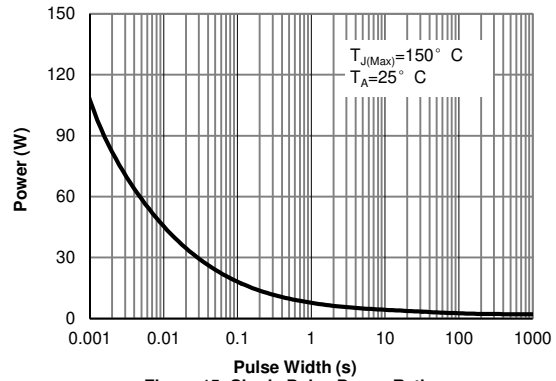


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

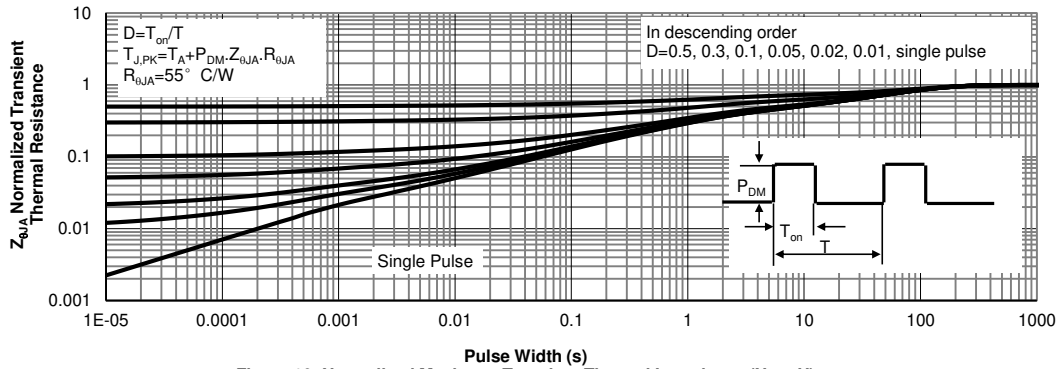
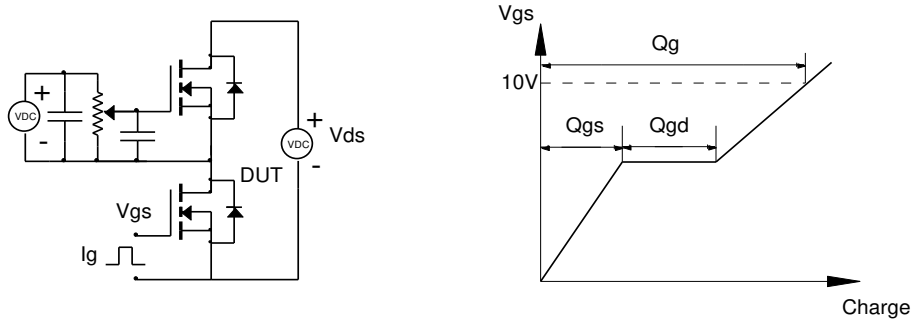
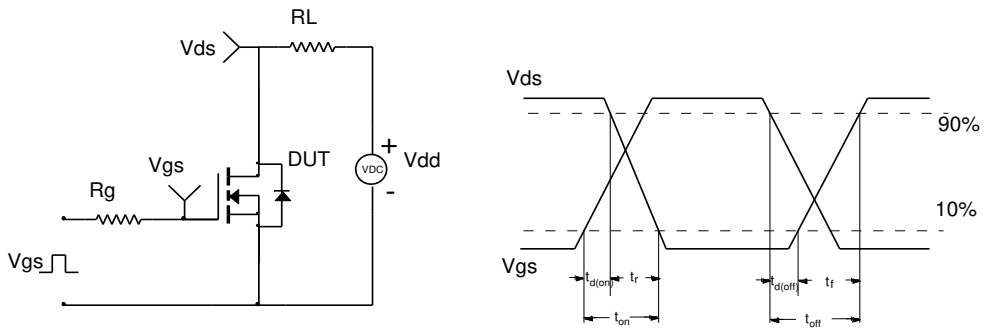


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

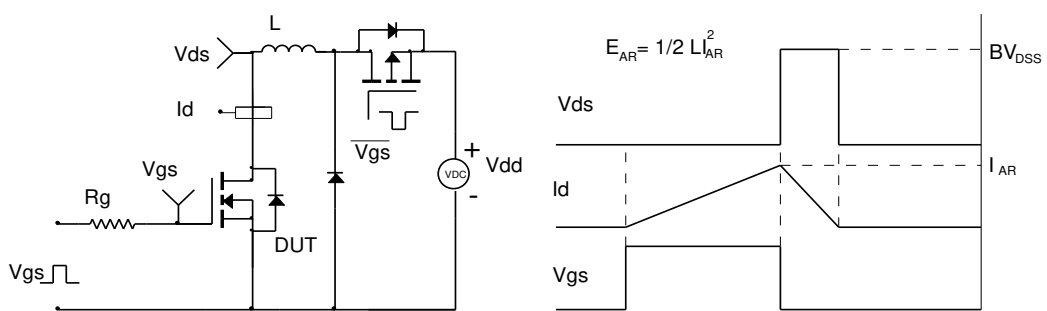
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

