ZL50074

# 32 K x 32 K Channel TDM Switch with 128 Input and 128 Output Streams

Data Sheet

January 2006

## Features

- 32,768 channel x 32,768 channel non-blocking digital Time Division Multiplex (TDM) switch at 65.536 Mbps, 32.768 Mbps or 16.384 Mbps
- 16,384 channel x 16,384 channel non-blocking digital TDM switch at 8.192 Mbps
- Up to 128 serial TDM input streams, divided into 32 groups with 4 input streams per group
- Up to 128 serial TDM output streams, divided into 32 groups with 4 output streams per group
- Per-group input bit delay for flexible sampling point selection
- Per-group output fractional bit advancement
- Four sets of output timing signals for interfacing additional devices
- Per-channel constant or variable throughput delay for frame integrity and low latency applications
- Per-channel high impedance output control
- Per-channel force-high output control
- Per-channel message mode

**Ordering Information**

| | | |
|---|---|---|
| ZL50074GAC | 484 Ball LBGA | Trays |
| ZL50074GAG2 | 484 Ball PBGA** | Trays |

**Pb Free Tin/Silver/Copper

**-40°C to +85°C**

- Control interface compatible with Intel and Motorola Selectable 32 bit and 16 bit non-multiplexed buses
- Connection Memory block programming
- Supports ST-BUS and GCI-Bus standards for input and output timing
- IEEE 1149.1 (JTAG) test port
- 3.3 V I/O with 5 V tolerant inputs; 1.8 V core

## Applications

- Large Switching Platforms
- Central Office Switches
- Wireless Base Stations and Controllers
- Multi-service Access Platforms

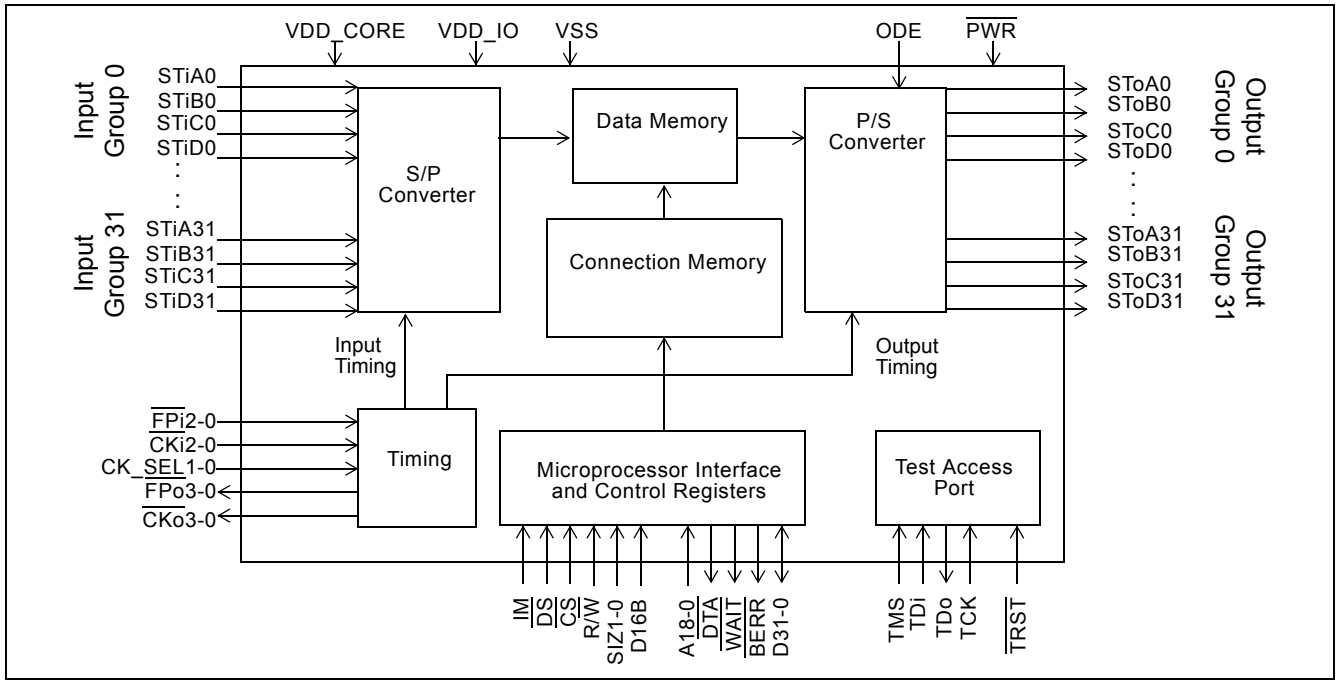


**Figure 1 - ZL50074 Functional Block Diagram**



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- Digital Loop Carriers
- Time Division Multiplexers
- Media Gateways

## Description

The ZL50074 is a non-blocking Time Division Multiplex (TDM) switch with maximum 32,768 x 32,768 channels. The device can switch 64 kbps or Nx64 kbps TDM channels from any input stream to any output stream.

All TDM input and output streams operate at the same rate, either 65.536 Mbps, 32.768 Mbps, 16.384 Mbps or 8.192 Mbps, programmed by the Global Rate Control Register. In 65 Mbps mode, only STiA and SToA streams are used, resulting in 32 input and 32 output streams. In 32 Mbps mode, STiA, SToA, STiB, and SToB streams are available, resulting in 64 input and 64 output streams. In 16 Mbps or 8 Mbps mode, STiA, SToA, STiB, SToB, STiC, SToC, STiD and SToD streams are all available, resulting in 128 input and 128 output streams. The full 32 K x 32 K channel switching capacity is maintained at bit rates of 65 Mbps, 32 Mbps and 16 Mbps. The capacity reduces to 16 K x 16 K when operating at 8 Mbps.

The ZL50074 uses a master clock ($\overline{\text{CKi}}$0) and frame pulse ($\overline{\text{FPi}}$0) to define the TDM data stream frame boundary and timing. A high speed system clock is derived internally from $\overline{\text{CKi}}$0 and $\overline{\text{FPi}}$0. The input and output data streams can independently reference their timings to one of the input clocks or to the internal system clock.

The ZL50074 has a variety of user configurable options designed to provide flexibility when data streams are connected to multiple TDM components or circuits. These include:

- Two additional programmable reference inputs, $\overline{\text{CKi}}$2 - 1 and $\overline{\text{FPi}}$2 - 1, which can be used to provide alternative sources for input and output stream timing
- Variable input bit delay and output advancement, to accommodate delays and frame offsets of streams connected through different data paths
- Four timing outputs, $\overline{\text{CKo}}$3 - 0 and $\overline{\text{FPo}}$3 - 0, which can be configured independently to provide a variety of clock and frame pulse options
- Support of both ST-BUS and GCI-Bus formats
- Per-channel variable delay mode for low latency applications and constant delay mode for frame integrity applications

The device contains two types of internal memory: Data Memory and Connection Memory. Incoming TDM data is stored in the Data Memory. TDM Data is read from the Data Memory controlled by the Connection Memory, and output on the TDM Output Streams.

There are two major modes of operation: Connection Mode and Message Mode. In Connection Mode, the contents of the Connection Memory define, for each output stream and channel, the input source stream and channel. In Message Mode, the Connection Memory is used for the storage of microprocessor data. Using Zarlink's Message Mode capability, microprocessor data can be broadcast to the data output streams on a per-channel basis. This feature is useful for transferring control and status information for external circuits or other TDM devices.

The non-multiplexed microprocessor port provides access to the internal Data Memory, Connection Memory and configuration registers used to program ZL50074 options. The port is configurable to interface with either Motorola or Intel-type microprocessors and is selectable to be either 32 bit or 16 bit.

The mandatory requirements of IEEE 1149.1 (JTAG) standard are supported via the dedicated Test Access Port.

# Table of Contents

# List of Figures

# List of Tables

## Change Summary

The following table captures the changes from the April 2005 issue.

| Page | Item | Change |
|---|---|---|
| 24 | 8.4.1, “Read Cycle“ | Clarified $\overline{\text{WAIT}}$ signal description in Read Cycle. |
| 25 | Figure 6 "Read Cycle Operation" | Corrected $\overline{\text{WAIT}}$ signal tristate timing in Read Cycle. |
| 25 | 8.4.2, “Write Cycle“ | Clarified $\overline{\text{WAIT}}$ signal description in Write Cycle. |
| 26 | Figure 7 "Write Cycle Operation" | Corrected $\overline{\text{WAIT}}$ signal tristate timing in Write Cycle. |

The following table captures the changes from the July 2004 issue.

| Page | Item | Change |
|---|---|---|
| 11 | "Pin Description" - CKo0-3 | Added special requirement for using output clock at 65.536 MHz. |
| 12 | "Pin Description" - $\overline{\text{DTA}}$, $\overline{\text{WAIT}}$ | Added more detailed description to the $\overline{\text{DTA}}$ and $\overline{\text{WAIT}}$ pins. |
| 48 | “AC Electrical Characteristics1 - FPi0-2 and CKi0-2 Timing“ | Added $t_{FPIS}$, $t_{FPIH}$ (input frame pulse setup and hold) maximum values. |
| 49 | Figure 9 "Frame Skew Timing Diagram" | Added $\overline{\text{FPi}}$1,2 frame pulse to Figure “Frame Skew Timing Diagram” to clarify frame boundary skew. |
| 50 | (1) “AC Electrical Characteristics1 - FPO0-3 and CKO0-3 (65.536 MHz) Timing“<br>(2) “AC Electrical Characteristics1 - FPO0-3 and CKO0-3 (32.768 MHz) Timing“<br>(3) “AC Electrical Characteristics1 - FPO0-3 and CKO0-3 (16.384 MHz) Timing“<br>(4) “AC Electrical Characteristics1 - FPO0-3 and CKO0-3 (8.192 MHz) Timing“ | Added $\overline{\text{CKO}}$0-3 and $\overline{\text{FPO}}$0-3 setup and hold parameters for all different clock rates. |
| 51 | “AC Electrical Characteristics - Output Clock Jitter Generation“ | Added this table to specify $\overline{\text{CKO}}$0-3 jitter generation. |
| 52 | “AC Electrical Characteristics - Serial Data Timing to CKi“ | (1) Values of parameters $t_{SIPS}$, $t_{SIPH}$, $t_{SINS}$, $t_{SINH}$, $t_{SIPV}$, $t_{SINV}$, $t_{SIPZ}$ and $t_{SINZ}$ are revised.<br>(2) Separated parameter $t_{CKD}$ into $t_{CKDP}$ and $t_{CKDN}$. |
| 53 | Figure 12 "Serial Data Timing to CKi" | Added more detail to figure. |
| 54 | “AC Electrical Characteristics - Serial Data Timing to CKo“ | Values of parameters $t_{SOPS}$, $t_{SOPH}$, $t_{SONS}$, $t_{SONH}$, $t_{SOPV}$, $t_{SONV}$, $t_{SOPZ}$ and $t_{SONZ}$ are revised. |
| 54 | Figure 13 "Serial Data Timing to CKo" | Added more detail to figure. |
| 56 | “AC Electrical Characteristics - CKo to Other CKo 1Skew“ | Added $\overline{\text{CKO}}$ skew parameters, $t_{CKOS}$, (clock source to internal APLL). |
| 56 | Figure 14 "CKo to other CKo Skew" | Added figure to show $t_{CKOS}$. |

**Pin Diagram - ZL50074 23 mm x 23 mm 484 Ball PBGA (as viewed through top of package)**

A1 corner identified by metallized marking

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $\overline{\text{CKo}}$ [0] | STiA [0] | D[30] | D[25] | D[20] | D[16] | D[15] | D[11] | D[7] | D[4] | D[0] | A[18] | A[14] | A[10] | A[7] | A[2] | A[1] | IC | $\overline{\text{DTA}}$ | $\overline{\text{PWR}}$ | STOA [31] | TCK |
| **B** | STOB [1] | STiD [1] | STOA [0] | D[31] | D[26] | D[21] | D16B | D[13] | D[9] | D[5] | D[3] | A[17] | A[11] | A[8] | A[6] | A[0] | $\overline{\text{BERR}}$ | SIZ[0] | STOB [31] | STiA [31] | TDo | STiA [30] |
| **C** | STiA [2] | STiA [3] | STiB [1] | STiD [0] | IM | D[27] | D[22] | D[19] | D[12] | D[6] | D[1] | A[15] | A[9] | A[3] | R/$\overline{\text{W}}$ | $\overline{\text{CS}}$ | $\overline{\text{FPo}}$ [3] | STiD [31] | $\overline{\text{TRST}}$ | STOD [30] | STiB [30] | STiD [29] |
| **D** | STiC [3] | STiD [2] | STOC [1] | STOD [0] | STOB [0] | STiC [0] | D[28] | D[23] | D[17] | D[8] | A[16] | A[13] | A[5] | $\overline{\text{DS}}$ | $\overline{\text{WAIT}}$ | STOD [31] | STiB [31] | TDi | STOB [30] | STiC [30] | STOA [29] | STOD [28] |
| **E** | STiD [4] | STOB [3] | STiC [2] | STOA [1] | STiA [1] | STOC [0] | STiB [0] | D[24] | D[18] | D[14] | D[2] | A[12] | A[4] | $\overline{\text{CKo}}$ [3] | SIZ[1] | STiC [31] | TMS | STOC [30] | STiD [30] | STOD [29] | STiA [29] | STiB [28] |
| **F** | STOB [4] | STOC [3] | STOB [2] | STOD [1] | STiC [1] | $V_{SS}$ | $V_{DD\_CORE}$ | D[29] | $V_{DD\_IO}$ | $V_{DD\_CORE}$ | D[10] | $V_{DD\_IO}$ | $V_{DD\_CORE}$ | STOC [31] | $V_{DD\_IO}$ | $V_{SS}$ | $V_{DD\_CORE}$ | STOA [30] | STOC [29] | STiC [29] | STOB [28] | STiA [28] |
| **G** | STOD [4] | STOD [3] | STOD [2] | STiB [2] | $\overline{\text{FPo}}$ [0] | $V_{DD\_IO}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{SS}$ | STOB [29] | STiB [29] | STiC [28] | $\overline{\text{CKi}}$ [2] | STiD [27] |
| **H** | STiA [5] | STiA [4] | STiD [3] | STOC [2] | STOA [2] | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{DD\_CORE}$ | STOA [28] | STOC [28] | STiD [28] | STOD [27] | STiC [27] | STiA [27] |
| **J** | STiB [5] | $\overline{\text{CKi}}$ [1] | STiC [4] | STOA [3] | STiB [3] | $V_{DD\_IO}$ | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{DD\_IO}$ | STOB [27] | STOC [27] | STiB [27] | IC | STOC [26] |
| **K** | STOB [5] | STiD [5] | $\overline{\text{FPi}}$ [1] | STOC [4] | STOA [4] | STiB [4] | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{DD\_CORE}$ | STOA [27] | $\overline{\text{FPi}}$ [2] | STOA [26] | STOB [26] | STiD [26] |
| **L** | ODE | STOD [5] | STOC [5] | STiD [6] | STiC [5] | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD\_CORE}$ | STOD [26] | STiC [26] | STiB [26] | STiA [26] | STOD [25] | STOC [25] |
| **M** | STiA [6] | STiB [6] | STiC [6] | STiC [7] | STOA [5] | $V_{DD\_IO}$ | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{DD\_IO}$ | STiA [25] | STiD [25] | STOB [25] | STOA [25] | IC |
| **N** | STOB [6] | STOC [6] | STOD [6] | STOA [7] | STOA [6] | $V_{SS}$ | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | STOD [23] | STOC [24] | STiD [24] | STOB [24] | STiB [25] | STiC [25] |
| **P** | STiA [7] | STiB [7] | STOB [7] | STiA [8] | STOA [8] | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD\_IO}$ | $V_{DD\_CORE}$ | $V_{DD\_CORE}$ | STOA [23] | STiC [23] | STiB [24] | STOA [24] | STOD [24] |
| **R** | STiD [7] | STOC [7] | IC | STOB [8] | STiB [8] | $V_{DD\_IO}$ | $V_{DD\_CORE}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD\_IO}$ | $\overline{\text{CKo}}$ [2] | STiD [22] | STiB [23] | STiA [24] | STiC [24] |
| **T** | STOD [7] | $V_{SS}$ | STOC [8] | STiD [9] | STiB [10] | STOD [9] | $V_{SS}$ | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD\_CORE}$ | $V_{DD\_IO}$ | $V_{SS}$ | STOA [21] | $\overline{\text{FPo}}$ [2] | STOC [22] | STiD [23] | STOC [23] |
| **U** | STiC [8] | STOD [8] | STiC [9] | STiA [10] | STOC [10] | $V_{SS}$ | $V_{DD\_IO}$ | STOC [12] | $V_{DD\_IO}$ | $V_{DD\_CORE}$ | STiA [16] | $V_{DD\_IO}$ | $V_{DD\_CORE}$ | STOA [18] | $V_{DD\_IO}$ | STiC [19] | $V_{DD\_CORE}$ | STOC [20] | STiD [21] | STiC [22] | STOD [22] | STOB [23] |
| **V** | STiD [8] | STiB [9] | STOC [9] | STOB [10] | STOD [10] | STOB [11] | STiC [12] | STiB [13] | STOA [13] | STiC [15] | STOB [16] | STOC [16] | IC | CK_SEL[1] | STiB [18] | STOA [19] | STiA [20] | STOB [20] | STOD [20] | STOC [21] | STOA [22] | STiA [23] |
| **W** | STiA [9] | STOB [9] | STiD [10] | STiA [11] | STOA [11] | STiB [12] | STOD [12] | STiC [13] | STiA [14] | STOD [14] | STOC [15] | $\overline{\text{CKi}}$ [0] | IC | STOB [17] | CK_SEL[0] | STOC [18] | STiD [19] | STOD [19] | STiD [20] | STiC [21] | STiA [22] | STOB [22] |
| **Y** | STOA [9] | STOA [10] | STiB [11] | STOC [11] | STOA [12] | $\overline{\text{FPo}}$ [1] | STiD [13] | STiB [14] | STOB [14] | STiD [15] | STOD [15] | STOD [16] | IC | STiC [17] | STOC [17] | STiA [18] | STOB [18] | STiB [19] | STiB [20] | STOA [20] | STOB [21] | STiB [22] |
| **AA** | STiC [10] | STiC [11] | STOD [11] | STiD [12] | STiA [13] | STOB [13] | STOD [13] | STOA [14] | STiA [15] | STOA [15] | STiB [16] | STOA [16] | $\overline{\text{FPi}}$ [0] | STiA [17] | STOA [17] | IC | IC | STOD [18] | STOB [19] | STOC [19] | STiA [21] | STOD [21] |
| **AB** | STiD [11] | STiA [12] | STOB [12] | $\overline{\text{CKo}}$ [1] | STOC [13] | STiC [14] | STiD [14] | STOC [14] | STiB [15] | STOB [15] | STiC [16] | STiD [16] | NC | NC | STiB [17] | STiD [17] | STOD [17] | STiC [18] | STiD [18] | STiA [19] | STiC [20] | STiB [21] |

**Pin Description**

| Pin | Name | Description |
|---|---|---|
| **TDM Interface** | | |
| F7, F10, F13, F17, G9, G12, G15, H6, H10, H13, H16, J7, K8, K15, K17, L6, L16, M7, N8, N15, P6, P16, P17, R7, R10, R13, T9, T12, T15, U10, U13, U17 | $V_{DD\_CORE}$ | **Power Supply for the Core Logic:** +1.8 V |
| F9, F12, F15, G6, G10, G13, G16, H7, H11, H14, J6, J8, J15, J17, K16, L7, M6, M8, M15, M17, N16, P7, P8, P15, R6, R11, R14, R17, T10, T16, U7, U9, U12, U15 | $V_{DD\_IO}$ | **Power Supply for the I/O:** +3.3 V |
| F6, F16, G7, G8, G11, G14, G17, H8, H9, H12, H15, J9, J10, J11, J12, J13, J14, J16, K7, K9, K10, K11, K12, K13, K14, L8, L9, L10, L11, L12, L13, L14, L15, M9, M10, M11, M12, M13, M14, M16, N6, N7, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, R8, R9, R12, R15, R16, T2, T7, T8, T11, T13, T14, T17, U6 | $V_{SS}$ | **Ground** |
| A2, E5, C1, C2, H2, H1, M1, P1, P4, W1, U4, W4, AB2, AA5, W9, AA9, U11, AA14, Y16, AB20, V17, AA21, W21, V22, R21, M18, L20, H22, F22, E21, B22, B20 | STiA0-31 | **Serial TDM Input Data 'A' Streams (5 V Tolerant Input with Internal Pull-down)**<br>32 serial TDM input data streams. All streams are at the same rate: 65.536 Mbps, 32.678 Mbps, 16.384 Mbps or 8.192 Mbps, programmed by the Global Rate Control Register (Section 12.8).<br>The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 12.3).<br>Unused inputs are pulled low by internal pull-down resistors and may be left unconnected. |
| E7, C3, G4, J5, K6, J1, M2, P2, R5, V2, T5, Y3, W6, V8, Y8, AB9, AA11, AB15, V15, Y18, Y19, AB22, Y22, R20, P20, N21, L19, J20, E22, G19, C21, D17 | STiB0-31 | **Serial TDM Input Data 'B' Streams (5 V Tolerant Input with Internal Pull-down)**<br>32 serial TDM input data streams. All streams are at the same rate: 32.678 Mbps, 16.384 Mbps or 8.192 Mbps, programmed by the Global Rate Control Register (Section 12.8). These streams are unused when the device data rate is 65.536 Mbps.<br>The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 12.3).<br>Unused inputs are pulled low by internal pull-down resistors and may be left unconnected. |

**Pin Description (continued)**

| Pin | Name | Description |
|---|---|---|
| D6, F5, E3, D1, J3, L5, M3, M4, U1, U3, AA1, AA2, V7, W8, AB6, V10, AB11, Y14, AB18, U16, AB21, W20, U20, P19, R22, N22, L18, H21, G20, F20, D20, E16 | STiC0-31 | **Serial TDM Input Data 'C' Streams (5 V Tolerant Input with Internal Pull-down)**<br>32 serial TDM input data streams. All streams are at the same rate: 16.384 Mbps or 8.192 Mbps, programmed by the Global Rate Control Register (Section 12.8). These streams are unused when the device data rate is 65.536 Mbps or 32.678 Mbps.<br>The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 12.3).<br>Unused inputs are pulled low by internal pull-down resistors and may be left unconnected. |
| C4, B2, D2, H3, E1, K2, L4, R1, V1, T4, W3, AB1, AA4, Y7, AB7, Y10, AB12, AB16, AB19, W17, W19, U19, R19, T21, N19, M19, K22, G22, H19, C22, E19, C18 | STiD0-31 | **Serial TDM Input Data 'D' Streams (5 V Tolerant Input with Internal Pull-down)**<br>32 serial TDM input data streams. All streams are at the same rate: 16.384 Mbps or 8.192 Mbps, programmed by the Global Rate Control Register (Section 12.8). These streams are unused when the device data rate is 65.536 Mbps or 32.678 Mbps.<br>The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 12.3).<br>Unused inputs are pulled low by internal pull-down resistors and may be left unconnected. |
| B3, E4, H5, J4, K5, M5, N5, N4, P5, Y1, Y2, W5, Y5, V9, AA8, AA10, AA12, AA15, U14, V16, Y20, T18, V21, P18, P21, M21, K20, K18, H17, D21, F18, A21 | SToA0-31 | **Serial TDM Output Data 'A' Streams (5 V Tolerant, 3.3 V Tri-state Slew-Rate Controlled Outputs)**<br>32 serial TDM output data streams. All streams are at the same rate: 65.536 Mbps, 32.678 Mbps, 16.384 Mbps or 8.192 Mbps, programmed by the Global Rate Control Register (Section 12.8).<br>The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 12.3). |
| D5, B1, F3, E2, F1, K1, N1, P3, R4, W2, V4, V6, AB3, AA6, Y9, AB10, V11, W14, Y17, AA19, V18, Y21, W22, U22, N20, M20, K21, J18, F21, G18, D19, B19 | SToB0-31 | **Serial TDM Output Data 'B' Streams (5 V Tolerant, 3.3 V Tri-state Slew-Rate Controlled Outputs)**<br>32 serial TDM output data streams. All streams are at the same rate: 32.678 Mbps, 16.384 Mbps or 8.192 Mbps, programmed by the Global Rate Control Register (Section 12.8). These streams are unused when the device data rate is 65.536 Mbps.<br>The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 12.3).<br>Unused outputs are tristated and may be left unconnected. |
| E6, D3, H4, F2, K4, L3, N2, R2, T3, V3, U5, Y4, U8, AB5, AB8, W11, V12, Y15, W16, AA20, U18, V20, T20, T22, N18, L22, J22, J19, H18, F19, E18, F14 | SToC0-31 | **Serial TDM Output Data 'C' Streams (5 V Tolerant, 3.3 V Tri-state Slew-Rate Controlled Outputs)**<br>32 serial TDM output data streams. All streams are at the same rate: 16.384 Mbps or 8.192 Mbps, programmed by the Global Rate Control Register (Section 12.8). These streams are unused when the device data rate is 65.536 Mbps or 32.678 Mbps.<br>The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 12.3).<br>Unused outputs are tristated and may be left unconnected. |

**Pin Description (continued)**

| Pin | Name | Description |
|---|---|---|
| D4, F4, G3, G2, G1, L2, N3, T1, U2, T6, V5, AA3, W7, AA7, W10, Y11, Y12, AB17, AA18, W18, V19, AA22, U21, N17, P22, L21, L17, H20, D22, E20, C20, D16 | SToD0-31 | **Serial TDM Output Data 'D' Streams (5 V Tolerant, 3.3 V Tri-state Slew-Rate Controlled Outputs)**<br>32 serial TDM output data streams. All streams are at the same rate: 16.384 Mbps or 8.192 Mbps, programmed by the Global Rate Control Register (Section 12.8). These streams are unused when the device data rate is 65.536 Mbps or 32.678 Mbps.<br>The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 12.3).<br>Unused outputs are tristated and may be left unconnected. |
| W12 | $\overline{\text{CKi}}$0 | **ST-BUS/GCI-Bus Clock Input (5 V Tolerant Schmitt-Triggered Input)**<br>This pin accepts an 8.192 MHz, 16.384 MHz, 32.678 MHz or 65.536 MHz clock. This clock must be provided for correct operation of the ZL50074. The frequency of the $\overline{\text{CKi}}$0 input is selected by the CK_SEL1-0 inputs. The active clock edge may be either rising or falling, programmed by the Input Clock Control Register (Section 12.4). |
| AA13 | $\overline{\text{FPi}}$0 | **ST-BUS/GCI-Bus Frame Pulse Input (5 V Tolerant Input)**<br>This pin accepts the 8 kHz frame pulse which marks the frame boundary of the TDM data streams. The pulse width is nominally one $\overline{\text{CKi}}$0 clock period (assuming ST-BUS mode) selected by the CK_SEL1-0 inputs. The active state of the frame pulse may be either high or low, programmed by the Input Clock Control Register (Section 12.4). |
| J2, G21 | $\overline{\text{CKi}}$1-2 | **ST-BUS/GCI-Bus Clock Inputs (5 V Tolerant Schmitt Triggered Inputs)**<br>These optional TDM clock inputs are at 8.192 MHz, 16.384 MHz, 32.678 MHz or 65.536 MHz. The frequency of each clock input is automatically detected by the ZL50074. Refer to Section 2.0 for TDM timing options. The active clock edge may be either rising or falling, programmed by the Input Clock Control Register (Section 12.4). Unused inputs must be connected to a defined logic level. |
| K3, K19 | $\overline{\text{FPi}}$1-2 | **ST-BUS/GCI-Bus Frame Pulse Inputs (5 V Tolerant Inputs)**<br>These 8 kHz input pulses correspond to the optional $\overline{\text{CKi}}$2-1 clock inputs. The frame pulses mark the frame boundary of the TDM data streams. Refer to Section 2.0 for TDM timing options. Each pulse width is nominally one $\overline{\text{CKi}}$ clock period (assuming ST-BUS mode). The active state of the frame pulse may be either high or low, programmed by the Input Clock Control Register (Section 12.4). Unused inputs must be connected to a defined logic level. |

**Pin Description (continued)**

| Pin | Name | Description |
|---|---|---|
| A1, AB4, R18, E14 | $\overline{\text{CKo}}$0-3 | **ST-BUS/GCI-Bus Clock Outputs (3.3 V Outputs with Slew-Rate Control)**<br>These clock outputs can be programmed to generate 8.192 MHz, 16.384 MHz, 32.678 MHz or 65.536 MHz TDM clock outputs. The active edge can be programmed to be either rising or falling. The source of the clock outputs can be derived from either the $\overline{\text{CKi}}$2-0 inputs or the internal system clock. The frequency, active edge and source of each clock output can be programmed independently by the Output Clock Control Register (Section 12.5). For 65.536 MHz output clock, the total loading on the output should not be larger than 10pF. |
| G5, Y6, T19, C17 | $\overline{\text{FPo}}$0-3 | **ST-BUS/GCI-Bus Frame Pulse Outputs (3.3 V Outputs with Slew-Rate Control)**<br>These 8 kHz output pulses mark the frame boundary of the TDM data streams. The pulse width is nominally one clock period of the corresponding $\overline{\text{CKo}}$ output. The active state of each frame pulse may be either high or low, independently programmed by the Output Clock Control Register (Section 12.5). |
| W15, V14 | CK_SEL0-1 | **Master Clock Input Select (5 V Tolerant Inputs)**<br>Inputs used to select the frequency and frame alignment of $\overline{\text{CKi}}$0 and $\overline{\text{FPi}}$0:<br>CK_SEL1 = 0, CK_SEL0 = 0, 8.192 MHz<br>CK_SEL1 = 0, CK_SEL0 = 1, 16.384 MHz<br>CK_SEL1 = 1, CK_SEL0 = 0, 32.768 MHz<br>CK_SEL1 = 1, CK_SEL0 = 1, 65.536 MHz |
| L1 | ODE | **Output Drive Enable (5 V Tolerant Input with Internal Pull-up)**<br>This is the asynchronous output enable control for the output streams. When it is high, the streams are enabled. When it is low, the output streams are tristated. |
| A18, J21, M22, R3, V13, W13, Y13, AA16, AA17 | IC | **Internal Connections**<br>In normal mode these pins **MUST** be connected low |
| AB13, AB14 | NC | **No Connection**<br>In normal mode these pins **MUST** be left unconnected. |
| **Microprocessor Port and Reset** | | |
| A11, C11, E11, B11, A10, B10, C10, A9, D10, B9, F11, A8, C9, B8, E10, A7, A6, D9, E9, C8, A5, B6, C7, D8, E8, A4, B5, C6, D7, F8, A3, B4 | D0-31 | **Microprocessor Port Data Bus (5 V Tolerant Bi-directional with Slew-Rate Output Control)**<br>32 or 16 bit bidirectional data bus. Used for microprocessor access to internal memories and registers. When 16 bit mode is selected (D16B is logic 1), D31-16 are unused and must be connected to defined logic levels. |
| B16, A17, A16, C14, E13, D13, B15, A15, B14, C13, A14, B13, E12, D12, A13, C12, D11, B12, A12 | A0-18 | **Microprocessor Port Address Bus (5 V Tolerant Inputs)**<br>19 bit address bus for the internal memories and registers. In 16 bit bus mode (D16B is logic 1), please note A0 is not used and must be connected to a defined logic level.<br>In Intel 32 bit mode: A1 = $BE_3$, A0 = $BE_2$ |
| C16 | $\overline{\text{CS}}$ | **Chip Select Input (5 V Tolerant Input)**<br>Active low input used with $\overline{\text{DS}}$ to enable read and write access to the ZL50074. |

**Pin Description (continued)**

| Pin | Name | Description |
|---|---|---|
| D14 | $\overline{DS}$ | **Data Strobe Input (5 V Tolerant Input)**<br>Active low input used with $\overline{CS}$ to enable read and write access to the ZL50074. |
| C15 | R/$\overline{W}$ | **Read/Write Input (5 V Tolerant Input)**<br>This input controls the direction of the data bus lines (D31 - 0) during a microprocessor access. This pin is set high and low for the read and write access respectively. |
| A19 | $\overline{DTA}$ | **Data Transfer Acknowledge (5 V Tolerant, 3.3 V Tri-state Output with Slew-Rate)**<br>This active low output indicates that a data bus transfer is complete. An external pull-up resistor is required to hold this pin HIGH when output is high-impedance. |
| B17 | $\overline{BERR}$ | **Transfer Bus Error Output with Slew Rate Control (5 V Tolerant, 3.3 V Tri-state Outputs with Slew-Rate Control)**<br>This pin goes low whenever the microprocessor attempts to access an invalid memory space inside the device. In Motorola bus mode, if this bus error signal is activated, the data transfer acknowledge signal, $\overline{DTA}$, will not be generated. In Intel bus mode, the generation of the $\overline{DTA}$ is not affected by this $\overline{BERR}$ signal. An external pull-up resistor is required to hold a HIGH level when output is high-impedance. |
| D15 | $\overline{WAIT}$ | **Data Transfer Wait Output (5 V Tolerant, 3.3 V Tri-state Output with Slew Rate)**<br>Active low wait signal output. An external pull-up resistor is required to hold this pin HIGH when output is high-impedance. |
| B18, E15 | SIZ0-1 | **Data Transfer Size/Upper and Lower Data Strobe Inputs (5 V Tolerant Inputs)**<br>Motorola 32-bit mode - signals indicate data transfer size, refer to Section 8.0.<br>Motorola 16-bit mode:SIZ0 - $\overline{LDS}$, SIZ1 - $\overline{UDS}$.<br>Active low upper and lower data strobes, $\overline{UDS}$ and $\overline{LDS}$, indicate whether the upper byte, D15 - 8, and/or lower byte, D7 - 0, is being accessed.<br>Intel 32/16-bit mode: SIZ0 - $\overline{BE0}$, SIZ1 - $\overline{BE1}$<br>Active low Intel type bus-enable signals, $\overline{BE1}$ and $\overline{BE0}$ |
| C5 | IM | **Microprocessor Port Bus Mode Select (5 V Tolerant Input)**<br>Control input:<br>0 = Motorola mode<br>1 = Intel mode |
| B7 | D16B | **Microprocessor Port Bus 16/32 Bit Mode Select (5 V Tolerant Input with Internal Pull-down)**<br>Control input:<br>0 = 32 bit data bus<br>1 = 16 bit data bus |

**Pin Description (continued)**

| Pin | Name | Description |
|---|---|---|
| A20 | $\overline{\text{PWR}}$ | **Device Reset (5 V Tolerant Schmitt-Triggered Input)**<br>Asynchronous reset input used to initialize the ZL50074.<br>0 = Reset<br>1 = Normal<br>See Section 9.0, Power-up and Initialization of the ZL50074 for detailed description of Reset state. |
| **IEEE 1149.1 Test Access Port (TAP)** | | |
| D18 | TDi | **Test Data (5 V Tolerant Input with Internal Pull-up)**<br>Serial test data input. When not used, this input may be left unconnected. |
| B21 | TDo | **Test Data (3.3 V Output)**<br>Serial test data output |
| A22 | TCK | **Test Clock (5 V Tolerant Schmitt-Triggered Input with Internal Pull-up)**<br>Provides the clock to the JTAG test logic |
| C19 | $\overline{\text{TRST}}$ | **Test Reset (5 V Tolerant Schmitt-Triggered Input with Internal Pull-up)**<br>Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low during power-up to ensure that the device is in the normal functional mode. When JTAG is not being used, this pin should be pulled low during normal operation. |
| E17 | TMS | **Test Mode Select (5 V Tolerant Input with Internal Pull-up)**<br>JTAG signal that controls the state transitions of the TAP controller. When not used, this pin is pulled high by an internal pull-up resistor and may be left unconnected. |

# 1.0 Functional Description

## 1.1 Overview

The device has 128 ST-BUS/GCI-Bus inputs (STiA0 - 31, STiB0 - 31, STiC0 - 31, STiD0 - 31) and 128 ST-BUS/GCI-Bus outputs (SToA0 - 31, SToB0 - 31, SToC0 - 31, SToD0 - 31). It is a non-blocking digital switch with 32,768 64 kbps channels and is capable of operating at 8.192 Mbps, 16.384 Mbps, 32.768 Mbps or 65.536 Mbps. The inputs accept serial data streams and the outputs deliver serial data streams at one of these data rates. All input and output streams operate at the same rate. There are 32 input groups with each group consisting of 4 streams (‘A’, ‘B’, ‘C’ and ‘D’). If the data rate is set to 16.384 Mbps or 8.192 Mbps, STiA0 - 31, STiB0 - 31, STiC0 - 31 and STiD0 - 31 are used for the input traffic. When the data rate is set to 32.768 Mbps, STiA0 - 31 and STiB0 - 31 are used for the input traffic; STiC0 - 31 and STiD0 - 31 are not used. When the data rate is set to 65.536 Mbps, STiA0 - 31 are used for the input traffic; STiB0 - 31, STiC0 - 31, and STiD0 - 31 are not used. There are 32 output groups with each group consisting of 4 streams (‘A’, ‘B’, ‘C’, and ‘D’). If the data rate is set to 16.384 Mbps or 8.192 Mbps, SToA0 - 31, SToB0 - 31, SToC0 - 31 and SToD0 - 31 are used for the output traffic. If the data rate is set to 32.768 Mbps, SToA0 - 31 and SToB0 - 31 are used for the output traffic; STiC0 - 31 and STiD0 - 31 are in high impedance. When the data rate is set to 65.536 Mbps, SToA0 - 31 are used for the output traffic; SToB0 - 31, SToC0 - 31, and SToD0 - 31 are in high impedance.

By using Zarlink’s message mode capability, the microprocessor can store data in the connection memory which can be broadcast to the output streams on a per-channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS/GCI-Bus devices.

The ZL50074 uses the ST-BUS/GCI-Bus master input frame pulse ($\overline{FPi0}$) and the ST-BUS/GCI-Bus master input clock ($\overline{CKi0}$) to define the input frame boundary and timing for sampling the ST-BUS/GCI-Bus input streams. The rate of the input clock is defined by setting the CK_SEL1 - 0 pins. In addition, two more frame pulses and clocks can be accepted. The frequencies of these signals are automatically detected by the ZL50074.

A selectable Motorola or Intel compatible non-multiplexed microprocessor port allows users to program the device to operate in various modes under different switching configurations. Users can use the microprocessor port to perform internal register and memory read and write operations. The microprocessor port can be selectable to be either a 32 bit or 16 bit data bus and to have either a 19 bit or 17 bit address bus. This is selected by setting the D16B pin. There are seven control signals ($\overline{CS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{DTA}$, $\overline{WAIT}$, $\overline{BERR}$ and IM).

The device supports the mandatory requirements for the IEEE 1149.1 (JTAG) standard via the test port.

## 1.2 Switching Configuration

The ZL50074 switches 64 kbps and Nx64 kbps data and voice channels from the TDM input streams, to timeslots in the TDM output streams. The device is non-blocking; all 32 K input channels can be switched through to the outputs. Any input channel can be switched to any available output channel. The maximum switching capacity and the number of channels per stream are shown in Table 1 for different data rates of operation.

| TDM Stream Data Rate | Number of Input TDM Data Streams | Number of Output TDM Data Streams | Number of 64 kbps Channels per Stream | Maximum Switch Capacity (streams x channels = total) |
|---|---|---|---|---|
| 65 Mbps | 32 | 32 | 1024 | 32 x 1024 = 32,768 |
| 32 Mbps | 64 | 64 | 512 | 64 x 512 = 32,768 |
| 16 Mbps | 128 | 128 | 256 | 128 x 256 = 32,768 |
| 8 Mbps | 128 | 128 | 128 | 128 x 128 = 16,384 |

**Table 1 - Data Rate and Maximum Switch Size**

## 1.3 Stream Provisioning

The ZL50074 is a large switch with a comprehensive list of user configurable, ’per-group’ programmable features. In order to facilitate ease of use, the ZL50074 offers a simple programming model. Streams are grouped in sets of four, with each group sharing the same configured characteristics. In this way it is possible to reduce programming complexity, while still maintaining flexible ’per-group’ configuration options:

- Input stream clock source selection, see Section 2.0
- Output stream clock source selection, see Section 2.0
- Input stream sampling point selection, see Section 5.1
- Output stream fractional bit advance, see Section 5.2
- Input and output stream inversion control; see Section 12.3

There are 32 input and 32 output groups. Depending on the data rate set for the device there will be either 1, 2 or 4 streams activated in each group. If the data rate is set for 65.536 Mbps, the ‘A’ streams will be activated; the ‘B’, ‘C’ and ‘D’ streams will not be activated. If the data rate is set for 32.768 Mbps, the ‘A’ and ‘B’ streams will be activated; the ‘C’ and ‘D’ streams will not be activated. If the data rate is set for 16.384 Mbps or 8.192 Mbps, the ‘A’, ‘B’, ‘C’ and ‘D’ streams will all be activated. The maximum channel capacity of a group is 1024 channels when operating at any data rate except for 8.192 Mbps, in which case the maximum operating channel capacity decreases to 512 channels.

Table 1 shows the maximum number of streams available at different bit rates. The ZL50074 deactivates unused streams when operating at the higher bit rates as shown in Table 2.

| Input or Output Group n (n = 0 - 31) | 65 Mbps | 32 Mbps | 16 Mbps | 8 Mbps |
|---|---|---|---|---|
| STiAn / SToAn | Active | Active | Active | Active |
| STiBn / SToBn | Not Active | Active | Active | Active |
| STiCn / SToCn | Not Active | Not Active | Active | Active |
| STiDn / SToDn | Not Active | Not Active | Active | Active |

**Table 2 - TDM Stream Bit Rates**

All TDM input and output data streams operate at the same rate, programmed by the Global Rate Control Register (Section 12.8).

## 2.0 Input Clock ($\overline{\text{CKi}}$) and Input Frame Pulse ($\overline{\text{FPi}}$) Timing

The input timing for the ZL50074 can be set for one of four different frequencies. They can also be set for ST-BUS or GCI-Bus mode with positive or negative input. The $\overline{\text{CKi}}$0 and $\overline{\text{FPi}}$0 input timing must be provided in order for the device to be used. There are two additional input clocks and frame pulses that can be provided. CKi0 is used to generate the internal clock. This clock is used for all the internal logic and can be used as one of the clocks that defines the timing for the input and output data. The input stream clock source is selected by the ISSRC1 - 0 (bits 1 - 0) in the Group Control Register. The output stream clock source is selected by the OSSRC1 - 0 (bits 17 - 16) in the Group Control Register.

The $\overline{\text{CKi}}$0 and $\overline{\text{FPi}}$0 input frequency is set via the CK_SEL1 - 0 pins as shown in Table 3. By default the $\overline{\text{CKi}}$0 and $\overline{\text{FPi}}$0 pins accept ST-BUS, negative input timing. The input frame pulse format (ST-BUS/GCI-Bus), frame pulse polarity, and clock polarity can be programmed by the GCISEL0 (bit 2), FPIPOL0 (bit 1), and CKIPSL0 (bit 0) in the Input Clock Control Register (ICCR), as described in Section 12.4.

| CK_SEL1 | CK_SEL0 | Input $\overline{\text{CKi}}$0 and $\overline{\text{FPi}}$0 |
|---|---|---|
| 0 | 0 | 8.192 MHz |
| 0 | 1 | 16.384 MHz |
| 1 | 0 | 32.768 MHz |
| 1 | 1 | 65.536 MHz |

**Table 3 - $\overline{\text{CKi}}$0 and $\overline{\text{FPi}}$0 Setting via CK_SEL1 - 0**

Two additional input clocks ($\overline{\text{CKi}}$2 - 1) and frame pulses ($\overline{\text{FPi}}$2 - 1) can be accepted. These signals can be 8.192 MHz, 16.384 MHz, 32.768 MHz or 65.536 MHz and the rates are automatically detected by the device. These clocks and their frame boundaries must be phase aligned with the $\overline{\text{CKi}}$0 and its frame boundary within a 30 ns skew but can have different jitter values. The clocks do not have to have the same frequency. If these additional clocks are not used, the pins must be connected to a defined logic level.

These additional input clocks and frame pulses can be used as alternative clock sources for the input streams, output streams, and output clocks / frame pulses. The input streams' clock sources are controlled by the ISSRC1-0 (bits 1 - 0) in the Group Control Registers (GCR). The output streams' clock sources are controlled by the OSSRC1-0 (bits 17 - 16) in the Group Control Registers (GCR). The output clocks' / frame pulses' clock sources are controlled by the CKO3SRC1-0 (bits 22-21), CKO2SRC1-0 (bits 15-14), CKO1SRC1-0 (bits 8-7), and CKO0SRC1-0 (bits 1-0) in the Output Clock Control Register (OCCR). The clock sources can be set to either the internal system clock or one of the three input clock signals. These are used to provide a direct interface to jittery peripherals.

When the internal system clock is not used as the clock source, there are limitations to the data rate and the output clock rate. For all the input and output stream groups that do not use the internal system clock as their clock source, the data rate is limited to be no higher than the selected clock source's rate (e.g., if $\overline{CKi1}$ runs at 16.384 MHz and it is selected as the clock source for input stream group 3, then the maximum data rate of STiA3, STiB3, STiC3, and STiD3 is 16.384 Mbps). Similarly, for all the output clocks that do not use the internal system clock as their clock source, the clock rate is limited to be no higher than the selected clock source's rate (e.g., if $\overline{CKi1}$ runs at 32.768 MHz and it is selected as the clock source for output clock $\overline{CKo0}$, then the maximum clock rate of $\overline{CKo0}$ is 32.768 MHz).

## 3.0 Output Clock ($\overline{CKo}$) and Output Frame Pulse ($\overline{FPo}$) Timing

There are four output timing pairs, $\overline{CKo3}$ - 0 and $\overline{FPo3}$ - 0. By default these signals generate ST-BUS, negative timing, and use the internal system clock as reference clock source. Their default clock rates are 65.536 MHz for $\overline{CKo0}$, 32.768 MHz for $\overline{CKo1}$, 16.384 MHz for $\overline{CKo2}$, and 8.192 MHz for $\overline{CKo3}$. Their properties can also be individually programmed in the Output Clock Control Register (OCCR) to control the frame pulse format (ST-BUS/GCI-Bus), frame pulse polarity, clock polarity, clock rate (8.192 MHz, 16.384 MHz, 32.768 MHz or 65.536 MHz), and reference clock source. Refer to Section 12.5 for programming details. Note that the reference clock source can be set to either the internal system clock or one of the three input clock signals. If one of the three input clock signals is selected as the reference source, the output clock cannot be programmed to generate a higher clock frequency than the reference source. As each output timing pair has its own bit settings, they can be set to provide different output timings. For 65.536 MHz output clock, the total loading on the output should not be larger than 10pF.

## 4.0 Output Channel Control

To be able to interface with external buffers, the output signals can be set to enter a high impedance or drive high state on a per-channel basis. The Per Channel Function (bits 31 - 29) in the Connection Memory Bits can be set to 001 to drive the channel output high, or to 000, 110 or 111, to set the channel into a high impedance state.

## 5.0 Data Input Delay and Data Output Advancement

The Group Control Registers (GCR) are used to adjust the input delay and output advancement for each input and output data groups. Each group is independently programmed.

### 5.1 Input Sampling Point Delay Programming

The input sampling point delay programming feature provides users with the flexibility of handling different wire delays when incoming traffic is from different sources.

By default, all input streams have zero delay, such that bit 7 is the first bit that appears after the input frame boundary (assuming ST-BUS formatting). The nominal input sampling point with zero delay is at the 3/4 bit time. The input delay is enabled by the Input Sample Point Delay (bit 8 - 4) in the Group Control Registers 0 - 31 (GCR0 - 31) as described in Section 12.3 on page 36. The input sampling point delay can range from 0 to 7 3/4 bit delay with a 1/4 bit resolution on a per group basis.

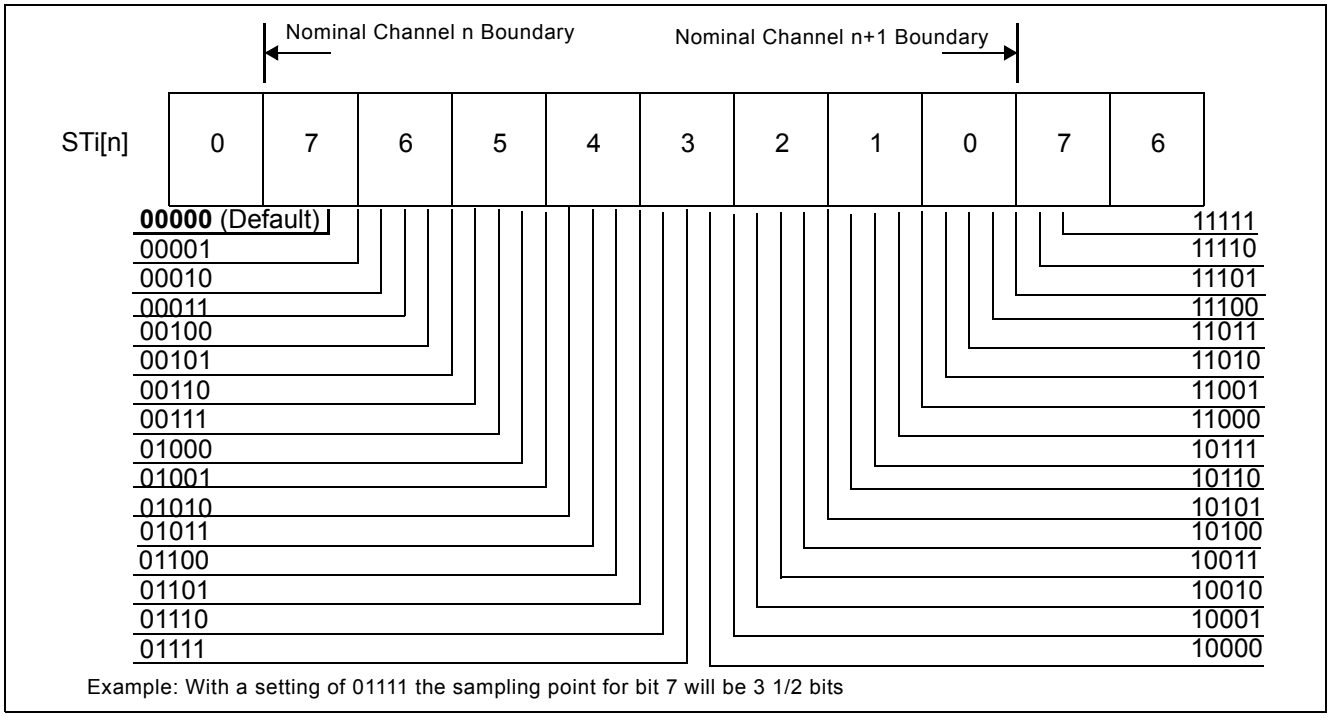



**Figure 2 - Input Sampling Point Delay Programming**

There are limitations when the ZL50074 is programmed to use $\overline{CKi}2$ - 0 as the input stream clock source as opposed to the internal clock:

- The granularity of the delay becomes 1/2 the selected reference clock period, or 1/4 bit, whichever is longer.
- If the selected reference clock frequency is the same as the stream bit rate, the granularity of the delay is 1/2 bit. In this case, the least significant bit of the ISPD register is not used; the remaining 4 bits select the total delay in 1/2 bit increments, to a maximum of 7 1/2 bits. Also, the 0 bit delay reference point changes from the 3/4 bit position to the 1/2 bit position.

## 5.2 Fractional Bit Advancement on Output

See Section 12.3, Group Control Registers, for programming details.

This feature is used to advance the output data with respect to the output frame boundary. Each group has its own bit advancement value which can be programmed in the Group Control Registers 0 - 31 (GCR0 - 31).

By default all output streams have zero bit advancement such that bit 7 is the first bit that appears after the output frame boundary (assuming ST-BUS formatting). The output advancement is enabled by the Output Stream Bit Advancement (bits 21 - 20) of the Group Control Registers 0 - 31 (GCR0 - 31), as described in Section 12.3. The output delay can vary from 0 to 22.8 ns with a 7.6 ns increment. The exception to this is when the device is programmed at 65 Mbps, in which case the increment is 3.8 ns with a total advancement of 11.4 ns.

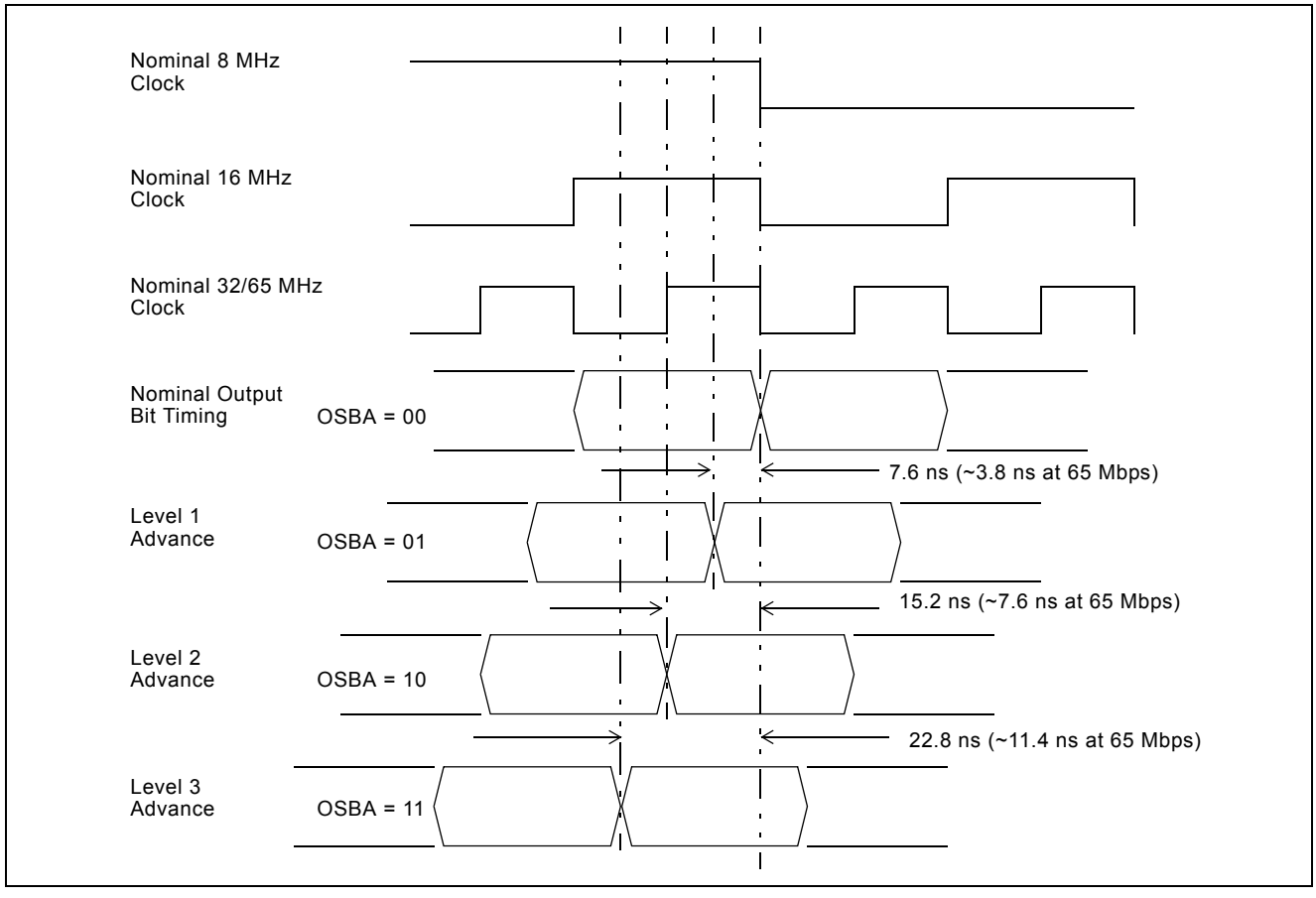



**Figure 3 - Output Bit Advancement Timing**

This programming feature is provided to assist in designs where per stream routing delays are significant and different.

The OSBA bits in the Group Control Registers are used to set the bit-advancement for each of the corresponding serial output stream groups. Figure 3 illustrates the effect of the OSBA settings on the output timing.

There are limitations when the ZL50074 is programmed to use $\overline{CKi}$2 - 0 as the output stream clock source:

- If the selected reference clock frequency is 65 MHz or 32 MHz, the granularity of the advancement is reduced to 1/2 the clock period.
- If the selected reference clock frequency is 16 MHz or 8 MHz, bit advancement is not available and the output streams are driven at the nominal times.

## 6.0 Message Mode

In Message Mode (MSG), microprocessor data can be broadcast to the output data streams on a per-channel basis. This feature is useful for transferring control and status information to external circuits or other TDM devices.

For a given output channel, when the corresponding Per Channel Function (bits 31 - 29) in the Connection Memory are set to Message Mode (010), the Connection Memory's lowest data byte (bits 7 - 0) is output in the timeslot. Refer to Section 12.1.1, Connection Memory Bit Functions, for programming details.

To increase programming bandwidth, the ZL50074 has separate addressable 32 bit memory locations, called Connection Memory Least Significant Bytes (LSB), which provide direct access to the Connection Memories' Lowest data bytes (bits 7 - 0). Up to four consecutive message mode channels can be set with one Connection Memory LSB access. Refer to Section 12.1.2, Connection Memory LSB, for programming details.

### 6.1 Data Memory Read

All TDM input channels can be read via the microprocessor port. This feature is useful for receiving control and status information from external circuits or other TDM devices. Each 32 bit Data Memory access enables up to four consecutive input channels to be monitored. The Data Memory field is read only; any attempt to write to this address range will result in a bus error condition signalled back to the host processor. Refer to Section 12.2, Data Memory, for programming details.

The latency of data reads is up to 3 frames, depending on when the input timeslots are sampled.

### 6.2 Connection Memory Block Programming

See Section 12.6, Block Init Register, and Section 12.7, Block Init Enable Register, for programming details.

This feature allows for fast initialization of the connection memory after power up. When the block programming mode is enabled, the contents of Block Init Register are written to all Connection Memory Bits. This operation completes in one 125 μs frame. During Connection Memory initialization, all TDM output streams are set to high impedance.

## 7.0 Data Delay Through the Switching Paths

See Section 12.1.1, Connection Memory Bit Functions, for programming details.

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform timeslot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, select variable throughput delay to ensure minimum delay between input and output data. In wideband data application, select constant delay to maintain the frame integrity of the information through the switch. The delay through the device varies according to the type of throughput delay selected by programming the Per Channel Function (bits 31 - 29) in the Connection Memories. When these bits are set to 011, the channel is in variable delay mode. When they are set to 100, the channel is in constant delay mode.

### 7.1 Constant Delay Mode

In this mode the frame integrity is maintained in all switching configurations. The delay though the switch is 2 frames - Input Channel + Output Channel. This can result in a minimum delay of 1 frame + 1 channel if the last channel of a stream is switched to the first channel of a stream. The maximum delay is 1 channel short of 3 frames delay. This occurs when the first channel of a stream is switched to the last channel of a stream.

The data throughput delay is expressed as a function of ST-BUS/GCI-Bus frames, input channel number (n) and output channel number (m). The data throughput delay (T) is:

**T = 2 frames + (n - m)**

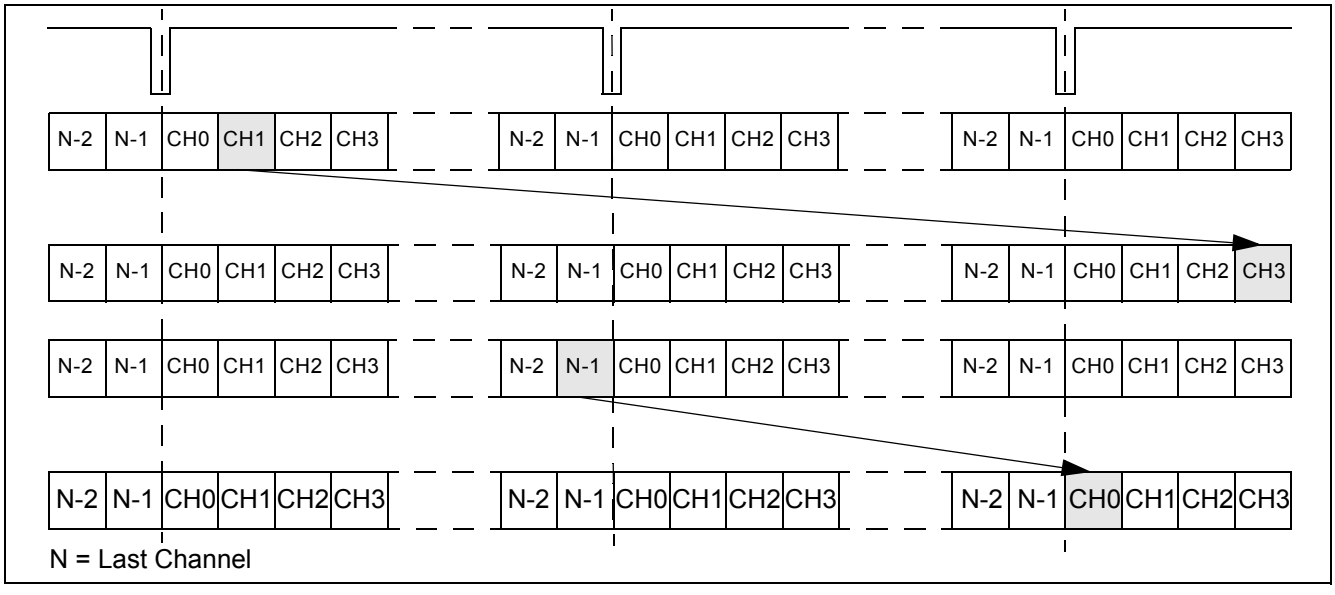



**Figure 4 - Data Throughput Delay for Constant Delay**

## 7.2 Variable Delay Mode

Variable delay mode causes the output channel to be transmitted as soon as possible. This is a useful mode for voice applications where the minimum throughput delay is more important than data integrity. The delay through the switch is minimum 3 channels and maximum 1 frame + 2 channels.

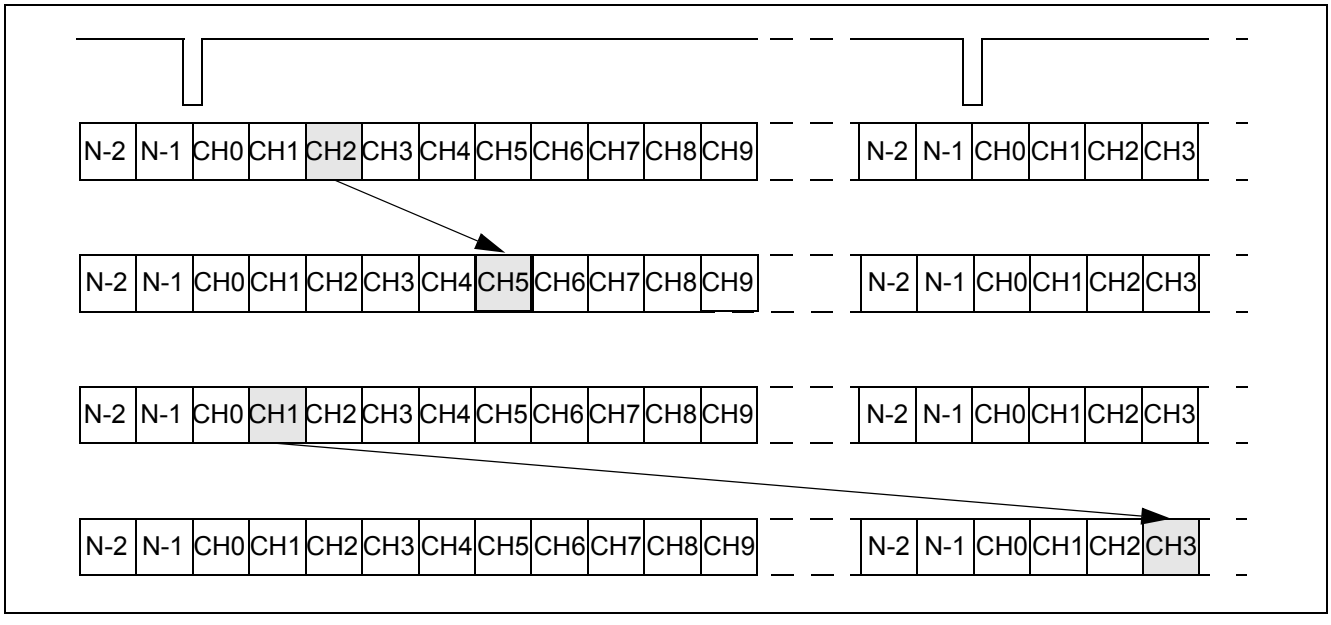



**Figure 5 - Data Throughput Delay for Variable Delay**

## 8.0 Microprocessor Port

The ZL50074 has a generic microprocessor port that provides access to the internal Data Memory (read access only), Connection Memory and Control Registers.

The port size can be configured to be either 32 bit or 16 bit, controlled by the D16B pin.

The port works with either Motorola or Intel type microprocessor buses, selected by the IM pin.

### 8.1 Addressing

The Data Memory, Connection Memory and Control Registers are assigned 32 bit fields in the ZL50074 memory space. The Address Bus, A18 - 0, controls access to each 32 bit location. Byte addressing is also provided to give the user programming flexibility, if access to less than 32 bits is required.

Each 32 bit memory or register location spans four consecutive addresses. Example:

- The 32 bit Group Control Register for TDM Group 0 is located at address range 40200 - 40203 Hex

The Least Significant address identifies the Most Significant Byte (MSB) in the 32 bit field, as illustrated in Table 4.

| Address (Hex) | Memory/Register Bits |
|---|---|
| 40200 | Bits 31:24 (MSB) |
| 40201 | Bits 23:16 |
| 40202 | Bits 15:8 |
| 40203 | Bits 7:0 (LSB) |

**Table 4 - Example of Address and Byte Significance**

### 8.2 32 Bit Bus Operation

In 32 bit mode (D16B = 0), all 32 bits of the Data Bus, D31 - 0, may be used for write and read transfers. D31 on the bus maps to Bit 31 of the internal memory or register, D30 maps to Bit 30, etc. The least significant address bits, A1 - 0, and the Data Transfer Size inputs, SIZ0 - 1, identify which bytes are being accessed.

In Motorola Bus mode (IM = 0), A1 - 0 identify the first byte in the 32 bit field to be transferred, as shown in Table 5. The SIZ0 - 1 inputs indicate the access transfer size, as shown in Table 6.

| A1 | A0 | Byte Addressed |
|---|---|---|
| 0 | 0 | Bit 31:24 |
| 0 | 1 | Bit 23:16 |
| 1 | 0 | Bit 15:8 |
| 1 | 1 | Bit 7:0 |

**Table 5 - 32 Bit Motorola Mode Byte Addressing**

For example, to transfer all 32 bits in a single access: A1 = 0. A0 = 0, SIZ1 = 0, SIZ0 = 0. To transfer D15 - 8 only: A1 = 1, A0 = 0, SIZ1 = 0, SIZ0 = 1.

| SIZ1 | SIZ0 | Access Transfer Size |
|---|---|---|
| 0 | 0 | 4 bytes |
| 0 | 1 | 1 Byte |
| 1 | 0 | 2 Bytes |
| 1 | 1 | 3 Bytes |

**Table 6 - 32 Bit Motorola Mode Access Transfer Size**

In Intel Bus Mode (IM = 1), A1 - 0, and SIZ1 - 0 form active low byte enable signals, consistent with BE3 - 0 available on the Intel i960 processor, as shown in Table 7.

| Pin | Equivalent i960 Signal | Byte Addressed |
|---|---|---|
| A1 | $\overline{BE3}$ | Bit 31:24 |
| A0 | $\overline{BE2}$ | Bit 23:16 |
| SIZ1 | $\overline{BE1}$ | Bit 15:8 |
| SIZ0 | $\overline{BE0}$ | Bit 7:0 |

**Table 7 - 32 Bit Intel Mode Bus Enable Signals**

Byte addressing applies only to write accesses. On read cycles, all 32 bits are output on every access.

### 8.3 16 Bit Bus Operation

In 16 bit mode (D16B = 1), D15 - 0 are used for data transfers to/from the ZL50074. D31 - 16 are unused and must be connected to a defined logic level. D15 on the bus maps to Bit 31 and Bit 15 of the internal 32 bit memory or register, D14 maps to Bit 30 and Bit 14, etc.

In 16 bit mode, the least significant address bit, A0, is not used, and must be connected to defined logic level. In this case, address bit A1 and the Data Transfer Size inputs, SIZ1 - 0, identify which bytes are being accessed.

In Motorola Bus Mode (IM = 0), SIZ1 - 0 form active low data strobe signals, consistent with $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ available on the MC68000 and MC68302 processors, as shown in Table 8.

In Intel Bus Mode (IM = 1), SIZ1 - 0 form active low byte enable signals, consistent with $\overline{\text{BE1}}$ and $\overline{\text{BE0}}$ available on the Intel i960 processor, as shown in Table 8.

| Pin Name | Motorola Mode MC68000, MC68302 Equivalent Function IM = 0 | Intel Mode i960 Equivalent Function IM = 1 | Data Bus Bytes Enabled |
|---|---|---|---|
| SIZ1 | $\overline{\text{UDS}}$ | $\overline{\text{BE1}}$ | D15-8 |
| SIZ0 | $\overline{\text{LDS}}$ | $\overline{\text{BE0}}$ | D7-0 |

**Table 8 - Byte Enable Signals**

In both Intel and Motorola modes, the A1 address input is used to identify the word alignment in internal memory.

A1 = 0 Bits 31:16

A1 = 1 Bits 15:0

16-bit word alignment are shown in Table 9. An example of byte addressing is given in Table 10.

| Microprocessor 16 Bit Data Bus | SIZ1 | SIZ0 | A1 | Internal 32-Bit Memory or Register |
|---|---|---|---|---|
| D15 - 8 | 0 | 1 | 0 | Bits 31:24 |
| | 0 | 1 | 1 | Bits 15:8 |
| D7 - 0 | 1 | 0 | 0 | Bits 23:16 |
| | 1 | 0 | 1 | Bits 7:0 |
| D15 - 0 | 0 | 0 | 0 | Bits 31:16 |
| | 0 | 0 | 1 | Bits 15:0 |
| | 1 | 1 | X[1] | No access |

**Table 9 - 16 Bit Mode Word Alignment**

1. X - Don’t Care

| Address (Hex) | Register Description | Register Byte | A18 - 0 (binary) | SIZ1 | SIZ0 | Comments |
|---|---|---|---|---|---|---|
| 40200 or 40201 | Group Control Register (Group 0) | Bits 23:16 | 100 0000 0010 0000 000X† | 1 | 0 | 8 bit transfer |
| 40282 or 40283 | Input Clock Control Register | Bits 15:8 | 100 0000 0010 1000 001X† | 0 | 1 | 8 bit transfer |
| 40286 or 40287 | Output Clock Control Register | Bits 15:0 | 100 0000 0010 1000 011X† | 0 | 0 | 16 bit transfer |
| 40284 or 40285 | Output Clock Control Register | Bits 31:16 | 100 0000 0010 1000 010X† | 0 | 0 | 16 bit transfer |

**Table 10 - 16 Bit Mode Example Byte Address**

† Don't Care. A0 is not used

## 8.4 Bus Operation

### 8.4.1 Read Cycle

The operation of a read cycle is illustrated in Figure 6.

- The microprocessor asserts the R/$\overline{W}$ control signal high, to signal a read cycle. It also drives the address A, transfer size, SIZ1 - 0, and chip select logic drives the $\overline{CS}$ signal active low to select the ZL50074.
- The microprocessor then drives the $\overline{DS}$ signal active low, to signal the start of the bus cycle. The $\overline{DS}$ signal is held low for the duration of the bus cycle.
- $\overline{WAIT}$ is asserted active low
- The ZL50074 accesses the requested memory or register location(s), and places the requested data onto the data bus, D31 - 0 (D15 - 0 in 16 bit Mode). All data bus pins are driven, whether or not they are being used for the specific data transfer. Unused pins will present unknown data. If the address is to an unused area of the memory space, unknown data is presented on the data bus.
- The ZL50074 then de-asserts $\overline{WAIT}$, and asserts either $\overline{DTA}$ or $\overline{BERR}$, depending on the validity of the data transfer
- When the microprocessor observes the active low state of the $\overline{DTA}$ or the $\overline{BERR}$ signal or the low to high transition of the $\overline{WAIT}$ signal, it terminates the bus cycle by driving the $\overline{DS}$ pin inactive high
- When the ZL50074 sees the $\overline{DS}$ signal go inactive high, it removes the assertions on the $\overline{DTA}$ or $\overline{BERR}$ signals by driving them inactive high
- When the ZL50074 sees the $\overline{CS}$ signal go inactive high, it tri-states the data bus, D31 - 0 (D15 - 0 in 16 bit Mode) and the $\overline{DTA}$, $\overline{BERR}$ and $\overline{WAIT}$ signals. However, if $\overline{CS}$ goes inactive high before $\overline{DS}$ goes inactive high, the $\overline{DTA}$, $\overline{BERR}$ and $\overline{WAIT}$ signals are driven inactive high before they are tri-stated.
- In Intel mode, $\overline{DTA}$ is always driven to signal the end of a bus cycle, regardless of $\overline{BERR}$

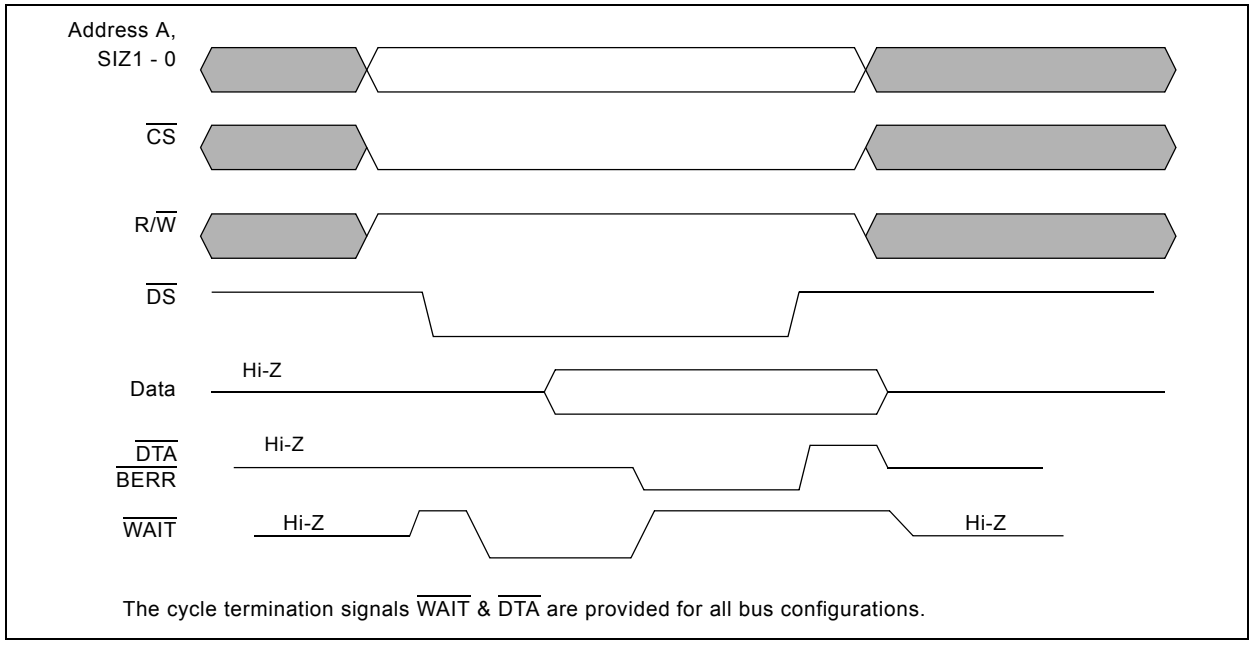



**Figure 6 - Read Cycle Operation**

### 8.4.2 Write Cycle

The operation of the write cycle is illustrated in Figure 7.

- The microprocessor asserts the R/$\overline{W}$ control signal low, to signal a write cycle. It also drives the address A, data transfer size, SIZ1 - 0, and chip select logic drives the $\overline{CS}$ signal active low to select the ZL50074
- The microprocessor then drives the data bus, D31 - 0 (D15 - 0 in 16 bit Mode) with the data to be written, and then drives the $\overline{DS}$ signal active low, to signal the start of the bus cycle. The $\overline{DS}$ signal is held low for the duration of the bus cycle
- $\overline{WAIT}$ is asserted active low
- The ZL50074 transfers the data presented on the data bus pins into the indicated memory or register location(s). If the address is to an unused area of the memory space, or to the data memory, no data is transferred. The microprocessor port cannot write to the Data Memory.
- The ZL50074 then de-asserts $\overline{WAIT}$, and asserts either $\overline{DTA}$ or $\overline{BERR}$, depending on the validity of the data transfer
- When the microprocessor observes the active low state of the $\overline{DTA}$ or the $\overline{BERR}$ signal or the low-to-high transition of the $\overline{WAIT}$ signal, it terminates the bus cycle by driving the $\overline{DS}$ pin inactive high
- When the ZL50074 sees the $\overline{DS}$ signal go inactive high, it removes the assertions on the $\overline{DTA}$ or $\overline{BERR}$ signals by driving them inactive high
- When the ZL50074 sees the $\overline{CS}$ signal go inactive high, it tri-states the $\overline{DTA}$, $\overline{BERR}$ and $\overline{WAIT}$ signals. However, if $\overline{CS}$ goes inactive high before $\overline{DS}$ goes inactive high, the $\overline{DTA}$, $\overline{BERR}$ and $\overline{WAIT}$ signals are driven inactive high before they are tri-stated.
- In Intel mode, $\overline{DTA}$ is always driven to signal the end of a bus cycle, regardless of $\overline{BERR}$

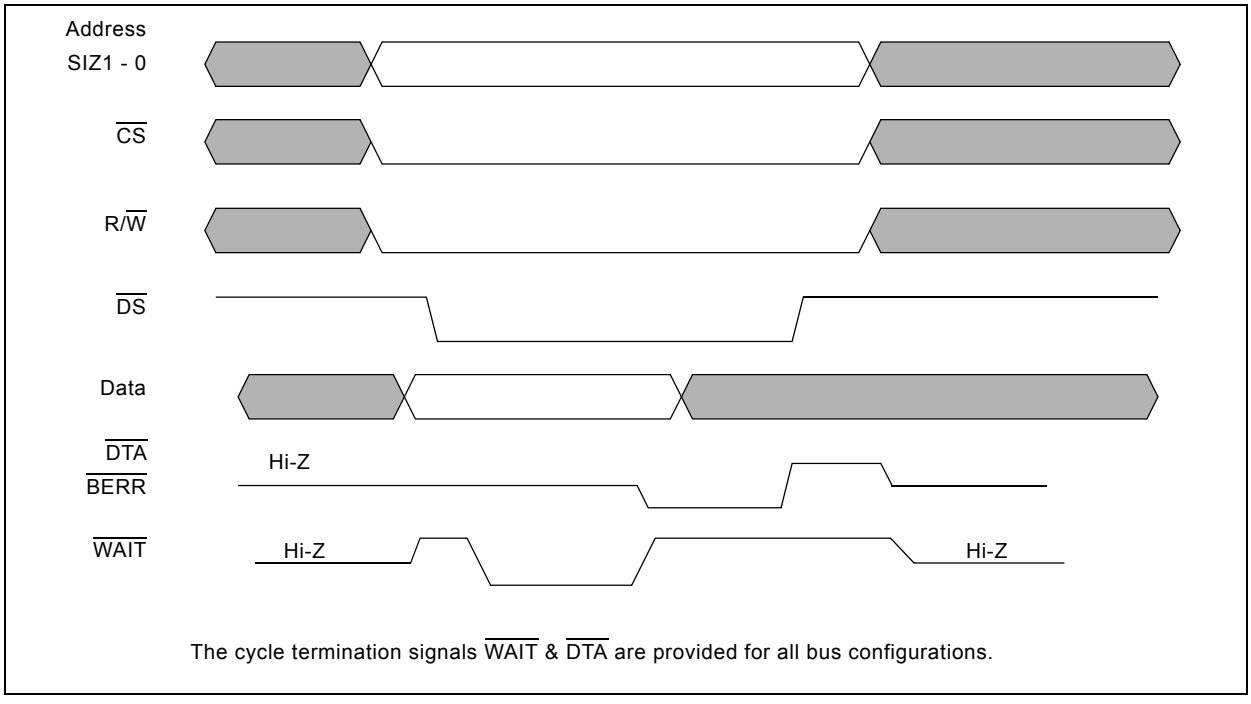



**Figure 7 - Write Cycle Operation**

## 9.0 Power-up and Initialization of the ZL50074

### 9.1 Device Reset and Initialization

The $\overline{PWR}$ pin is used to reset the ZL50074. When this pin is low, the following functions are performed:

- Asynchronously puts the microprocessor port in a reset state
- Tristates all of the output streams (SToA0 - 31, SToB0 - 31, SToC0 - 31, SToD0 - 31)
- Preloads all of the registers with their default values (refer to the individual registers for default values)
- Clears all internal counters

### 9.2 Power Supply Sequencing

The ZL50074 has two separate power supplies: $V_{DD\_IO}$ (3.3 V) and $V_{DD\_CORE}$ (1.8 V). The recommended power-up sequence is for $V_{DD\_IO}$ to be applied first, followed by the $V_{DD\_CORE}$ supply. $V_{DD\_CORE}$ should not lead $V_{DD\_IO}$ supply by more than 0.3 V. Both supplies may be powered-down simultaneously.

### 9.3 Initialization

Upon power up, the ZL50074 should be initialized as follows:

- Assert $\overline{PWR}$ to low immediately after power is applied
- Set the $\overline{TRST}$ pin low to disable the JTAG TAP controller
- Deassert the $\overline{PWR}$ pin.
- Apply the Master Clock Input ($\overline{CKi}0$) and Master Frame Pulse Input ($\overline{FPi}0$) to the values defined by the CK_SEL1 - 0 pins
- Set the ODE pin low to disable the output streams

**Note:** After the $\overline{PWR}$ reset is removed, and on the application of a suitable master clock input, it takes approximately 1ms for the internal initialization to complete

- Automatic block initialization of the Connection Memory to all zeros occurs, without microprocessor intervention
- All Group Control Registers are preset to $000C000C_H$, corresponding to no link inversions, no fractional output bit advancements, internal clock source, and no input sample point delays
- The Input Clock Control Register is preset to $0DB_H$, corresponding to:
  - All clock inputs set to negative logic sense
  - All frame pulse inputs set to negative logic sense
  - All input frame pulses set to ST-BUS timing
- The Output Clock Control Register is pre-set to $060D1C3C_H$, corresponding to:
  - All clock outputs set to negative logic sense
  - All frame pulse outputs set to negative logic sense
  - All output frame pulses set to ST-BUS timing
  - All output clock source selections to internal
  - Clock outputs, $\overline{CKo}0$ - 3 are preset to rates of 65 MHz, 32 MHz, 16 MHz and 8 MHz, respectively
- Global Rate Control Register is set to 00, corresponding to a bit rate of 8 Mbps

**Note**: If the master clock input, $\overline{CKi}0$, is not available, the microprocessor port will assert $\overline{BERR}$ on all accesses and read cycles.

## 10.0 IEEE 1149.1 Test Access Port

The JTAG test port is implemented to meet the mandatory requirements of the IEEE 1149.1 (JTAG) standard. The operation of the boundary-scan circuity is controlled by an external Test Access Port (TAP) Controller.

The ZL50074 uses the public instructions defined in IEEE 1149.1, with the provision of a 16-bit Instruction Register, and three scannable Test Data Registers: Boundary Scan Register, Bypass Register and Device Identification Register.

### 10.1 Test Access Port (TAP)

The Test Access Port (TAP) accesses the ZL50074 test functions. The interface consists of 4 input and 1 output signal. as follows:

- **Test Clock (TCK)** - TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent in the functional mode. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.
- **Test Mode Select (TMS)** - The TAP Controller uses the logic signals received at the TMS input to control test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to $V_{DD\_IO}$ when it is not driven from an external source.
- **Test Data Input (TDi)** - Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to $V_{DD\_IO}$ when it is not driven from an external source.

- **Test Data Output (TDo)** - Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDo. The data out of the TDo is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDo driver is set to a high impedance state.
- **Test Reset ($\overline{\text{TRST}}$)** - Resets the JTAG scan structure. This pin is internally pulled to $V_{DD\_IO}$ when it is not driven from an external source. When JTAG is not in use, this pin must be tied low for normal operation.

The TAP signals are only applied when the ZL50074 is required to be in test mode. When in normal, non-test mode, $\overline{\text{TRST}}$ must be connected low to disable the test logic. The remaining test pins may be left unconnected.

### 10.2 Instruction Register

The ZL50074 uses the public instructions defined in the IEEE 1149.1 standard. The JTAG interface contains a 16-bit instruction register. Instructions are serially loaded into the instruction register from the TDi when the TAP controller is in its shifted-OR state. These instructions are subsequently decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current and to define the serial test data register path that is used to shift data between TDi and TDo during register scanning.

### 10.3 Test Data Register

As specified in the IEEE 1149.1 standard, the ZL50074 JTAG Interface contains three test data registers:

- **The Boundary-Scan Register** - The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the ZL50074 core logic
- **The Bypass Register** - The Bypass register is a single stage shift register that provides a one-bit path from TDi to TDo
- T**he Device Identification Register** - The JTAG device ID for the ZL50074 is $C39A14B_H$

| | | |
|---|---|---|
| Version | <31:28> | 0000 |
| Part Number | <27:12> | 1100 0011 1001 1010 |
| Manufacturer ID | <11:1> | 0001 0100 101 |
| LSB | <0> | 1 |

### 10.4 Boundary Scan Description Language (BSDL)

A Boundary Scan Description Language (BSDL) file is available from Zarlink Semiconductor to aid in the use of the IEEE 1149.1 test interface.

## 11.0 Memory Map of ZL50074

The memory map for the ZL50074 is given in Table 11.

| Address (Hex) | Description |
|---|---|
| 00000 - 1FFFF | Connection Memory |
| 20000 - 27FFF | Connection Memory LSB |
| 28000 - 2FFFF | Data Memory: Read only; Bus error on write ($\overline{\text{BERR}}$) |
| 30000 - 401FF | Invalid Address. Access causes Bus error ($\overline{\text{BERR}}$) |
| 40200 - 4027F | Group Control Registers |
| 40280 - 40283 | Input Clock Control Register |
| 40284 - 40287 | Output Clock Control Register |
| 40288 - 4028B | Block Init Register |
| 4028C - 4028F | Block Init Enable |
| 40290 - 40293 | Global Rate Control Register |
| 40294 - 7FFFF | Invalid Address. Access causes Bus error ($\overline{\text{BERR}}$) |

**Table 11 - Memory Map**

## 12.0 Detailed Memory and Register Descriptions

This section describes all the memories and registers that are used in this device.

### 12.1 Connection Memory

Address range 00000 - 1FFFF hex.

On power-up, all Connection Memory locations are initialized automatically to $00000000_H$, using the Block Initialization feature, as described in Section 12.6 and Section 12.7.

The 32 bit Connection Memory has 32,768 locations. Each 32 bit long-word is used to program the desired source data and any other per-channel characteristics of one output time-slot.

The memory map for the Connection Memory is sub-divided into 32 blocks, each corresponding to one of the possible 32 output stream group numbers. The address ranges for these blocks are illustrated in Table 12.

| Output Group | Start Address (Hex) | Address Range (Hex) | Output Group | Start Address (Hex) | Address Range (Hex) |
|---|---|---|---|---|---|
| 0 | 000000 | 000000 - 000FFF | 16 | 010000 | 010000 - 010FFF |
| 1 | 001000 | 001000 - 001FFF | 17 | 011000 | 011000 - 011FFF |
| 2 | 002000 | 002000 - 002FFF | 18 | 012000 | 012000 - 012FFF |
| 3 | 003000 | 003000 - 003FFF | 19 | 013000 | 013000 - 013FFF |
| 4 | 004000 | 004000 - 004FFF | 20 | 014000 | 014000 - 014FFF |
| 5 | 005000 | 005000 - 005FFF | 21 | 015000 | 015000 - 015FFF |
| 6 | 006000 | 006000 - 006FFF | 22 | 016000 | 016000 - 016FFF |
| 7 | 007000 | 007000 - 007FFF | 23 | 017000 | 017000 - 017FFF |
| 8 | 008000 | 008000 - 008FFF | 24 | 018000 | 018000 - 018FFF |
| 9 | 009000 | 009000 - 009FFF | 25 | 019000 | 019000 - 019FFF |
| 10 | 00A000 | 00A000 - 00AFFF | 26 | 01A000 | 01A000 - 01AFFF |
| 11 | 00B000 | 00B000 - 00BFFF | 27 | 01B000 | 01B000 - 01BFFF |
| 12 | 00C000 | 00C000 - 00CFFF | 28 | 01C000 | 01C000 - 01CFFF |
| 13 | 00D000 | 00D000 - 00DFFF | 29 | 01D000 | 01D000 - 01DFFF |
| 14 | 00E000 | 00E000 - 00EFFF | 30 | 01E000 | 01E000 - 01EFFF |
| 15 | 00F000 | 00F000 - 00FFFF | 31 | 01F000 | 01F000 - 01FFFF |

**Table 12 - Connection Memory Group Address Mapping**

The mapping of each output stream, SToA*n*, SToB*n*, SToC*n* and SToD*n*, depends on the programmed bit rate in the Global Rate Control Register. The address offset range for each stream is illustrated in Table 13.

| Device Data Rate | Timeslot Range | Output Stream | Stream Address Offset Range (Hex) |
|---|---|---|---|
| 65 Mbps | 0 - 1023 | SToA*n* | 00000 - 00FFF |
| | | SToB*n*, C*n*, D*n* | N/A |
| 32 Mbps | 0 - 511 | SToA*n* | 00000 - 007FF |
| | | SToB*n* | 00800 - 00FFF |
| | | SToC*n*, D*n* | N/A |
| 16 Mbps | 0 - 255 | SToA*n* | 00000 - 003FF |
| | | SToB*n* | 00400 - 007FF |
| | | SToC*n* | 00800 - 00BFF |
| | | SToD*n* | 00C00 - 00FFF |
| 8 Mbps | 0 - 127 | SToA*n* | 00000 - 001FF |
| | | SToB*n* | 00200 - 003FF |
| | | SToC*n* | 00400 - 005FF |
| | | SToD*n* | 00600 - 007FF |
| | N/A | $\overline{\text{BERR}}$ | 00800 - 00FFF |

**Table 13 - Connection Memory Stream Address Offset at Various Output Rates**

The address range for a particular stream is given by adding the group start address, as indicated in Table 12, to the appropriate stream offset range, as indicated in Table 13. For example, the Connection Memory address range for SToB12 operating at 32 Mbps is 00C800-00CFFF; the Connection Memory address range for SToC4 operating at 8 Mbps is 004400-0045FF.

Each output channel timeslot occupies a range of 4 addresses in the Connection Memories. The timeslot address offset is illustrated in Table 14. It shows the maximum number of timeslots that a stream can have, but the actual number of timeslots available depends on the output data rates, as illustrated in Table 1 and Table 13.

| Timeslot | | | | Address Offset hex |
|---|---|---|---|---|
| **SToA*n*** | **SToB*n*** | **SToC*n*** | **SToD*n*** | |
| 0 | 0 | 0 | 0 | 000 |
| 1 | 1 | 1 | 1 | 004 |
| 2 | 2 | 2 | 2 | 008 |
| - | - | - | - | - |
| 126 | 126 | 126 | 126 | 1F8 |
| 127 | 127 | 127 | 127 | 1FC |
| 128 | 128 | 128 | 128 | 200 |
| 129 | 129 | 129 | 129 | 204 |
| - | - | - | - | - |
| 254 | 254 | 254 | 254 | 3F8 |
| 255 | 255 | 255 | 255 | 3FC |
| 256 | 256 | | | 400 |
| 257 | 257 | | | 404 |
| - | - | - | - | - |
| 510 | 510 | | | 7F8 |
| 511 | 511 | | | 7FC |
| 512 | | | | 800 |
| 513 | | | | 804 |
| - | | | | - |
| 1021 | | | | FF4 |
| 1022 | | | | FF8 |
| 1023 | | | | FFC |

**Table 14 - Connection Memory Timeslot Address Offset Range**

### 12.1.1 Connection Memory Bit Functions

The bit functions of the connection memory are illustrated in Table 15.

External Read/Write Address: $000000_H$
Reset Value: $0000_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PCF 2 | PCF 1 | PCF 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | GP 4 | GP 3 | GP 2 | GP 1 | GP 0 | STCH 9 | STCH 8 | STCH 7 | STCH 6 | STCH 5 | STCH 4 | STCH 3 | STCH 2 | STCH 1 | STCH 0 |

| Bit | Name | Description |
|---|---|---|
| 31 - 29 | PCF2 - 0 | **Per Channel Function**<br>PCF2 - 0 / Function / Description<br>000 / OT / Output is tri-stated<br>001 / FH / Output drives high always<br>010 / MSG / Output is in message mode<br>011 / VAR / Variable delay connection mode<br>100 / CD / Constant delay connection mode<br>101 / RESERVED / Reserved. Do not use.<br>110 / OT / Output is tri-stated<br>111 / OT / Output is tri-stated |
| 28 - 15 | Unused | **Reserved.** In normal functional mode, these bits **MUST** be set to zero. |
| 14 - 10 | GP4 - 0 | **Source Group Selection.** These bits define the input/source group number (31 - 0). |
| 9 - 0 | STCH 9 - 0 | **Source Stream and Channel Selection / Message Mode Data**<br>In connection mode (constant/variable delay), these bits define the input/source stream and channel number, depending on the data rate.<br>For 65.536 Mbps, bits 9 - 0 select the input channel (0 - 1023).<br>For 32.768 Mbps, bits 9 - 1 select the input channel (0 - 511). Bit 0 selects stream STiA (0) or STiB (1)<br>For 16.869 Mbps, bits 9 - 2 select the input channel (0 - 255). Bits 1 - 0 select stream STiA (00), STiB (01), STiC (10), or STiD (11)<br>For 8.192 Mbps, bits 9 - 3 select the input channel (0 - 127). Bit 2 MUST be set to 0. Bits 1 - 0 select stream STiA (00), STiB (01), STiC (10), or STiD (11).<br>In message mode, bits 7 - 0 define the output data. The data is output sequentially with bit 7 being output first. Bits 9 - 8 are not used. |

**Table 15 - Connection Memory Bits (CMB)**

### 12.1.2 Connection Memory LSB

The Connection Memory Least Significant Byte field is provided to give a convenient alternative way to modify the output data for a stream in message mode. In this memory address range, all of the connection memory least significant bytes (bits 7 - 0) are available for read/write in consecutive address locations. This feature is provided for programming convenience. It can allow higher programming bandwidth on message mode streams. For example, one longword access to this memory space can read or set the message bytes in four consecutive connection memory locations. Access to this memory space is big-endian, with the most significant bytes on the data bus accessing the lower address of the connection memory. For example, for 32-bit data bus, to access the Connection Memory LSB associated with channels 3 - 0 on a particular stream, the data bus D31 - 24 carry data for channel 0, D23 - 16 carry data for channel 1, D15 - 8 carry data for channel 2, and D7 - 0 carry data for channel 3. Addressing into each of the streams is illustrated in Table 16.

| Output Group | Start Address (Hex) | Address Range (Hex) | Output Group | Start Address (Hex) | Address Range (Hex) |
|---|---|---|---|---|---|
| 0 | 020000 | 020000 - 0203FF | 16 | 024000 | 024000 - 0243FF |
| 1 | 020400 | 020400 - 0207FF | 17 | 024400 | 024400 - 0247FF |
| 2 | 020800 | 020800 - 020BFF | 18 | 024800 | 024800 - 024BFF |
| 3 | 020C00 | 020C00 - 020FFF | 19 | 024C00 | 024C00 - 024FFF |
| 4 | 021000 | 021000 - 0213FF | 20 | 025000 | 025000 - 0253FF |
| 5 | 021400 | 021400 - 0217FF | 21 | 025400 | 025400 - 0257FF |
| 6 | 021800 | 021800 - 021BFF | 22 | 025800 | 025800 - 025BFF |
| 7 | 021C00 | 021C00 - 021FFF | 23 | 025C00 | 025C00 - 025FFF |
| 8 | 022000 | 022000 - 0223FF | 24 | 026000 | 026000 - 0263FF |
| 9 | 022400 | 022400 - 0227FF | 25 | 026400 | 026400 - 0267FF |
| 10 | 022800 | 022800 - 022BFF | 26 | 026800 | 026800 - 026BFF |
| 11 | 022C00 | 022C00 - 022FFF | 27 | 026C00 | 026C00 - 026FFF |
| 12 | 023000 | 023000 - 0233FF | 28 | 027000 | 027000 - 0273FF |
| 13 | 023400 | 023400 - 0237FF | 29 | 027400 | 027400 - 0277FF |
| 14 | 023800 | 023800 - 023BFF | 30 | 027800 | 027800 - 027BFF |
| 15 | 023C00 | 023C00 - 023FFF | 31 | 027C00 | 027C00 - 027FFF |

**Table 16 - Connection Memory LSB Group Address Mapping**

| Device Data Rate | Timeslot Range | Output Stream | Stream Address Offset Range (Hex) |
|---|---|---|---|
| 65 Mbps | 0 - 1023 | STo*An* | 00000 - 003FF |
| | | STo*Bn, Cn, Dn* | N/A |
| 32 Mbps | 0 - 511 | STo*An* | 00000 - 001FF |
| | | STo*Bn* | 00200 - 003FF |
| | | STo*Cn, Dn* | N/A |
| 16 Mbps | 0 - 255 | STo*An* | 00000 - 000FF |
| | | STo*Bn* | 00100 - 001FF |
| | | STo*Cn* | 00200 - 002FF |
| | | STo*Dn* | 00300 - 003FF |
| 8 Mbps | 0 - 127 | STo*An* | 00000 - 0007F |
| | | STo*Bn* | 00080 - 000FF |
| | | STo*Cn* | 00100 - 0017F |
| | | STo*Dn* | 00180 - 001FF |
| | N/A | $\overline{\text{BERR}}$ | 00200 - 003FF |

**Table 17 - Connection Memory LSB Stream Address Offset at Various Output Rates**

Within each stream group, the mapping of each of the actual output streams, STo*An*, STo*Bn*, STo*Cn* and STo*Dn*, depends on the device data rate programmed into the Global Rate Control Register. The address offsets to these control areas for each of the output streams are illustrated in Table 17.

## 12.2 Data Memory

The data memory field is a read only address range used to monitor the data being received by the input streams. Addressing into each of the streams is illustrated in Table 18.

| Input Group | Start Address (Hex) | Address Range (Hex) | Input Group | Start Address (Hex) | Address Range (Hex) |
|---|---|---|---|---|---|
| 0 | 028000 | 028000 - 0283FF | 16 | 02C000 | 02C000 - 02C3FF |
| 1 | 028400 | 028400 - 0287FF | 17 | 02C400 | 02C400 - 02C7FF |
| 2 | 028800 | 028800 - 028BFF | 18 | 02C800 | 02C800 - 02CBFF |
| 3 | 028C00 | 028C00 - 028FFF | 19 | 02CC00 | 02CC00 - 02CFFF |
| 4 | 029000 | 029000 - 0293FF | 20 | 02D000 | 02D000 - 02D3FF |
| 5 | 029400 | 029400 - 0297FF | 21 | 02D400 | 02D400 - 02D7FF |
| 6 | 029800 | 029800 - 029BFF | 22 | 02D800 | 02D800 - 02DBFF |
| 7 | 029C00 | 029C00 - 029FFF | 23 | 02DC00 | 02DC00 - 02DFFF |
| 8 | 02A000 | 02A000 - 02A3FF | 24 | 02E000 | 02E000 - 02E3FF |
| 9 | 02A400 | 02A400 - 02A7FF | 25 | 02E400 | 02E400 - 02E7FF |
| 10 | 02A800 | 02A800 - 02ABFF | 26 | 02E800 | 02E800 - 02EBFF |
| 11 | 02AC00 | 02AC00 - 02AFFF | 27 | 02EC00 | 02EC00 - 02EFFF |

**Table 18 - Data Memory Group Address Mapping**

| Input Group | Start Address (Hex) | Address Range (Hex) | Input Group | Start Address (Hex) | Address Range (Hex) |
|---|---|---|---|---|---|
| 12 | 02B000 | 02B000 - 02B3FF | 28 | 02F000 | 02F000 - 02F3FF |
| 13 | 02B400 | 02B400 - 02B7FF | 29 | 02F400 | 02F400 - 02F7FF |
| 14 | 02B800 | 02B800 - 02BBFF | 30 | 02F800 | 02F800 - 02FBFF |
| 15 | 02BC00 | 02BC00 - 02BFFF | 31 | 02FC00 | 02FC00 - 02FFFF |

**Table 18 - Data Memory Group Address Mapping (continued)**

Within each stream group, the mapping of each of the actual input streams, STiA*n*, STiB*n*, STiC*n* and STiD*n*, depends on the device data rate programmed into the Global Rate Control Register. The address offsets to these data areas for each of the input streams are illustrated in Table 19.

| Device Data Rate | Time-slot Range | Output Streams | Address Offset Range (Hex) |
|---|---|---|---|
| 65 Mbps | 0 - 1023 | STiA*n* | 00000 - 003FF |
| | | STiB*n,* C*n,* D*n* | N/A |
| 32 Mbps | 0 - 511 | STiA*n* | 00000 - 001FF |
| | | STiB*n* | 00200 - 003FF |
| | | STiC*n,* D*n* | N/A |
| 16 Mbps | 0 - 255 | STiA*n* | 00000 - 000FF |
| | | STiB*n* | 00100 - 001FF |
| | | STiC*n* | 00200 - 002FF |
| | | STiD*n* | 00300 - 003FF |
| 8 Mbps | 0 - 127 | STiA*n* | 00000 - 0007F |
| | | STiB*n* | 00080 - 000FF |
| | | STiC*n* | 00100 - 0017F |
| | | STiD*n* | 00180 - 001FF |
| | N/A | $\overline{\text{BERR}}$ | 00200 - 003FF |

**Table 19 - Data Memory Stream Address Offset at Various Output Rates**

The address ranges for the data memory portion corresponding to each of the actual input streams, STiA*n*, STiB*n*, STiC*n* and STiD*n*, for any particular input group number is calculated by adding the Start Address for the particular group, as indicated in Table 18, to the appropriate Address Offset Range, as indicated in Table 19. The time-slots map linearly into the appropriate address offset range. (i.e., timeslots 0, 1, 2, ... map into addresses 00000, 00001, 00002, ...)

The entire data memory is a read only structure. Any write attempts will result in a bus error. **$\overline{\text{BERR}}$** is driven active low to terminate the bus cycle.

## 12.3 Group Control Registers

The ZL50074 addresses the issues of a simple programming model and automatic stream configuration by defining a basic switching bit rate of 65.536 Mbps and by grouping the I/O streams. Each TDM I/O group contains 4 input and 4 output streams. The 4 input streams in the same group have identical input characteristics, and similarly, the 4 output streams in the same group have identical output characteristics. However, input and output streams in the same group can have different input and output operation characteristics.

The Group Control Registers are provided for setting the operating characteristics of the TDM input and output streams. All of the Group Control Registers are mapped long-word aligned on 32 bit boundaries in the memory space. Each of the 32 registers is used to control one group. The mapping of the Group Control Registers to the I/O group numbers is illustrated in Table 20. The bit functions of each of the Group Control Registers are illustrated in Table 21.

| TDM Group | Group Control Register Address (Hex) |
|---|---|
| 0 | 40200-40203 |
| 1 | 40204-40207 |
| 2 | 40208-4020B |
| 3 | 4020C-4020F |
| :<br>: | :<br>: |
| 29 | 40274-40277 |
| 30 | 40278-4027B |
| 31 | 4027C-4027F |

**Table 20 - Group Control Register Addressing**

External Read/Write Address: $40200_H$ - $4027F_H$
Reset Value: $000C000C_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OSI | OSBA 1 | OSBA 0 | 1 | 1 | OSSRC 1 | OSSRC 0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | ISI | ISPD 4 | ISPD 3 | ISPD 2 | ISPD 1 | ISPD 0 | 1 | 1 | ISSRC 1 | ISSRC 0 |

| Bit | Name | Description |
|---|---|---|
| 31 - 23 | Unused | **Reserved.** In normal functional mode, these bits **MUST** be set to zero. |
| 22 | OSI | **Output Stream Inversion**<br>For normal operation, this bit is set low.<br>To invert the output stream, set this bit high. |

**Table 21 - Group Control Register**

External Read/Write Address: $40200_H$ - $4027F_H$
Reset Value: $000C000C_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OSI | OSBA 1 | OSBA 0 | 1 | 1 | OSSRC 1 | OSSRC 0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | ISI | ISPD 4 | ISPD 3 | ISPD 2 | ISPD 1 | ISPD 0 | 1 | 1 | ISSRC 1 | ISSRC 0 |

| Bit | Name | Description |
|---|---|---|
| 21 - 20 | OSBA1 - 0 | **Output Stream Bit Advancement**<br>OSBA1 - 0 / Non-65 Mbps / 65 Mbps<br>00 / 0 ns / 0 ns<br>01 / 7.6 ns / 3.8 ns<br>10 / 15.2 ns / 7.6 ns<br>11 / 22.8 ns / 11.4 ns |
| 19 - 18 | Unused | **Reserved.** In normal functional mode, these bits **MUST** be set to 11. |
| 17 - 16 | OSSRC1 - 0 | **Output Stream Clock Source Select**<br>OSSRC1 - 0 / Output Timing Source<br>00 / Internal System Clock<br>01 / $\overline{CKi}0$ and $\overline{FPi}0$<br>10 / $\overline{CKi}1$ and $\overline{FPi}1$<br>11 / $\overline{CKi}2$ and $\overline{FPi}2$ |
| 15 - 10 | Unused | **Reserved.** In normal functional mode, these bits **MUST** be set to zero. |
| 9 | ISI | **Input Stream Inversion**<br>For normal operation, this bit is set low.<br>To invert the input stream, set this bit high. |
| 8 - 4 | ISPD4 - 0 | **Input Sampling Point Delay**<br>Default Sampling Point is 3/4. Adjust according to Figure 2 on page 17. |
| 3 - 2 | Unused | **Reserved.** In normal functional mode, these bits **MUST** be set to 11. |

**Table 21 - Group Control Register (continued)**

External Read/Write Address: $40200_H$ - $4027F_H$
Reset Value: $000C000C_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OSI | OSBA 1 | OSBA 0 | 1 | 1 | OSSRC 1 | OSSRC 0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | ISI | ISPD 4 | ISPD 3 | ISPD 2 | ISPD 1 | ISPD 0 | 1 | 1 | ISSRC 1 | ISSRC 0 |

| Bit | Name | Description |
|---|---|---|
| 1 - 0 | ISSRC1 - 0 | **Input Stream Clock Source Select** |

| ISSRC1 - 0 | Input Timing Source |
|---|---|
| 00 | Internal System Clock |
| 01 | $\overline{CKi}0$ and $\overline{FPi}0$ |
| 10 | $\overline{CKi}1$ and $\overline{FPi}1$ |
| 11 | $\overline{CKi}2$ and $\overline{FPi}2$ |

**Table 21 - Group Control Register (continued)**

The Group Control Register is a static control register. Changes to bit settings may disrupt data flow on the selected port for a maximum of 2 frames.

## 12.4 Input Clock Control Register

The Input Clock Control Register is used to select the logic sense of the input clock.

External Read/Write Address: $40280_H$
Reset Value: $0DB_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | GCI SEL2 | FPI POL2 | CKI POL2 | GCI SEL1 | FPI POL1 | CKI POL1 | GCI SEL0 | FPI POL0 | CKI POL0 |

| Bit | Name | Description |
|---|---|---|
| 31 - 9 | Unused | **Reserved.** In normal functional mode, these bits **MUST** be set to zero. |
| 8 | GCISEL2 | **GCI-Bus Selection for $\overline{\text{FPi2}}$**<br>When this bit is low, $\overline{\text{FPi2}}$ is set for ST-BUS mode.<br>When this bit is high, $\overline{\text{FPi2}}$ is set for GCI-Bus mode. |
| 7 | FPIPOL2 | **Frame Pulse Polarity Selection for $\overline{\text{FPi2}}$**<br>When this bit is low, $\overline{\text{FPi2}}$ is set for active high.<br>When this bit is high, $\overline{\text{FPi2}}$ is set for active low. |
| 6 | CKIPOL2 | **Clock Polarity Selection for $\overline{\text{CKi2}}$**<br>When this bit is low, $\overline{\text{CKi2}}$ is set for the positive clock edge.<br>When this bit is high, $\overline{\text{CKi2}}$ is set for the negative clock edge. |
| 5 | GCISEL1 | **GCI-Bus Selection for $\overline{\text{FPi1}}$**<br>When this bit is low, $\overline{\text{FPi1}}$ is set for ST-BUS mode.<br>When this bit is high, $\overline{\text{FPi1}}$ is set for GCI-Bus mode. |
| 4 | FPIPOL1 | **Frame Pulse Polarity Selection for $\overline{\text{FPi1}}$**<br>When this bit is low, $\overline{\text{FPi1}}$ is set for active high.<br>When this bit is high, $\overline{\text{FPi1}}$ is set for active low. |
| 3 | CKIPOL1 | **Clock Polarity Selection for $\overline{\text{CKi1}}$**<br>When this bit is low, $\overline{\text{CKi1}}$ is set for the positive clock edge.<br>When this bit is high, $\overline{\text{CKi1}}$ is set for the negative clock edge. |
| 2 | GCISEL0 | **GCI-Bus Selection for $\overline{\text{FPi0}}$**<br>When this bit is low, $\overline{\text{FPi0}}$ is set for ST-BUS mode.<br>When this bit is high, $\overline{\text{FPi0}}$ is set for GCI-Bus mode. |
| 1 | FPIPOL0 | **Frame Pulse Polarity Selection for $\overline{\text{FPi0}}$**<br>When this bit is low, $\overline{\text{FPi0}}$ is set for active high.<br>When this bit is high, $\overline{\text{FPi0}}$ is set for active low. |
| 0 | CKIPOL0 | **Clock Polarity Selection for $\overline{\text{CKi0}}$**<br>When this bit is low, $\overline{\text{CKi0}}$ is set for the positive clock edge.<br>When this bit is high, $\overline{\text{CKi0}}$ is set for the negative clock edge. |

**Table 22 - Input Clock Control Register**

## 12.5 Output Clock Control Register

The Output Clock Control Register is used to select the desired source, frequency, and logic sense of the output clocks. The bit functions of the Output Clock Control Register are illustrated in Table 23.

External Read/Write Address: $40284_H$
Reset Value: $060D1C3C_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | GCO SEL3 | FPO POL3 | CKO POL3 | CKO3 RATE1 | CKO3 RATE0 | CKO3 SRC1 | CKO3 SRC0 | GCO SEL2 | FPO POL2 | CKO POL2 | CKO2 RATE1 | CKO2 RATE0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CKO2 SRC1 | CKO2 SRC0 | GCO SEL1 | FPO POL1 | CKO POL1 | CKO1 RATE1 | CKO1 RATE0 | CKO1 SRC1 | CKO1 SRC0 | GCO SEL0 | FPO POL0 | CKO POL0 | CKO0 RATE1 | CKO0 RATE0 | CKO0 SRC1 | CKO0 SRC0 |

| Bit | Name | Description |
|---|---|---|
| 31 - 28 | Unused | **Reserved.** In normal functional mode, these bits **MUST** be set to zero. |
| 27 | GCO SEL3 | **GCI-Bus Selection for $\overline{FPo3}$**<br>When this bit is low, $\overline{FPo3}$ is set for ST-BUS mode.<br>When this bit is high, $\overline{FPo3}$ is set for GCI-Bus mode. |
| 26 | FPO POL3 | **Frame Pulse Polarity Selection for $\overline{FPo3}$**<br>When this bit is low, $\overline{FPo3}$ is set for active high.<br>When this bit is high, $\overline{FPo3}$ is set for active low. |
| 25 | CKO POL3 | **Clock Polarity Selection for $\overline{CKo3}$**<br>When this bit is low, $\overline{CKo3}$ is set for the positive clock edge.<br>When this bit is high, $\overline{CKo3}$ is set for the negative clock edge. |
| 24 - 23 | CKO3 RATE 1 - 0 | **Output Clock Rate for $\overline{CKo3}$ and $\overline{FPo3}$**<br>The output clock rate can not exceed the selected clock source rate. All rates are available when the internal system clock is selected as clock source. |
| 22 - 21 | CKO3 SRC 1 - 0 | **Output Clock Source for $\overline{CKo3}$ and $\overline{FPo3}$** |

| CKO3RATE1 - 0 | $\overline{CKo3}$ | $\overline{FPo3}$ |
|---|---|---|
| 00 | 8.192 MHz | 120 ns |
| 01 | 16.384 MHz | 60 ns |
| 10 | 32.768 MHz | 30 ns |
| 11 | 65.536 MHz | 15 ns |

| CKO3SRC1 - 0 | Output Timing Source |
|---|---|
| 00 | Internal System Clock |
| 01 | $\overline{CKi0}$ and $\overline{FPi0}$ |
| 10 | $\overline{CKi1}$ and $\overline{FPi1}$ |
| 11 | $\overline{CKi2}$ and $\overline{FPi2}$ |

**Table 23 - Output Clock Control Register**

External Read/Write Address: $40284_H$
Reset Value: $060D1C3C_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | GCO SEL3 | FPO POL3 | CKO POL3 | CKO3 RATE1 | CKO3 RATE0 | CKO3 SRC1 | CKO3 SRC0 | GCO SEL2 | FPO POL2 | CKO POL2 | CKO2 RATE1 | CKO2 RATE0 |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CKO2 SRC1 | CKO2 SRC0 | GCO SEL1 | FPO POL1 | CKO POL1 | CKO1 RATE1 | CKO1 RATE0 | CKO1 SRC1 | CKO1 SRC0 | GCO SEL0 | FPO POL0 | CKO POL0 | CKO0 RATE1 | CKO0 RATE0 | CKO0 SRC1 | CKO0 SRC0 |

| Bit | Name | Description |
|---|---|---|
| 20 | GCO SEL2 | **GCI-Bus Selection for $\overline{FPo2}$**<br>When this bit is low, $\overline{FPo2}$ is set for ST-BUS mode.<br>When this bit is high, $\overline{FPo2}$ is set for GCI-Bus mode. |
| 19 | FPO POL2 | **Frame Pulse Polarity Selection for $\overline{FPo2}$**<br>When this bit is low, $\overline{FPo2}$ is set for active high.<br>When this bit is high, $\overline{FPo2}$ is set for active low. |
| 18 | CKO POL2 | **Clock Polarity Selection for $\overline{CKo2}$**<br>When this bit is low, $\overline{CKo2}$ is set for the positive clock edge.<br>When this bit is high, $\overline{CKo2}$ is set for the negative clock edge. |
| 17 - 16 | CKO2 RATE 1 - 0 | **Output Clock Rate for $\overline{CKo2}$ and $\overline{FPo2}$**<br>The output clock rate can not exceed the selected clock source rate. All rates are available when the internal system clock is selected as clock source**.**<br>CKO2RATE1 - 0 / $\overline{CKo2}$ / $\overline{FPo2}$<br>00 / 8.192 MHz / 120 ns<br>01 / 16.384 MHz / 60 ns<br>10 / 32.768 MHz / 30 ns<br>11 / 65.536 MHz / 15 ns |
| 15 - 14 | CKO2 SRC 1 - 0 | **Output Clock Source for $\overline{CKo2}$ and $\overline{FPo2}$**<br>CKO2SRC1 - 0 / Output Timing Source<br>00 / Internal System Clock<br>01 / $\overline{CKi0}$ and $\overline{FPi0}$<br>10 / $\overline{CKi1}$ and $\overline{FPi1}$<br>11 / $\overline{CKi2}$ and $\overline{FPi2}$ |
| 13 | GCO SEL1 | **GCI-Bus Selection for $\overline{FPo1}$**<br>When this bit is low, $\overline{FPo1}$ is set for ST-BUS mode.<br>When this bit is high, $\overline{FPo1}$ is set for GCI-Bus mode. |

**Table 23 - Output Clock Control Register (continued)**

External Read/Write Address: $40284_H$
Reset Value: $060D1C3C_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | GCO SEL3 | FPO POL3 | CKO POL3 | CKO3 RATE1 | CKO3 RATE0 | CKO3 SRC1 | CKO3 SRC0 | GCO SEL2 | FPO POL2 | CKO POL2 | CKO2 RATE1 | CKO2 RATE0 |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CKO2 SRC1 | CKO2 SRC0 | GCO SEL1 | FPO POL1 | CKO POL1 | CKO1 RATE1 | CKO1 RATE0 | CKO1 SRC1 | CKO1 SRC0 | GCO SEL0 | FPO POL0 | CKO POL0 | CKO0 RATE1 | CKO0 RATE0 | CKO0 SRC1 | CKO0 SRC0 |

| Bit | Name | Description |
|---|---|---|
| 12 | FPO POL1 | **Frame Pulse Polarity Selection for $\overline{FPo1}$**<br>When this bit is low, $\overline{FPo1}$ is set for active high.<br>When this bit is high, $\overline{FPo1}$ is set for active low. |
| 11 | CKO POL1 | **Clock Polarity Selection for $\overline{CKo1}$**<br>When this bit is low, $\overline{CKo1}$ is set for the positive clock edge.<br>When this bit is high, $\overline{CKo1}$ is set for the negative clock edge. |
| 10 - 9 | CKO1 RATE 1 - 0 | **Output Clock Rate for $\overline{CKo1}$ and $\overline{FPo1}$**<br>The output clock rate can not exceed the selected clock source rate. All rates are available when the internal system clock is selected as clock source**.** |
| 8 - 7 | CKO1 SRC 1 - 0 | **Output Clock Source for $\overline{CKo1}$ and $\overline{FPo1}$** |
| 6 | GCO SEL0 | **GCI-Bus Selection for $\overline{FPo0}$**<br>When this bit is low, $\overline{FPo0}$ is set for ST-BUS mode.<br>When this bit is high, $\overline{FPo0}$ is set for GCI-Bus mode. |
| 5 | FPO POL0 | **Frame Pulse Polarity Selection for $\overline{FPo0}$**<br>When this bit is low, $\overline{FPo0}$ is set for active high.<br>When this bit is high, $\overline{FPo0}$ is set for active low. |

| CKO1RATE1 - 0 | $\overline{CKo1}$ | $\overline{FPo1}$ |
|---|---|---|
| 00 | 8.192 MHz | 120 ns |
| 01 | 16.384 MHz | 60 ns |
| 10 | 32.768 MHz | 30 ns |
| 11 | 65.536 MHz | 15 ns |

| CKO1SRC1 - 0 | Output Timing Source |
|---|---|
| 00 | Internal System Clock |
| 01 | $\overline{CKi0}$ and $\overline{FPi0}$ |
| 10 | $\overline{CKi1}$ and $\overline{FPi1}$ |
| 11 | $\overline{CKi2}$ and $\overline{FPi2}$ |

**Table 23 - Output Clock Control Register (continued)**

External Read/Write Address: $40284_H$
Reset Value: $060D1C3C_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | GCO SEL3 | FPO POL3 | CKO POL3 | CKO3 RATE1 | CKO3 RATE0 | CKO3 SRC1 | CKO3 SRC0 | GCO SEL2 | FPO POL2 | CKO POL2 | CKO2 RATE1 | CKO2 RATE0 |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CKO2 SRC1 | CKO2 SRC0 | GCO SEL1 | FPO POL1 | CKO POL1 | CKO1 RATE1 | CKO1 RATE0 | CKO1 SRC1 | CKO1 SRC0 | GCO SEL0 | FPO POL0 | CKO POL0 | CKO0 RATE1 | CKO0 RATE0 | CKO0 SRC1 | CKO0 SRC0 |

| Bit | Name | Description |
|---|---|---|
| 4 | CKO POL0 | **Clock Polarity Selection for $\overline{CKo0}$**<br>When this bit is low, $\overline{CKo0}$ is set for the positive clock edge.<br>When this bit is high, $\overline{CKo0}$ is set for the negative clock edge. |
| 3 - 2 | CKO0 RATE 1 - 0 | **Output Clock Rate for $\overline{CKo0}$ and $\overline{FPo0}$**<br>The output clock rate can not exceed the selected clock source rate. All rates are available when the internal system clock is selected as clock source. |
| 1 - 0 | CKO0 SRC 1 - 0 | **Output Clock Source for $\overline{CKo0}$ and $\overline{FPo0}$** |

| CKO0RATE1 - 0 | $\overline{CKo0}$ | $\overline{FPo0}$ |
|---|---|---|
| 00 | 8.192 MHz | 120 ns |
| 01 | 16.384 MHz | 60 ns |
| 10 | 32.768 MHz | 30 ns |
| 11 | 65.536 MHz | 15 ns |

| CKO0SRC1 - 0 | Output Timing Source |
|---|---|
| 00 | Internal System Clock |
| 01 | $\overline{CKi0}$ and $\overline{FPi0}$ |
| 10 | $\overline{CKi1}$ and $\overline{FPi1}$ |
| 11 | $\overline{CKi2}$ and $\overline{FPi2}$ |

**Table 23 - Output Clock Control Register (continued)**

## 12.6 Block Init Register

The Block Init Register is a 32 bit read/write register at address 040288 - $04028B_H$.

The Block Init Register is used during block initialization of the connection memory. A block initialization automatically occurs at power-up. However, it is possible to perform a block initialization at any time. During Block Initialization, the value of the Block Init Register is copied to all connection memory locations in an operation that runs in about 120 μs. If the Block Init Register is modified during a block initialization, the new value used is ignored.

## 12.7 Block Init Enable Register

The Block Init Enable Register is a 32 bit read/write register at address 04028C - $04028F_H$.

The Block Init Enable Register is used to initiate a block initialization of the connection memory. A block initialization automatically occurs at power-up. Since the Block Init Register is cleared at power-up this automatic block initialization will write all zeros to all Connection Memory Bits. However, it is possible to perform a block initialization at any time. To begin a block initialization, the hex value 31415926 must be written to the Block Init Enable Register. If a block initialization is signaled while one is in progress, the signal is ignored, and the currently active block initialization is allowed to complete.

The value read back from the Block Init Enable Register is different from the value written. It represents both the block initialization status, and the power-up reset initialization status. The meaning of the initialization status bits is illustrated in Table 24. The bits 31 - 2 always read back 0.

| Bit | Name | Description |
|---|---|---|
| 0 | Block Init Status | 0 if Block initialization is completed;<br>1 if Block initialization is in progress. |
| 1 | Reset Init Status | 0 if Reset initialization is completed;<br>1 if Reset initialization is in progress. |

**Table 24 - Block and Power-up Initialization Status Bits**

Any access to the connection memory or the data memory during a block initialization or a reset initialization will result in a bus error, $\overline{BERR}$. All TDM outputs are tri-stated during any block initialization.

## 12.8 Global Rate Control Register

The Global Rate Control Register is used to select the data rate of all the input and output streams. On power-up, the GBR bits are both reset to 0, corresponding to a rate of 8.192 Mbps.

External Read/Write Address: 040290 - $040293_H$
Reset Value: $0000_H$

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | GBR 1 | GBR 0 |

| Bit | Name | Description |
|---|---|---|
| 31 - 2 | Unused | **Reserved.** In normal functional mode, these bits **MUST** be set to zero. |
| 1 - 0 | GBR1 - 0 | **Global Bit Rate Selection**<br><br>GBR 1 - 0 / Input and Output Data Rate<br>00 / 8 Mbps - Group A, B, C and D<br>01 / 16 Mbps - Group A, B, C and D<br>10 / 32 Mbps - Group A and B<br>Group C and D inputs are unused<br>Group C and D outputs are tristated<br>11 / 65 Mbps - Group A<br>Group B, C and D inputs are unused<br>Group B, C and D outputs are tristated<br><br>Each input and output group can individually select different clock sources. If the internal system clock is used as the clock source, all the above data rates are available. Otherwise, the data rate cannot exceed the selected clock source's rate. |

## 13.0 DC/AC Electrical Characteristics

**Absolute Maximum Ratings[1] -** Voltages are with respect to ground (VSS) unless otherwise stated.

| | Characteristics | Sym. | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|
| 1 | Chip I/O Supply Voltage | $V_{DD\_IO}$ | -0.5 | | 5.0 | V |
| 2 | Chip Core Supply Voltage | $V_{DD\_CORE}$ | -0.5 | | 5.0 | V |
| 3 | Input Voltage (non-5 V tolerant inputs) | $V_{I\_3V}$ | -0.5 | | $V_{DD\_IO}$ + 0.5 | V |
| 4 | Input Voltage (5 V tolerant inputs) | $V_{I\_5V}$ | -0.5 | | 7.0 | V |
| 5 | Continuous Current at digital outputs | $I_o$ | | | 15 | mA |
| 6 | Package power dissipation | $P_D$ | | | 2.1 | W |
| 7 | Storage temperature | $T_S$ | - 55 | | +125 | °C |

Note 1: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Note 2: Typical figures are at 25°C, $V_{DD\_CORE}$ at 1.8 V and $V_{DD\_IO}$ at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

**Recommended Operating Conditions -** Voltages are with respect to ground (VSS) unless otherwise stated.

| | Characteristics | Sym. | Min. | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|
| 1 | Operating Temperature | $T_{OP}$ | -40 | 25 | +85 | °C |
| 2 | Positive Supply Core | $V_{DD\_CORE}$ | 1.71 | 1.8 | 1.89 | V |
| 3 | Positive Supply I/O | $V_{DD\_IO}$ | 3.0 | 3.3 | 3.6 | V |
| 4 | Input Voltage (non-5V tolerant inputs) | $V_{I\_3V}$ | 0 | | $V_{DD\_IO}$ | V |
| 5 | Input Voltage (5V tolerant inputs) | $V_{I\_5V}$ | 0 | | 5.5 | |

Note 1: Typical figures are at 25°C, $V_{DD\_CORE}$ at 1.8 V and $V_{DD\_IO}$ at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

**DC Electrical Characteristics -** Voltages are with respect to ground (VSS) unless otherwise stated.

| | Characteristics | Sym. | Min. | Typ.[1] | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| 1 | Core Supply Current[2] | $I_{DD\_CORE}$ | | | 500 | mA | |
| 2 | I/O Supply Current | $I_{DD\_IO}$ | | | 62 | mA | Outputs unloaded |
| 3 | Leakage Current | $I_{DDQ}$ | | 105 | | µA | |
| 4 | Dynamic Power Dissipation | $P_{DD}$ | | | 1.2 | W | Outputs Unloaded |
| 5 | Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| 6 | Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| 7 | Input Leakage (input pins)[3] | $I_{IL}$ | | | 5 | µA | $0 \leq < V_I \leq V_{DD\_IO}$ |
| 8 | Input Leakage (bi-directional pins | $I_{BL}$ | | | 5 | µA | $0 \leq < V_I \leq V_{DD\_IO}$ |
| 9 | Weak Pull-up Current | $I_{PU}$ | | -33 | | µA | Input at 0V |
| 10 | Weak Pull-down Current | $I_{PD}$ | | 33 | | µA | Input at $V_{DD\_IO}$ |
| 11 | Input Pin Capacitance | $C_I$ | | 3 | | pF | |
| 12 | Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = 8 mA |
| 13 | Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 8 mA |

1. Typical figures are at 25°C, $V_{DD\_CORE}$ at 1.8 V and $V_{DD\_IO}$ at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.
2. SToA = 65 Mbps with random patterns. CKo0 = 65 MHz, CKo1 = 32 MHz
3. Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (Vin).

**AC Electrical Characteristics[1] - Timing Parameter Measurement Voltage Levels -** Voltages are with respect to ground (VSS) unless otherwise stated.

| | Characteristics | Sym. | Level | Unit | Test Conditions |
|---|---|---|---|---|---|
| 1 | CMOS Threshold | $V_{CT}$ | 0.5 $V_{DD\_IO}$ | V | |
| 2 | Rise/Fall Threshold Voltage High | $V_{HM}$ | 0.7 $V_{DD\_IO}$ | V | |
| 3 | Rise/Fall Threshold Voltage Low | $V_{LM}$ | 0.3 $V_{DD\_IO}$ | V | |

1. Characteristics are over recommended operating conditions unless otherwise stated.

**AC Electrical Characteristics[1] - $\overline{\text{FPi}}$0-2 and $\overline{\text{CKi}}$0-2 Timing**

| No. | Characteristic (Figure ) | Sym. | Min. | Typ.[2] | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | $\overline{\text{FPi}}$0-2 Input Frame Pulse Setup Time | $t_{FPIS}$ | 3 | | 12 | ns | $\overline{\text{CKi}}$ = 65.536 MHz |
| | | | 3 | | 25 | ns | $\overline{\text{CKi}}$ = 32.768 MHz |
| | | | 3 | | 55 | ns | $\overline{\text{CKi}}$ = 16.384 MHz |
| | | | 3 | | 115 | ns | $\overline{\text{CKi}}$ = 8.192 MHz |
| 2 | $\overline{\text{FPi}}$0-2 Input Frame Pulse Hold Time | $t_{FPIH}$ | 2 | | 12 | ns | $\overline{\text{CKi}}$ = 65.536 MHz |
| | | | 2 | | 25 | ns | $\overline{\text{CKi}}$ = 32.768 MHz |
| | | | 2 | | 55 | ns | $\overline{\text{CKi}}$ = 16.384 MHz |
| | | | 2 | | 115 | ns | $\overline{\text{CKi}}$ = 8.192 MHz |
| 3 | $\overline{\text{FPi}}$0-2 Input Frame Pulse width | $t_{FPIW}$ | 5 | | 24 | ns | $\overline{\text{CKi}}$ = 65.536 MHz |
| | | | 5 | | 50 | ns | $\overline{\text{CKi}}$ = 32.768 MHz |
| | | | 5 | | 110 | ns | $\overline{\text{CKi}}$ = 16.384 MHz |
| | | | 5 | | 230 | ns | $\overline{\text{CKi}}$ = 8.192 MHz |
| 4 | $\overline{\text{CKi}}$0-2 Input Clock Period (average value, does not consider the effects of jitter) | $t_{CKIP}$ | 15 | 15.26 | 15.5 | ns | 65.536 MHz |
| | | | 30 | 30.5 | 31 | ns | 32.768 MHz |
| | | | 60 | 61.0 | 62 | ns | 16.384 MHz |
| | | | 120 | 122 | 124 | ns | 8.192 MHz |
| 5 | $\overline{\text{CKi}}$ Input Clock High Time | $t_{CKIH}$ | 4 | | | ns | |
| 6 | $\overline{\text{CKi}}$ Input Clock Low Time | $t_{CKIL}$ | 4 | | | ns | |
| 7 | $\overline{\text{CKi}}$ Input Clock Rise/Fall Time | $t_{rCKI}$, $t_{fCKI}$ | 0 | | 6 | ns | |
| 8 | $\overline{\text{CKi}}$ Input Clock Cycle to Cycle Variation | $t_{CVC}$ | | | 2 | ns p-p | Standard rating[3]. STi at 65 Mbps |
| | | | | | 4 | ns p-p | Standard rating[3]. STi at 32 Mbps |
| | | | | | 10 | ns p-p | Standard rating[3]. STi at 16 Mbps |
| | | | | | 20 | ns p-p | Standard rating[3]. STi at 8 Mbps |
| | | | | | 20% of $t_{CKIP}$ | p-p | Extended rating. With alternate clock source[4] or high $\overline{\text{CKi}}$0 rate[5] |

Note 1: Characteristics are over recommended operating conditions unless otherwise stated.

Note 2: Typical figures are at 25°C, $V_{DD\_CORE}$ at 1.8 V and $V_{DD\_IO}$ at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

Note 3: When using internal APLL clock source and the $\overline{\text{CKi}}$0 frequency is less than or equal to the data rate.

Note 4: When using input clock source $\overline{\text{CKi}}$2-0 instead of the internal APLL clock source.

Note 5: When using internal APLL clock source and the $\overline{\text{CKi}}$0 frequency is higher than or equal to twice the data rate.

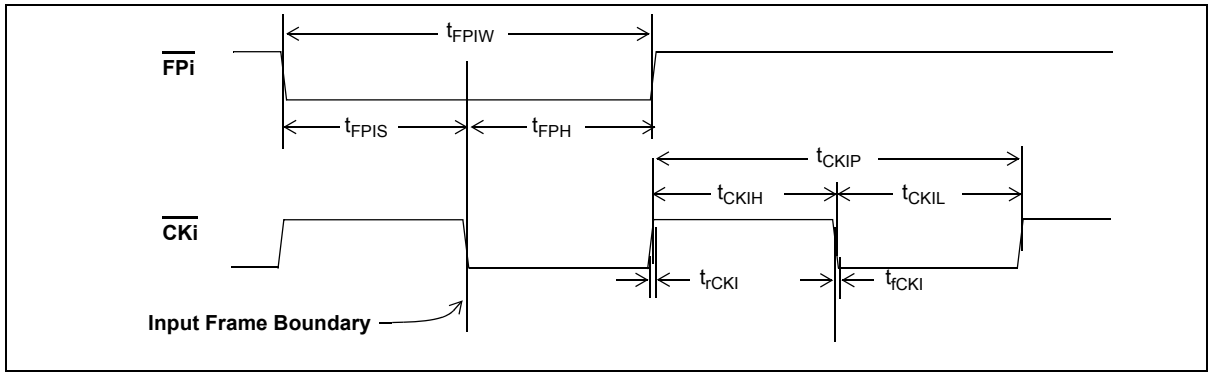



**Figure 8 - Frame Pulse Input and Clock Input**

### AC Electrical Characteristics[1] - $\overline{\text{FPi}}$ and $\overline{\text{CKi}}$ Skew

| No. | Characteristic (Figure 9) | Sym. | Min. | Typ.[2] | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | $\overline{\text{CKi0}}$ to $\overline{\text{CKi1}}$, $\overline{2}$ Skew | $t_{CKSK}$ | -30 | | +30 | ns | $C_L$ 50 pF<br>Assume no jitter on input clocks |

1. Characteristics are over recommended operating conditions unless otherwise stated.
2. Typical figures are at 25°C, $V_{DD\_CORE}$ at 1.8 V and $V_{DD\_IO}$ at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

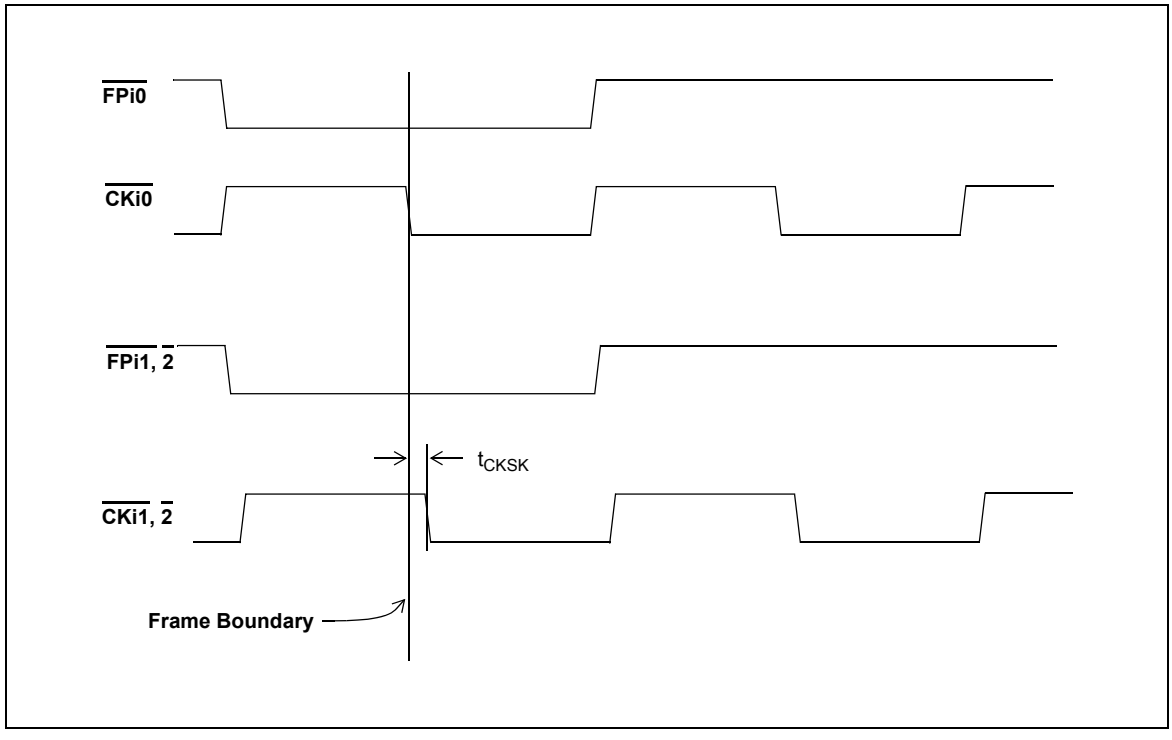



**Figure 9 - Frame Skew Timing Diagram**

**AC Electrical Characteristics[1] - $\overline{\text{FPO}}$0-3 and $\overline{\text{CKO}}$0-3 (65.536 MHz) Timing**

| No. | Characteristic | Sym. | Min. | Typ.[2] | Max. | Units | Notes[3] |
|---|---|---|---|---|---|---|---|
| 1 | $\overline{\text{FPO}}$0-3 Output Frame Pulse Setup Time | $t_{FPOS}$ | 5.5 | | 9.5 | ns | $C_L$=30 pF |
| 2 | $\overline{\text{FPO}}$0-3 Output Frame Pulse Hold Time | $t_{FPOH}$ | 5.5 | | 9.5 | ns | $C_L$=30 pF |
| 3 | $\overline{\text{CKO}}$0-3 Output Clock Period | $t_{CKOP}$ | 14.5 | | 15.5 | ns | $C_L$=30 pF |

**AC Electrical Characteristics[1] - $\overline{\text{FPO}}$0-3 and $\overline{\text{CKO}}$0-3 (32.768 MHz) Timing**

| No. | Characteristic | Sym. | Min. | Typ.[2] | Max. | Units | Notes[3] |
|---|---|---|---|---|---|---|---|
| 1 | $\overline{\text{FPO}}$0-3 Output Frame Pulse Setup Time | $t_{FPOS}$ | 14.0 | | 16.5 | ns | $C_L$=30 pF |
| 2 | $\overline{\text{FPO}}$0-3 Output Frame Pulse Hold Time | $t_{FPOH}$ | 14.0 | | 16.5 | ns | $C_L$=30 pF |
| 3 | $\overline{\text{CKO}}$0-3 Output Clock Period | $t_{CKOP}$ | 30.0 | | 31.0 | ns | $C_L$=30pF |

**AC Electrical Characteristics[1] - $\overline{\text{FPO}}_{0\text{-}3}$ and $\overline{\text{CKO}}_{0\text{-}3}$ (16.384 MHz) Timing**

| No. | Characteristic | Sym. | Min. | Typ.[2] | Max. | Units | Notes[3] |
|---|---|---|---|---|---|---|---|
| 1 | $\overline{\text{FPO}}$0-3 Output Frame Pulse Setup Time | $t_{FPOS}$ | 29.0 | | 31.0 | ns | $C_L$=30 pF |
| 2 | $\overline{\text{FPO}}$0-3 Output Frame Pulse Hold Time | $t_{FPOH}$ | 29.0 | | 31.0 | ns | $C_L$=30 pF |
| 3 | $\overline{\text{CKO}}$0-3 Output Clock Period | $t_{CKOP}$ | 60.5 | | 61.5 | ns | $C_L$=30 pF |

**AC Electrical Characteristics[1] - $\overline{\text{FPO}}_{0\text{-}3}$ and $\overline{\text{CKO}}_{0\text{-}3}$ (8.192 MHz) Timing**

| No. | Characteristic | Sym. | Min. | Typ.[2] | Max. | Units | Notes[3] |
|---|---|---|---|---|---|---|---|
| 1 | $\overline{\text{FPO}}$0-3 Output Frame Pulse Setup Time | $t_{FPOS}$ | 60.0 | | 62.0 | ns | $C_L$=30 pF |
| 2 | $\overline{\text{FPO}}$0-3 Output Frame Pulse Hold Time | $t_{FPOH}$ | 60.0 | | 62.0 | ns | $C_L$=30 pF |
| 3 | $\overline{\text{CKO}}$0-3 Output Clock Period | $t_{CKOP}$ | 121.5 | | 122.5 | ns | $C_L$=30 pF |

Note 1: Characteristics are over recommended operating conditions unless otherwise stated.

Note 2: Typical figures are at 25°C, $V_{DD\_CORE}$ at 1.8 V and $V_{DD\_IO}$ at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

Note 3: $\overline{\text{CKo}}$ clock source set to internal 131 MHz APLL, and CKi0 and FPi0 meet all the timing requirements.

Note 4: When CKo source is set to one of the CKi/FPi, its output timings directly follow its source.

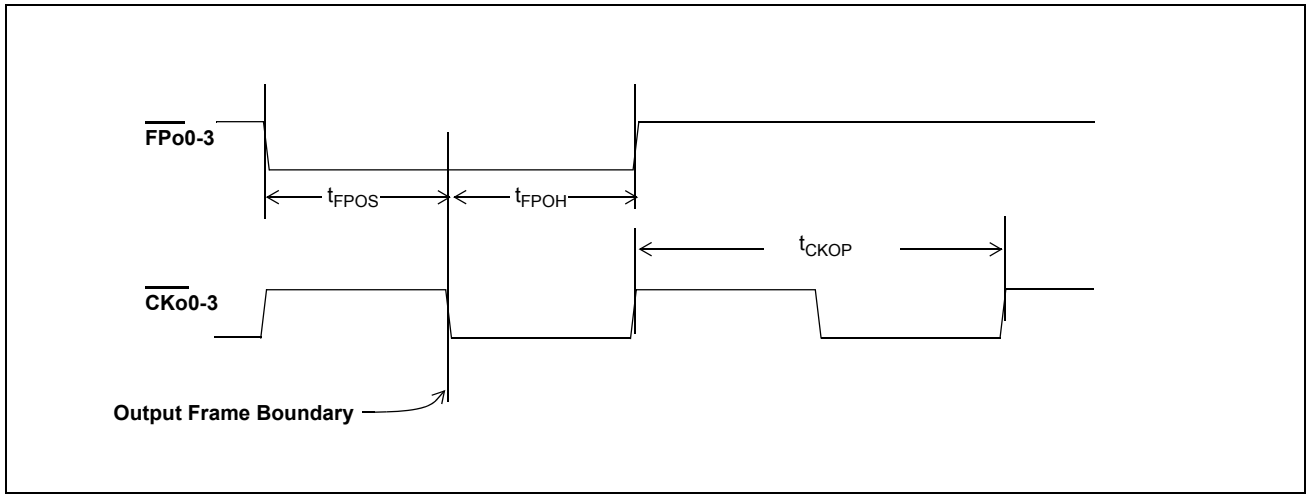



**Figure 10 - ST-Bus Frame Pulse and Clock Output Timing**

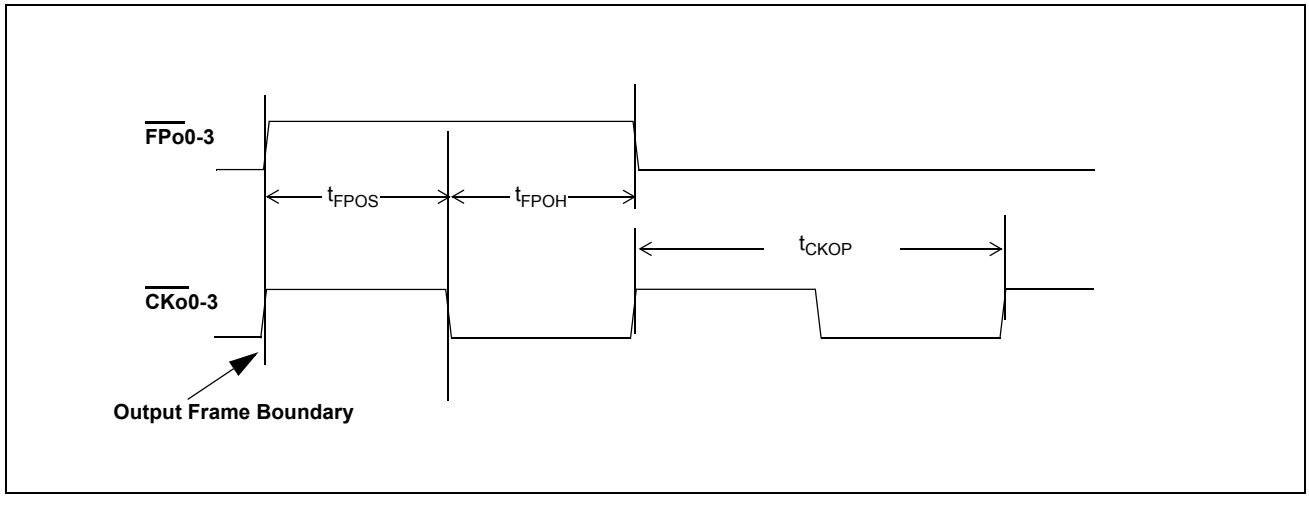



**Figure 11 - GCI Frame Pulse and Clock Output Timing**

### AC Electrical Characteristics - Output Clock Jitter Generation

| No. | Characteristic | Max. | Units | Notes[1,2] |
|---|---|---|---|---|
| 1 | Jitter at $\overline{CKO}$0-3 (8.192 MHz) | 1050 | ps-pp | |
| 2 | Jitter at $\overline{CKO}$0-3 (16.384 MHz) | 1030 | ps-pp | |
| 3 | Jitter at $\overline{CKO}$0-3 (32.768 MHz) | 920 | ps-pp | |
| 4 | Jitter at $\overline{CKO}$0-3 (65.536 MHz) | 810 | ps-pp | |

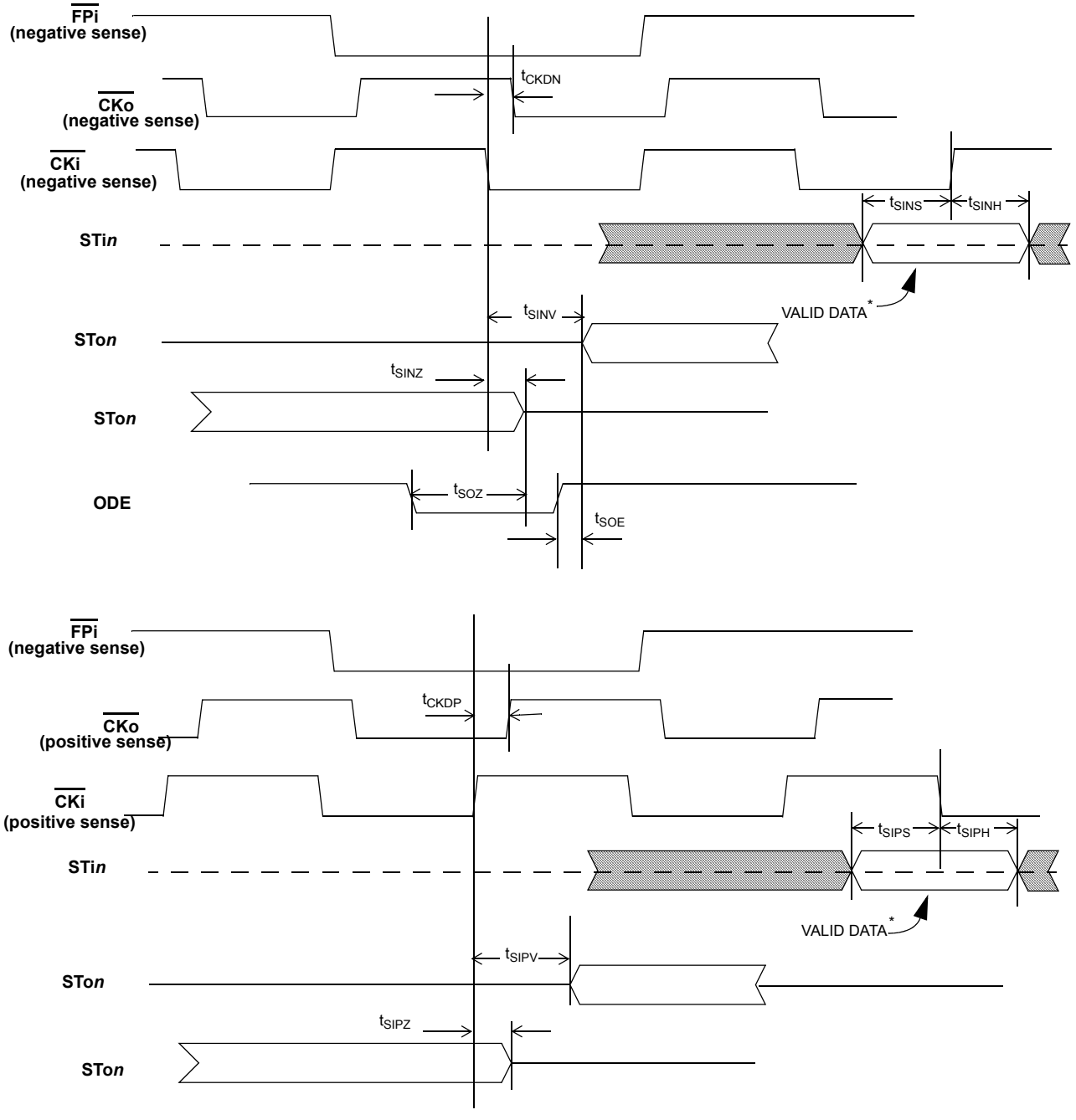
Note 1: $\overline{CKi}$ at 8 MHz, output clock source set to internal APLL. No jitter presented on the Cki0 input.

Note 2: For 65.536 MHz output clock, the total loading on the output should not be larger than 10pF.

**AC Electrical Characteristics[1] - Serial Data Timing[2] to $\overline{CKi}$**

| No. | Characteristic (Figure 12) | Sym. | Min. | Typ.[3] | Max. | Units | Notes[4] |
|---|---|---|---|---|---|---|---|
| 1 | $\overline{CKi}$ to $\overline{CKo}$ Positive edge Propagation Delay | $t_{CKDP}$ | 3.5 | | 8 | ns | $\overline{CKo}$ clock source = $\overline{CKi}$ |
| | | | 4.1 | | 9.2 | ns | $\overline{CKo}$ Clock source = Internal 131 MHz APLL output |
| 2 | $\overline{CKi}$ to $\overline{CKo}$ Negative edge Propagation Delay | $t_{CKDN}$ | 4.5 | | 9.2 | | $\overline{CKo}$ clock source = $\overline{CKi}$ |
| | | | 5 | | 10.1 | | $\overline{CKo}$ Clock source = Internal 131 MHz APLL output |
| 3 | STi to posedge $\overline{CKi}$ setup | $t_{SIPS}$ | -0.8 | | | ns | |
| 4 | STi to posedge $\overline{CKi}$ hold | $t_{SIPH}$ | 5.9 | | | ns | |
| 5 | STi to negedge $\overline{CKi}$ setup | $t_{SINS}$ | -0.8 | | | ns | |
| 6 | STi to negedge $\overline{CKi}$ hold | $t_{SINH}$ | 5.9 | | | ns | |
| 7 | Posedge $\overline{CKi}$ to Output Data Valid | $t_{SIPV}$ | 4.8 | | 11.6 | ns | SToA[5] |
| | | | 4.1 | | 13.7 | ns | SToB, C, D[5] |
| 8 | Negedge $\overline{CKi}$ to Output Data Valid | $t_{SINV}$ | 5.8 | | 12.9 | ns | SToA[5] |
| | | | 4.5 | | 14.8 | ns | SToB, C, D[5] |
| 9 | Posedge $\overline{CKi}$ to Output Data tri-state | $t_{SIPZ}$ | 4.3 | | 14.6 | ns | SToA[5] |
| | | | 4.6 | | 14.5 | ns | SToB, C, D[5] |
| 10 | Negedge $\overline{CKi}$ to Output Data tri-state | $t_{SINZ}$ | 5.3 | | 13 | ns | SToA[5] |
| | | | 5.7 | | 13.6 | ns | SToB, C, D[5] |
| 11 | ODE to Output Data tri-state | $t_{SOZ}$ | | | 10 | ns | SToA $C_L$ = 30pF, $R_L$ = 1 K[5] |
| | | | | | 11 | ns | SToB, C, D $C_L$ = 30pF, $R_L$ = 1 K[5] |
| 12 | ODE to Output Data Enable | $t_{SOE}$ | 4.5 | | 15 | ns | SToA[5] |
| | | | 6 | | 20 | ns | SToB, C, D[5] |

1. Characteristics are over recommended operating conditions unless otherwise stated.
2. All of these specifications refer to ST-BUS inputs and outputs with clock source set to $\overline{CKi}$.
3. Typical figures are at 25°C, $V_{DD\_CORE}$ at 1.8 V and $V_{DD\_IO}$ at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.
4. Loads on all serial outputs set to 30 pF
5. High Impedance is measured by pulling to the appropriate rail with $R_L$, with timing corrected to cancel time taken to discharge $C_L$.




**Note 1: $\overline{CKi}$ frequency is assumed to be twice of the STin data rate, so that the sampling point is at the 3/4 point of the bit cell, or 1 1/2 clock period after the active clock edge**

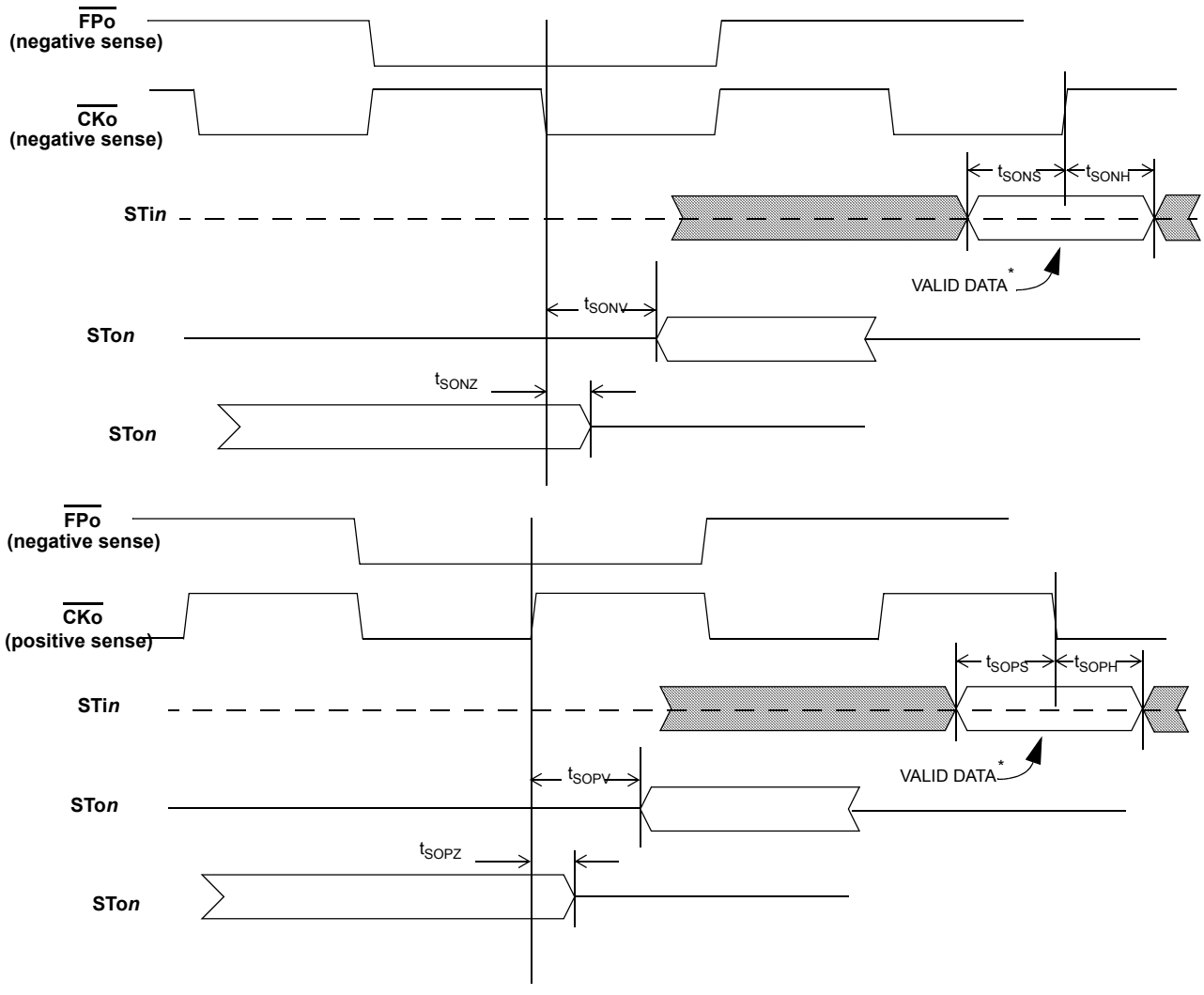
**Note 2: If $\overline{CKi}$ frequency is the same as the STin data rate, the sampling point moves to the 1/2 point of the bit cell, or 1/2 clock period after the active clock edge.**

**Figure 12 - Serial Data Timing to $\overline{CKi}$**

### AC Electrical Characteristics - Serial Data Timing[1] to $\overline{CKo}$[2]

| No. | Characteristic (Figure ) | Sym. | Min. | Typ. | Max. | Units | Notes[3] |
|---|---|---|---|---|---|---|---|
| 1 | STi to posedge $\overline{CKo}$ setup | $t_{SOPS}$ | 7.3 | | | ns | |
| 2 | STi to posedge $\overline{CKo}$ hold | $t_{SOPH}$ | -2.0 | | | ns | |
| 3 | STi to negedge $\overline{CKo}$ setup | $t_{SONS}$ | 7.3 | | | ns | |
| 4 | STi to negedge $\overline{CKo}$ hold | $t_{SONH}$ | -2.0 | | | ns | |
| 5 | Posedge $\overline{CKo}$ to Output Data Valid | $t_{SOPV}$ | 0.1 | | 2.7 | ns | SToA[4] |
| | | | 0 | | 4.6 | ns | SToB, C, D[4] |
| 6 | Negedge $\overline{CKo}$ to Output Data Valid | $t_{SONV}$ | -1.2 | | 1.7 | ns | SToA[4] |
| | | | -1.6 | | 3.7 | ns | SToB, C, D[4] |
| 7 | Posedge $\overline{CKo}$ to Output Data tri-state | $t_{SOPZ}$ | 0.9 | | 4.9 | ns | SToA[4] |
| | | | 0.1 | | 5.1 | ns | SToB, C, D[4] |
| 8 | Negedge $\overline{CKo}$ to Output Data tri-state | $t_{SONZ}$ | 0.4 | | 4.7 | ns | SToA[4] |
| | | | 0 | | 4.8 | ns | SToB, C, D[4] |

1. Data Capture points vary with respect to $\overline{CKo}$ edge depending on clock rates & fractional delay settings.
2. All of these specifications refer to ST-BUS inputs, ST-BUS outputs and $\overline{CKo}$ outputs set to internal clock source.
3. Typical figures are at 25°C, $V_{DD\_CORE}$ at 1.8 V and $V_{DD\_IO}$ at 3.3 V and are for design aid only: not guaranteed and not subject to production testing
4. Loads on all serial outputs set to 30 pF




**Note 1: $\overline{\text{CKo}}$ frequency is assumed to be twice of the STin data rate, so that the sampling point is at the 3/4 point of the bit cell, or 1 1/2 clock period after the active clock edge**

**Note 2: If $\overline{\text{CKo}}$ frequency is the same as the STin data rate, the sampling point moves to the 1/2 point of the bit cell, or 1/2 clock period after the active clock edge.**

**Figure 13 - Serial Data Timing to $\overline{\text{CKo}}$**

### AC Electrical Characteristics - $\overline{\text{CKo}}$ to Other $\overline{\text{CKo}}$ [1] Skew

| No. | Characteristic (Figure 12) | Sym. | Min. | Typ.[2] | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | $\overline{\text{CKo}}$1 to $\overline{\text{CKo}}$0 skew | $t_{CKOS1-0}$ | 0 | | 1.2 | ns | |
| 2 | $\overline{\text{CKo}}$2 to $\overline{\text{CKo}}$0 skew | $t_{CKOS2-0}$ | 0 | | 1.2 | ns | |
| 3 | $\overline{\text{CKo}}$1 to $\overline{\text{CKo}}$3 skew | $t_{CKOS1-3}$ | 0 | | 1.2 | ns | |
| 4 | $\overline{\text{CKo}}$2 to $\overline{\text{CKo}}$3 skew | $t_{CKOS2-3}$ | 0 | | 1.2 | ns | |
| 5 | $\overline{\text{CKo}}$3 to $\overline{\text{CKo}}$0 skew | $t_{CKOS3-0}$ | -0.6 | | 0.6 | ns | |
| 6 | $\overline{\text{CKo}}$2 to $\overline{\text{CKo}}$1 skew | $t_{CKOS2-1}$ | -0.6 | | 0.6 | ns | |

Note 1: All of these specifications refer to ST-BUS inputs, ST-BUS outputs and $\overline{\text{CKo}}$ outputs set to internal clock source.

Note 2: Typical figures are at 25°C, $V_{DD\_CORE}$ at 1.8 V and $V_{DD\_IO}$ at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

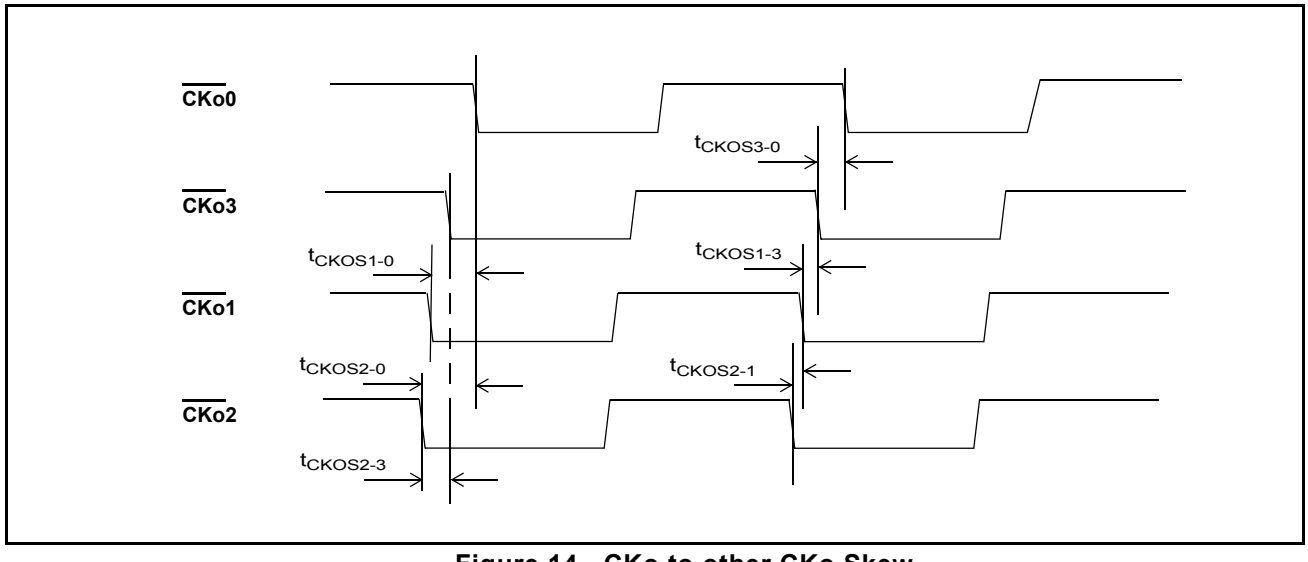



**Figure 14 - CKo to other CKo Skew**

**AC Electrical Characteristics - Microprocessor Bus Interface**

| No | Characteristics (Figure , & Figure 16) | Sym. | Min. | Typ.[1] | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | $\overline{DS}$ Recovery | $t_{DSRE}$ | 5 | | | ns | |
| 2 | $\overline{CS}$ Recovery | $t_{CSRE}$ | 0 | | | ns | |
| 3 | $\overline{CS}$ asserted setup to $\overline{DS}$ asserted | $t_{CSS}$ | 0 | | | ns | |
| 4 | Address, SIZ0-1, R/$\overline{W}$ setup to $\overline{DS}$ asserted | $t_{ADS}$ | 0 | | | ns | |
| 5 | $\overline{CS}$ hold from $\overline{DS}$ deasserted | $t_{CSH}$ | 0 | | | ns | |
| 6 | Address, SIZ0-1, R/$\overline{W}$ hold from $\overline{DS}$ deasserted | $t_{ADH}$ | 0 | | | ns | |
| 7 | Data valid to $\overline{DTA}$ asserted on read | $t_{DSR}$ | 0 | | | ns | $C_L$ = 50 pF, $R_L$ = 1 k[2] |
| 8 | $\overline{CS}$ deasserted to Data tri-stated on read | $t_{DZ}$ | | | 5 | ns | $C_L$ = 50 pF, $R_L$ = 1 k[2] |
| 9 | Data setup to $\overline{DS}$ asserted on write | $t_{WDS}$ | 0 | | | ns | |
| 10 | $\overline{CS}$ asserted to $\overline{WAIT}$ deasserted | $t_{CSWA}$ | | | 9 | ns | $C_L$ = 30 pF, $R_L$ = 1K[2] |
| 11 | Data hold from $\overline{DTA}$ asserted on write | $t_{DHW}$ | 0 | | | ns | |
| 12 | $\overline{DS}$ asserted to $\overline{WAIT}$ Asserted | $t_{WDD}$ | | | 9 | ns | $C_L$ = 50 pF, $R_L$ = 1 k[2] |
| 13 | $\overline{WAIT}$ deasserted to $\overline{DTA}$/$\overline{BERR}$ asserted skew | $t_{AKS}$ | 0 | | 10 | ns | $C_L$ = 50 pF, $R_L$ = 1 k[2] |
| 14 | $\overline{DS}$ asserted to $\overline{DTA}$ Asserted | $t_{AKD}$ | 35 | | 155 | ns | Connection Memory |
| | | | 50 | | 75 | ns | All other registers |
| 15 | $\overline{DS}$ deasserted to $\overline{DTA}$ Deasserted | $t_{AKH}$ | | | 7 | ns | $C_L$ = 30 pF, $R_L$ = 1 K[2] |
| 16 | $\overline{CS}$ deasserted to $\overline{DTA}$ tri-stated | $t_{DTHZ}$ | | | 13 | ns | $C_L$ = 30 pF, $R_L$ = 1 K[2] |
| 17 | $\overline{CS}$ deasserted to $\overline{WAIT}$ tri-stated | $t_{WAHZ}$ | | | 6 | ns | $C_L$ = 30 pF, $R_L$ = 1K[2] |
| 18 | $\overline{BE}$ or $\overline{UDS}$/$\overline{LDS}$ skew | $t_{DSK}$ | | | 20 | ns | |
| 19 | $\overline{BE}$ or $\overline{UDS}$/$\overline{LDS}$ to $\overline{DS}$ set-up | $t_{BEDS}$ | 0 | | | | |

1. Typical figures are at 25°C, $V_{DD\_CORE}$ at 1.8 V and $V_{DD\_IO}$ at 3.3 V and are for design aid only: not guaranteed and not subject to production testing
2. High Impedance is measured by pulling to the appropriate rail with $R_L$, with timing corrected to cancel time taken to discharge $C_L$.

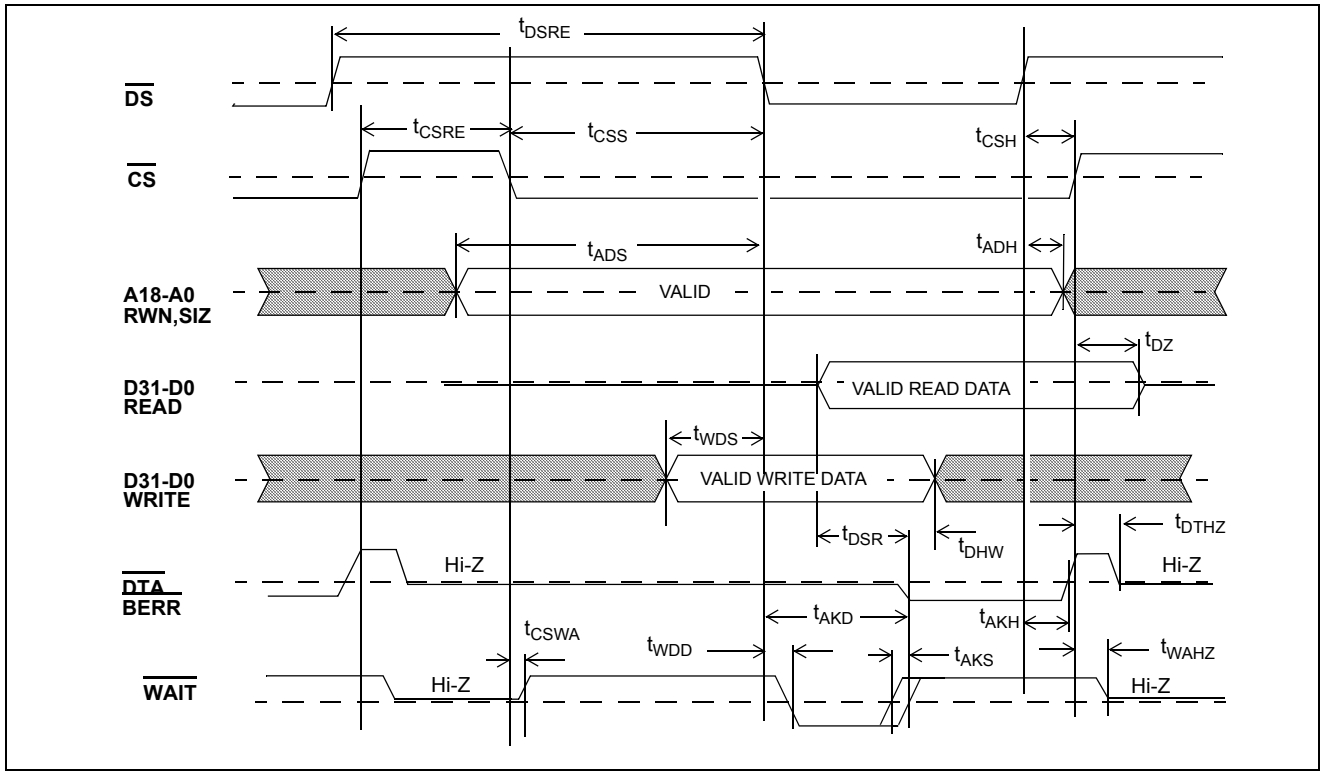



**Figure 15 - Microprocessor Bus Interface Timing**

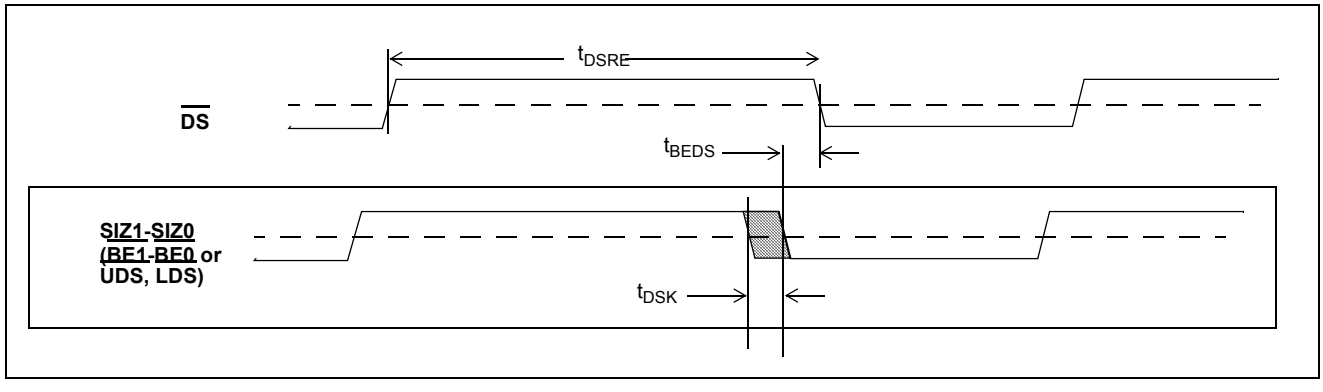



**Figure 16 - Intel Mode Timing**

**AC Electrical Characteristics[1] - JTAG Test Port and $\overline{\text{Reset}}$ Pin Timing**

| No. | Characteristic (Figure 17) | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | TCK Clock Period | $t_{TCKP}$ | 100 | | | ns | |
| 2 | TCK Clock Frequency | $t_{TCKF}$ | | | 10 | MHz | |
| 3 | TCK Clock Pulse Width High | $t_{TCKH}$ | 20 | | | ns | |
| 4 | TCK Clock Pulse Width Low | $t_{TCKL}$ | 20 | | | ns | |
| 5 | TMS Set-up Time | $t_{TMSS}$ | 10 | | | ns | |
| 6 | TMS Hold Time | $t_{TMSH}$ | 10 | | | ns | |
| 7 | TDi Input Set-up Time | $t_{TDIS}$ | 20 | | | ns | |
| 8 | TDi Input Hold Time | $t_{TDIH}$ | 60 | | | ns | |
| 9 | TDo Output Delay | $t_{TDOD}$ | | | 20 | ns | $C_L$ = 30 pF |
| 10 | $\overline{\text{TRST}}$ pulse width | $t_{TRSTW}$ | 20 | | | ns | |
| 11 | $\overline{\text{PWR}}$ pulse width | $t_{TPWR}$ | 20 | | | ns | |

1. Characteristics are over recommended operating conditions unless otherwise stated.

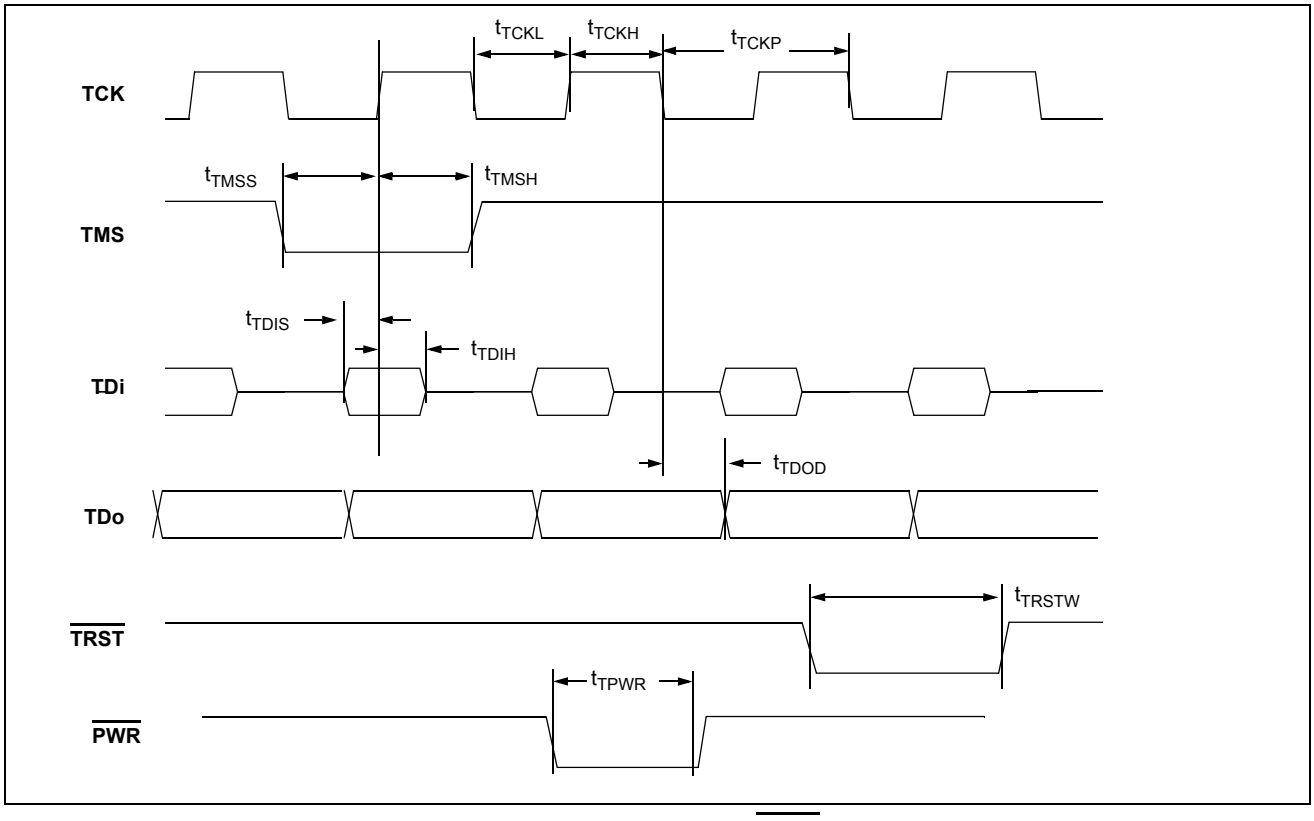
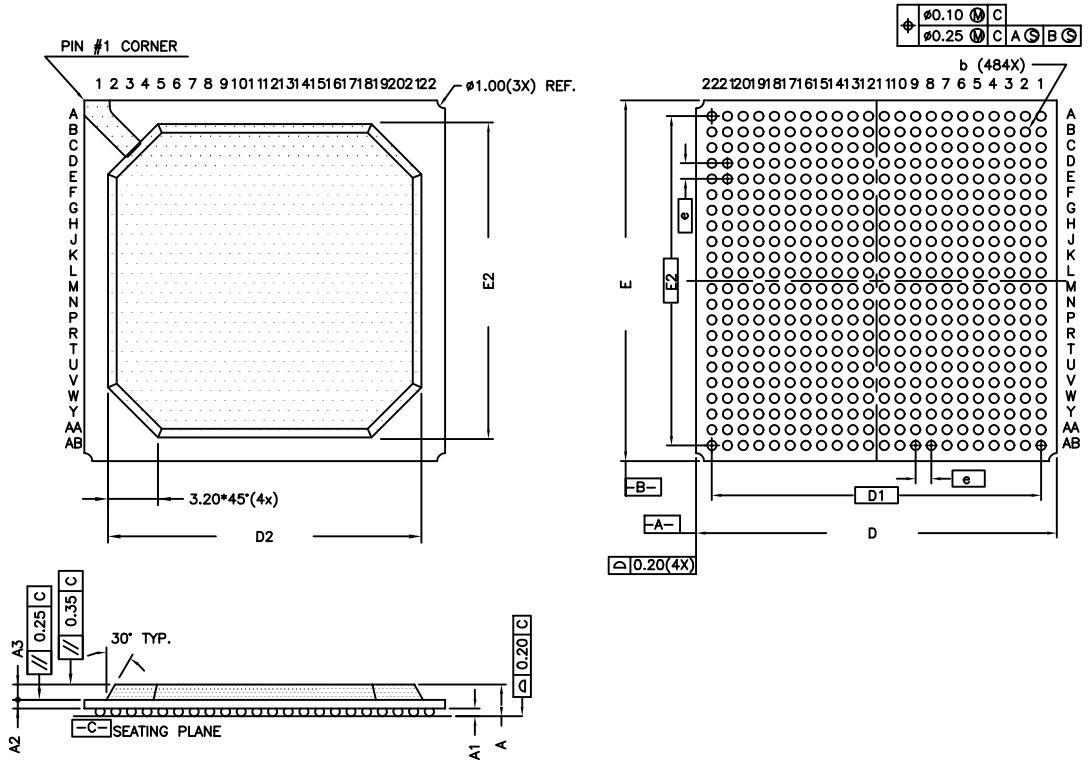



**Figure 17 - JTAG Test Port & $\overline{\text{PWR}}$ Reset Timing**




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 1.90 | 2.03 | 2.16 |
| A1 | 0.40 | 0.50 | 0.60 |
| A2 | | 0.56 Ref. | |
| A3 | | 0.97 Ref. | |
| b | 0.50 | 0.60 | 0.70 |
| D | 22.80 | 23.00 | 23.20 |
| D1 | | 21.00 Ref. | |
| D2 | | 20.00 Ref. | |
| E | 22.80 | 23.00 | 23.20 |
| E1 | | 21.00 Ref. | |
| E2 | | 20.00 Ref. | |
| e | | 1.00 Ref. | |

Confirms to JEDEC MS-034
AAJ-1 iss. A

NOTE:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER
3. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. NOT TO SCALE.
6. DETAILS OF A1 CORNER ARE OPTIONAL, AND MAY CONSIST OF INK DOT, LASER MARK OR METALISED MARKING, BUT MUST BE LOCATED WITHIN ZONE INDICATED.

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