BLF7G22L-100P; BLF7G22LS-100P Power LDMOS transistor Rev. 4 — 1 September 2015

AMPLEON

Product data sheet

Product profile

1.1 General description

100 W LDMOS power transistor for base station applications at frequencies from 2000 MHz to 2200 MHz.

Typical performance Table 1.

Typical RF performance at $T_{case} = 25$ °C in a common source class-AB production test circuit.

Test signal	f	I _{Dq}	V _{DS}	P _{L(AV)}	Gp	η_D	ACPR _{5M}
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	2110 to 2170	720	28	20	19.1	28.5	_34 <u>[1]</u>

^[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (2000 MHz to 2200 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

RF power amplifiers for W-CDMA base stations and multi carrier applications in the 2000 MHz to 2200 MHz frequency range

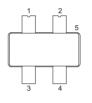
2. Pinning information

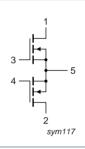
Table 2. Pinning

	9			
Pin	Description		Simplified outline	Graphic symbol
BLF7G22L-	100P (SOT1121A)			
1	drain1			
2	drain2		1 2 [~] [~]	1
3	gate1			<u>,</u> [⊷
4	gate2		5	3 - 5
5	source	<u>[1]</u>	3 4	4 1
				2 sym117

BLF7G22LS-100P (SOT1121B)

1	drain1	
2	drain2	
3	gate1	
4	gate2	
5	source	[1]





[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BLF7G22L-100P	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1121A		
BLF7G22LS-100P	-	earless flanged LDMOST ceramic package; 4 leads	SOT1121B		

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
R _{th(j-c)}	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 20 W	0.36	K/W

6. Characteristics

Table 6. Characteristics

 $T_i = 25$ °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.6 \text{ mA}$	65	70	-	V
V _{GS(th)}	gate-source threshold voltage	$V_{DS} = 10 \text{ V}; I_{D} = 60 \text{ mA}$	1.5	2	2.3	V
I _{DSS}	drain leakage current	$V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V}$	-	-	2	μА
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	12.3	-	Α
I _{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	200	nΑ
9 _{fs}	forward transconductance	V_{DS} = 10 V; I_{D} = 60 mA	-	530	-	mS
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 2100 \text{ mA}$	-	240	-	mΩ

7. Test information

Table 7. Functional test information

Test signal: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1, 1-64 PDPCH; f_1 = 2112.5 MHz; f_2 = 2117.5 MHz; f_3 = 2162.5 MHz; f_4 = 2167.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 720 mA; T_{case} = 25 °C; 2 sections combined unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$P_{L(AV)}$	average output power		-	20	-	W
Gp	power gain	$P_{L(AV)} = 20 W$	17.8	19.1	-	dB
RLin	input return loss	$P_{L(AV)} = 20 W$	-	-16	-9	dB
η_{D}	drain efficiency	$P_{L(AV)} = 20 W$	24	28.5	-	%
ACPR _{5M}	adjacent channel power ratio (5 MHz)	$P_{L(AV)} = 20 W$	-	-34	-28	dBc

7.1 Ruggedness in class-AB operation

The BLF7G22L-100P and BLF7G22LS-100P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 28 \text{ V}$; $I_{Dq} = 720 \text{ mA}$; $P_L = 100 \text{ W}$ (CW); f = 2110 MHz.

7.2 Impedance information

Typical push-pull impedance

Measured load pull data. Typical values unless otherwise specified.

f	Z _S	Z _L
MHz	Ω	Ω
2110	1.79 – j4.95	2.27 – j3.64
2140	2.37 - j5.49	2.27 – j3.64
2170	2.54 - j5.86	1.84 – j3.57

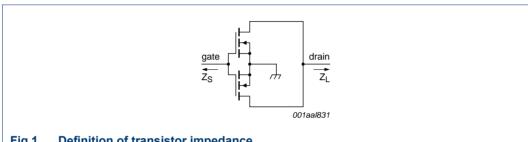
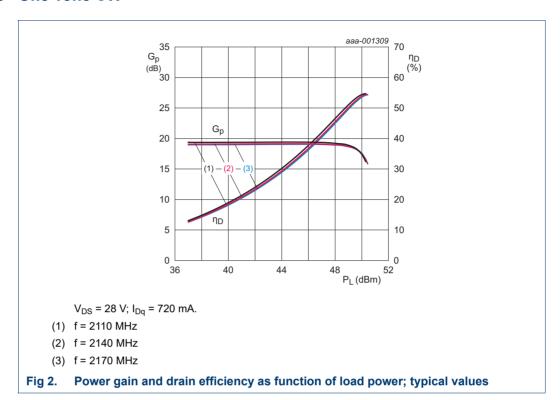
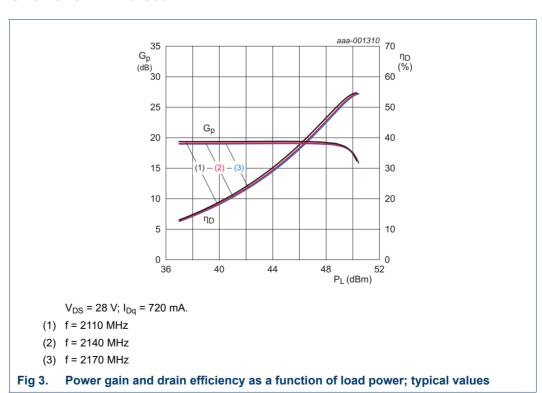


Fig 1. **Definition of transistor impedance**

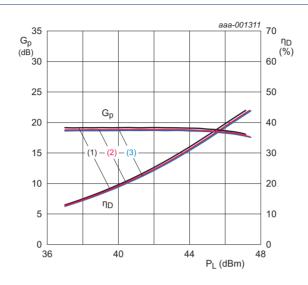
7.3 One Tone CW



7.4 One Tone CW-Pulsed



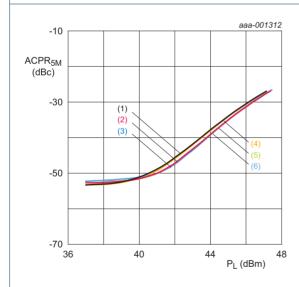
7.5 1-Carrier W-CDMA



 $V_{DS} = 28 \text{ V}; I_{Dq} = 720 \text{ mA}.$

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

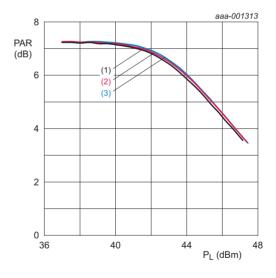
Fig 4. Power gain and drain efficiency as a function of load power; typical values



 V_{DS} = 28 V; I_{Dq} = 720 mA.

- (1) f = 2110 MHz; f + 5 MHz
- (2) f = 2140 MHz; f + 5 MHz
- (3) f = 2170 MHz; f + 5 MHz
- (4) f = 2110 MHz; f 5 MHz
- (5) f = 2140 MHz; f 5 MHz
- (6) f = 2170 MHz; f 5 MHz

Fig 5. Adjacent channel power ratio (±5 MHz) as a function of load power; typical values

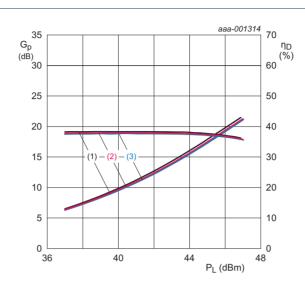


 $V_{DS} = 28 \text{ V}; I_{Dq} = 720 \text{ mA}.$

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

Fig 6. Peak-to-average ratio as a function of load power; typical values

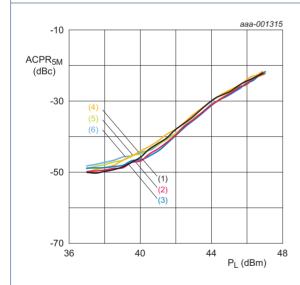
7.6 2-Carrier W-CDMA



 V_{DS} = 28 V; I_{Dq} = 720 mA.

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

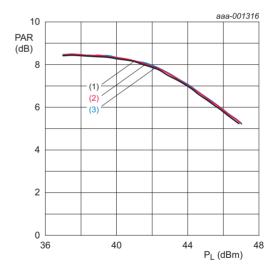
Fig 7. Power gain and drain efficiency as a function of load power; typical values



 V_{DS} = 28 V; I_{Dq} = 720 mA.

- (1) f = 2110 MHz; f + 5 MHz
- (2) f = 2140 MHz; f + 5 MHz
- (3) f = 2170 MHz; f + 5 MHz
- (4) f = 2110 MHz; f 5 MHz
- (5) f = 2140 MHz; f 5 MHz
- (6) f = 2170 MHz; f 5 MHz

Fig 8. Adjacent channel power ratio (±5 MHz) as a function of load power; typical values



 $V_{DS} = 28 \text{ V}; I_{Dq} = 720 \text{ mA}.$

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

Fig 9. Peak-to-average ratio as a function of load power; typical values

7.7 Test circuit

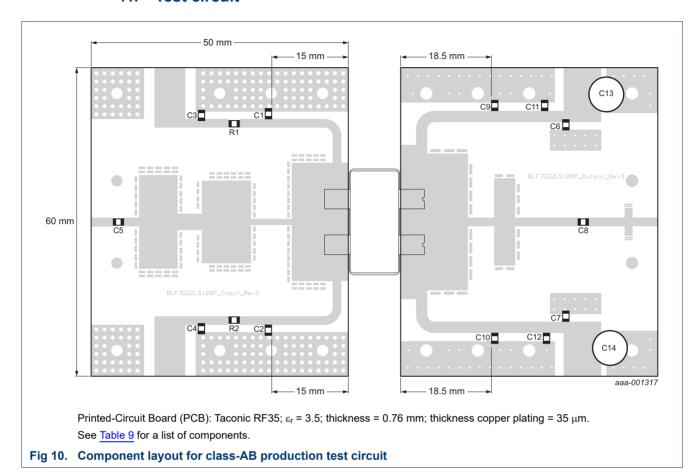


Table 9. List of components

For test circuit see Figure 10.

Component	Description	Value	Remarks
C1, C2, C9, C10	multilayer ceramic chip capacitor	8.2 pF	[1]
C3, C4, C6, C7	multilayer ceramic chip capacitor	1 μF	Murata
C5, C8	multilayer ceramic chip capacitor	33 pF	[2]
C11, C12	multilayer ceramic chip capacitor	0.1 μF	Murata
C13, C14	electrolytic capacitor	1000 μF; 50 V	
R1, R2	Chip resistor	5.1 Ω	Vishay Dale 0805

^[1] American Technical Ceramics type 100A or capacitor of same quality.

^[2] American Technical Ceramics type 800B or capacitor of same quality.

8. Package outline

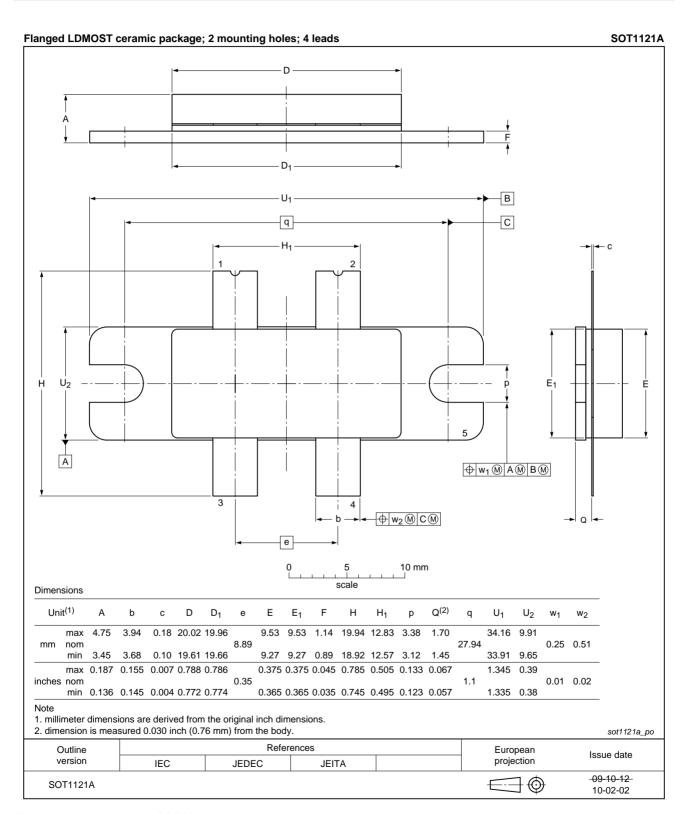


Fig 11. Package outline SOT1121A

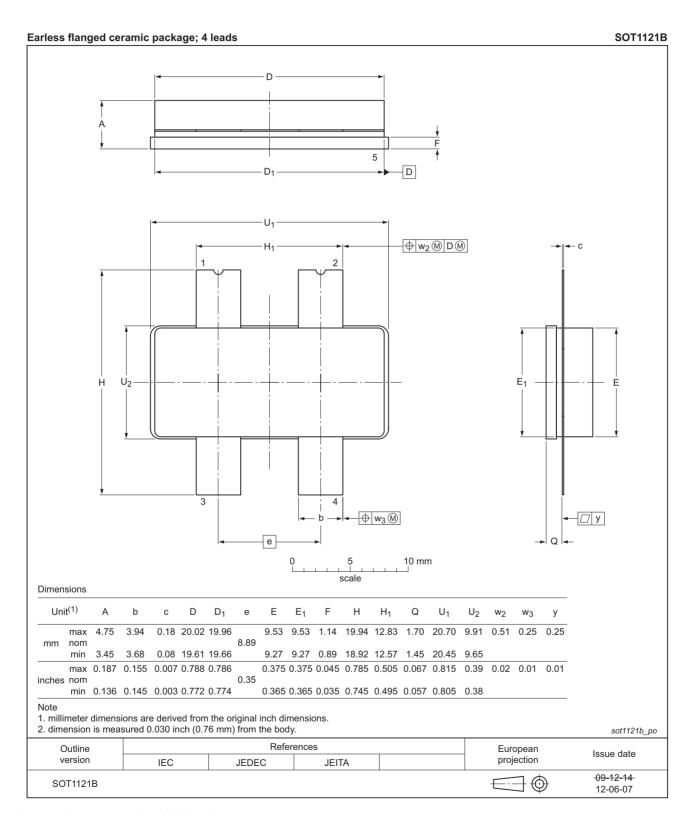


Fig 12. Package outline SOT1121B

9. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical Channel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
PDPCH	Transmission Power of Dedicated Physical Channel
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BLF7G22L-100P_BLF7G22LS-100P#4	20150901	Product data sheet	-	BLF7G22L-100P_BL F7G22LS-100P v.3	
Modifications:	 The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. 				
	 Legal texts have been adapted to the new company name where appropriate. 				
BLF7G22L-100P_BLF7G22LS-100P v.3	20120102	Product data sheet	-	BLF7G22L-100P_BL F7G22LS-100P v.2	
BLF7G22L-100P_BLF7G22LS-100P v.2	20111110	Preliminary data sheet	-	BLF7G22L-100P_BL F7G22LS-100P v.1	
BLF7G22L-100P_BLF7G22LS-100P v.1	20110519	Objective data sheet	-	-	

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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