500mW MONAURAL SPEAKER AMPLIFIER

■FEATURES

- ●Operating Voltage +2.7 to +5.5V
- ●Operating Current 3mA typ.
  in Shutdown Mode 2μA max. (Shutdown Mode)
- ●Output Power 500mW typ. (V^+=5V, R_L=8Ω, THD=1%)
  500mW typ. (V^+=5V, R_L=16Ω, THD=1%)
  270mW typ. (V^+=3.3V, R_L=8Ω, THD=1%)
- ●Single-end input and Differential input corresponds
- ●Pop Noise Suppression Circuit
- ●Thermal Shutdown Circuit
- ●CMOS Technology
- ●Package Outline MSOP8(VSP8)*, HSOP8-M1,
  DFN8-V1(ESON8-V1)

* MEET JEDEC MO-187-DA

■GENERAL DESCRIPTION

The NJU72060 is a 500mW-output audio power amplifier. It is suitable for various applications which are required functions such as voice guidance, notification sound, and alarm.

The NJU72060 has a shutdown function providing low current consumption at no input signals (mute). It also reduces pop noise turning active and shutdown mode.

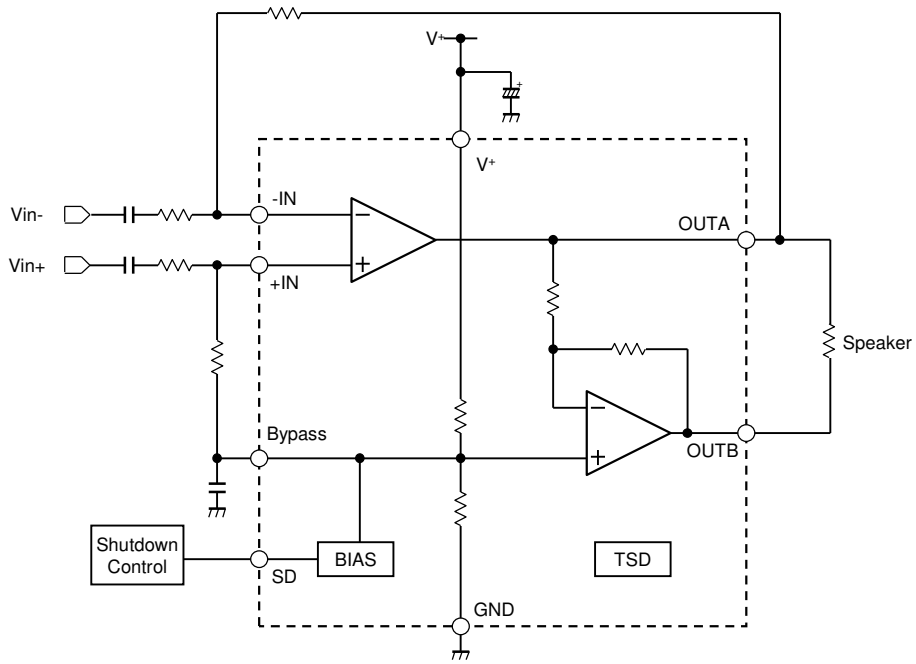
■APPLICATION

- ●All household electrical appliances
- ●All housing equipment
- ●All portable equipment

■MONAURAL SPEAKER AMPLIFIER VARIATION

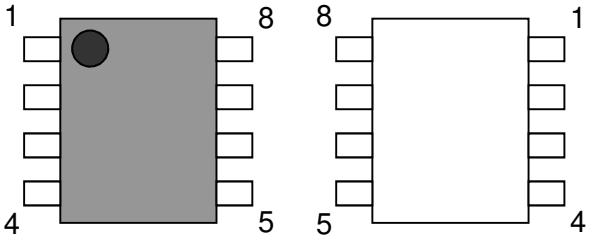
Output Power	Part No.	Notes
3.0W	NJU8759	Class D
1.2W	NJU7089	-
1.2W	NJU72065	with Volume

■APPLICATION CIRCUIT

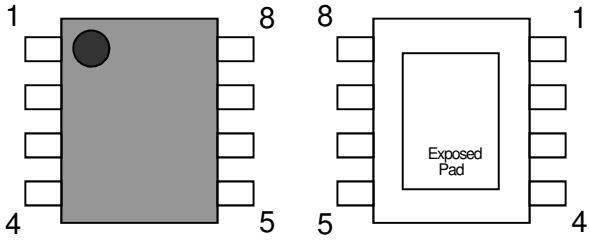


■PIN CONFIGURATION

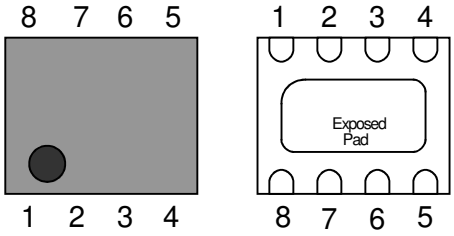
MSOP8(VSP8) MEET JEDEC MO-187-DA



HSOP8-M1



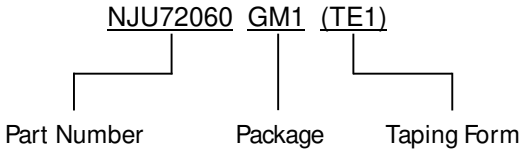
DFN8-V1(ESON8-V1)



PIN NO.	SYMBOL	FUNCTION
1	SD	Shutdown terminal
2	Bypass	Reference voltage terminal
3	+IN	Noninverted input terminal
4	-IN	Inverted input terminal
5	OUTA	Output A terminal
6	V+	Supply voltage terminal
7	GND	Ground terminal
8	OUTB	Output B terminal
Exposed Pad (1)	-	Ground terminal (HSOP8-M1, ESON8-V1)

(1): The PAD in the center part on the back is connected with the internal GND, therefore it connects to GND.

■MARK INFORMATION



■ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ(pcs)
NJU72060R	VSP8	YES	YES	Sn2Bi	72060	21	2,000
NJU72060GM1	HSOP8-M1	YES	YES	Pure Sn	72060	81	3,000
NJU72060KV1	ESON8-V1	YES	YES	SnAnCu	72060	4.6	3,000

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	+7	V
Input Voltage (1)	V_{IN}	-0.3 to V^+ +0.3	V
Output Current	I_O	400	mA
Power Dissipation (Ta=25°C)	P_D	(2-layer / 4-layer)	mW
MSOP8(VSP8) (2)		520 / 680	
HSOP8-M1 (3)		720 / 1800	
DFN8-V1(ESON8-V1) (3)		530 / 1400	
Junction Temperature	T_{jmax}	+150	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

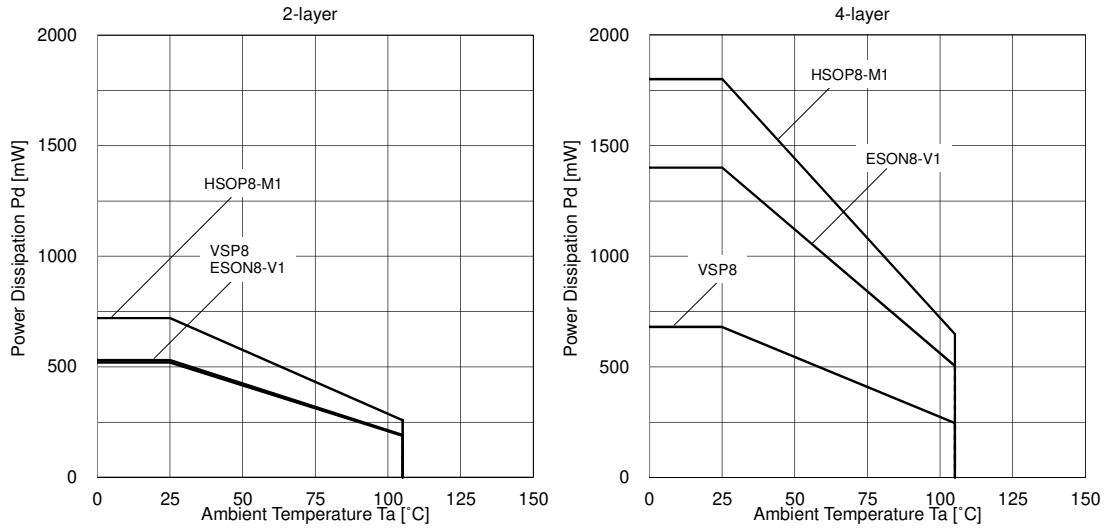
(1): SD, +IN, -IN, OUTA, OUTB terminal.

■THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction-to-ambient thermal resistance	Θja	(2-layer / 4-layer)	°C/W
MSOP8(VSP8) (2)		242.6 / 182.5	
HSOP8-M1 (3)		174.6 / 70.7	
DFN8-V1(ESON8-V1) (3)		234.7 / 86.8	
Junction-to-Top of package characterization parameter	ψjt	(2-layer / 4-layer)	°C/W
MSOP8(VSP8) (2)		57.9 / 49.2	
HSOP8-M1 (3)		42.2 / 28.4	
DFN8-V1(ESON8-V1) (3)		29.7 / 21.5	

(2): Mounted on glass epoxy board. (76.2x114.3x1.6mm:based on EIA/JEDEC standard, 2layers FR-4)
Mounted on glass epoxy board. (76.2x114.3x1.6mm:based on EIA/JEDEC standard, 4layers FR-4)
(3): Mounted on glass epoxy board. (101.5x114.5x1.6mm:based on EIA/JEDEC standard, 2layers FR-4, with Exposed Pad)
Mounted on glass epoxy board. (101.5x114.5x1.6mm:based on EIA/JEDEC standard, 4layers FR-4, with Exposed Pad)
For 4layers: Applying 99.5x99.5mm inner Cu area and a thermal via hole to a board on JEDEC standard JESD51-5.

■POWER DISSIPATION vs. AMBIENT TEMPERATURE



■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Operating Voltage Range	V^+	+2.7 to +5.5	V
Operating Temperature Range	T_{opr}	-40 to +105	°C

■ELECTRICAL CHARACTERISTICS

♦**Amplifier** (Ta=25°C, V^+=+5V, G_V=6dB, f=1kHz, R_L=8Ω, Active mode unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current 1	I_{DD1}	No signal, R_L=∞	-	3	6	mA
Operating Current 2	I_{DD2}	No signal, R_L=∞, V_{SD}=0.25V	-	-	2	μA
Output Power 1	P_{O1}	THD≤1%, BW=400Hz-20kHz	-	500	-	mW
Output Power 2	P_{O2}	THD≤1%, BW=400Hz-20kHz, R_L=16Ω	-	500	-	mW
Output Power 3	P_{O3}	THD≤1%, BW=400Hz-20kHz, V^+=3.3V	-	270	-	mW
Maximum Output Voltage 1	V_{OM1}	V_{IN}=0V, OUTA-OUTB	2.5	3	-	V
Maximum Output Voltage 2	V_{OM2}	V_{IN}=5V, OUTA-OUTB	-	-3	-2.5	V
Voltage Gain	G_V	V_{in}=0.5Vrms	5	6	7	dB
Shutdown Attenuation	ATT_{SD}	ΔV_{IN}=±2.5V, Shutdown	-	135	-	dB
Total Harmonic Distortion	THD+N	P_O=400mW, BW=400Hz-20kHz	-	0.2	-	%
Supply Voltage Rejection Ratio	SVR	V^+=3 to 5V	-	70	-	dB
Output Voltage	V_O	-	-	2.5	-	V
Output Offset Voltage	V_{OD}	No signal	-	-	35	mV

♦**Control Logic** (Ta=25°C unless otherwise specified)

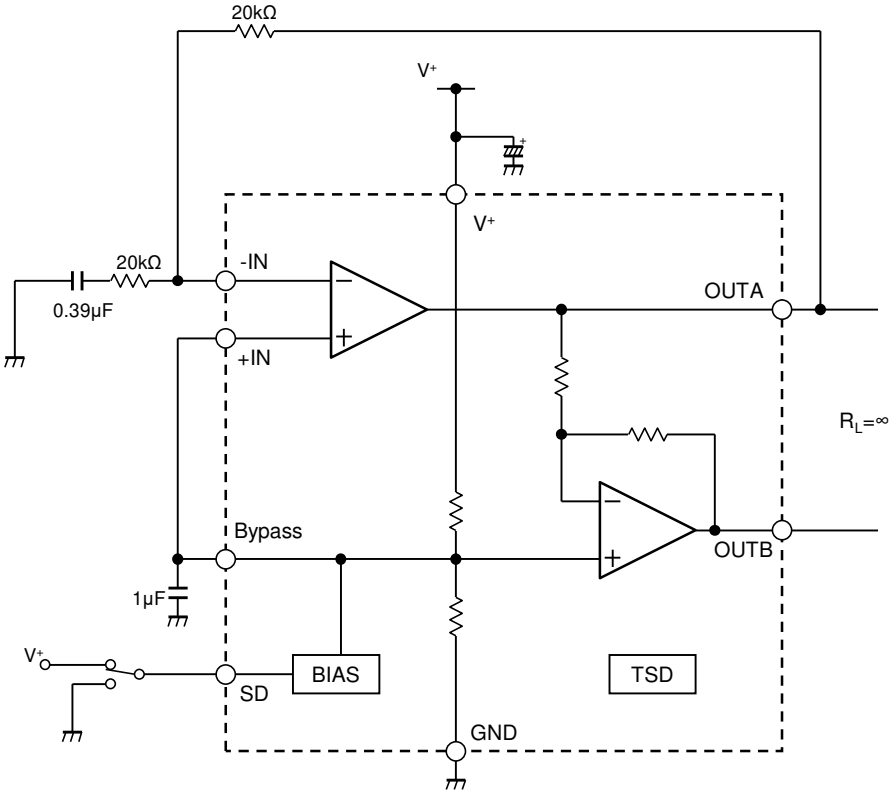
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SD Terminal High Level Input Voltage	V_{IH}	-	1.5	-	V^+	V
SD Terminal Low Level Input Voltage	V_{IL}	-	0	-	0.25	V

■CONTROL TERMINAL EXPLANATION

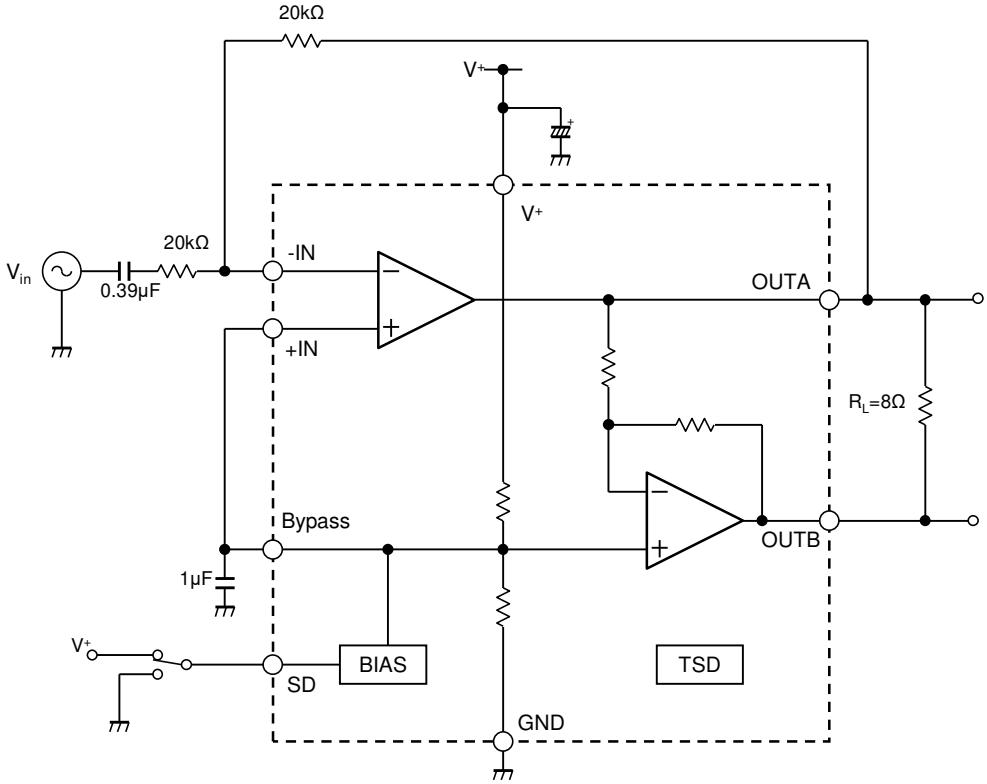
MODE	CONTROL SIGNAL (SD Terminal)	STATUS
Shutdown	L (=V_{IL})	IC is standby.
Active	H (=V_{IH})	IC is active.

■TEST CIRCUIT

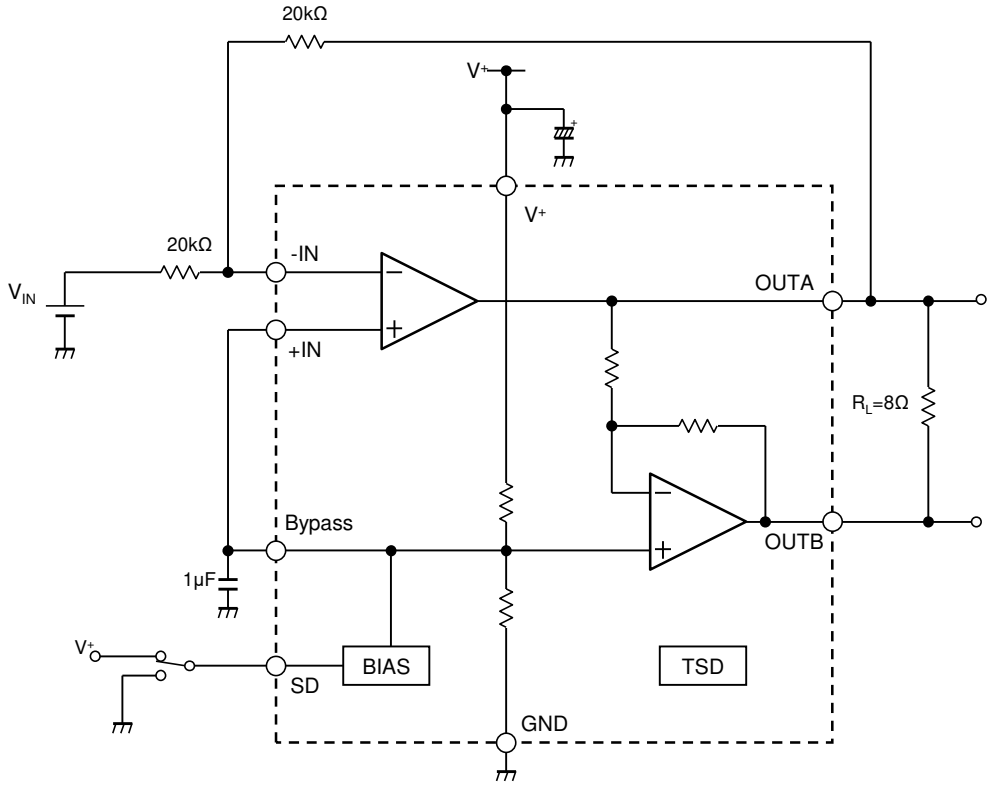
♦ I_{DD1}, I_{DD2}



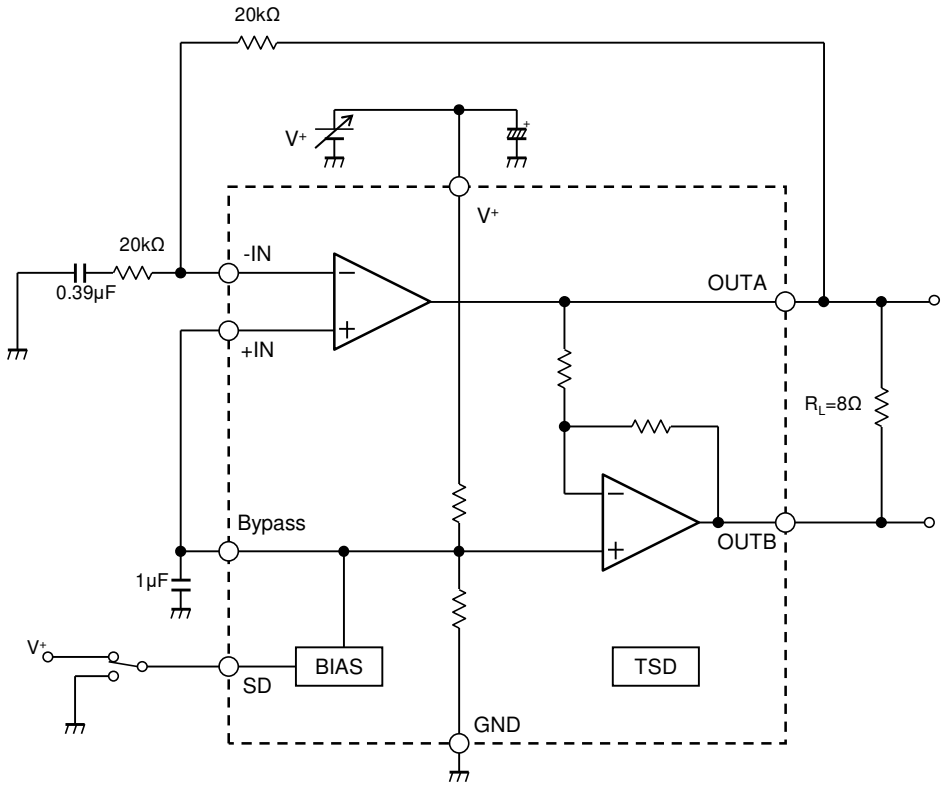
♦ P_{O1}, P_{O2}, P_{O3}, G_V, THD+N, V_O, V_{OD}



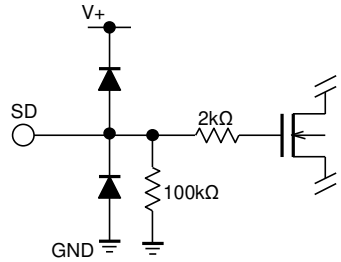
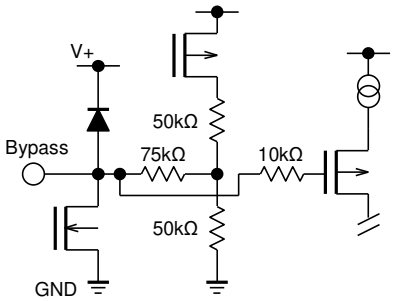
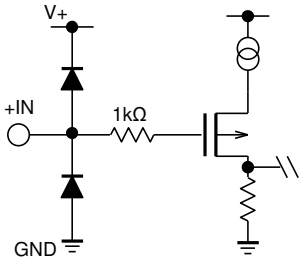
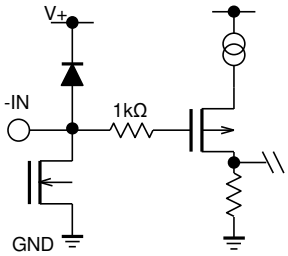
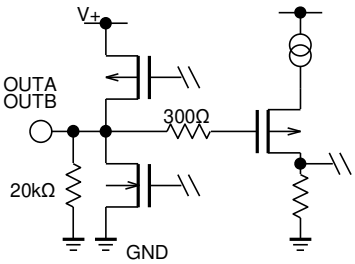
♦ V_{OM1}, V_{OM2}, ATT_{SD}



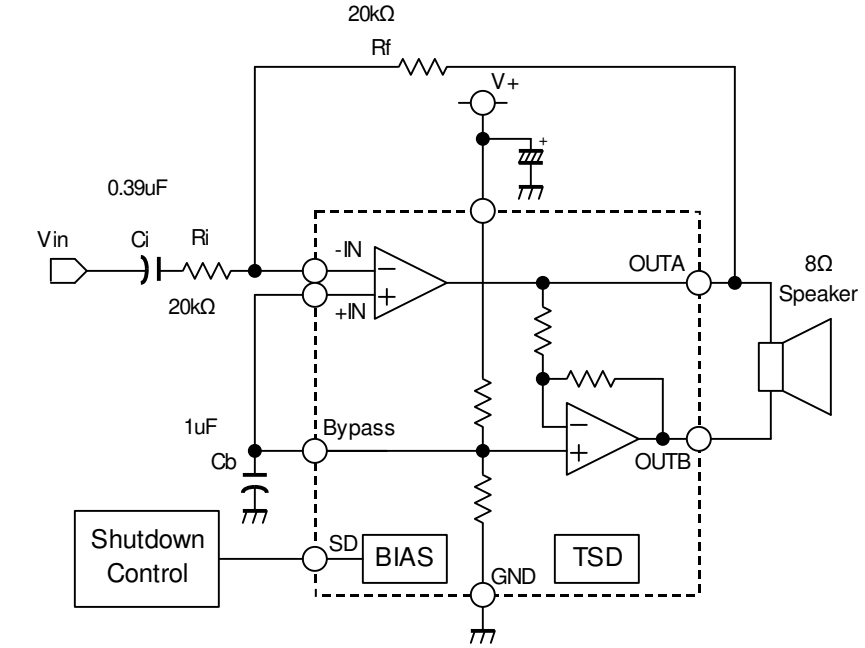
♦ SVR

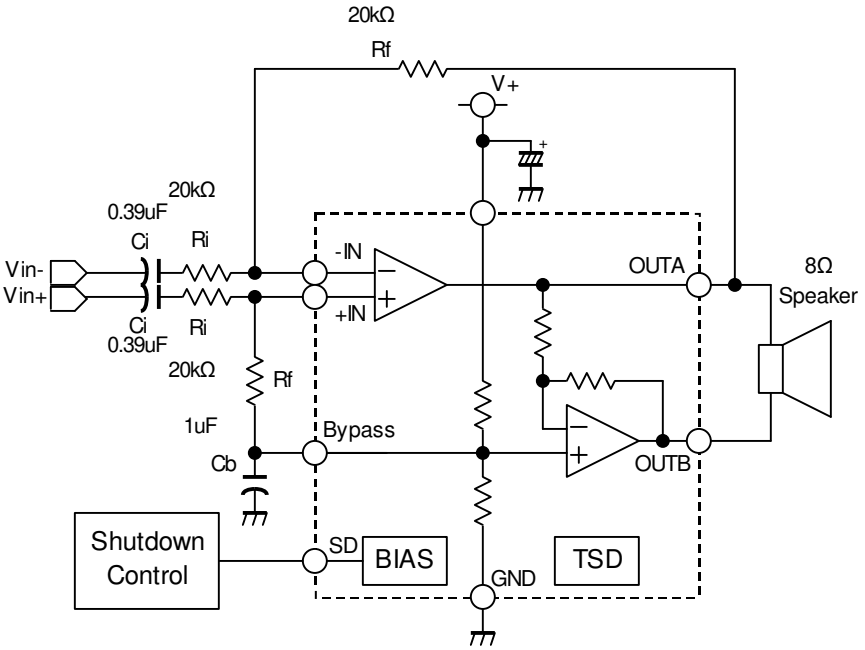


■TERMINAL DESCRIPTION

PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
1	SD	Shutdown terminal		0V
2	Bypass	Reference voltage terminal		$V^+/2$
3	+IN	Noninverted input terminal		$V^+/2$
4	-IN	Inverted input terminal		$V^+/2$
5 8	OUTA OUTB	Output A terminal Output B terminal		$V^+/2$

■APPLICATION CIRCUIT





■PRECAUTIONS FOR USE OF AUDIO AMPLIFIER IC

1. Power Supply

Use a stable power supply to operate the IC stably. Furthermore, please design so that unexpected abnormal overcurrent does not flow more than necessary to prevent the IC breakdown and the spread of the effects.

2. Inductive Load

If your design includes an inductive load, the IC malfunction or breakdown caused by the current resulting from the inrush current at ON or the current resulting from the back electromotive force at OFF. Incorporate a protection circuit into the design to prevent these. The IC breakdown may cause smoke or ignition.

3. External parts

Carefully select external parts (such as input and feedback resistors and capacitors), load components (such as a speaker) taking into consideration absolute maximum ratings, characteristics variation by temperature and leakage current characteristics.

If there is a leakage current such as input or negative feedback capacitor, the IC output DC voltage will increase. So, if this output voltage is connected to a speaker, overcurrent or speaker failure or IC failure may cause smoke or ignition.

4. Auxiliary functions

Some audio amplifier ICs have the auxiliary functions which suppress breaking themselves under unexpected abnormal conditions. These auxiliary functions are not guarantee as they operate over absolute maximum ratings. It is essential to design as the auxiliary functions do not operate. Do not design depending on the auxiliary functions.

4.1 Thermal shutdown circuit

The thermal shutdown circuit is a suspension circuit of IC's operation to prevent the junction temperature endlessly increase under unexpected abnormal conditions. The IC will return to operate under normal junction temperature.

The thermal shutdown function is not guarantee as it operates over temperature of absolute maximum ratings. Depending on the method of use and usage conditions may cause the thermal shutdown circuit to not operate properly or the IC breakdown before operation.

4.2 Current Limit Circuit

The current limit circuit limits output current to below a constant value to prevent output current endlessly increase under unexpected abnormal conditions.

Depending on the method of use and usage conditions such as exceeding absolute maximum ratings may cause the current limit circuit to not operate properly or the IC breakdown before operation.

■APPLICATION NOTES

The NJU72060 is a 0.5W monaural speaker amplifier. It operates from 2.7V supply. So it can reduce output coupling capacitor because it has a BTL amplifier. The voltage gain is set by the user-selected resister (Ri, Rf). The NJU72060 equips with a shutdown [SD] mode. It reduces supply current and turns to mute at shutdown mode. It reduces pop noise at turning shutdown and active mode.

In this application note, the usage of this IC and its operation are discussed.

1. Operating Overview

Fig.1 and Fig.2 shows the NJU72060 block diagram. It comprises of two power amplifiers (Amp-A, Amp-B), a bias circuit (BIAS), and a thermal shutdown (TSD) circuit. The Amp-A uses external resistors and it has adjustable gain. The Amp-B is configured with a fixed gain of Av=-1 and produces the inverted signal of Amp-A output. The NJU72060 outputs twice voltage and four times power compared to a single-ended amplifier because it is BTL amplifier which speaker's load resistance is connected between the OUTA terminal and the OUTB terminal. It stops all circuits at the shutdown [SD] mode. As a result, the shutdown mode reduces the supply current. Time constant which is made up the external capacitor (Cb) and internal resistance reduces disturbing pop noise at turning active and shutdown mode. For details, see 3. Pop Noise at turning SD terminal. But Cb value depends on the turn-on time (shutdown to active time). For details, see 4. Turn on time / turn off time.

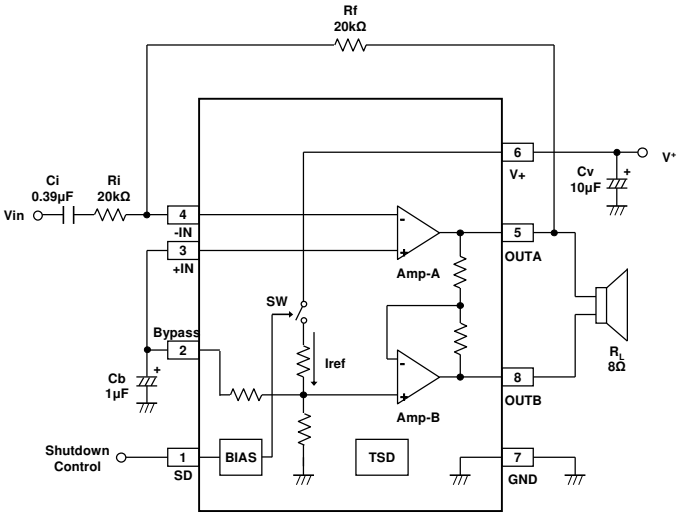


Fig.1 Block diagram and Application circuit (Single-end Input)

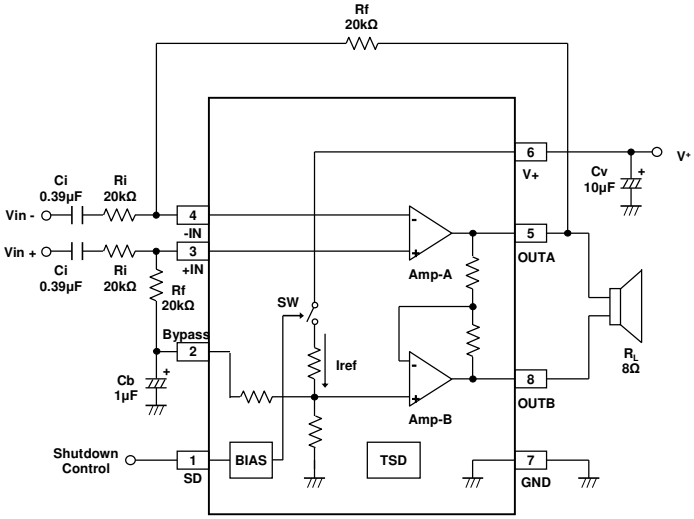


Fig. 2 Block diagram and Application circuit (Differential Input)

2. External Component

2.1 Bypass Capacitor

Power source bypass capacitor (Cv) reduces a noise and it stabilizes power source. Cv should have margin for temperature characteristics and the better characteristic in high frequency. Design to provide low impedance for the wiring between the IC and the capacitor. It is necessary to provide lower impedance in case that the NJU72060 uses high current. So it is recommended a ceramic chip capacitor which has low ESR.

2.2 Input Resistor and Feedback Resistor

The NJU72060's gain depends on Input Resistor (Ri) and Feedback Resistor (Rf). The values of Ri and Rf affect output noise and disturbing pop noise in case that they increase.

So Ri affects frequency response. It is necessary to consider about 2.3 Input Coupling Capacitor and select Ri.

The NJU72060's BTL output voltage gain (Gv) is set by the following.

$$Gv = \frac{V_{OUTA} - V_{OUTB}}{V_{-IN} - V_{+IN}} = 20 \cdot Log\left(2 \cdot \frac{R_f}{R_i}\right) \quad [dB]$$

2.3 Input Coupling Capacitor

The input coupling capacitor (Ci) is necessary for DC cut. Ci forms a HPF with Ri and low frequency signal is cut. Lower frequency signal is passed through in case that values of Ci and Ri increase, but pop noise may be loud.

The input coupling capacitor (Ci) is set by the following under the condition that the cutoff frequency is fc.

$$C_i = \frac{1}{2\pi \cdot R_i \cdot f_c} [F]$$

2.4 Bypass Capacitor for Reference Voltage

The capacitor (Cb) is connected to the Bypass terminal and it reduces a noise and it stabilizes reference voltage. The value of Cb causes pop noise, PSRR and turn on time. Pop noise and PSRR are improved in case that value of Cb is increases. See 3. Pop Noise at turning SD terminal and 5. PSRR vs Cb, 7. Volume. But turn on time is longer in case that Cb increases. See 4. Turn on time / Turn off time.

Table 1 shows recommendation value range of external component. It is merely recommendation. There is possibility in the using in case that their value varies from the recommendation. In the using, it should verify the characteristics.

Table 1. Function and recommendation value range of external components

Component	Function	Recommendation value	
		Default	Range
Cv	Bypass capacitor for power source	10μF	1μF<Cv
Ri	Input resistor	20kΩ	10kΩ<Ri<50kΩ
Rf	Feedback resistor	20kΩ	10kΩ<Rf<50kΩ
Ci	Input coupling capacitor	0.39μF	0.047μF<Ci
Cb	Bypass capacitor for reference voltage	1μF	0.1μF<Cb
R_L	Load resistor(speaker)	8Ω	4Ω<R_L

3. Pop Noise at turning SD terminal

The NJU72060 has pop noise suppression circuit when it turns SD terminal. But pop noise depends on the value of external components. This section shows the point of pop noise reduction.

3.1 Turn on: Shutdown (SD terminal=Low) to Active (SD terminal=High)

The NJU72060 is BTL amplifier and it does not generate sound, if there is no difference voltage between two outputs at turning to active mode. But difference voltage which Amp-A output voltage is higher than the reference voltage (the Bypass terminal voltage) and Amp-B output voltage is lower than the reference voltage (the Bypass terminal voltage) occurs and generates pop noise at turning to active mode because input coupling capacitor (Ci) is charged. In order to reduce pop noise, the NJU72060 is operated by a voltage follower amplifier Amp-2 until the reference voltage rises (Fig. 3), and both the output of Amp-A and Amp-B become the same potential as the reference voltage as a result, there will be no potential difference and pop noise can be prevented. It is designed that the amplifier operates after charged Ci and risen the -IN terminal voltage in the typical circuit (Fig. 4).

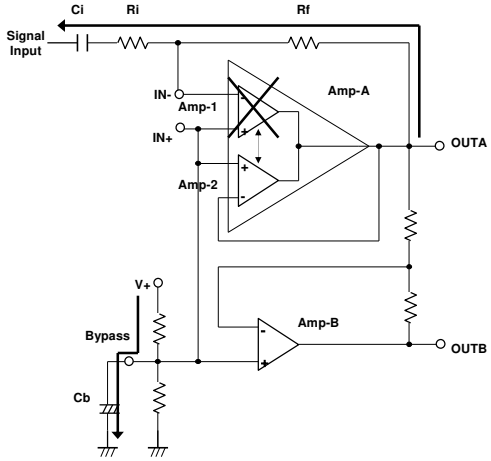


Fig.3 During voltage follower operation

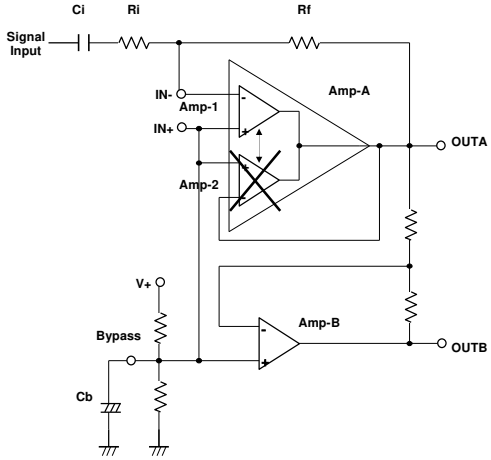


Fig. 4 During inverting amplifier operation

Pop noise is low in case that difference voltage between the +IN terminal and the –IN terminal is low (in other words, Ci has been charged) at the moment of switching from Amp-2 to Amp-1 (Fig.5). Increasing the value of Ci, input resistor (Ri) and feedback resistor (Rf) increases the time constant for charging Ci, so the potential difference between the –IN terminal and the +IN terminal will occur at the moment the internal amplifier switches (Fig.6). Since this potential difference is amplified and it outputs to the OUT terminal, the pop noise increases.

It is necessary that Ci decreases and bypass capacitor for reference voltage (Cb) increase for pop noise reduction. It is important to be careful to select the value of them because low frequency signal is cut in case that Ci decreases and turn on time is long in the case that Cb increases.

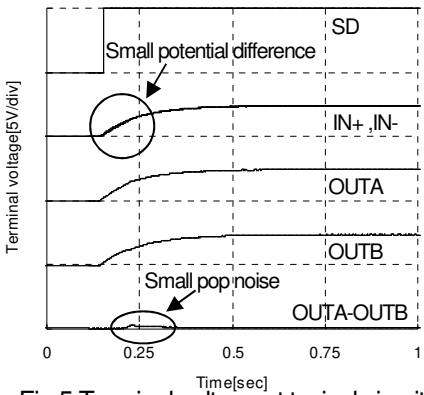


Fig.5 Terminal voltage at typical circuit

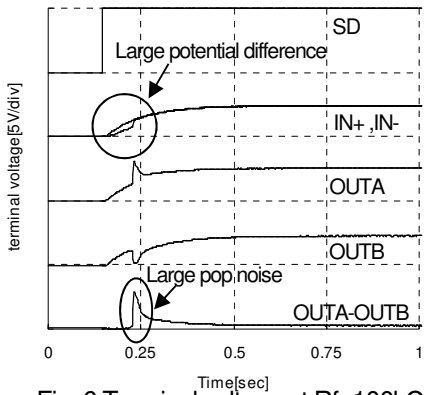


Fig. 6 Terminal voltage at Rf=100kΩ

Table 2 to 6 shows the value of Cb for equivalent pop noise of application circuit which sets default value.

Table 2. The value of Cb at Ri=10kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Ci	0.047μF	0.1μF	0.33μF	0.33μF	0.33μF	0.33μF
	0.1μF	0.33μF	0.33μF	1μF	1μF	1μF
	0.39μF	1μF	1μF	2μF	2μF	3.3μF
	0.47μF	1μF	2μF	2μF	3.3μF	3.3μF
	1μF	2μF	3.3μF	4.7μF	10μF	10μF

Table 3. The value of Cb at Ri=20kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Ci	0.047μF	0.1μF	0.33μF	0.33μF	0.33μF	0.33μF
	0.1μF	0.33μF	0.33μF	1μF	1μF	1μF
	0.39μF	1μF	1μF	2μF	2μF	3.3μF
	0.47μF	1μF	2μF	2μF	3.3μF	3.3μF
	1μF	2μF	3.3μF	4.7μF	10μF	10μF

Table 4. The value of Cb at Ri=30kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Ci	0.047μF	0.1μF	0.33μF	0.33μF	0.33μF	0.33μF
	0.1μF	0.33μF	0.33μF	1μF	1μF	1μF
	0.39μF	1μF	1μF	2μF	2μF	3.3μF
	0.47μF	1μF	2μF	2μF	3.3μF	3.3μF
	1μF	2μF	3.3μF	4.7μF	10μF	10μF

Table 5. The value of Cb at Ri=40kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Ci	0.047μF	0.1μF	0.33μF	0.33μF	0.33μF	0.33μF
	0.1μF	0.33μF	0.33μF	1μF	1μF	1μF
	0.39μF	1μF	1μF	2μF	2μF	3.3μF
	0.47μF	1μF	2μF	2μF	3.3μF	3.3μF
	1μF	2μF	3.3μF	4.7μF	10μF	10μF

Table 6. The value of Cb at Ri=50kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Ci	0.047μF	0.1μF	0.33μF	0.33μF	0.33μF	0.33μF
	0.1μF	0.33μF	0.33μF	1μF	1μF	1μF
	0.39μF	1μF	1μF	2μF	2μF	3.3μF
	0.47μF	1μF	2μF	2μF	3.3μF	3.3μF
	1μF	2μF	3.3μF	4.7μF	10μF	10μF

3.2 Turn off: Active (SD terminal=High) to Shutdown (SD terminal=Low)

The NJU72060's output stops steeply at turning to standby mode (Fig.7). Pop noise is low under the condition of using BTL amplifier because Amp-A and Amp-B of outputs are turned off simultaneously. And the reference voltage (the bypass terminal voltage) is turned off simultaneously too. Accordingly, pop noise is reduced in case that active mode and standby mode are continued to turn. It is necessary to be careful under the condition of using single-end amplifier because pop noise occurs.

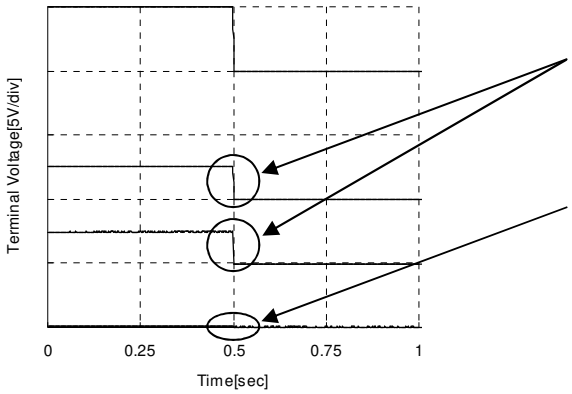


Fig.7 Terminal voltage at shutdown

Pop noise at shutdown is reduced by stopping the output stages of Amp-A and Amp-B at the same time. The output potential decreases by the time constant of the input capacitor (Ci) and the internal circuit.

Pop noise is low under the condition of using BTL amplifier because Amp-A and Amp-B outputs are turned off simultaneously.

4. Turn on time / turn off time

Pop noise and PSRR are improved in case that value of bypass capacitor for reference voltage (Cb) increases. But turn on time (shutdown to active time) is longer because Ci is charged. The NJU72060's output stops steeply at turning off (active to shutdown).

Fig.8 to 11 shows typical characteristics of turn on time vs the value of Cb. Turn on time is prescribe time of stabilized output signal after turning SD terminal from low to high.

There is variation in turn on time because there is variation of the bypass terminal resistor.

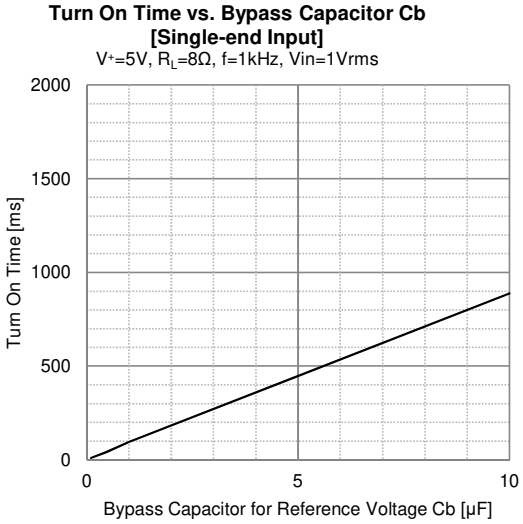


Fig. 8 Turn on time vs. Cb
(Single-end input, V^+=5V)

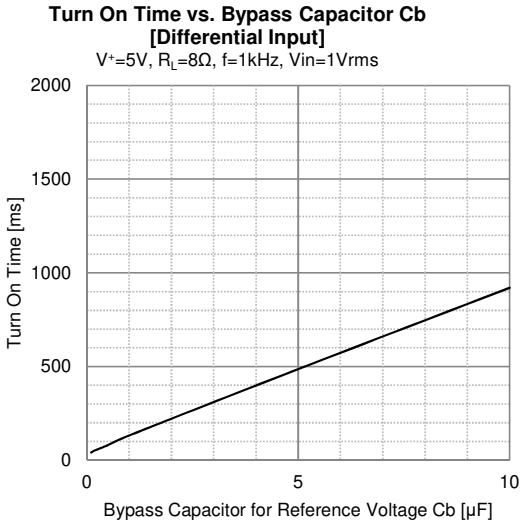


Fig. 9 Turn on time vs. Cb
(Differential input, V^+=5V)

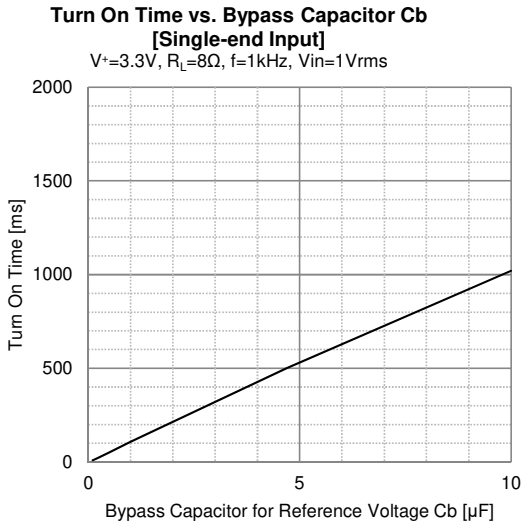


Fig. 10 Turn on time vs. Cb
(Single-end input, V^+=3.3V)

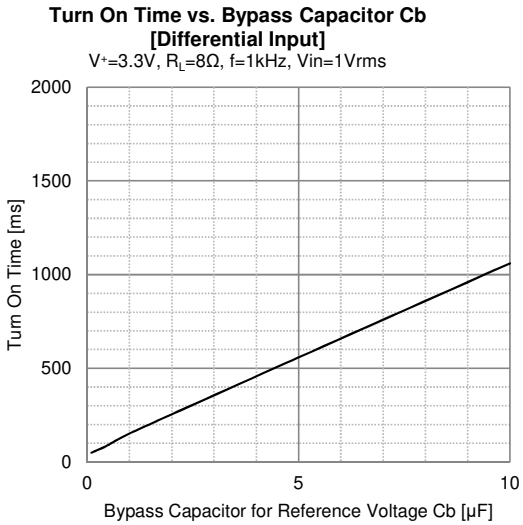


Fig. 11 Turn on time vs. Cb
(Differential input, V^+=3.3V)

5. PSRR vs Cb

PSRR is improved in case that value of bypass capacitor for reference voltage (Cb) increases. But the value of Cb causes pop noise and turn on time (standby to active time) too. It is important to consider when selects the value.

Fig. 12 to 15 shows typical characteristics of PSRR vs the value of Cb.

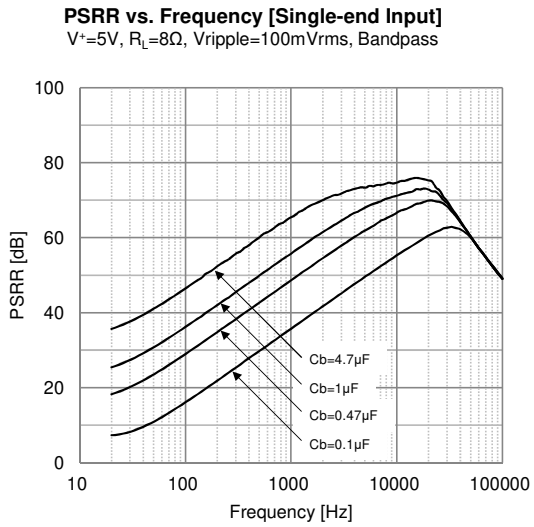


Fig. 12 PSRR vs. Cb
(Single-end input, V^+=5V)

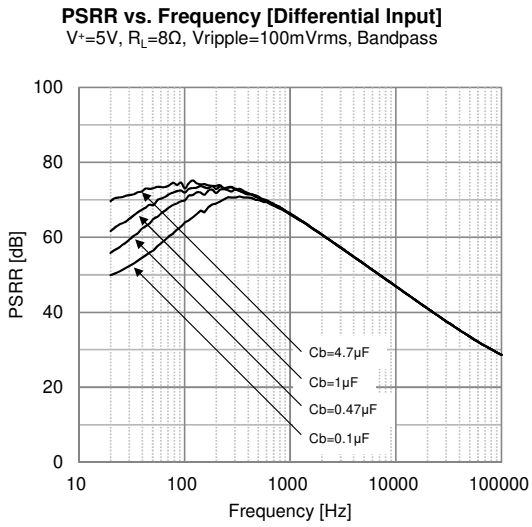


Fig. 13 PSRR vs. Cb
(Differential input, V^+=5V)

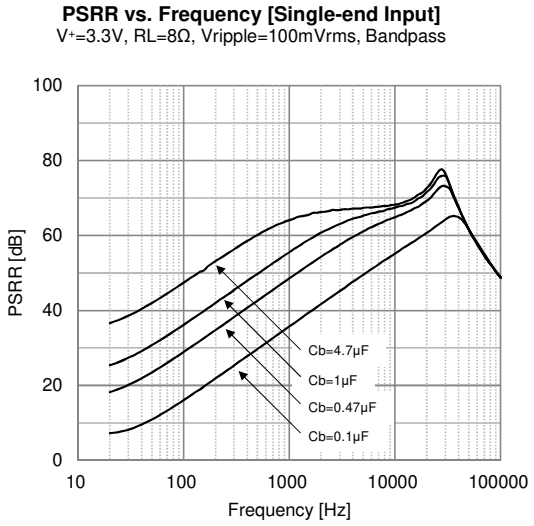


Fig. 14 PSRR vs. Cb
(Single-end input, V^+=3.3V)

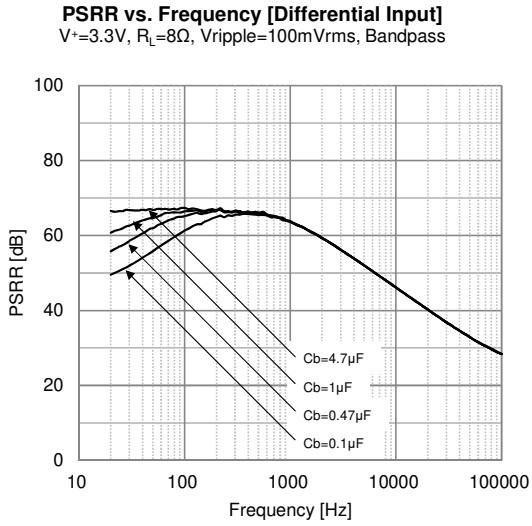


Fig. 15 PSRR vs. Cb
(Differential input, V^+=3.3V)

6. Auxiliary functions

The NJU72060 has the auxiliary functions which suppress breaking itself when the use of an unexpected condition occurs. These auxiliary functions are not guarantee as they operate over absolute maximum ratings. It is essential to design as the auxiliary functions do not operate. Do not design when use the auxiliary functions.

6.1 Thermal shutdown circuit

The NJU72060 operates the thermal shutdown circuit when the junction temperature is abnormally high temperature. So the OUTA terminal and the OUTB terminal become high impedance. The NJU72060's operation returns by itself in case that the junction temperature is normally.

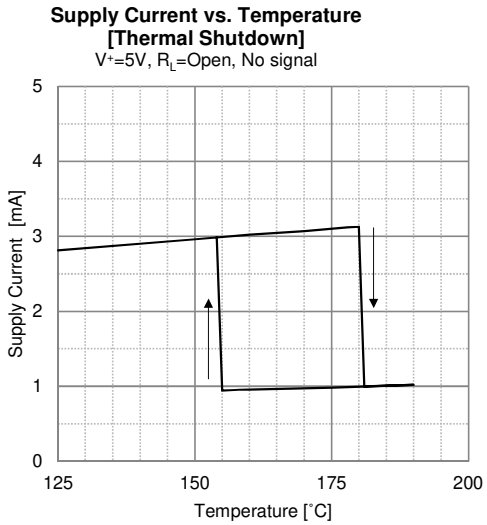


Fig. 16 Thermal Shutdown (V^+=5V)

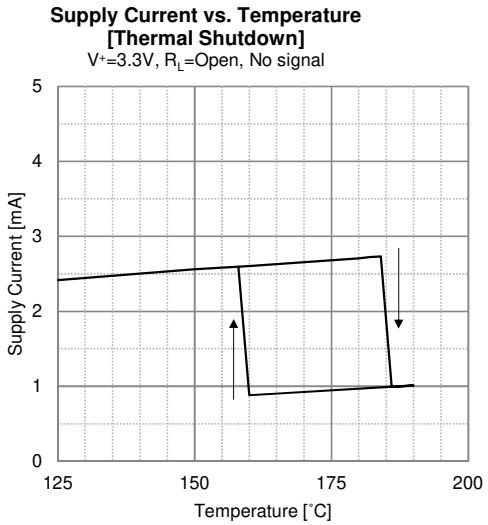


Fig. 17 Thermal Shutdown (V^+=3.3V)

6.2 Current Limit Circuit

The NJU72060 operates the current limit circuit when the current of over absolute maximum ratings flows through the OUTA terminal and the OUTB terminal. So it limits output current to below a constant value. It stops when the output current decreases.

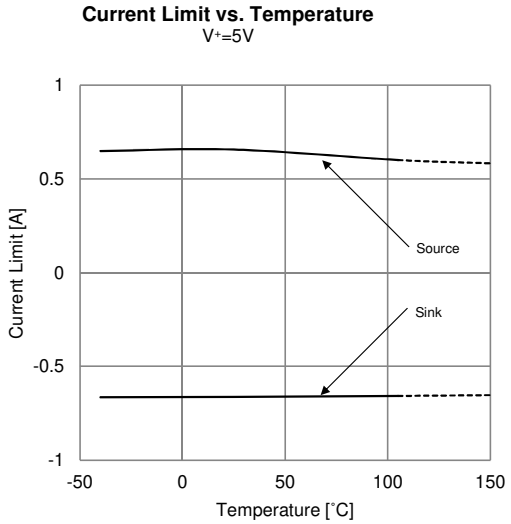


Fig. 18 Current Limit vs. Temperature (V^+=5V)

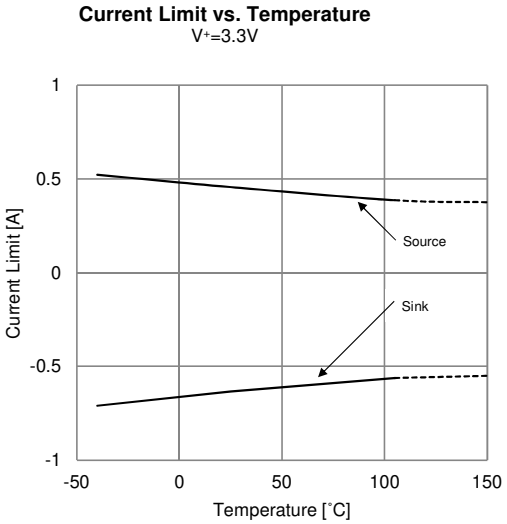


Fig. 19 Current Limit vs. Temperature (V^+=3.3V)

7. Output power

7.1 Output Current and output power

It is important to consider that the NJU72060 define output current in absolute maximum rating. For example, maximum output power (Po_max) is set by the following under the condition that output current ($Io_{(rms)}$[Arms], Io[A]), load resistance (R_L) is 8Ω, Output signal is sine wave

$$P_{O\_\max} < I_{O(rms)}{}^{\wedge 2} \cdot R_L = \left(\frac{I_O}{\sqrt{2}}\right)^2 \cdot R_L = \left(\frac{0.4}{\sqrt{2}}\right)^2 \cdot 8 = 0.64\,[W]$$

7.2 Power dissipation and output power

IC is heated by own operation and it breaks when the junction temperature (Tj) exceeds the permissible value. The permissible value is power dissipation P_D and it is necessary to use no exceeding it.

Fig. 20 shows power dissipation (P_D) vs ambient temperature (Ta). The plots depends on following two points. The first point is P_D at Ta=25˚C which is power dissipation of the absolute maximum ratings. Power dissipation on Ta<25˚C is same value. The second point is 0W which means that the IC cannot permit heating. This point is gotten by maximum junction temperature Tjmax which is maximum storage temperature of this IC. Fig. 20 is drawn by connecting those points and the definition which P_D lower than 25˚C is constant. P_D on Ta≥25˚C is set by the following.

$$P_D = \frac{Tj\max - Ta}{\theta ja}\,[W] \quad (Ta \geq 25°C)$$

Θja is thermal resistance between Tj and Ta and it depends on package material (resin, frame and so on).

Power dissipation (P) of own operating is gotten by the following.

$$\begin{aligned} Power\ Dissipation\ P &= (Supply\ Voltage\ V^+) \cdot (Supply\ Current\ for\ V^+\ terminal\ I_{ALL}) \\ &\quad - (Output\ Power\ P_O) \\ &= (Supply\ Voltage\ V^+) \cdot (Supply\ Current\ for\ the\ NJU72065\ I_{DD} \\ &\quad + Supply\ Current\ for\ Load\ Resistance\ I_{R_L}) - (Output\ Power\ P_O) \end{aligned}$$

The NJU72060 should be operated under the condition that this power dissipation (P) is lower than power dissipation (P_D). It is recommended to consider under the condition and have an enough margin for stabilized operation.

In the designing, power dissipation (P) should be verified in the using but temporary value is read by Power Dissipation vs Output Power on the datasheet's typical characteristics. Fig.21 shows typical characteristics under the conditions that Ta=25˚C, V^+=5V, Gv=+6dB and R_L=8Ω BTL. The following are examples.

Ex. 1 How to get maximum ambient temperature Ta
in the case of request which is maximum output power Po.

The NJU72060R is maximum junction temperature Tjmax=150˚C and MSOP8 (TVSP8) package's power dissipation P_D=680mW (4layer). Thermal resistance (θja) is gotten by the equation of power dissipation (P_D).

$$\theta ja = \frac{Tj\max - Ta}{P_D} = \frac{150 - 25}{0.68} = 183.8\,[°C/W]$$

Maximum ambient temperature Ta is set by the following under the conditions that V^+=5V, R_L=8Ω BTL and maximum output power Po=0.5W because maximum power dissipation (P) is approximately 0.65W by Fig. 21.

$$Ta = Tj\max - P_D \cdot \theta ja = 150 - 0.65 \cdot 183.8 = 30.5\,[°C]$$

Ex. 2 How to get maximum output power Po
in the case of request which is ambient temperature Ta.

Power dissipation (P_D) is gotten by the following under the conditions that Ta=60˚C and θja=183.8˚C/W which is set by Ex. 1.

$$P_D = \frac{Tj\max - Ta}{\theta ja} = \frac{150 - 60}{183.8} = 0.49\,[W]$$

Maximum output power (Po) is gotten approximately 0.15W by Fig. 21 under the conditions that V^+=5V, R_L=8Ω BTL, P_D=0.49W and Ta=60˚C.

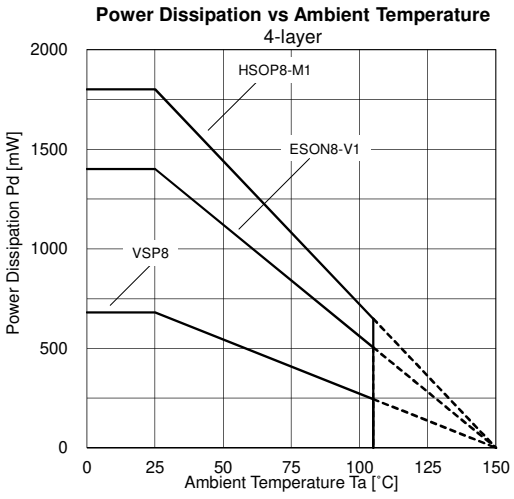


Fig. 20 Power Dissipation vs. Ambient Temperature

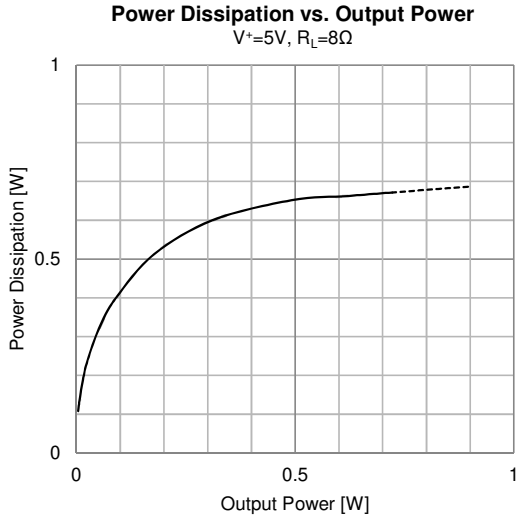


Fig. 21 Power Dissipation vs. Output Power

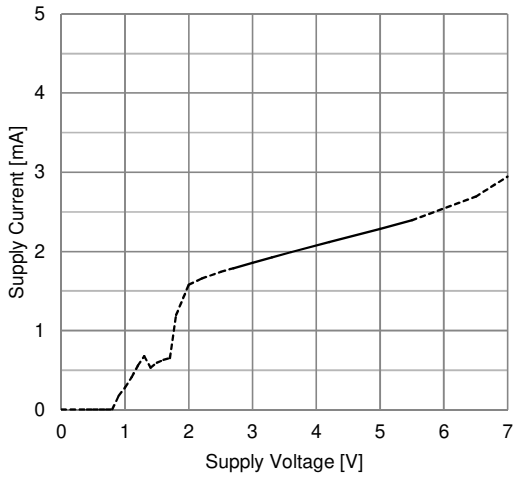
8. PCB layout

It is necessary to design a PCB appropriately in order to demonstrate the performance of IC. Power line, GND line and signal output line should be drawn wiring as low wiring resistance as possible. And all of the GND should be connect directly to the single point of power source bypass capacitor's GND

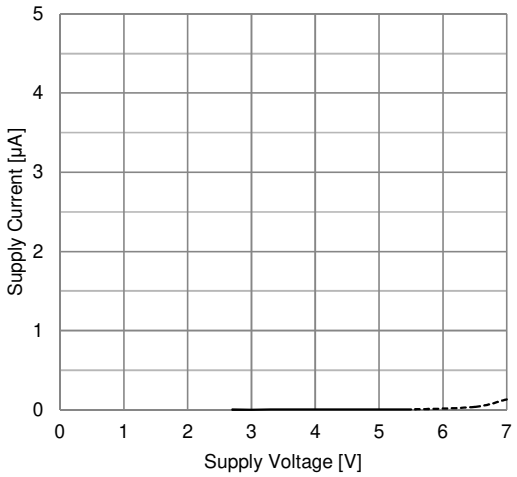
There is possibility that PSRR is low in case of 4 layer and over when the power plane is piled the wiring layer. It is recommended that the GND plane is inserted between the wiring layer and power plane.

■TYPICAL CHARACTERISTICS

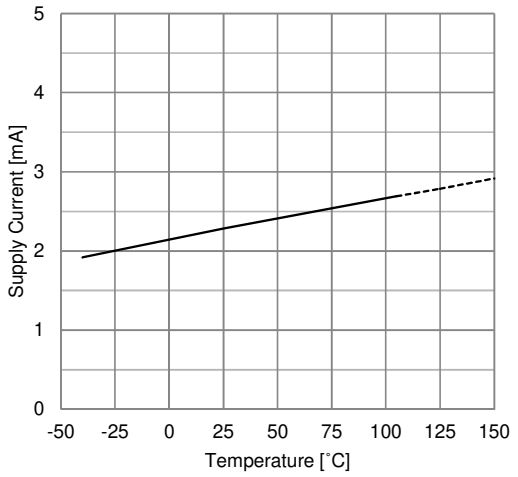
Supply Current vs. Supply Voltage
R_L=Open, No signal



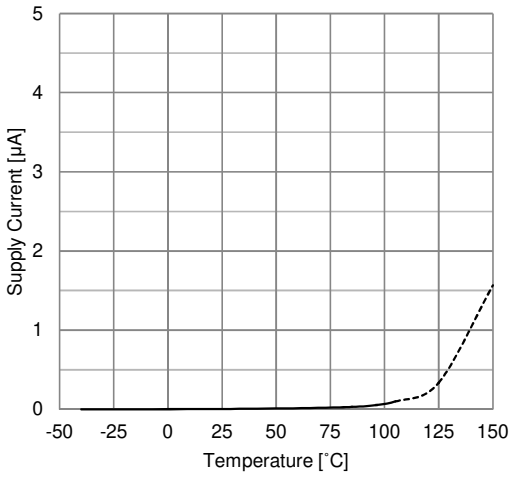
Supply Current vs. Supply Voltage [Shutdown]
R_L=Open, No signal



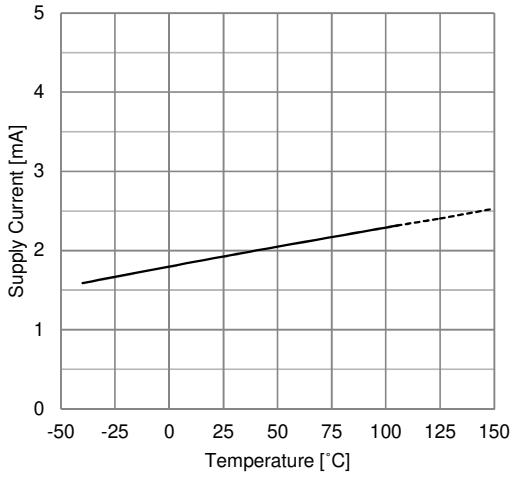
Supply Current vs. Temperature
V^+=+5V, R_L=Open, No signal



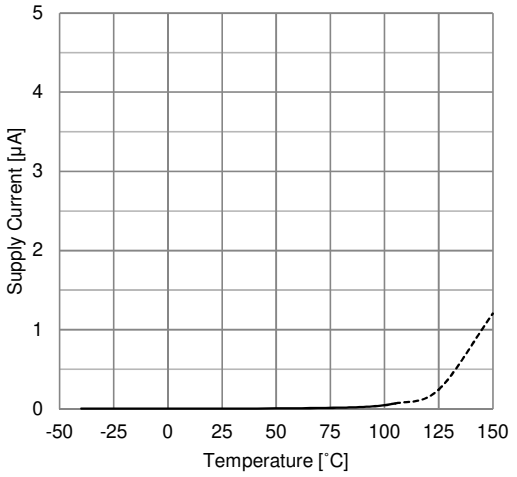
Supply Current vs. Temperature [Shutdown]
V^+=+5V, R_L=Open, No signal



Supply Current vs. Temperature
V^+=+3.3V, R_L=Open, No signal

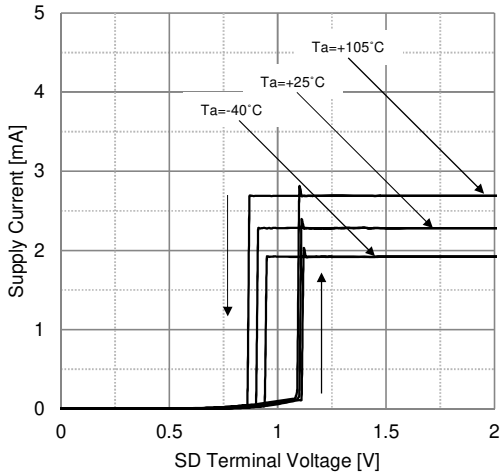


Supply Current vs. Temperature [Shutdown]
V^+=+3.3V, R_L=Open, No signal

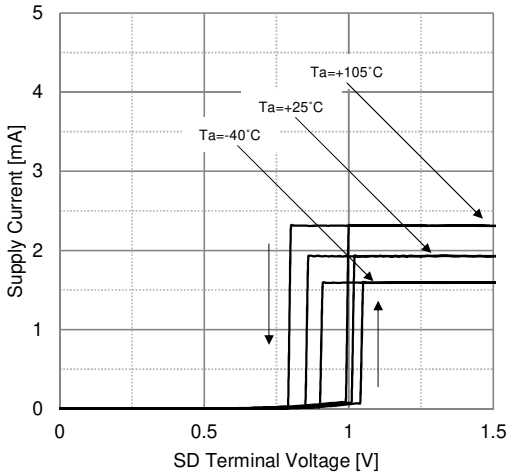


■TYPICAL CHARACTERISTICS

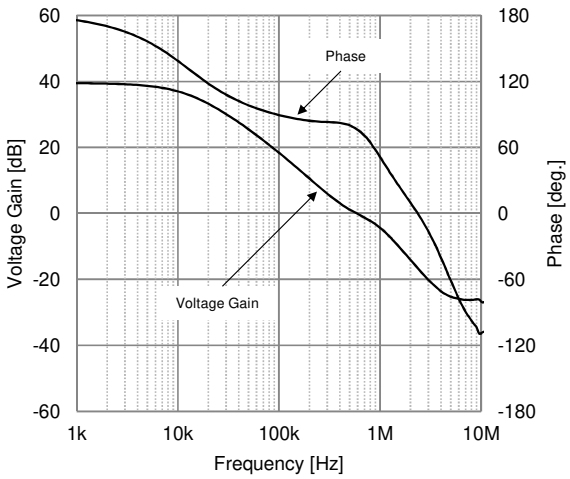
Supply Current vs. SD Terminal Voltage
V^+=+5V, R_L=Open, No signal



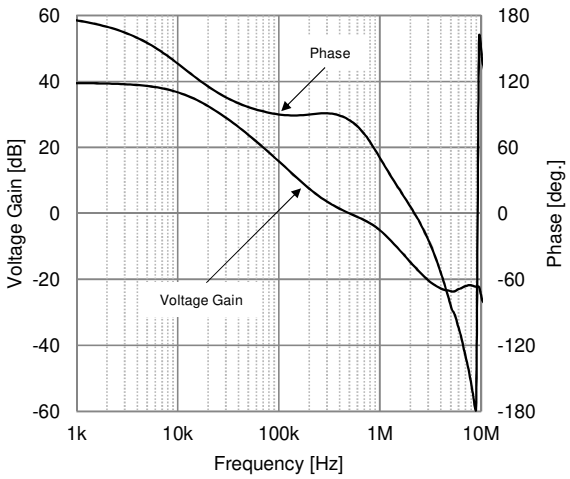
Supply Current vs. SD Terminal Voltage
V^+=+3.3V, R_L=Open, No signal



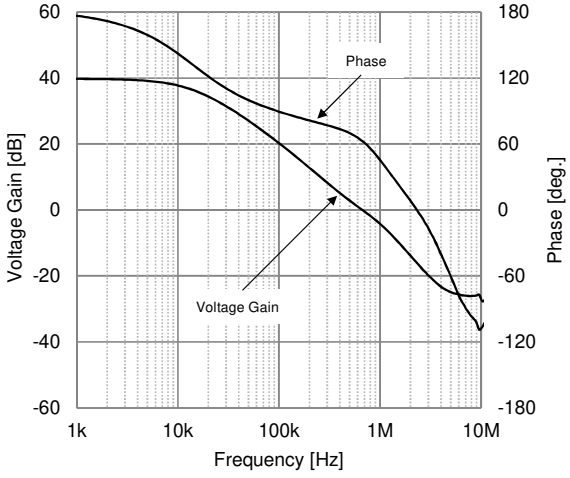
Voltage Gain / Phase vs. Frequency
V^+=+5V, R_L=8Ω, Gv=40dB



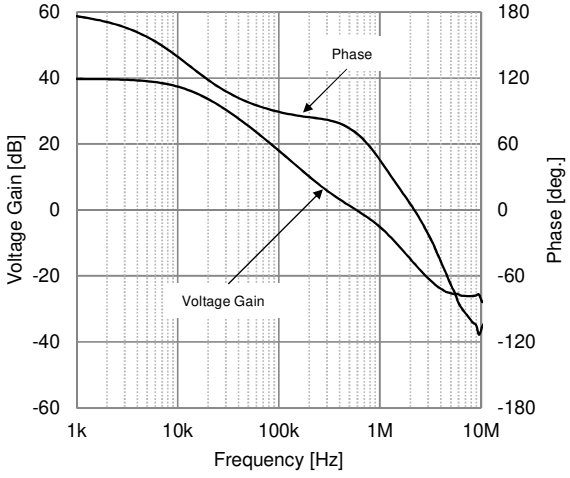
Voltage Gain / Phase vs. Frequency
V^+=+3.3V, R_L=8Ω, Gv=40dB



Voltage Gain / Phase vs. Frequency
V^+=5V, R_L=16Ω, Gv=40dB

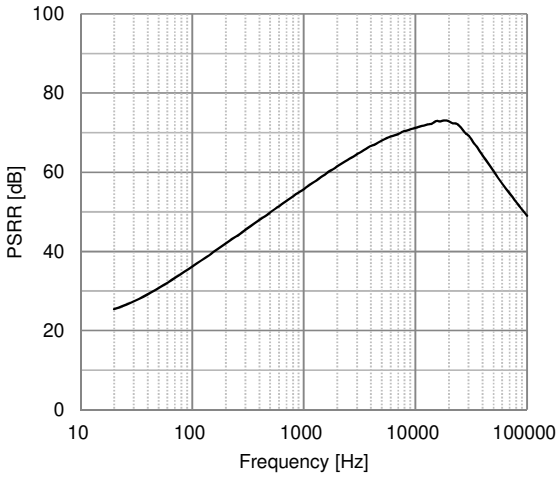


Voltage Gain / Phase vs. Frequency
V^+=3.3V, R_L=16Ω, Gv=40dB

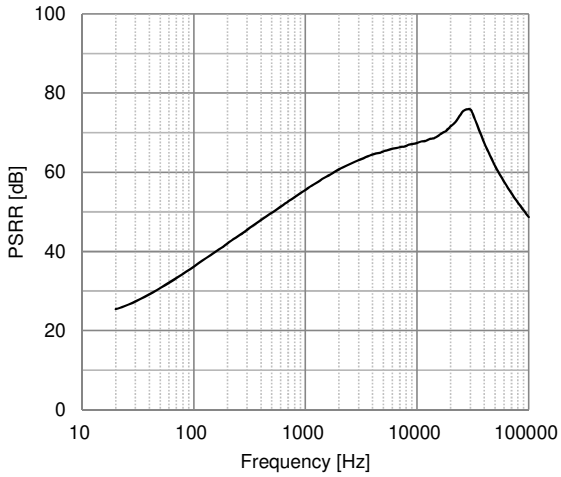


■TYPICAL CHARACTERISTICS

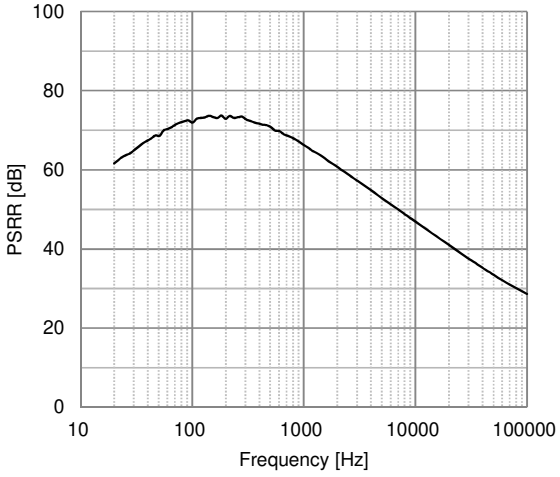
PSRR vs. Frequency [Single-end Input]
V^+=5V, R_L=8Ω, Vripple=100mVrms, Bandpass



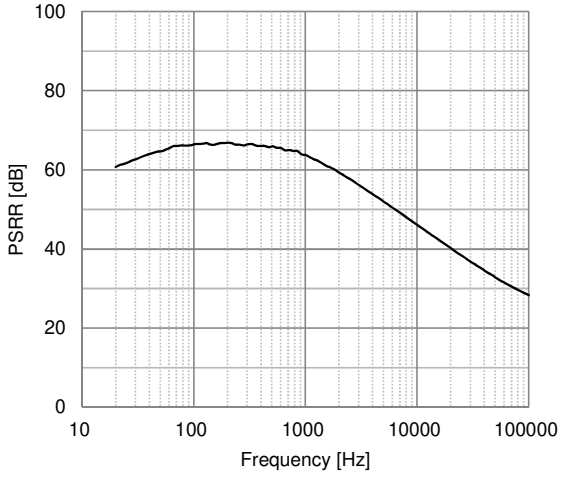
PSRR vs. Frequency [Single-end Input]
V^+=3.3V, RL=8Ω, Vripple=100mVrms, Bandpass



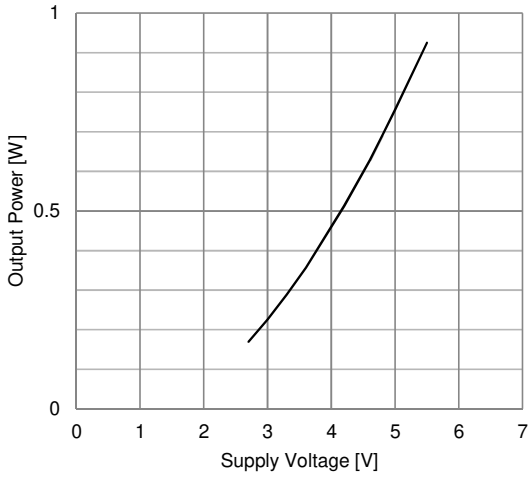
PSRR vs. Frequency [Differential Input]
V^+=5V, R_L=8Ω, Vripple=100mVrms, Bandpass



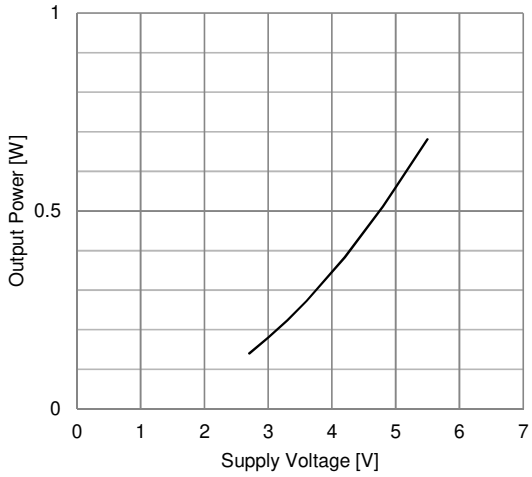
PSRR vs. Frequency [Differential Input]
V^+=3.3V, R_L=8Ω, Vripple=100mVrms, Bandpass



Output Power vs. Supply Voltage
R_L=8Ω, THD=1%

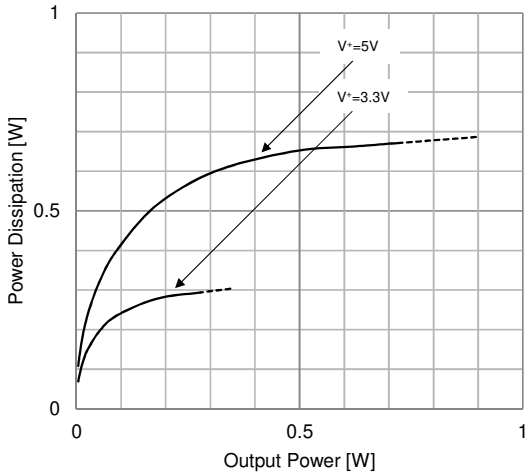


Output Power vs. Supply Voltage
R_L=16Ω, THD=1%

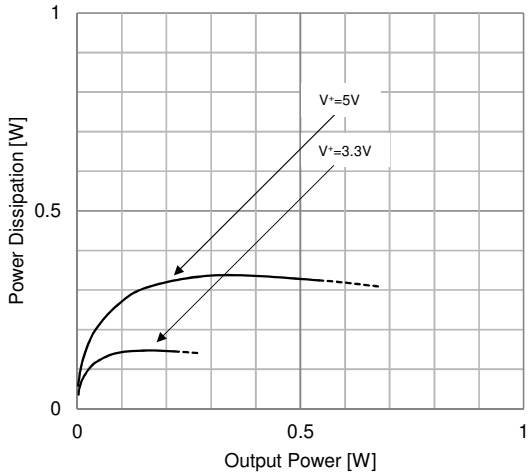


■TYPICAL CHARACTERISTICS

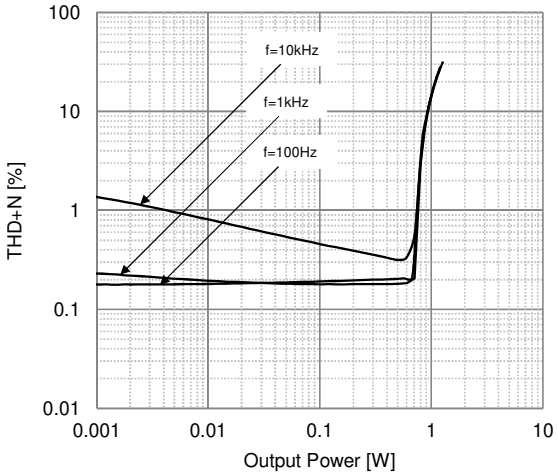
Power Dissipation vs. Output Power
R_L=8Ω



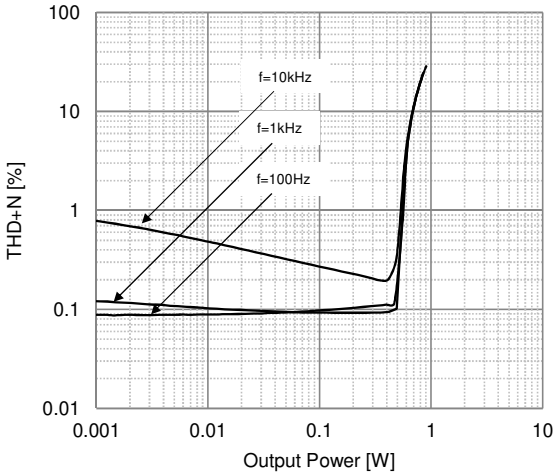
Power Dissipation vs. Output Power
R_L=16Ω



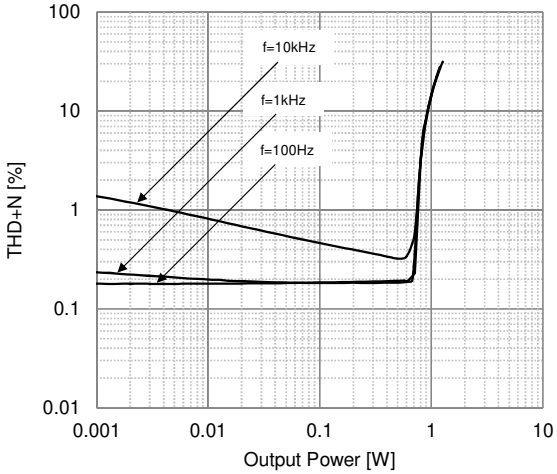
THD+N vs. Output Power [Single-end Input]
V^+=5V, R_L=8Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)



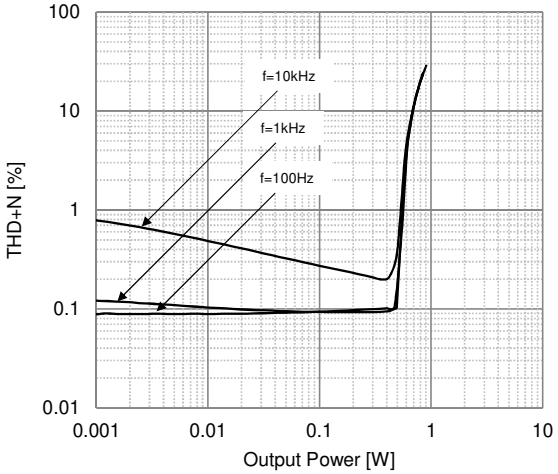
THD+N vs. Output Power [Single-end Input]
V^+=5V, R_L=16Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)



THD+N vs. Output Power [Differential Input]
V^+=5V, R_L=8Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)

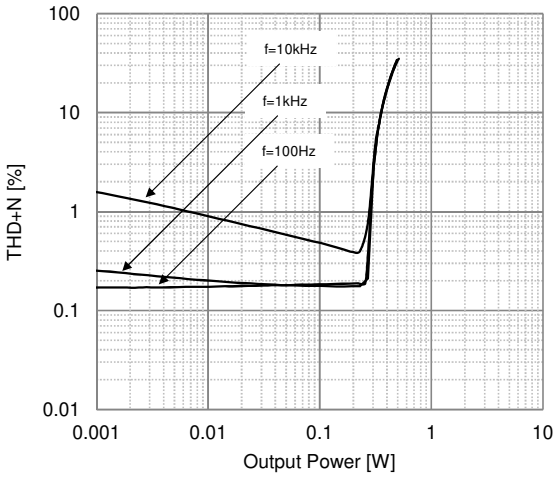


THD+N vs. Output Power [Differential Input]
V^+=5V, R_L=16Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)

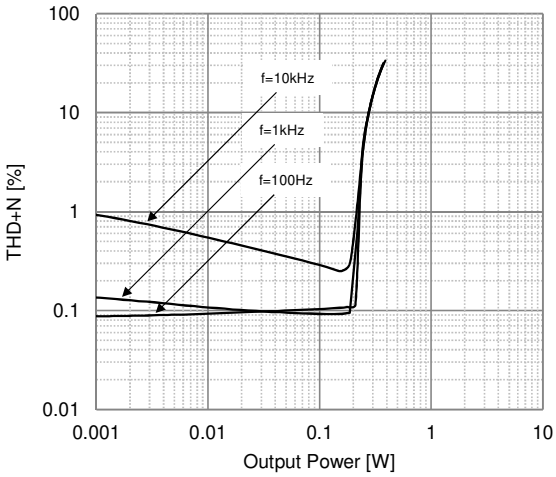


■TYPICAL CHARACTERISTICS

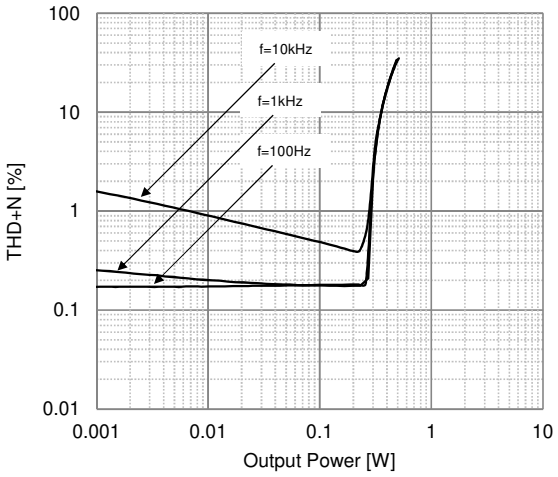
THD+N vs. Output Power [Single-end Input]
V^+=3.3V, R_L=8Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)



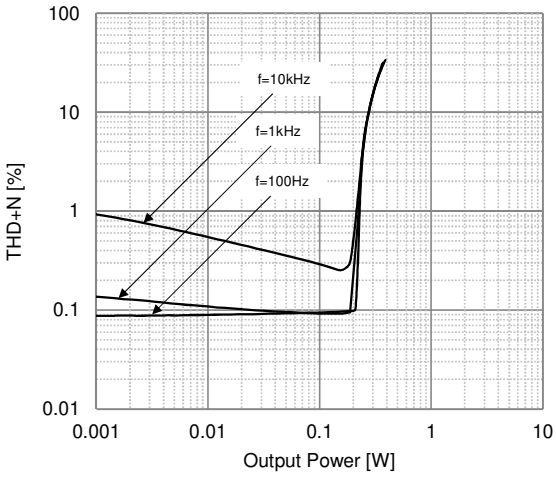
THD+N vs. Output Power [Single-end Input]
V^+=3.3V, R_L=16Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)



THD+N vs. Output Power [Differential Input]
V^+=3.3V, R_L=8Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)



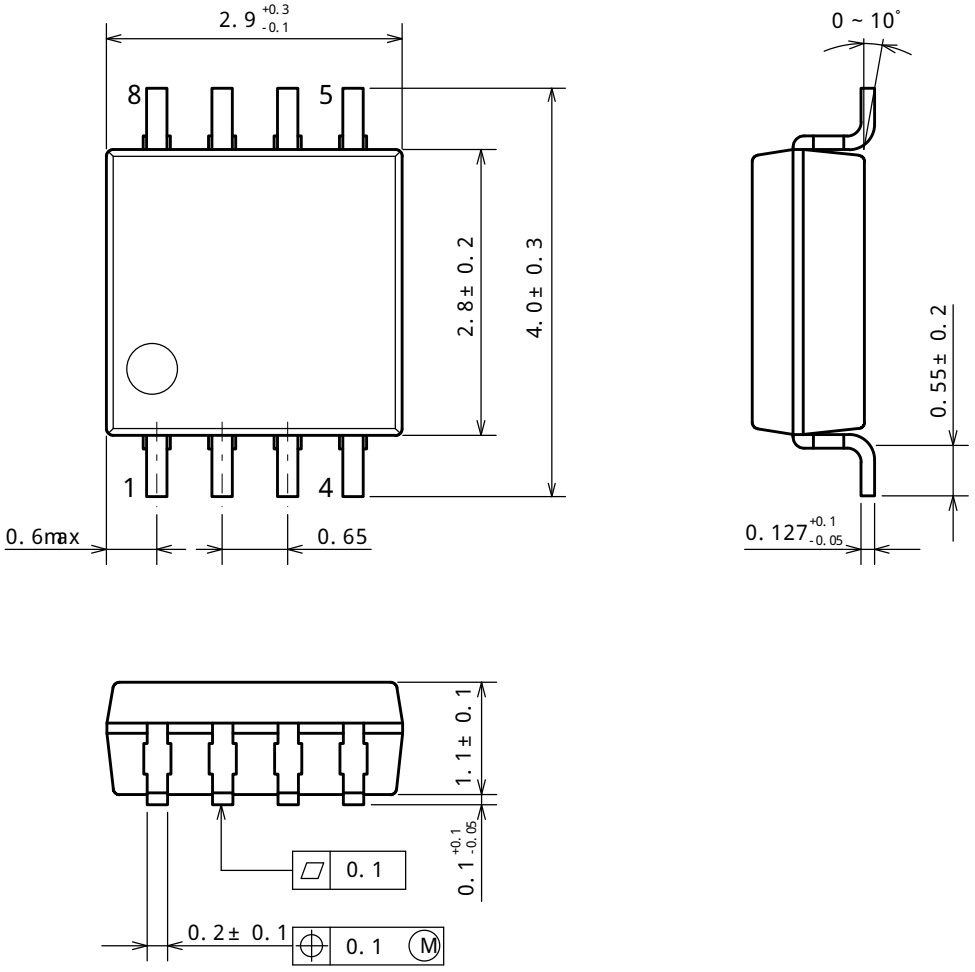
THD+N vs. Output Power [Differential Input]
V^+=3.3V, R_L=16Ω
BW: 22-22kHz(f=100Hz, 1kHz), 22-80kHz(f=10kHz)



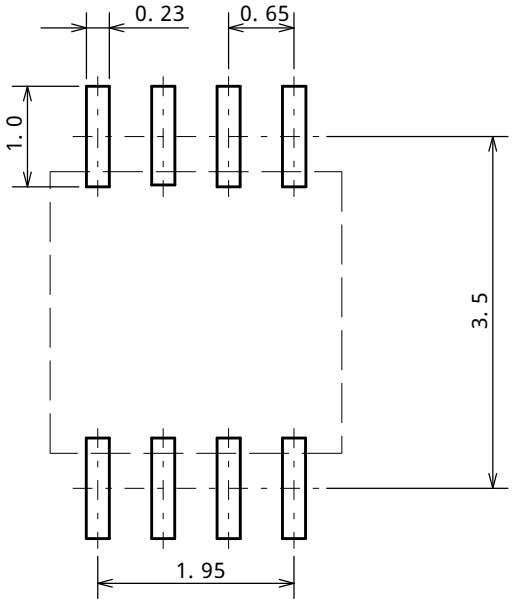
MSOP8 JEDEC MO-187-DA

Unit: mm

■ PACKAGE DIMENSIONS



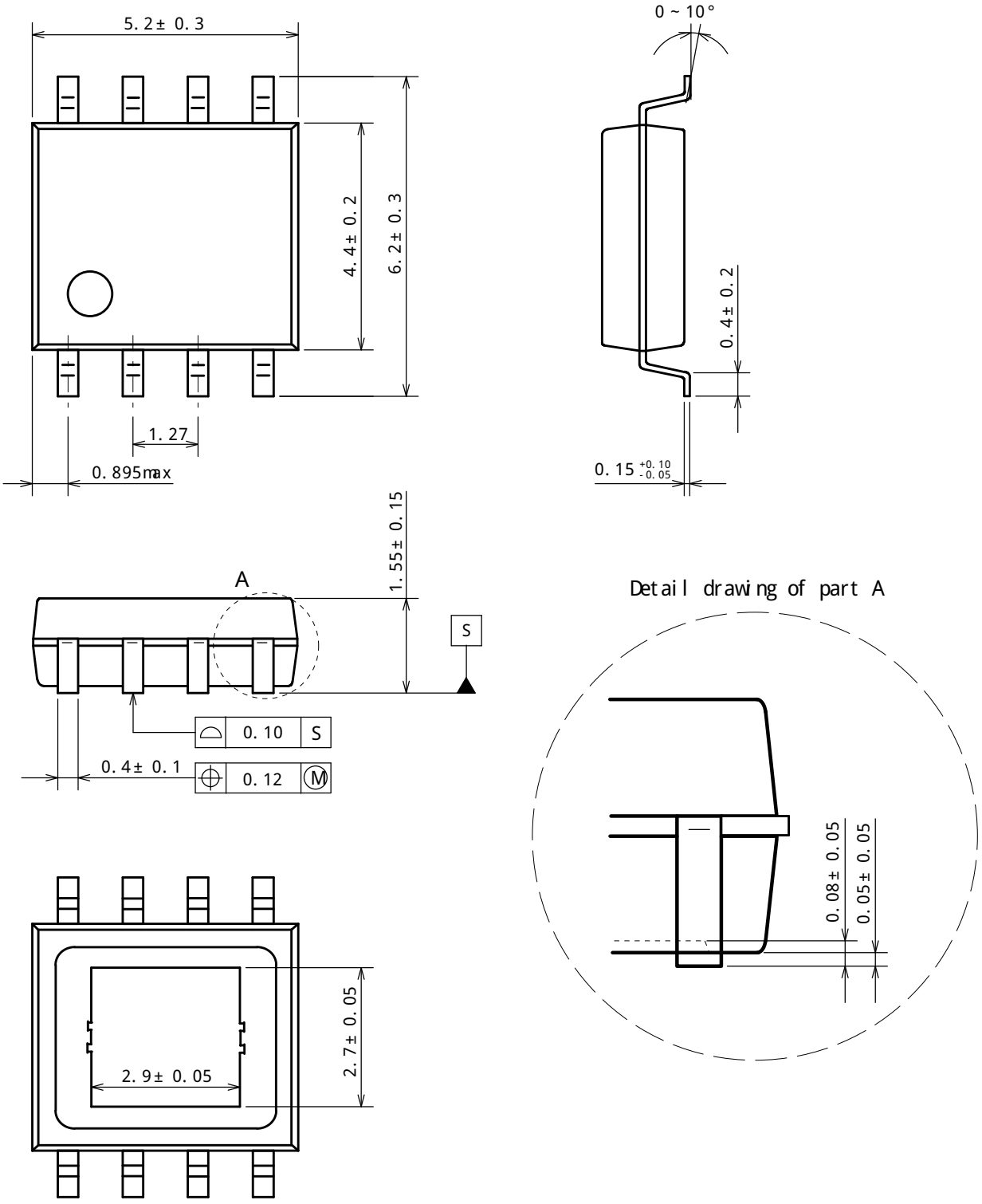
■ EXAMPLE OF SOLDER PADS DIMENSIONS



HSOP8-M1

Unit: mm

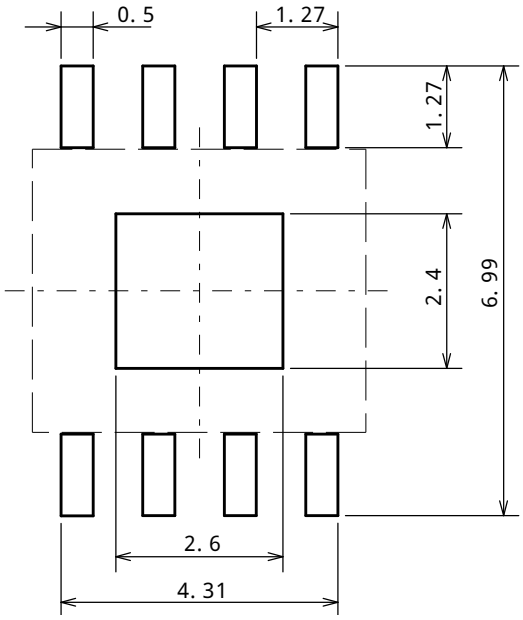
■PACKAGE DIMENSIONS



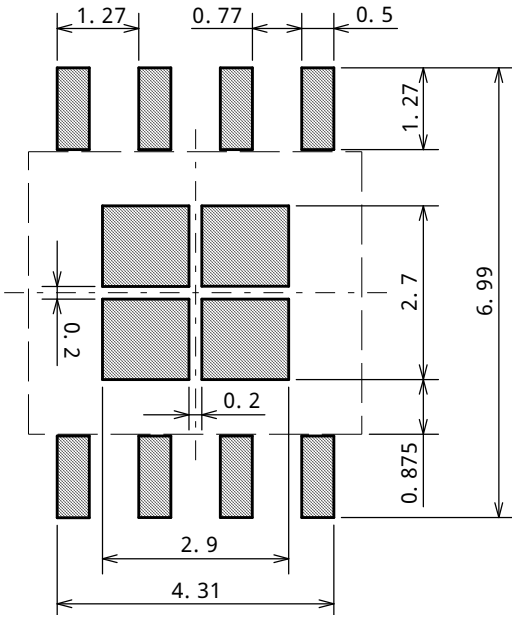
HSOP8-M1

Unit: mm

■EXAMPLE OF SOLDER PADS DIMENSIONS



<Solder pattern>



<Metal mask>

<Instructions for mounting>

Please note the following points when you mount HSOP-8 package IC because there is a standoff on the backside electrode.

(1) Temperature profile of lead and backside electrode.

It is necessary that both re-flow temperature profile of lead and backside electrode are higher than preset temperature.

When solder wet temperature is lower than lead/backside electrode temperature, there is possibility of defect mounting.

(2) Design of foot pattern / metal mask

Metal mask thickness of solder pattern print is more than 0.13mm.

(3) Solder paste

The mounting was evaluated with following solder paste, foot pattern and metal mask.

Because mounting might be greatly different according to the manufacturer and the product number even if the solder composition is the same.

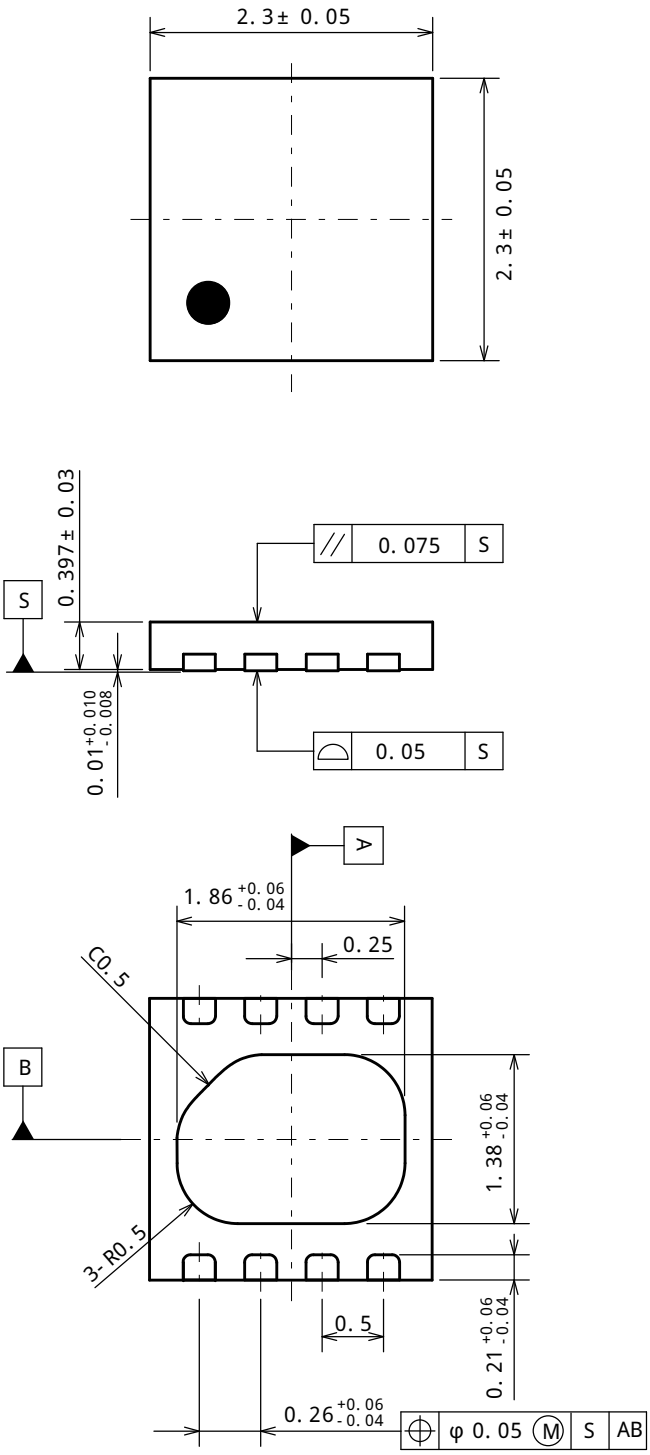
We will strongly recommend to evaluate mounting previously with using foot pattern, metal mask and solder paste.

Solder paste composition	Sn37Pb (Senju Metal Industry Co., Ltd :OZ7053-340F-C)
	Sn3Ag0.5Cu (Senju Metal Industry Co., Ltd :M705-GRN350-32-11)

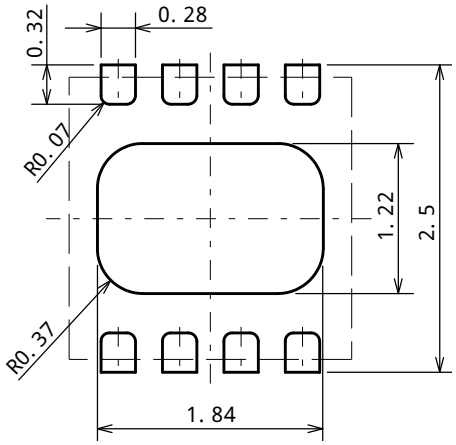
DFN8-V1

Unit: mm

■PACKAGE DIMENSIONS



■EXAMPLE OF SOLDER PADS DIMENSIONS

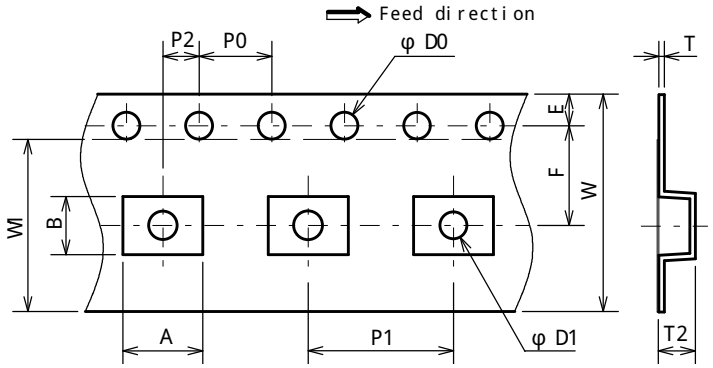


MSOP8 MEET JEDEC MO-187-DA

Unit: mm

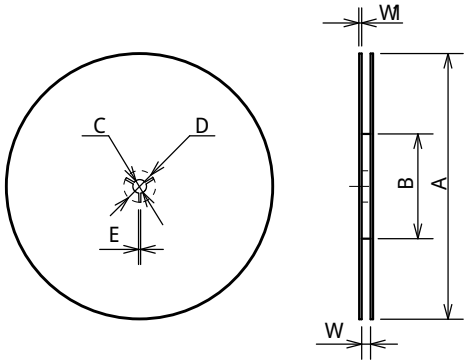
■PACKING SPEC

TAPING DIMENSIONS



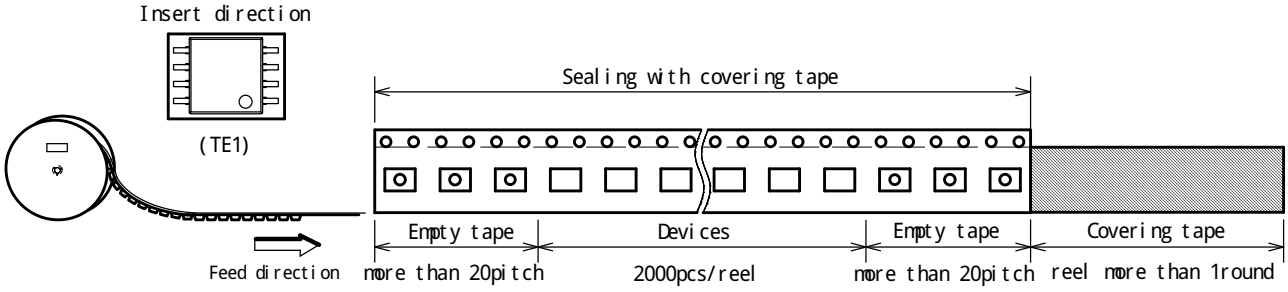
SYMBOL	DIMENSION	REMARKS
A	4.4	BOTTOM DIMENSION
B	3.2	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	$1.5^{+0.1}_{0}$	
E	1.75± 0.1	
F	5.5± 0.05	
P0	4.0± 0.1	
P1	8.0± 0.1	
P2	2.0± 0.05	
T	0.30± 0.05	
T2	2.0 (MAX.)	
W	12.0± 0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

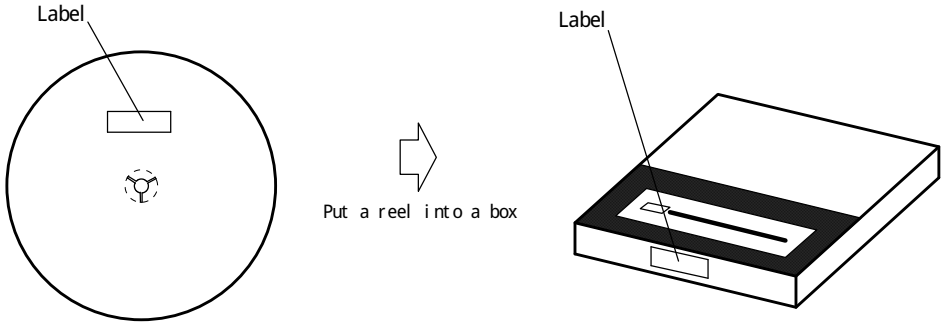


SYMBOL	DIMENSION
A	φ 254± 2
B	φ 100± 1
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	13.5± 0.5
W1	2.0± 0.2

TAPING STATE



PACKING STATE

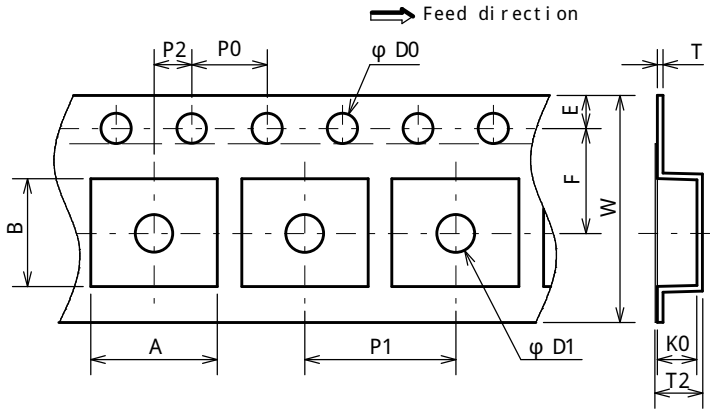


HSOP8-M1

■PACKING SPEC

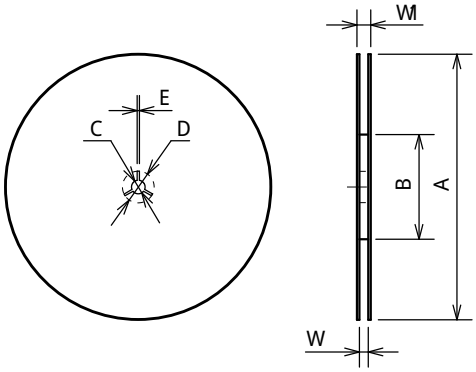
Unit: mm

TAPING DIMENSIONS



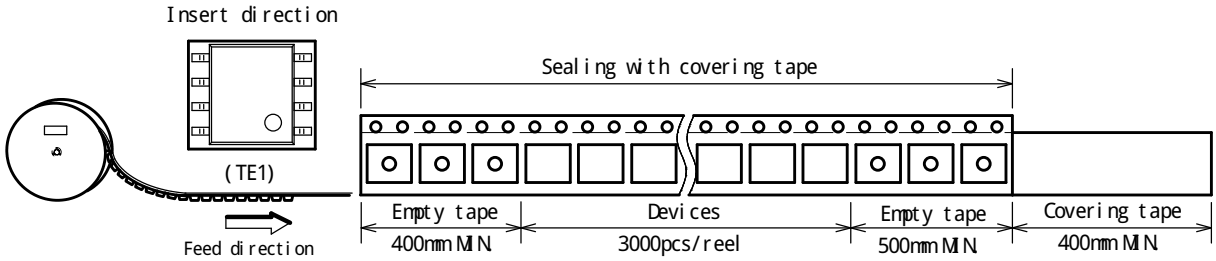
SYMBOL	DIMENSION	REMARKS
A	6.7± 0.1	
B	5.55± 0.1	
D0	1.55± 0.05	
D1	2.05± 0.05	
E	1.75± 0.1	
F	5.5± 0.05	
P0	4.0± 0.1	
P1	8.0± 0.1	
P2	2.0± 0.05	
T	0.3± 0.05	
T2	2.47	
K0	2.1± 0.1	
W	12.0± 0.2	

REEL DIMENSIONS

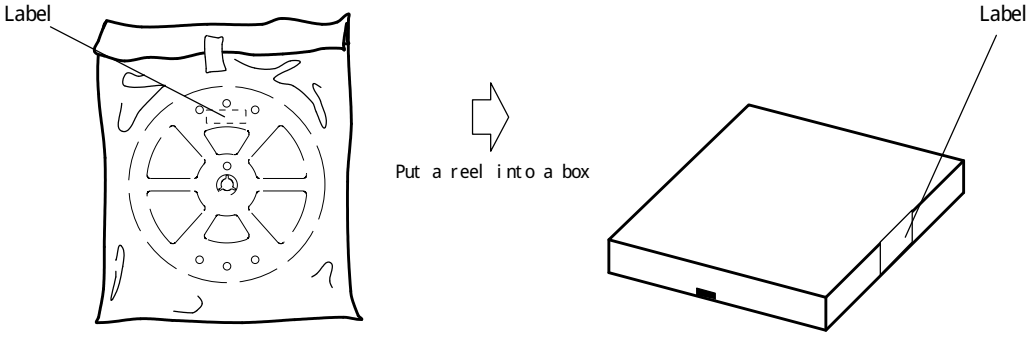


SYMBOL	DIMENSION
A	φ 330± 2
B	φ 80± 1
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	13.5± 0.5
W1	17.5± 1

TAPING STATE



PACKING STATE

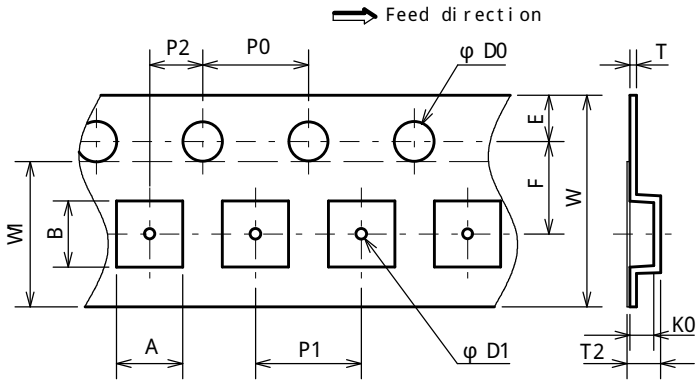


DFN8-V1

Unit: mm

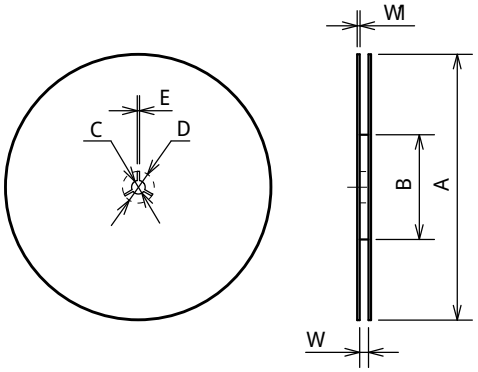
■PACKING SPEC

TAPING DIMENSIONS



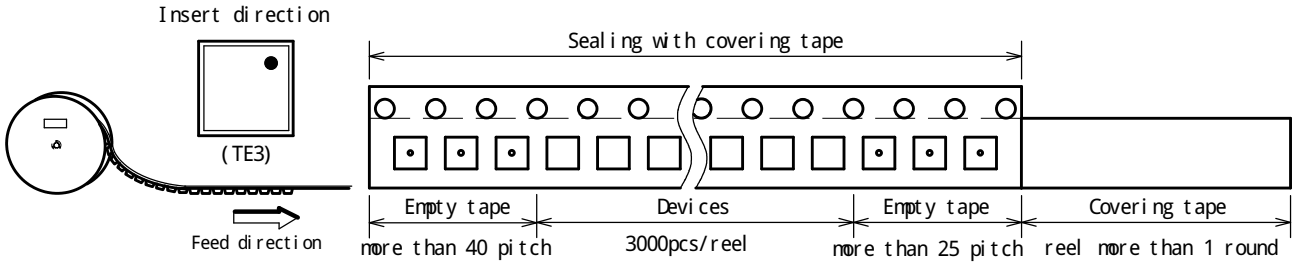
SYMBOL	DIMENSION	REMARKS
A	2.55± 0.05	BOTTOM DIMENSION
B	2.55± 0.05	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	0.5± 0.1	
E	1.75± 0.1	
F	3.5± 0.05	
P0	4.0± 0.1	
P1	4.0± 0.1	
P2	2.0± 0.05	
T	0.25± 0.05	
T2	1.00± 0.07	
K0	0.65± 0.05	
W	8.0± 0.2	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS

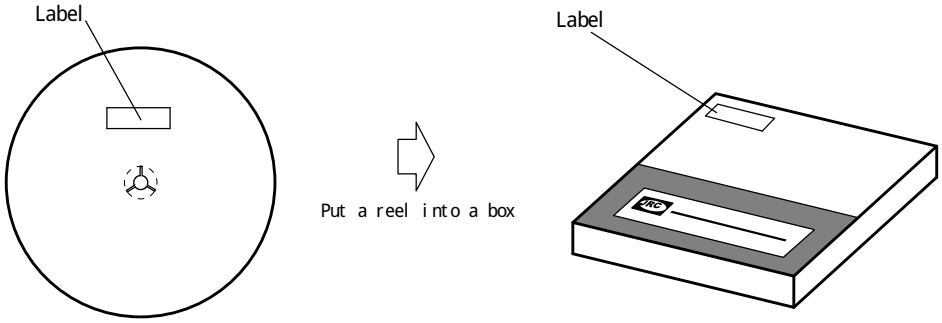


SYMBOL	DIMENSION
A	$\varphi 180^{0}_{-1.5}$
B	$\varphi 60^{+1}_{0}$
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	$9^{+0.3}_{0}$
W1	1.2

TAPING STATE



PACKING STATE

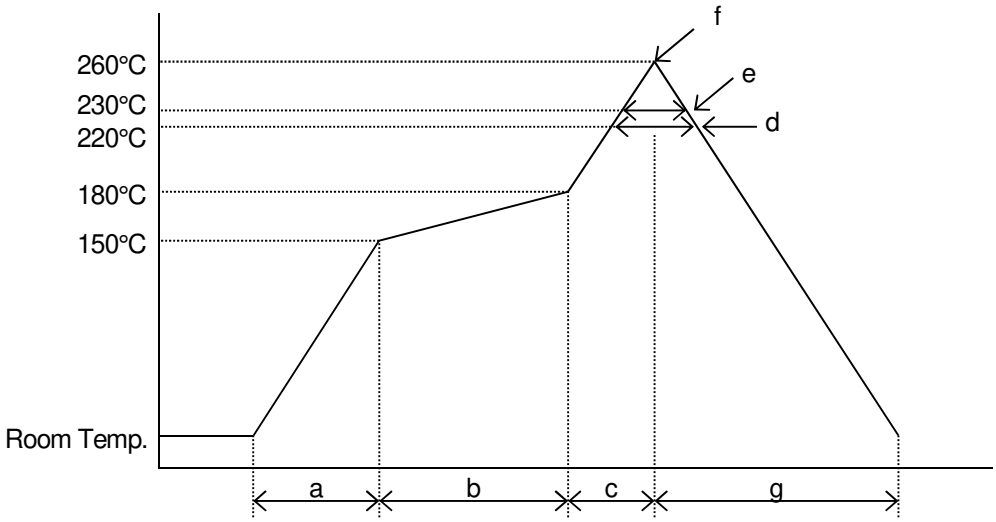


■RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING METHOD

EAE-D1006-000-02

*Recommended reflow soldering procedure



a :Temperature ramping rate	: 1 to 4°C/s
b :Pre-heating temperature	: 150 to 180°C
time	: 60 to 120s
c :Temperature ramp rate	: 1 to 4°C/s
d :220°C or higher time	: Shorter than 60s
e :230°C or higher time	: Shorter than 40s
f :Peak temperature	: Lower than 260°C
g :Temperature ramping rate	: 1 to 6°C/s

The temperature indicates at the surface of mold package.

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   Power Generator Control Equipment (Nuclear, Steam, Hydraulic)
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   Fire Alarm/Intruder Detector
   Vehicle Control Equipment (airplane, railroad, ship, etc.)
   Various Safety devices

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