ADS848xEVM

This user's guide describes the characteristics, operation, and use of the ADS8482 18-bit, 1-MHz, parallel interface and ADS8484 18-bit, 1.25-MHz, parallel interface, analog-to-digital converter (ADC) evaluation module (EVM). A complete circuit description, schematic diagram, and bill of materials are included. Throughout this document, the term *evaluation module* and the abbreviation *EVM* are synonymous with the ADS848xEVM. For ease of reading, this user's guide refers to the ADS8482EVM or ADS8484EVM as the *ADS848xEVM*. Operation of the EVM for both devices is identical, unless otherwise noted.

Contents

List of Figures

List of Tables

1 EVM Overview

1.1 Features

- Full-featured evaluation board for the high-speed, 18-bit ADS8482 and ADS8484 1-MSPS/1.25-MSPS, single-channel, parallel interface, SAR-type analog-to-digital converters
- Onboard signal conditioning
- Onboard reference
- Input and output digital buffers
- Onboard decoding for stacking multiple EVMs

2 Introduction

The ADS8482 is an 18-bit, 1-MSPS analog-to-digital converter (ADC) with an internal 4.096-V reference and a pseudo-bipolar, fully differential input. The ADS8484 is an 18-bit, 1.25-MSPS version of the same core design. These devices are capacitor-based, successive approximation register (SAR) converters with an inherent sample-and-hold stage. The ADS848x has 8-bit, 16-bit, and 18-bit parallel interface bus options, allowing a variety of processors to interface easily.

The ADS848xEVM is an evaluation and demonstration platform for the ADS848x ADC. The EVM board is a flexible design that allows the user to choose among many different analog signal conditioning, reference, and interface modes.

3 Analog Interface

The ADC accepts a pseudo-bipolar differential input. A pseudo-bipolar differential signal is a fully differential signal that has a common-mode voltage such that the voltage on each input is always equal to or greater than 0 V. The common-mode voltage should be half the reference voltage. The peak-to-peak amplitude on each input leg can be as large as the reference voltage.

The positive leg of the input signal can be applied at connector P1, pin 2 (shown in Table 1) or via the center pin of SMA connector J1. Likewise, the negative input signal can be applied at P1, pin 1 or via the center pin of SMA connector J2.

Table 1. Analog Input Connector

Description	Signal Name	Connector Pin No.		Signal Name	Description
Not connected	–	P1.1	P1.2	+	Noninverting input channel
Reserved	N/A	P1.3	P1.4	N/A	Reserved
Reserved	N/A	P1.5	P1.6	N/A	Reserved
Reserved	N/A	P1.7	P1.8	N/A	Reserved
Reserved	N/A	P1.9	P1.10	N/A	Reserved
Pin tied to ground	AGND	P1.11	P1.12	N/A	Reserved
Pin tied to ground	AGND	P1.13	P1.14	N/A	Reserved
Reserved	N/A	P1.15	P1.16	N/A	Reserved
Pin tied to ground	AGND	P1.17	P1.18	N/A	Reserved
Pin tied to ground	AGND	P1.19	P1.20	REF+	External reference input

3.1 Input Signal Conditioning

The analog input circuitry, consisting of three THS4031 operational amplifiers, allow the user to install passive components to configure the EVM for positive or negative gains, as well as input range scaling, filtering, and level translation (for example, adding a dc offset). The installed operational amplifiers are housed in an industry-standard SOIC footprint. This architecture enables the user to replace the THS4031 with a wide range of dual- and single-supply amplifiers housed in an SOIC package. When choosing the driver amplifier, the user should consider the following requirements: The driving amplifier must be able to settle the input to 18-bit level (0.00038%) within the sample time of the converter. It should have total harmonic distortion (THD) characteristics comparable to or better than the ADS848x over the bandwidth of interest. Lastly, the noise generated by the amplifier must be as low as possible, so as not to degrade (or source-limit) the performance of the ADS848x.

The RC circuit, at the input of the ADC, filters the input signal and helps charge the ADC sample-and-hold stage. The noise coming through the driver amplifier is also filtered using this single-pole filter. The 5-Ω series resistor works with the capacitor to filter the input signal, but also isolates the amplifier from the capacitive load. The 2200-pF capacitor works with the series resistor to filter the input signal and behaves like a charge reservoir, providing a discharge path for high-frequency noise and the input current transients that occur when the device switches from hold to sample mode. This external capacitor works with the amplifier to charge the internal sampling capacitor during sampling mode. In multiplexing applications, the values of these resistors and capacitor may need to be adjusted. As with the driving amplifier, the RC circuit must also be able to settle the signal to a 18-bit level within the sample time.

The supplies to the input amplifier are selectable with solder jumper pad SJP3 and SJP4. Shorting across pads 1 and 2 will ground the negative rail. Shorting across pads 2 and 3 will tie the negative supply of the amplifiers to the voltage applied at node –VCC.

When deciding on supply rails for bipolar amplifiers, a good rule is to add at least 2 V of head room on either side to achieve optimal performance. For example, if the signal applied to the amplifier is 0V to 4 V, then the amplifier rails should be at least –2 V and +6 V. For the 16-bit and 18-bit performance nodes, the amplifier-introduced distortion can become significant and degrade overall system perforamnce. For CMOS, or single-supply amplifiers, this configuration is not always possible. As with the bipolar amplifiers, single-supply amplifiers also degrade with larger amplitudes and at higher input frequencies. The user must test the amplifier separately to understand its respective characteristics across the given input conditions. Take care when reading product data sheets to understand how the device is characterized. It may not be possible to surmise from a cursory glance how well the amplifier will behave in a given system.

Single-ended signal sources are readily available; therefore, the ADS848xEVM ships in this configuration. The factory-set default configuration of the input driving circuitry is for converting a single-ended, unipolar signal to differential. The necessary dc component to offset the signal at U7 is generated by U4. U4 is the low-noise THS4032 amplifier. It can be configured to further filter the reference voltage IC, U2, and provide positive or negative gains. The ADS848xEVM leaves the factory with potentiometer, R24, set to 2.048 V and set as shown in Figure 1. If a fully differential signal source is available, it is recommended the input circuitry be set up as shown in Figure 2 or as Figure 40 in the ADS8484 product data sheet. Table 2 indicates how the solder pad jumpers should be set to select from the various supply and input options for the analog driver circuitry. The schematic for the ADS848xEVM is attached at the end of this document.

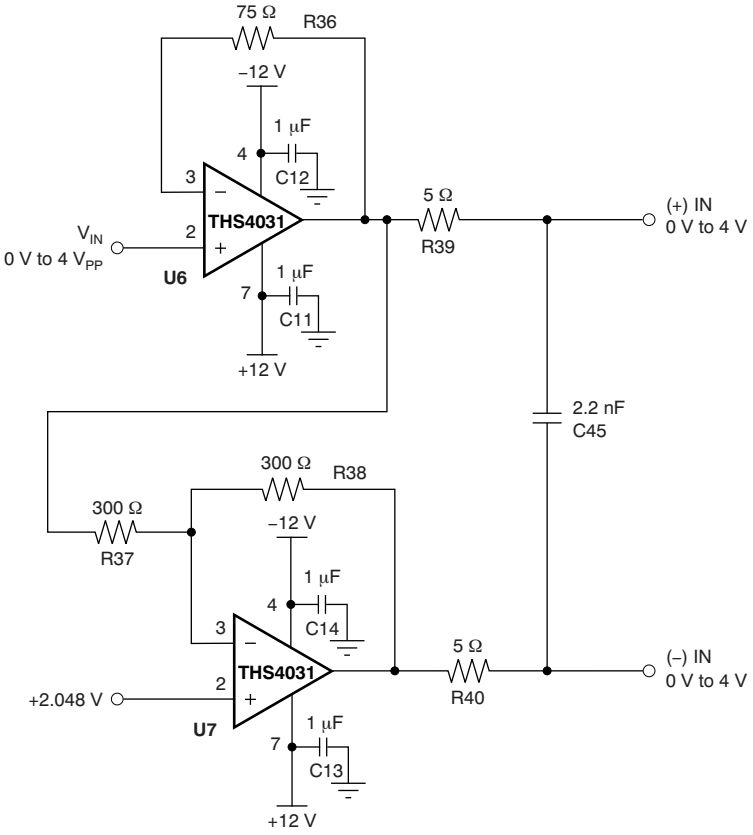


Figure 1. Input Buffer Circuit, Default Configuration

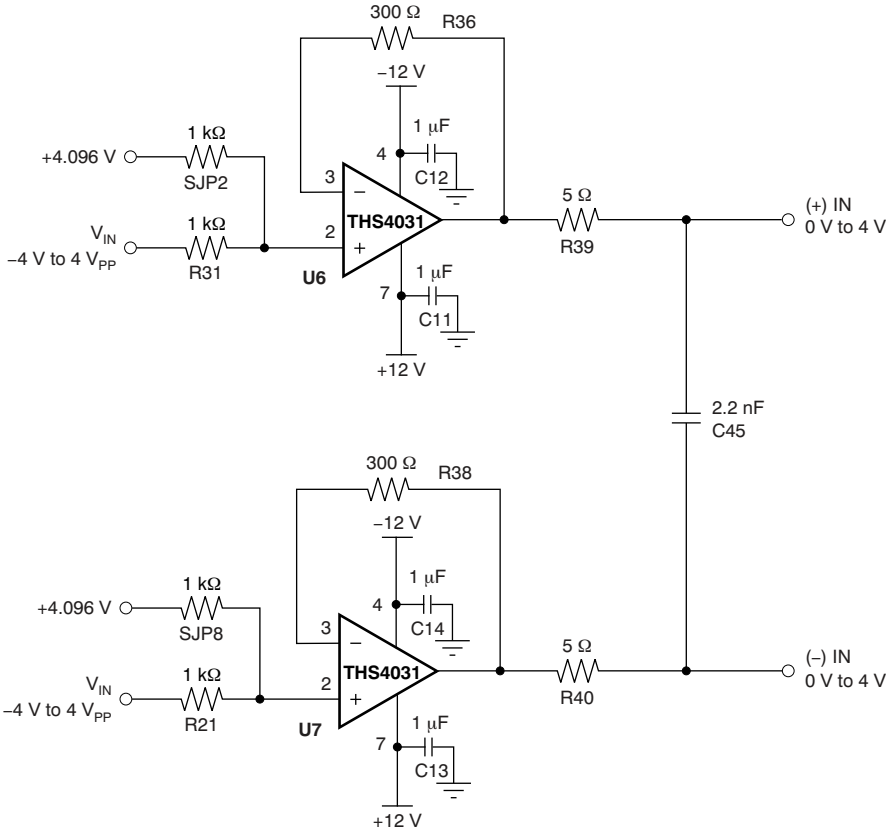


Figure 2. Input Buffer, Bipolar Fully Differential Input

Table 2. Analog Circuitry Jumper Configurations

Reference Designator	Description	Jumper Position	
		1-2	2-3
SJP1	Select onboard reference (REF3240)	**Installed** (1)	Not Installed
	Select user-supplied reference at P1 pin 20	Not Installed	Installed
SJP2	Short voltage node +dc to U6 pin 3	Installed	N/A
SJP3	Set U6 operational amplifier minus rail supply to ground	Installed	Not installed
	Set U6 operational amplifier minus rail supply to –VCC	Not installed	**Installed** (1)
SJP4	Set U7 operational amplifier minus rail supply to ground	Installed	Not Installed
	Set U7 operational amplifier minus rail supply to –VCC	Not installed	**Installed** (1)
SJP6	Set REFIN pin of ADS848x to on-chip (internal) reference voltage.	**Installed** (1)	Not installed
	Set REFIN pin of ADS848x to reference selected by SJP1.	Not installed	Installed
SJP7	Short voltage node –dc to U6 pin 2 via R35.	Installed	N/A
SJP8	Short voltage node +dc to U7 pin 3.	**Installed** (1)	N /A
SJP9	Short –IN pin of U5 to ground at C45.	Not Installed	N/A

(1) Indicates factory-installed option.

3.2 Reference

The ADS848x can operate with an external reference voltage in the range of 3 V up to 4.2 V. It generates an on-chip 4.096-V reference voltage. The ADS848xEVM allows the user to select the external reference voltage from three sources. The first option is to use the internally-generated 4.096 V from the ADC. The other two options are to select from the onboard reference (U1) or a user-supplied voltage applied at pin 20 of P1. See Table 2 for solder jumper options for selecting from the various reference sources.

The reference voltage provides the scale factor for the conversion result. The input voltage is measured against the reference voltage. It is imperative the reference voltage be clean, low-noise, and well-decoupled.

The default configuration uses the internal on-chip reference.

4 Digital Interface

The ADS848xEVM is designed for easy interfacing to multiple platforms. The digital interface input and output signals of the converter are on connectors P2, P3, and J6. These connectors are 0.1-inch center, plug and socket connectors that allow the user to plug the ADS848xEVM into the various motherboard interface boards from Texas Instruments, or connect via ribbon cable to a variety of user development boards. Table 3 through Table 6 list the connector pinouts and jumper settings.

Table 3. Pinout for Parallel Control Connector P3

Description	Signal Name	Connector Pin No.		Signal Name	Description
Not connected	$\overline{\text{DC\_CS}}$	P3.1	P3.2	+	Noninverting input channel
Reserved	N/A	P3.3	P3.4	GND	Ground
Reserved	N/A	P3.5	P3.6	GND	Ground
Address line 0	A0	P3.7	P3.8	GND	Ground
Address line 1	A1	P3.9	P3.10	GND	Ground
Address line 2	A2	P3.11	P3.12	GND	Ground
Reserved	N/A	P3.13	P3.14	GND	Ground
Reserved	N/A	P3.15	P3.16	GND	Ground
Convert Start	$\overline{\text{DC\_CONVST}}$	P3.17	P3.18	GND	Ground
Interrupt pin	INTC	P3.19	P3.20	GND	Ground

Conversions are initiated on the falling edge of the convert start signal. It is therefore critical to provide a clean, low-jitter, Convert Start ($\overline{\text{CONVST}}$) pulse when measuring large amplitude and/or high-frequency input signals.

The $\overline{\text{CONVST}}$ signal can be applied to the ADS848x from the decoder outputs, at J6 pin 5, or from connector P3 pin 17. Address decoder SN74ACH138 can be used to generate the Read (RD) and $\overline{\text{CONVST}}$ signals to the converter. Jumpers W3 and W4 allow the user to assign these two signals to different addresses in memory. This option allows for the stacking of up to two ADS848xEVMs into processor memory. See Table 4 for jumper settings. If a Convert Start signal is applied directly to P3 pin 17, it is then necessary to short W6 pins 1-2. This configuration bypasses the decoder output selected by the position of W4.

Note: The evaluation module does not allow the Chip Select ($\overline{\text{CS}}$) line of the converter to be assigned to different memory locations. It is therefore suggested that the $\overline{\text{CS}}$ line be grounded or wired to an appropriate signal of the processor.

Table 4. Jumper Settings

Reference Designator	Description	Pin No.	
		1-2	2-3
W1	Set digital buffer supply voltage to +5 V	**Installed** (1)	Not installed
	Set digital buffer supply voltage to +3.3 V	Not Installed	Installed
W2	Apply inverted BUSY to INTC signal	**Installed** (1)	Not installed
	Apply BUSY signal to INTC signal	Not installed	Installed
W3	Set $\overline{\text{RD}}$ signal to decoder output three [0x3].	**Installed** (1)	Not installed
	Set $\overline{\text{RD}}$ signal to decoder output four [0x4].	Not installed	Installed
W4	Set $\overline{\text{CONVST}}$ signal to decoder output one [0x1].	**Installed** (1)	Not installed
	Set $\overline{\text{CONVST}}$ signal to decoder output two [0x2].	Not Installed	Installed
W5	Set $\overline{\text{DC\_CS}}$ to $\overline{\text{CS}}$ of ADS848x	**Installed** (1)	N/A
W6	Set $\overline{\text{DC\_CONVST}}$ to $\overline{\text{CONVST}}$ of ADS848x.	**Installed** (1)	Installed
	Set decoder output to $\overline{\text{CONVST}}$ of ADS848x.	Not installed	**Installed** (1)

(1) Indicates factory-installed option.

The data bus is available at connector P2; see Table 5 for pinout information.

Table 5. Data Bus Connector P2

Description	Signal Name	Connector Pin No.		Signal Name	Description
Data bit 0	DB0	P2.1	P2.2	GND	Ground
Data bit 1	DB1	P2.3	P2.4	GN D	Ground
Data bit 2	DB2	P2.5	P2.6	GND	Ground
Data bit 3	DB3	P2.7	P2.8	GND	Ground
Data bit 4	DB4	P2.9	P2.10	GND	Ground
Data bit 5	DB5	P2.11	P2.12	GND	Ground
Data bit 6	DB6	P2.13	P2.14	GND	Ground
Data bit 7	DB7	P2.15	P2.16	GND	Ground
Data bit 8	DB8	P2.17	P2.18	GND	Ground
Data bit 9	DB9	P2.19	P2.20	GND	Ground
Data bit 10	DB10	P2.21	P2.22	GND	Ground
Data bit 11	DB11	P2.23	P2.24	GND	Ground
Data bit 12	DB12	P2.25	P2.26	GND	Ground
Data bit 13	DB13	P2.27	P2.28	GND	Ground
Data bit 14	DB14	P2.29	P2.30	GND	Ground

Table 5. Data Bus Connector P2 (continued)

Description	Signal Name	Connector Pin No.		Signal Name	Description
Data bit 15	DB15	P2.31	P2.32	GND	Ground
Data bit 16	DB16	P2.33	P2.34	GND	Ground
Data bit 17	DB17	P2.35	P2.36	GND	Ground

This evaluation module provides direct access to all the ADC input control and output signals via connector J4; see Table 6.

Table 6. Pinout for Converter Control Connector, J6

Description	Signal Name	Connector Pin No.		Signal Name	Description
Chip Select signal	$\overline{CS}$	J6.1	J6.2	GND	Ground
Read signal	$\overline{RD}$	J6.3	J6.4	GND	Ground
Convert Start signal	$\overline{CONVST}$	J6.5	J6.6	GND	Ground
Byte signal	BYTE	J6.7	J6.8	GND	Ground
18- or 16-bit bus signal	BUS18/$\overline{16}$	J6.9	J6.10	GND	Ground
Busy signal	BUSY	J6.11	J6.12	GND	Ground

5 Power Supplies

The EVM accepts four power supplies.

- A dual ±VA dc supply for the dual-supply operational amplifiers. Recommend ±6-VDC supply.
- A single +5-VDC supply for analog section of the board (analog-to-digital [A/D] + Reference).
- A single +5-V or +3.3-VDC supply for digital section of the board (A/D + address decoder + buffers).

These voltages can be provided in two ways.

1. Wire in voltages at test points on the EVM; Table 7 summarizes this option.

Table 7. Power-Supply Test Points

Test Point	Signal	Description
TP6	+BVDD	Apply +3.3 VDC or +5 VDC. See ADC data sheet for full range.
TP3	+AVCC	Apply +5 VDC.
TP4	+VA	Apply +6 VDC. Positive supply for amplifier.
TP5	–VA	Apply –6 VDC. Negative supply for amplifier.

2. Use the power connector J5, and derive the voltages elsewhere. The pinout for this connector is shown in Table 8. If using this connector, then set W1 jumper to connect +3.3 VD or +5 VD from connector to +BVDD. Short between pins 1-2 to select +5 VDC, or short between pins 2-3 to select +3.3 VDC as the source for the digital buffer voltage supply (+BVDD).

Table 8. Power Connector, J1, Pinout

Signal Power	Connector: J1		Signal
+VA (+6 V)	1	2	–VA (–6 V)
+5 VA	3	4	N/C
DGND	5	6	AGND
N/C	7	8	N/C
+3.3 VD	9	10	+5 VD

6 Using the ADS848xEVM

The ADS848xEVM functions as a reference design, a prototyping board, and a software test platform.

6.1 As a Reference Design

As a reference design, the ADS848xEVM contains the essential circuitry to showcase the analog-to-digital converter. This essential circuitry includes the input amplifier, reference circuit, and buffers. The ADS848xEVM analog input circuit is optimized for a wide bandwidth signal; therefore, the user may need to adjust the input buffer circuitry to better suit specific needs. In ac-type applications where signal distortion is a concern, the user should use high-quality capacitors such as mica, polypropylene, or COG-type capacitors in the signal path. In applications where the input is multiplexed, the A/D input resistor and capacitor may need to be adjusted further.

6.2 As a Prototype Board

As a prototype board, the ADS848xEVM features amplifiers in a standard 8-pin SOIC package. The board contains many resistor pads that allow the user to experiment with a host of circuits as desired. The ADS848xEVM can be used to evaluate both dual- and single-supply amplifiers in both inverting and noninverting configurations. The ADS848xEVM comes installed with a dual-supply amplifier that allows the user to take advantage of the full input voltage range of the converter. For applications that require single-supply operation and a smaller input voltage range, the THS4031 can be replaced with the single-supply amplifier such as the OPA300 or OPA350. Pad jumper SJP3 should be shorted between pads 1 and 2. This configuration shorts the minus supply pin of the amplifier to ground. Positive supply voltage can be applied at test point TP4 or at connector J5 pin 1.

6.3 As a Software Test Platform

As a software test platform, connectors P1, P2, and P3 plug into the parallel interface connectors of the 5-6K Interface Board. The 5-6K Interface Board sits on the C5000™ and C6000™ digital signal processor starter kits (DSK). The ADS848xEVM is then mapped into the processor memory space. The 5-6k Interface Board also provides an area for signal conditioning. This area can be used to install application circuit(s) for digitization by the ADS848x analog-to-digital converter. For more information, see the 5-6K Interface Board User's Guide (SLAU104) .

For the software engineer, the ADS848xEVM provides a simple platform for interfacing to the converter. The EVM provides standard 0.1-inch headers and sockets to wire into prototype boards. The user must provide only three address lines (A2, A1, and A0) and address valid line ($\overline{DC\_CS}$) to connector P2. To select which address combinations generate $\overline{RD}$ and $\overline{CONVST}$, set the jumpers as shown in Table 4. Recall that the Chip Select ($\overline{CS}$) signal is not memory-mapped or tied to P2; therefore, it must be controlled by a general-purpose pin or shorted to ground at J3 pin 1. If address decoding is not required, the EVM provides direct access to converter data bus by P3 and control by J3.

7 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this user's guide by its title and literature number. Updated documents can also be obtained through the TI Web site at www.ti.com.

Data Sheets:	Literature Number:
ADS8482	SLAS385
ADS8484	SLAS511
REF3240	SBVS058
REF3225	SBVS058
SN74AHC138	SCLS258
SN74AHC245	SCLS230
SN74AHC1G04	SCLS318
THS4031	SLOS224
THS4032	SLOS224

Appendix A ADS848xEVM Bill of Materials

Table A-1 lists the complete bill of materials for the ADS848xEVM. The schematic diagram also is provided for reference. Contact the Product Information Center or send an e-mail to dataconvapps@list.ti.com for questions regarding this EVM.

Table A-1. Bill of Materials

Qty	Value	Reference Designators	Footprint	Manufacturer	Manufacturer's Part No.	Description
3	0	R16 R17 R33	603	Panasonic - ECG or Alternate	ERJ-3GEY0R00V	RES 0Ω 1/16W 5% 0603 SMD
4	0	R9 R19 R22 R31	805	Panasonic - ECG or Alternate	ERJ-6GEY0R00V	RES 0.0Ω 1/10W 5% 0805 SMD
2	5.1	R39 R40	805	Panasonic - ECG or Alternate	ERJ-6GEYJ5R1V	RES 5.1Ω 1/10W 1% 0805
3	33	R5 R25 R26	603	Yageo America or Alternate	9C06031A33R0FKHF T	RES 33.0Ω 1/10W 1% 0603 SMD
2	49.9	R1 R2	603	Panasonic - ECG or Alternate	ERJ-3EKF49R9V	RES 49.9Ω 1/10W 1% 0603 SMD
3	300	R4 R27 R29	603	Yageo America or Alternate	RC0603FR-07300RL	RES 300Ω 1/10W 1% 0603 SMD
3	300	R36 R37 R38	805	Yageo America or Alternate	9C08052A3000FKHF T	RES 300Ω 1/8W 1% 0805 SMD
1	10k	R24	BOURNS_3296 Y	Bourns Inc.	3296Y-1-103	POT 10kΩ 3/8" SQ CERM SL MT
5	10k	R41–R45	603	Panasonic - ECG or Alternate	ERJ-3EKF1002V	RES 10.0kΩ 1/10W 1% 0603 SMD
1	10k	R46	805	Panasonic - ECG or Alternate	ERJ-6GEYJ103V	RES 10kΩ 1/8W 5% 0805 SMD
3	NI	R3 R6 R28	603	Not Installed	Not Installed	
11	NI	R7 R8 R10 R12 R13 R18 R20 R21 R32 R34 R35	805	Not Installed	Not Installed	
2	50	RP1 RP2	CTS_742	CTS Corporation	742C163470JTR	RES Array 47Ω 16TERM 8RES SMD
1	50	RP4	CTS_742_4RE S	CTS Corporation	742C083510JTR	RES Array 51Ω 8TERM 4RES SMD
1	1K	RP3	CTS_742	CTS Corporation	742C163102JTR	RES Array 1kΩ 16TERM 8RES SMD
4	MMZ2012R601A	L1 L2 L3 L4	805	TDK Corporation	MMZ2012R601A	FERRITE Chip 600Ω 500mA 0805
13	1000pF	C28–C36 C62–C65	603	TDK Corporation or Alternate	C1608X7R1H102K	CAP CER 1000PF 50V XR7 10% 0603
1	2200pF	C45	603	TDK Corporation or Alternate	C1608COG1H222J	CAP CER 2200PF 50V XR7 10% 0603
6	0.1µF	C66–C71	603	TDK Corporation or Alternate	C1608X7R1E104K	CAP CER 0.10µF 25V X7R 10% 0603
2	0.47µF	C1 C2	603	TDK Corporation or Alternate	C1608X5R1A474K	CAP CER 0.47µF 10V X5R 10% 0603
3	1µF	C3 C5 C7	603	TDK Corporation or Alternate	C1608X5R1A105KT	CAP CER 1.0µF 10V X5R 10% 0603
8	1µF	C9–C14 C41, C42	805	TDK Corporation or Alternate	C2012X7R1E105K	CAP CER 1.0µF 25V X7R 0805 T/R
8	2.2µF	C20–C27	603	TDK Corporation or Alternate	C1608X5R1A225MT	CAP CER 2.2µF 6.3V X5R 20% 0603
2	10µF	C38 C40	805	TDK Corporation or Alternate	C2012X5R0J106M	CAP CER 10µF 6.3V X5R 20% 0805
8	10µF	C48–C55	1206	TDK Corporation or Alternate	C3216X5R1C106M	CAP CER 10µF 16V X5R 20% 1206
1	22µF	C6	805	TDK Corporation or Alternate	C2012X5R0J226M	CAP CER 22µF 6.3V X5R 20% 0805
1	47µF	C37	1206	TDK Corporation or Alternate	C3216X5R0J476M	CAP CER 47µF 6.3V X5R 20% 1206

Table A-1. Bill of Materials (continued)

Qty	Value	Reference Designators	Footprint	Manufacturer	Manufacturer's Part No.	Description
14	NI	C4 C8 C15 C16 C18 C19 C46 C47 C56–C61	603	Not Installed	Not Installed	
4	NI	C13 C39 C43–C44	805	Not Installed	Not Installed	
1	REF3225	U1	6-SOT(DBV)	Texas Instruments	REF3225AIDBVR	4.096V 4ppm/°C, 100µA SOT23-6 Series (Bandgap) Voltage Reference
1	REF3240	U2	6-SOT(DBV)	Texas Instruments	REF3240AIDBVR	4.096V 4ppm/°C, 100µA SOT23-6 Series (Bandgap) Voltage Reference
1	NI	U3	8-SOP(D)	Not Installed	Not Installed	SOIC reference alternate
1	THS4032	U4	8-SOP(D)	Texas Instruments	THS4032CD	100-MHz Low Noise Voltage-Feedback Amplifier, Dual
1	ADS8482/ADS8484	U5	48-QFN(RGZ)	Texas Instruments	ADS848xIBRGZR	ADS848x 18-bit, 1-MSPS/1.25-MSPS ADC
2	THS4031	U6 U7	8-SOP(D)	Texas Instruments	THS4031IDR	100-MHz low-noise high-speed amplifier
4	SN74AHC245PWR	U8–U11	20-TSSOP(PW)	Texas Instruments	SN74AHC245PWR	Octal Bus Transceiver, 3-State
1	SN74AHC1G04DBV	U12	5-SOT(DBV)	Texas Instruments	SN74AHC1G04DBVR	Single Inverter Gate
1	SN74AHC138PWR	U13	16-TSSOP(PW)	Texas Instruments	SN74AHC138PWR	3-Line To 8-Line Decoder / Demultiplexer
2	SMA_PCB_MT	J1 J2	SMA_JACK	Johnson Components Inc.	142-0701-301	Right Angle SMA Connector
2	NI	J3 J4	SMA_JACK	Not Installed	Not Installed	
1	5X2X.1	J5	5X2X.1_SMT_ SOCKET	Samtec	SSW-110-22-S-D-VS	0.025" SMT SOCKET - BOTTOM SIDE OF PWB
1				Samtec	TSM-105-91-T-D-V-P	0.025" SMT Plug - top side of PWB
1	6X2X.1	J6	6X2X.1_SMT_ PLUG_&_ SOCKET	Samtec	TSM-106-91-T-D-V-P	0.025" SMT Plug - top side of PWB
2	10X2X.1	P1 P3	10X2X.1_SMT_ PLUG_&_ SOCKET	Samtec	SSW-110-22-S-D-VS	0.025" SMT SOCKET - BOTTOM SIDE OF PWB
2	10X2X.1			Samtec	TSM-110-01-T-D-V-P	0.025" SMT Plug - top side of PWB
1	18X2X.1_SMT_PLU G _&_SOCKET	P2	18X2.1_SMT_ PLUG_&_ SOCKET	Samtec	SSW-118-22-S-D-VS	0.025" SMT Socket - bottom side of PWB
1			Samtec	TSM-118-01-T-D-V-P	0.025" SMT Plug - top side of PWB	
5	3POS_JUMPER	W1–W4 W6	3pos_jump	Samtec	TSW-103-07-L-S	3 Position Jumper _ 0.1" spacing
1	3POS_JUMPER	W5	2pos_jump	Samtec	.TSW-102-07-L-S	2 Position Jumper _ 0.1" spacing
4	SJP2	SJP2 SJP7 SJP8 SJP9	SJP2	Not Installed	Not Installed	
4	SJP3	SJP1 SJP3 SJP4 SJP6	SJP3	Not Installed	Not Installed	
8	TP_0.025	TP3–TP7 TP9 TP11 TP12	test_point2	Keystone Electronics	5000K–ND	Test point PC MINI 0.040"D Red
6	TP_0.025	TP1 TP2 TP8 TP10 TP13 TP14	test_point2	Keystone Electronics	5001K–ND	Test point PC MINI 0.040"D Black

Appendix B ADS848xEVM LAYOUT

This appendix contains the EVM layout.

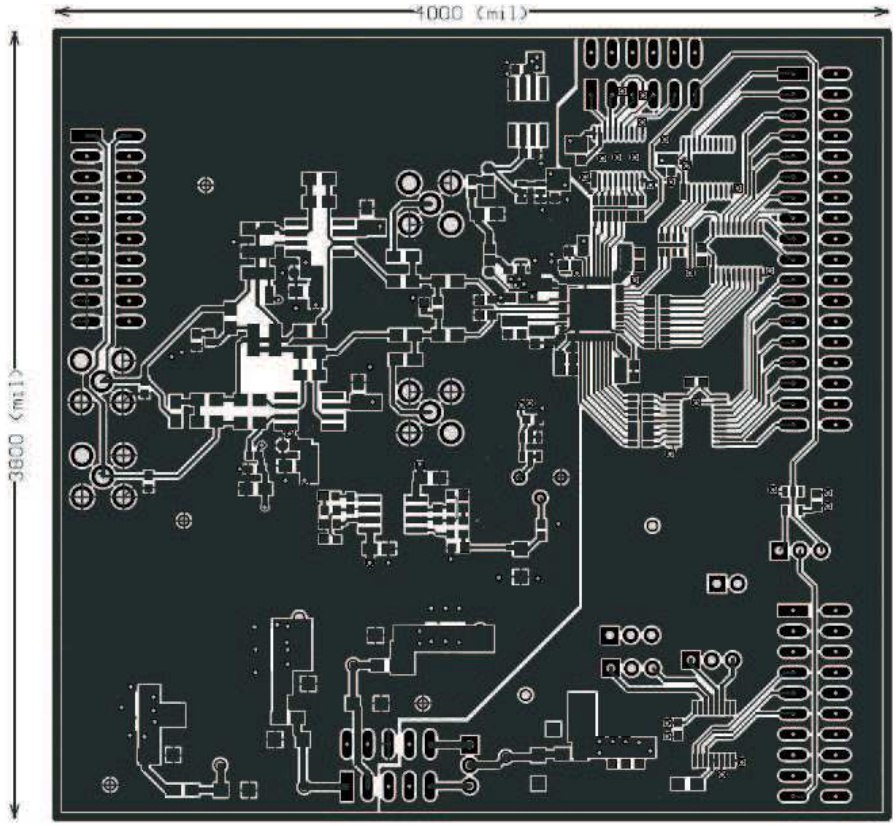


Figure B-1. Top Layer – Layer 1

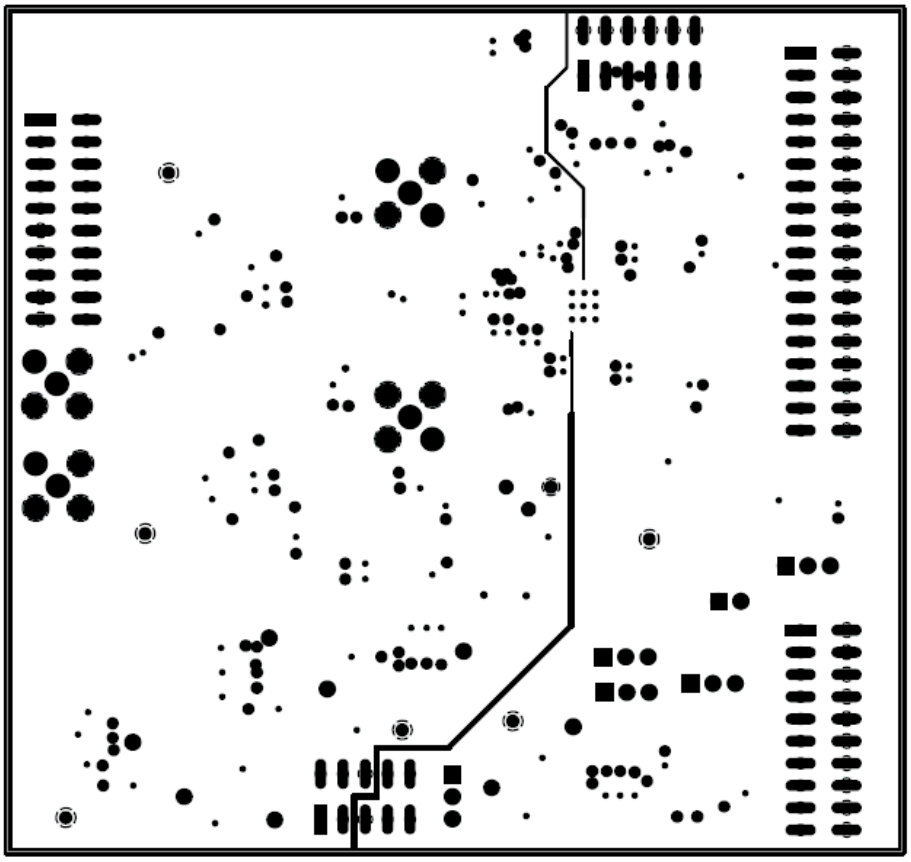


Figure B-2. Ground Plane – Layer 2

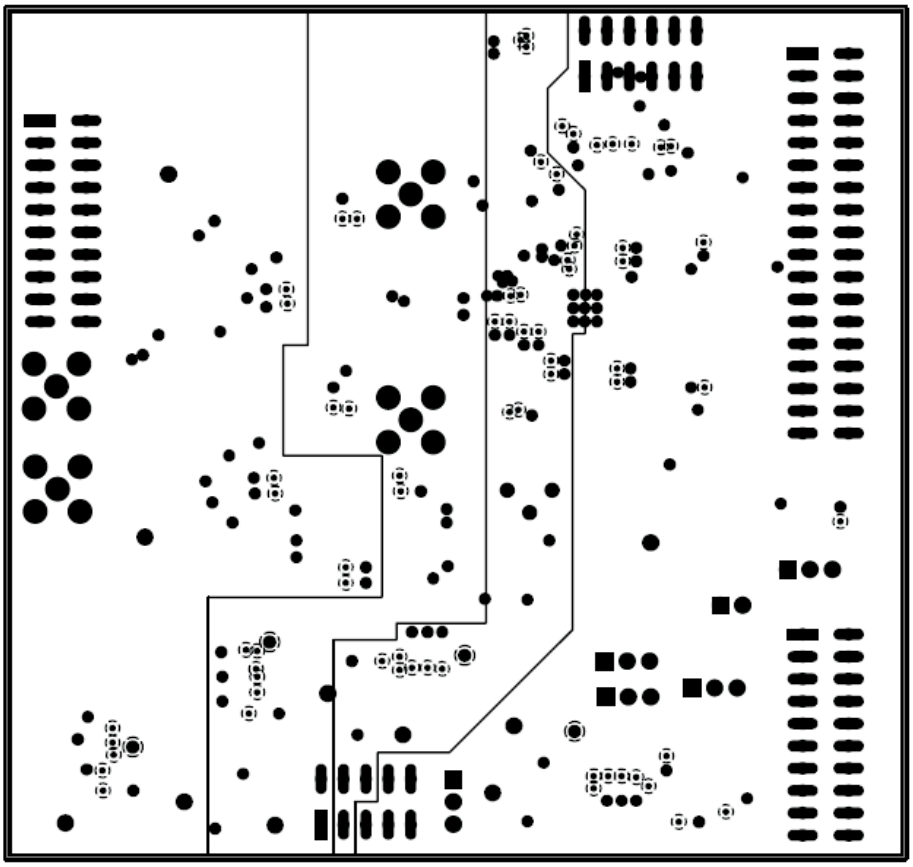


Figure B-3. Power Plane – Layer 3

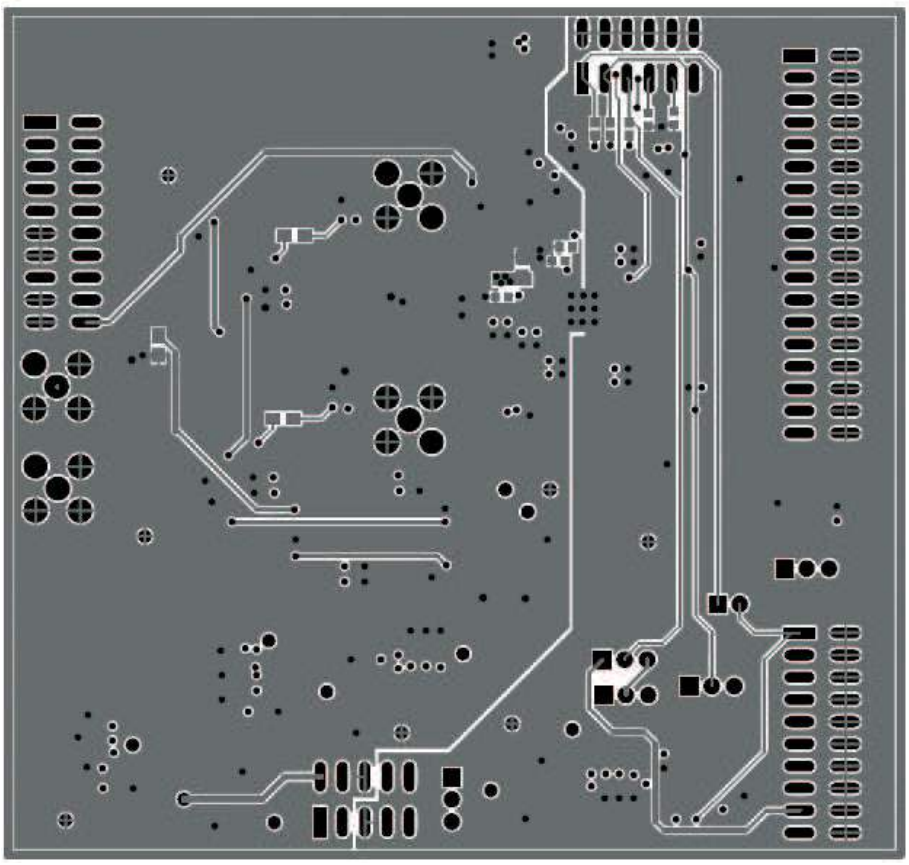


Figure B-4. Bottom Layer – Layer 4

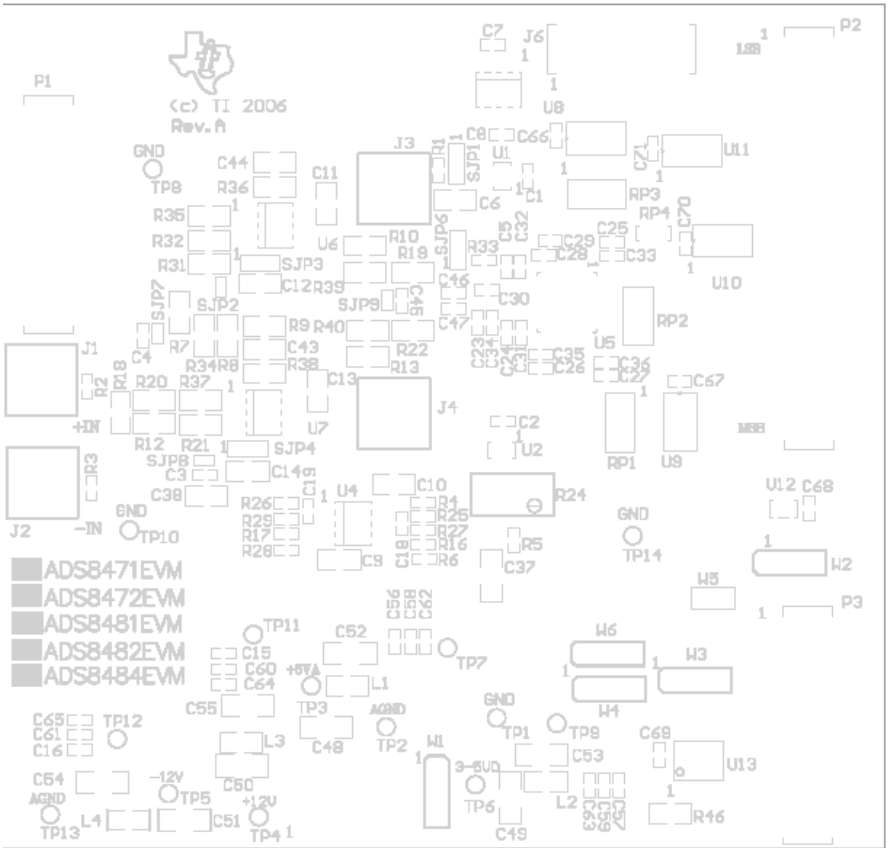


Figure B-5. Top Overlay

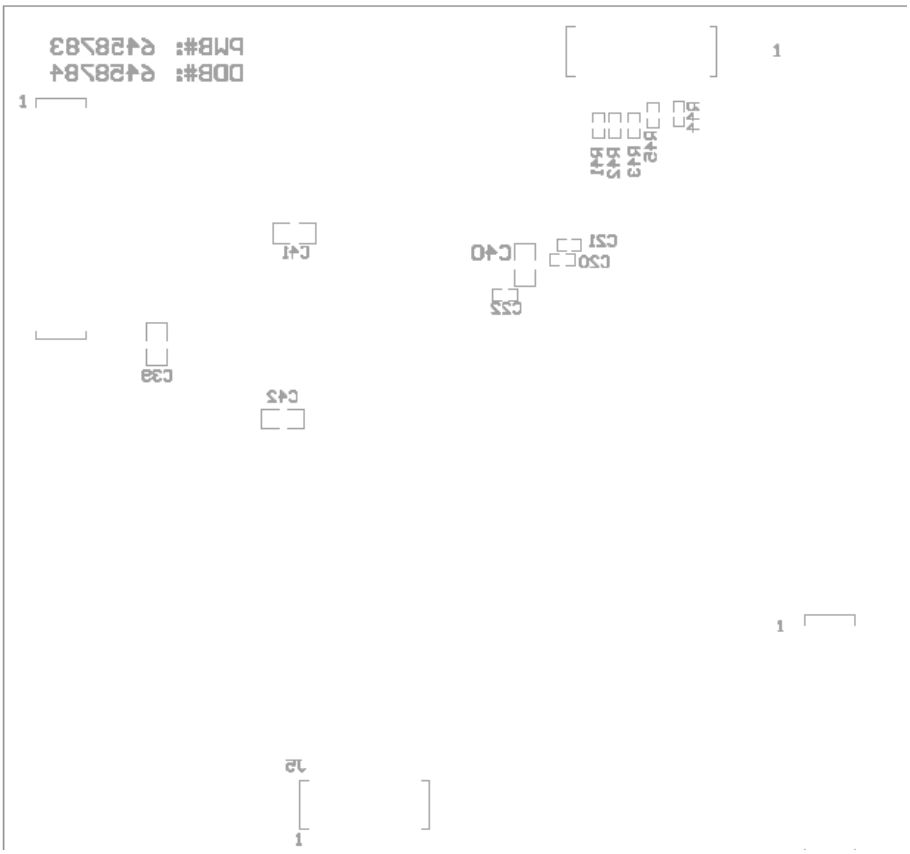
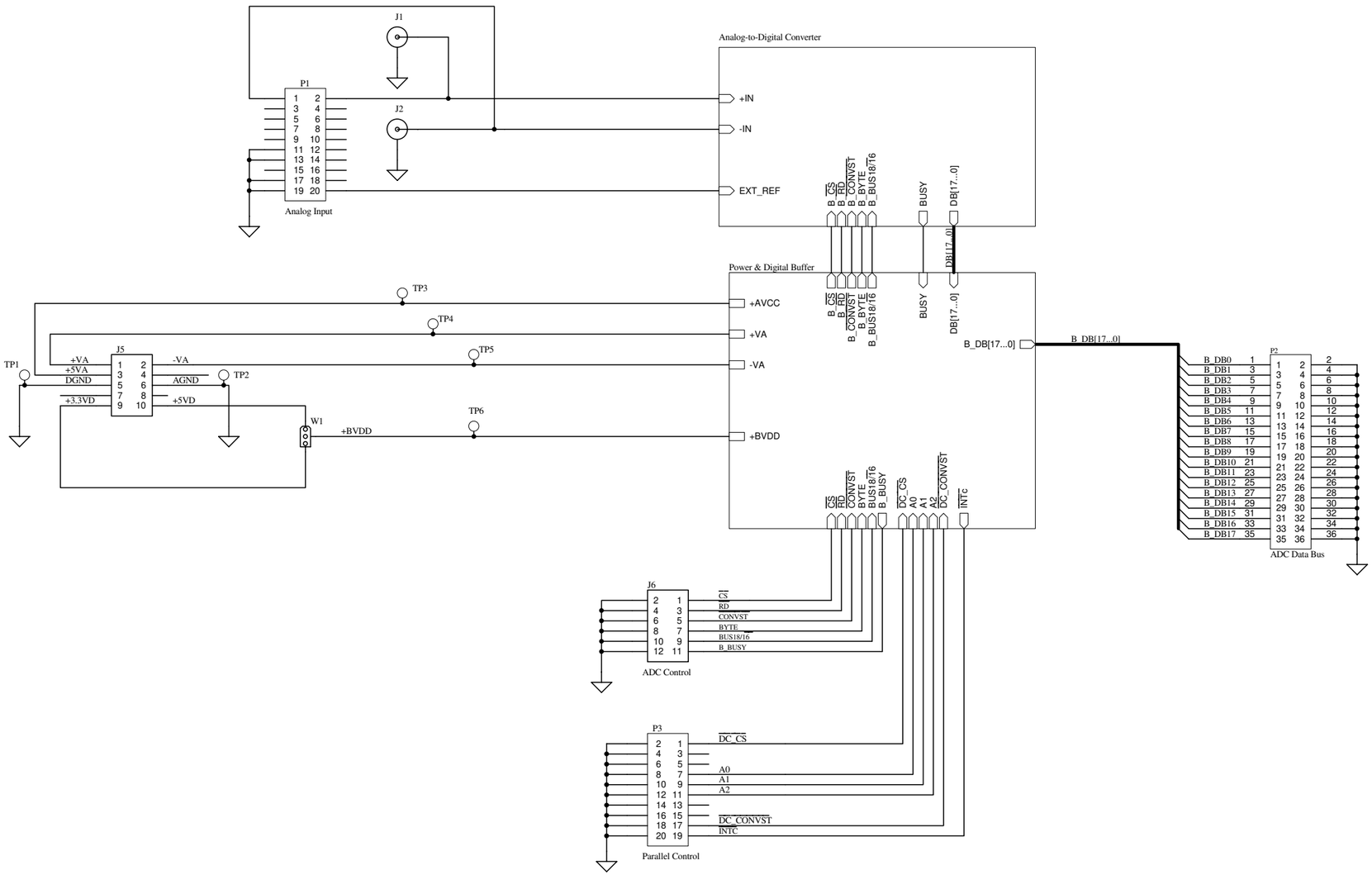


Figure B-6. Bottom Overlay

Appendix C ADS848xEVM Schematic

The ADS848xEVM schematic is appended to this page.

Revision History		
REV	ECN Number	Approved



Engineer:	Lijoy Philipose
Drawn By:	Lijoy Philipose
FILE:	BlockDiagram.sch

TEXAS INSTRUMENTS

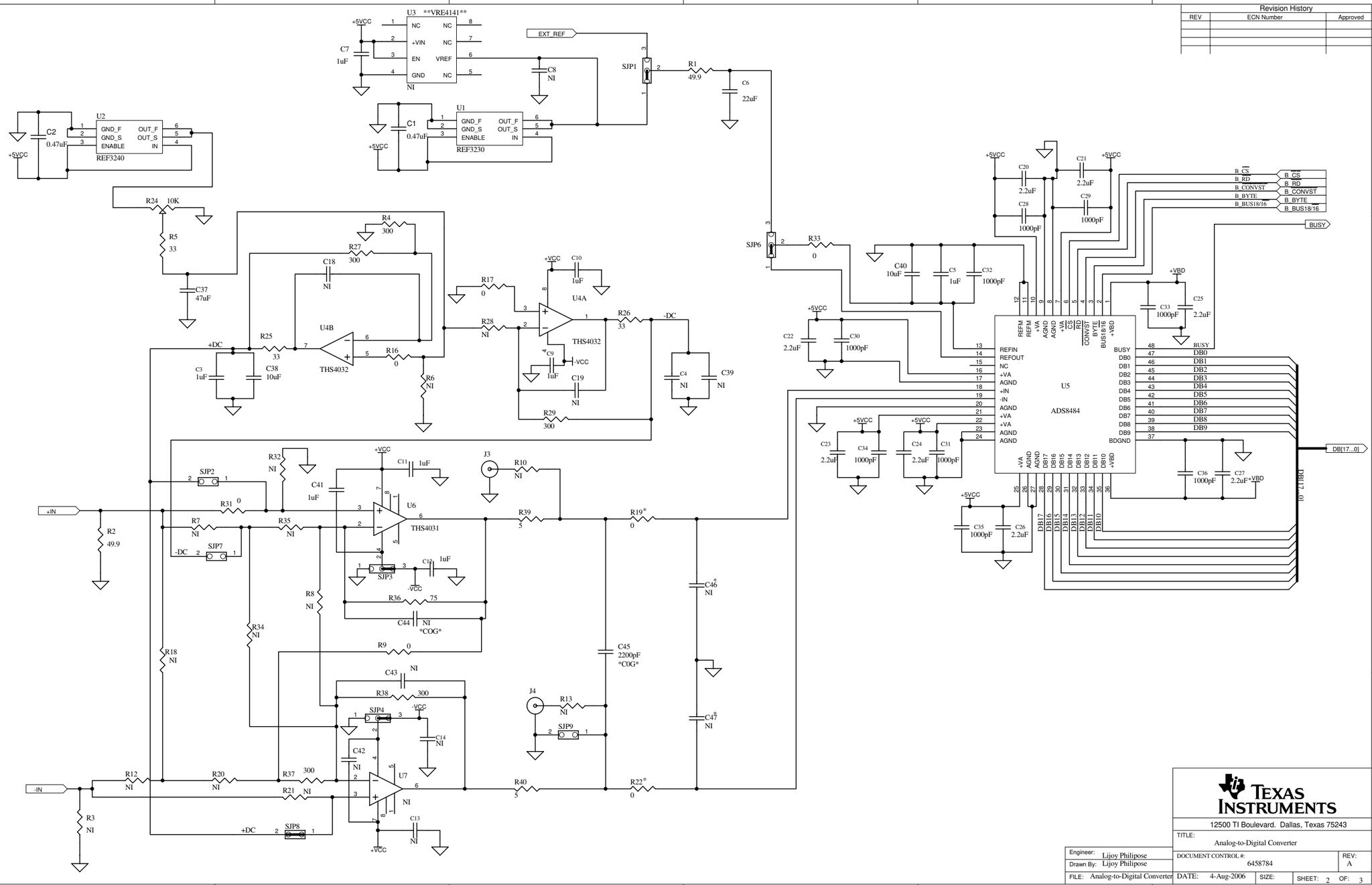
12500 TI Boulevard. Dallas, Texas 75243

TITLE: ADS8481/ADS8482EVM Block Diagram

DOCUMENT CONTROL #: 6458784 | REV: A

DATE: 4-Aug-2006 | SIZE: | SHEET: 1 OF: 3

Revision History		
REV	ECN Number	Approved



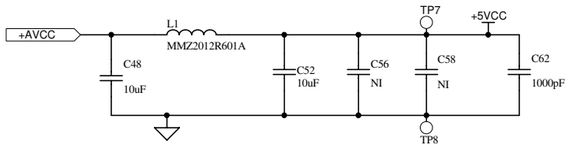
Engineer:	Lijoy Philipose
Drawn By:	Lijoy Philipose
FILE:	Analog-to-Digital Converter

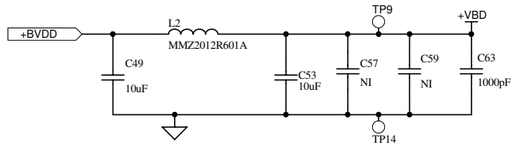
TEXAS INSTRUMENTS

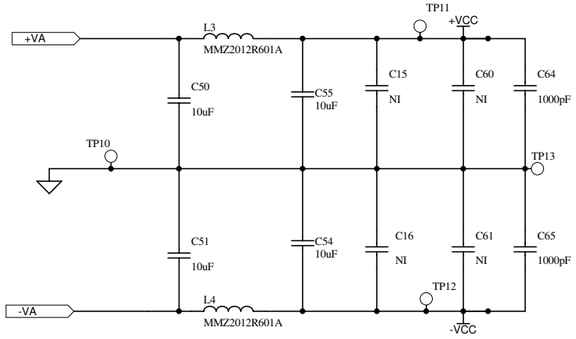
12500 TI Boulevard. Dallas, Texas 75243

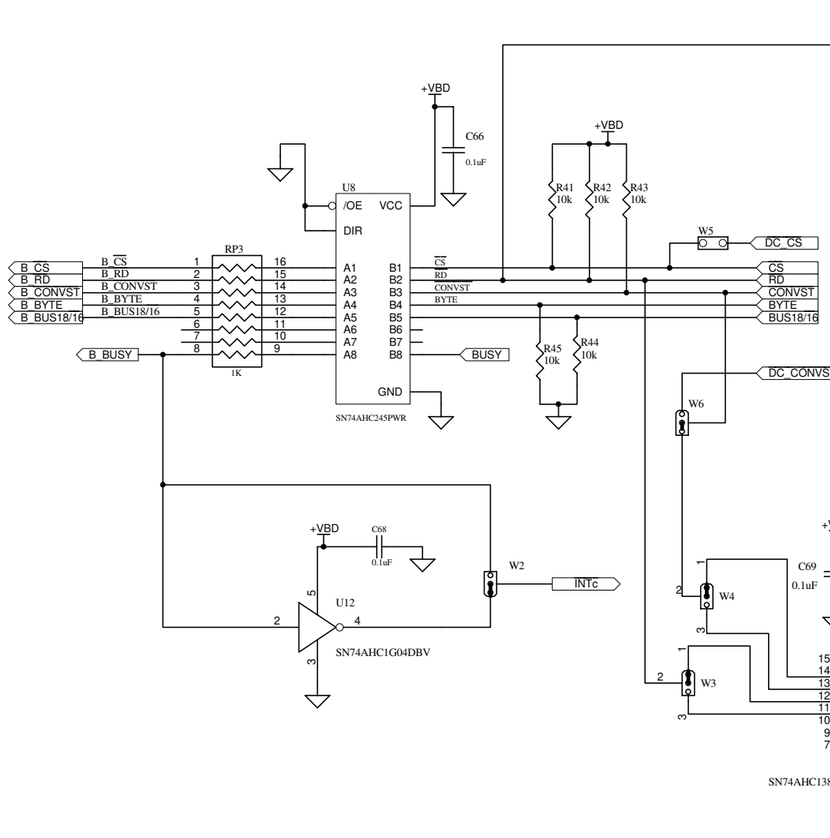
TITLE: Analog-to-Digital Converter		
DOCUMENT CONTROL #: 6458784		REV: A
DATE: 4-Aug-2006	SIZE:	SHEET: 2 OF: 3

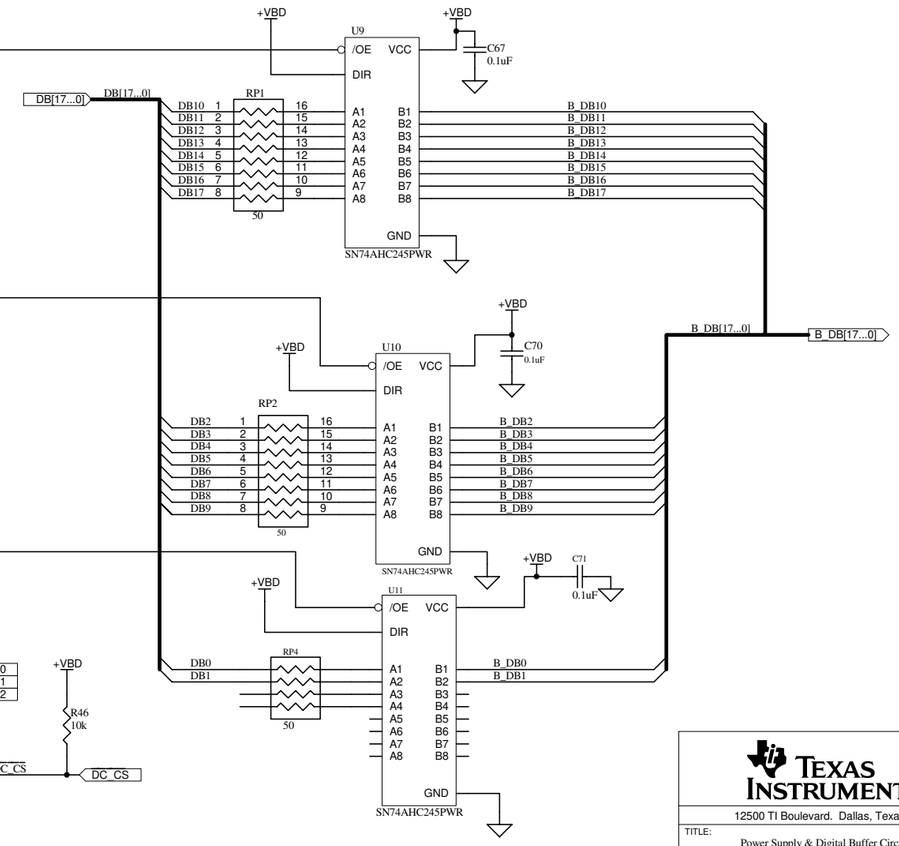
Revision History		
REV	ECN Number	Approved











TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

TITLE:	Power Supply & Digital Buffer Circuit
DOCUMENT CONTROL #:	6458784
REV:	5
DATE: 4-Aug-2006	SIZE:
SHEET: 3 OF: 3	
Engineer: Lijoy Philipose	
Drawn By: Lijoy Philipose	
FILE: Power & Digital Buffer	

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It is important to operate this EVM within the input voltage range of 0 V to 5 V and the output voltage range of 0 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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