3A, 1MHz, Synchronous Step-Down Converter

General Description

The RT8071D is a high efficiency synchronous, step-down DC/DC converter. Its input voltage ranges from 2.7V to 5.5V that provides an adjustable regulated output voltage from 0.6V to V_{IN} while delivering up to 3A of output current. The internal synchronous low On-resistance power switches increase efficiency and eliminate the need for an external Schottky diode. The switching frequency is fixed internally at 1MHz. The 100% duty cycle provides low dropout operation, hence extending battery life in portable systems. Current mode operation with internal compensation allows the transient response to be optimized over a wide range of loads and output capacitors. The RT8071D is available in the WDFN-10L 3x3 package.

Ordering Information

RT8071D□□

- Package Type
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

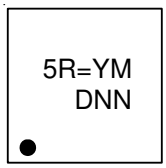
Features

- **High Efficiency : Up to 95%**
- **High Efficiency at Light Load**
- **Low $R_{DS(ON)}$ Power Switches : 69mΩ/49mΩ**
- **Fixed Frequency : 1MHz**
- **No Schottky Diode Required**
- **Internal Compensation**
- **0.6V Reference Allows Low Output Voltage**
- **Low Dropout Operation : 100% Duty Cycle**
- **OCP, UVP, OTP**

Applications

- Portable Instruments
- Battery Powered Equipments
- Notebook Computers
- Distributed Power Systems
- IP Phones
- Digital Cameras

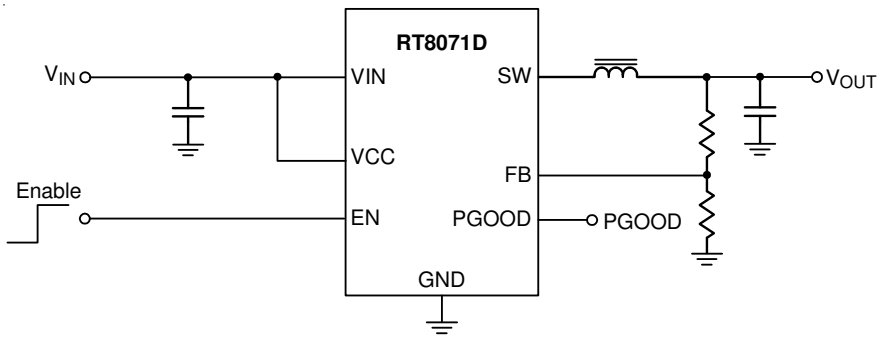
Marking Information



5R= : Product Code

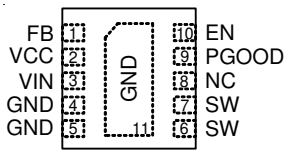
YMDNN : Date Code

Simplified Application Circuit



Pin Configurations

(TOP VIEW)

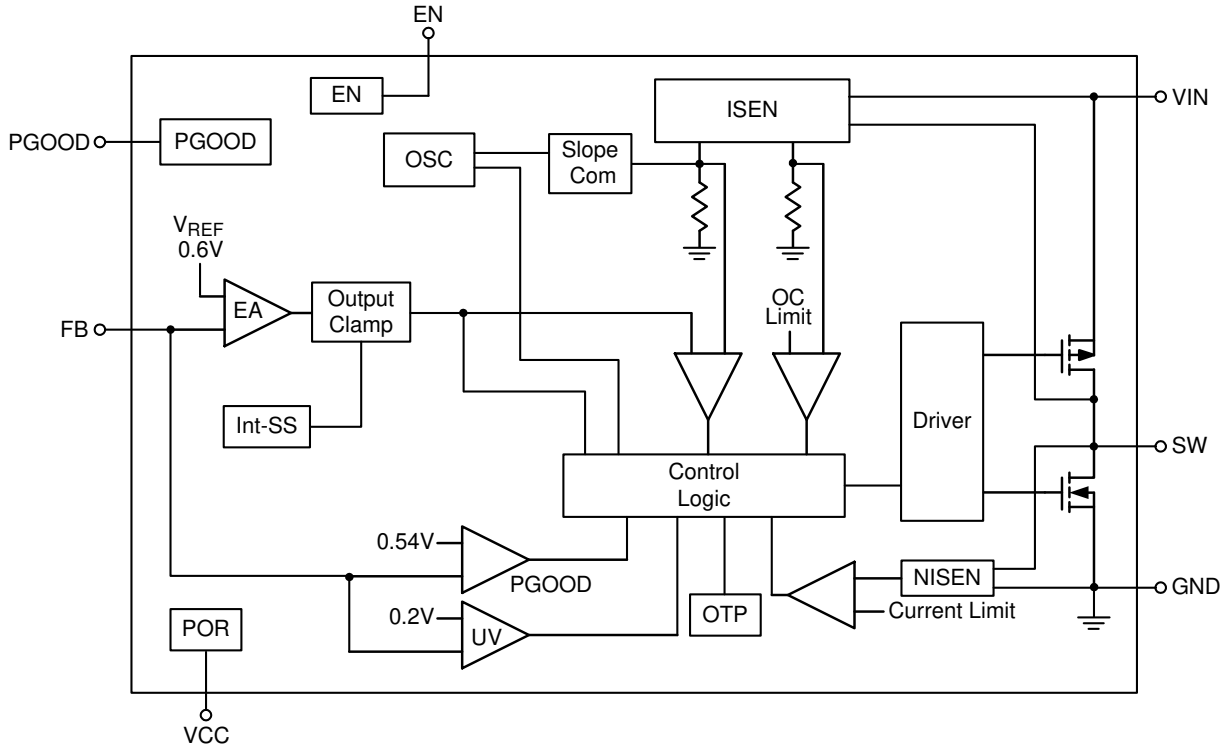


WDFN-10L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FB	Feedback Input. This pin receives the feedback voltage from a resistive voltage divider connected across the output.
2	VCC	Supply Voltage Input. Decouple this pin to GND with at least 1μF ceramic capacitor.
3	VIN	Power Input. Decouple this pin to GND with at least 10μF ceramic capacitor.
4, 5, 11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6, 7	SW	Switch Node. Connect this pin to the inductor.
8	NC	No Internal Connection.
9	PGOOD	Power Good Indicator. This pin is an open drain logic output. The PGOOD will be pulled to ground when the output voltage is less than 90% of the target output voltage.
10	EN	Enable Control Input. Pull high the EN pin to turn on the converter.

Function Block Diagram



Operation

The RT8071D is a synchronous low voltage Buck Converter that can support the input voltage range from 2.7V to 5.5V and the output current can be up to 3A. The RT8071D uses a constant frequency, current mode architecture. In normal operation, the high-side P-MOSFET is turned on when the Switch Controller is set by the oscillator (OSC) and is turned off when the current comparator resets the switch controller. High-side MOSFET peak current is measured by internal RSENSE. The Current Signal is where Slope Compensator works together with sensing voltage of RSENSE. The error amplifier EA adjusts COMP voltage by comparing the feedback signal (V_{FB}) from the output voltage with the internal 0.6V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, the COMP voltage then rises to allow higher inductor current to match the load current.

UV Comparator

If the feedback voltage (V_{FB}) is lower than threshold voltage 0.2V, the UV Comparator's output will go high and the Switch Controller will turn off the high-side MOSFET.

Oscillator (OSC)

The internal oscillator runs at nominal frequency 1MHz.

PGOOD Comparator

When the feedback voltage (V_{FB}) is higher than threshold voltage 0.54V, the PGOOD open drain output will be high impedance.

Enable

There is an internal pull down 500kΩ resistor at EN pin. When the EN pin is higher than 1.6V, the converter will be turned on. The EN pin can be connected to VIN through a 100kΩ resistor for automatic startup.

Soft-Start (SS)

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The V_{FB} voltage will track the internal ramp voltage during soft-start interval. The maximum soft-start time is 200μs.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN, VCC ---------- –0.3V to 6.5V
- SW to GND
  - DC ---------- –0.3V to 6.8V
  - < 20ns ---------- –2.5V to 9V
- Other Pins ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-10L 3x3 ---------- 1.429W
- Package Thermal Resistance (Note 2)
  - WDFN-10L 3x3, θ_{JA} ---------- 70°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 8.2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN, VCC ---------- 2.7V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Reference Voltage		V_{REF}		0.594	0.6	0.606	V
Feedback Leakage Current		I_{FB}		--	0.1	0.4	μA
DC Bias Current			Active , V_{FB} = 0.7V, Not Switching	--	110	170	μA
			Shutdown	--	--	1	
Output Voltage Line Regulation			V_{IN} = 2.7V to 5.5V, I_{OUT} = 0A	--	0.3	--	%/V
Output Voltage Load Regulation			I_{OUT} = 0A to 3A	–1	--	1	%
Switch Leakage Current				--	--	1	μA
Switching Frequency				0.8	1	1.2	MHz
Switch On Resistance	High-Side	$R_{DS(ON)\_P}$	V_{IN} = 5V	--	69	--	mΩ
	Low-Side	$R_{DS(ON)\_N}$	V_{IN} = 5V	--	49	--	
P-MOSFET Current Limit		I_{LIM}		4.8	--	--	A
Under-Voltage Lockout Threshold		V_{UVLO}	V_{CC} Rising	2.2	2.4	2.6	V
			V_{CC} Falling	2	2.2	2.4	
EN Input Voltage	Logic-High	V_{IH}		1.6	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
EN Pull Low Resistance				--	500	--	kΩ
Over Temperature Protection		T_{SD}		--	150	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Over-Temperature Protection Hysteresis			--	20	--	°C
Soft-Start Time	t_{SS}		--	--	200	μs
V_{OUT} Discharge Resistance			--	100	--	Ω
V_{OUT} Under-Voltage Protection (Latch-Off)			--	33	40	%
Power Good		Measures FB, With Respect to V_{REF}	85	90	--	%
Power Good Hysteresis			--	5	--	%

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

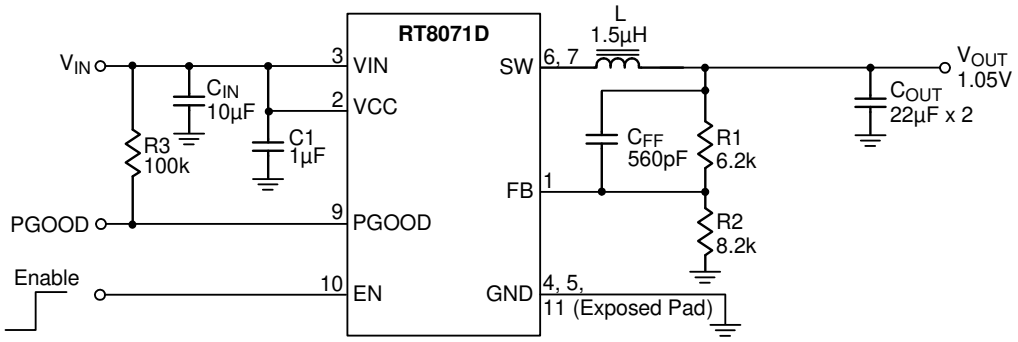
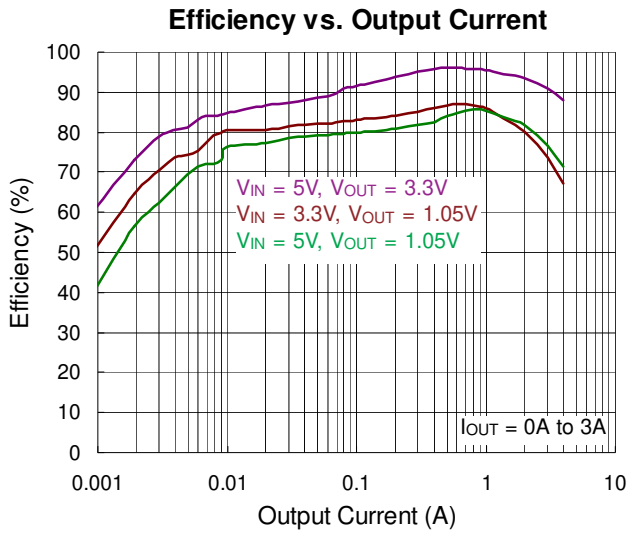
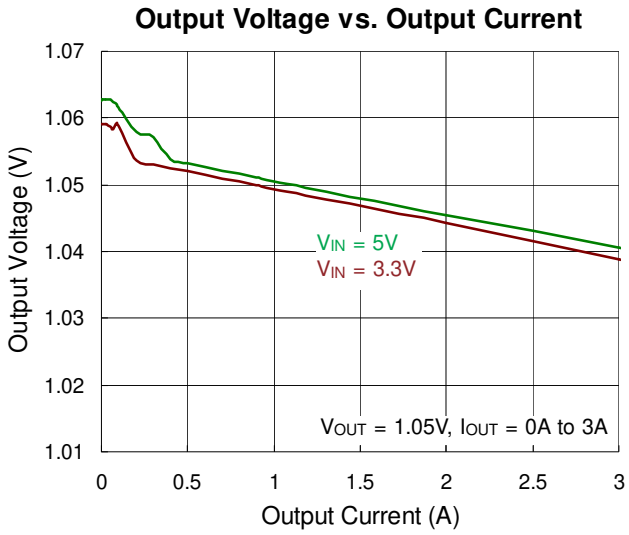


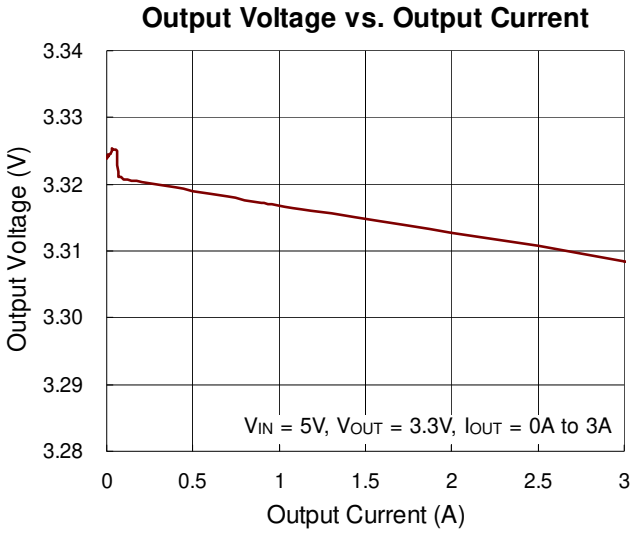
Table 1. Recommended Component Selection

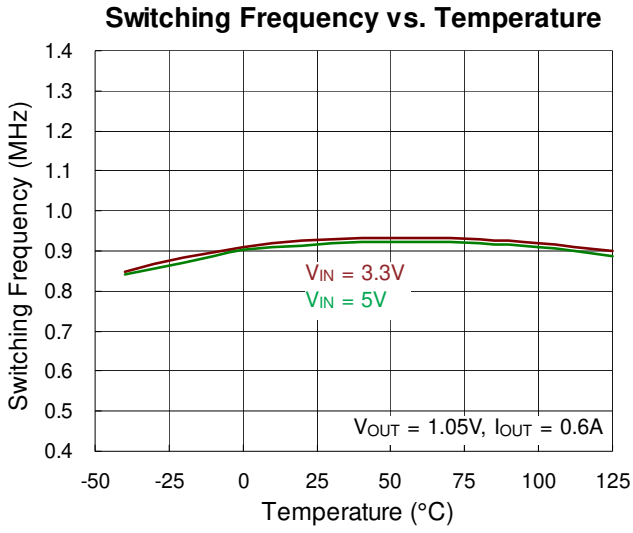
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{FF} (pF)	L (µH)	C_{OUT} (µF)
3.3	37	8.2	430	2	22 x 2
2.5	26	8.2	430	2	22 x 2
1.8	16.5	8.2	510	1.5	22 x 2
1.5	12.3	8.2	560	1.5	22 x 2
1.2	8.2	8.2	620	1.5	22 x 2
1	5.6	8.2	680	1.5	22 x 2

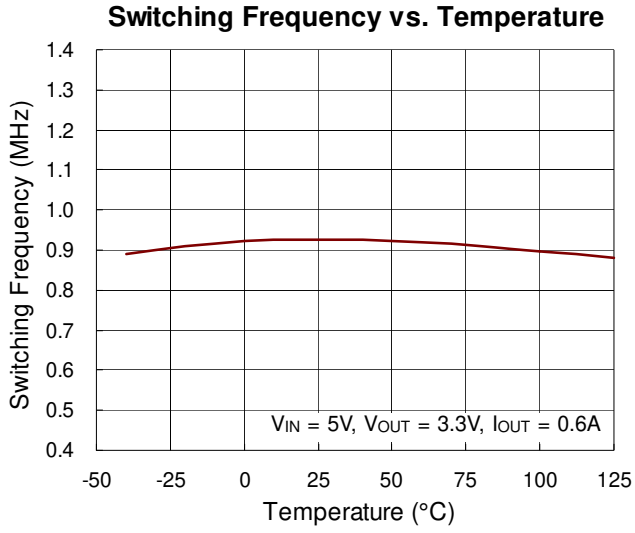
Typical Operating Characteristics

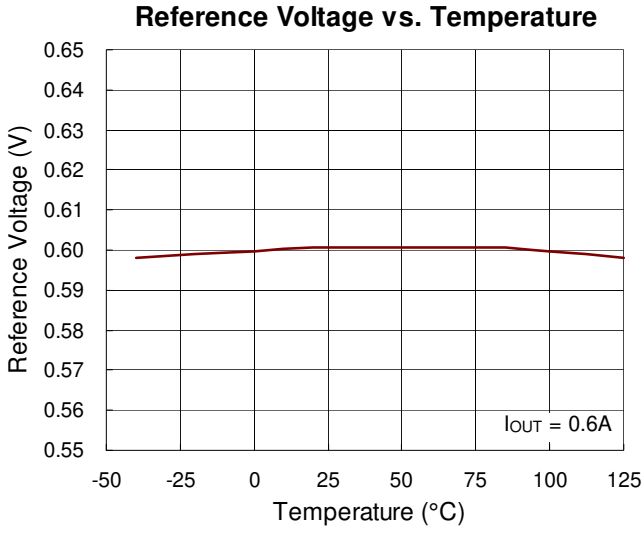




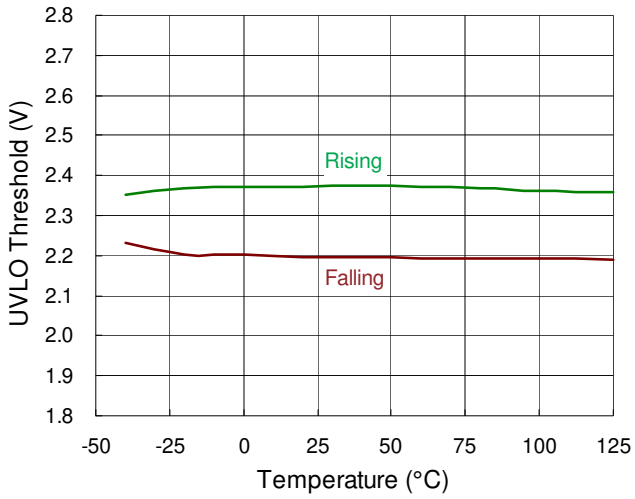




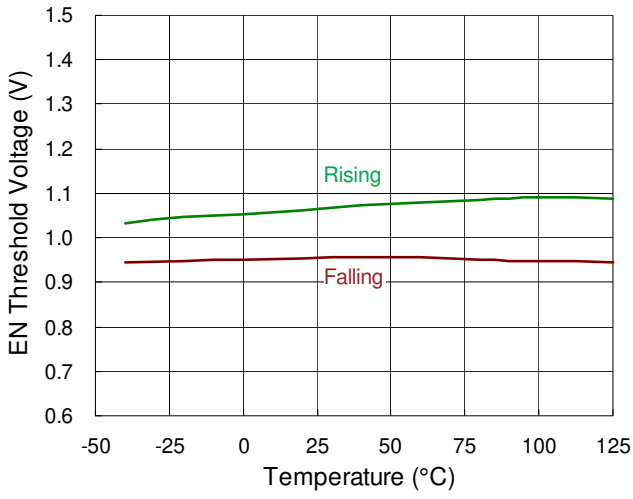




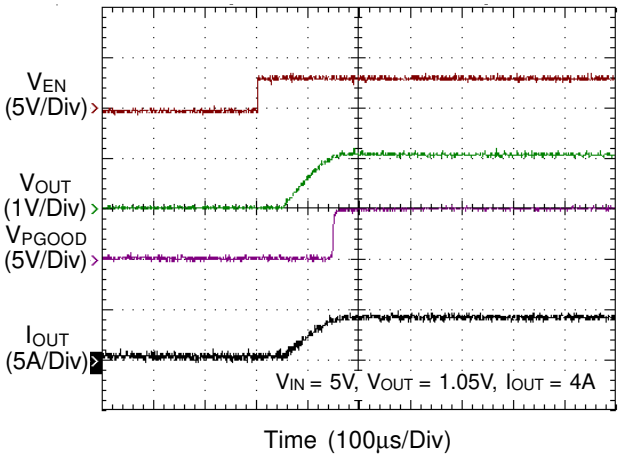
UVLO Threshold vs. Temperature



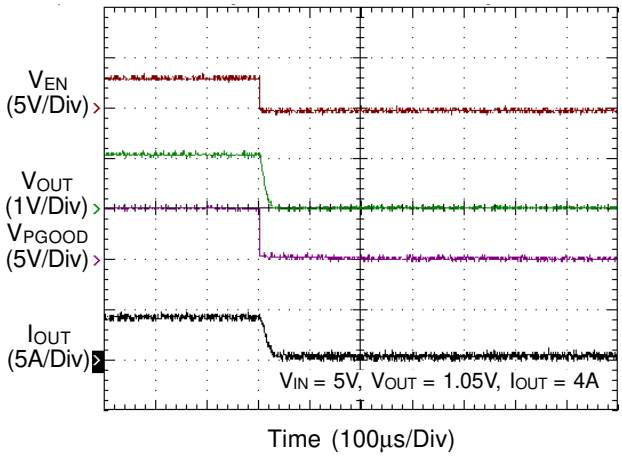
EN Threshold Voltage vs. Temperature



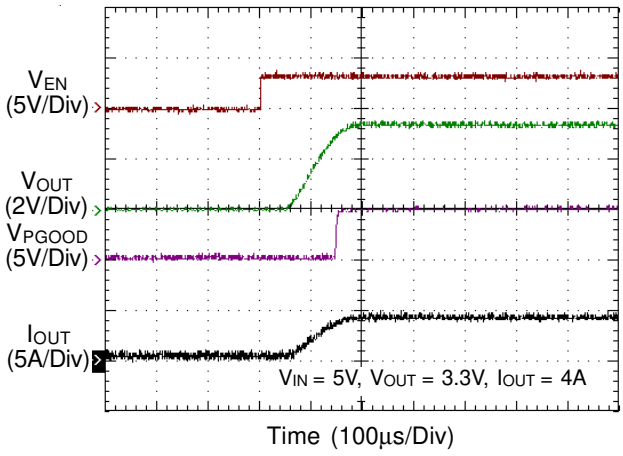
Power On from Enable Voltage



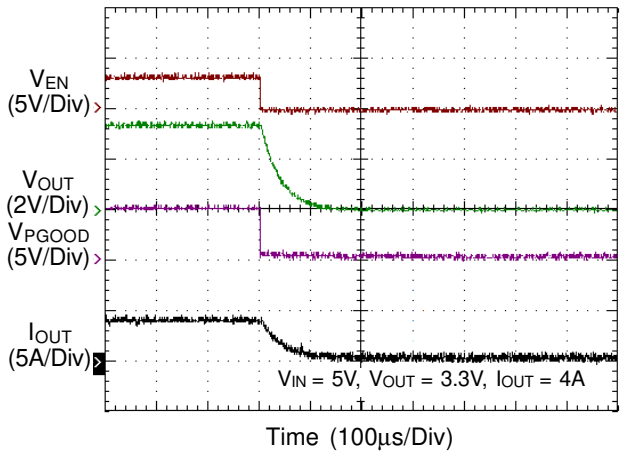
Power Off from Enable Voltage



Power On from Enable Voltage



Power Off from Enable Voltage



Application Information

The RT8071D is a single-phase step-down converter. It provides single feedback loop, current mode control with fast transient response. An internal 0.6V reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed switching frequency (1MHz) oscillator and internal compensation are integrated to minimize external component count. Protection features include over current protection, under voltage protection and over temperature protection.

Output Voltage Setting

Connect a resistive voltage divider at the FB between V_{OUT} and GND to adjust the output voltage. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is the feedback reference voltage 0.6V (typ.).

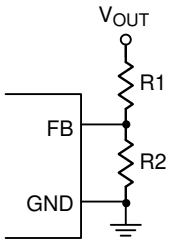


Figure 1. Setting V_{OUT} with a Voltage Divider

Chip Enable and Disable

The EN pin allows for power sequencing between the controller bias voltage and another voltage rail. The RT8071D remains in shutdown if the EN pin is lower than 400mV. When the EN pin rises above the V_{EN} trip point, the RT8071D begins a new initialization and soft-start cycle.

Internal Soft-Start

The RT8071D provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, the internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the voltage at the FB pin, causing PWM pulse width to increase slowly and in turn reduce the output surge current. The internal 0.6V reference takes over the loop control once the internal ramping-up voltage becomes higher than 0.6V.

UVLO Protection

The RT8071D has input Under-Voltage Lockout protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (2.4V typ.), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will stop switching. The UVLO rising and falling threshold voltage has a hysteresis to prevent noise-caused reset. The power sequence of the VCC and VIN need to be considered if they are powered separately. The driver voltage of high-side MOSET comes from VIN input and internal control circuit is powered by VCC. The VCC has to be powered earlier than the VIN to ensure that the high-side MOSFET has never turned on before the internal control circuit is ready. At power off, the voltage at the VIN has to be removed before the VCC goes below the threshold of UVLO.

Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times LIR \times I_{LOAD(MAX)} \times V_{IN}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current.

Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2} \times I_{LOAD(MAX)}\right)$$

The calculation above serves as a general reference. To further improve transient response, the output inductor can be further reduced. This relation should be considered along with the selection of the output capacitor.

Input Capacitor Selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 10μF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability.

Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{IN\_RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is selecting a proper capacitor for RMS current rating. One good design is using more than one capacitor with low equivalent series resistance (ESR) in parallel to form a capacitor bank.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{IN} \times f_{SW}}$$

Output Capacitor Selection

The output capacitor and the inductor form a low pass filter in the Buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in ripple voltage. The output voltage ripple (V_{P-P}) can be calculated by the following equation :

$$V_{P\_P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}}\right)$$

When load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage undershoot (V_{SAG}) can be calculated by the following equation :

$$V_{SAG} = \Delta I_{LOAD} \times ESR$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, the ESL contributes to part of the voltage sag. Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR.

Unlike the electrolytic capacitor, the ceramic capacitor has relatively low ESR and can reduce the voltage deviation during load transient. However, the ceramic capacitor can only provide low capacitance value. Therefore, use a mixed combination of electrolytic capacitor and ceramic capacitor to obtain better transient performance.

Power Good Output (PGOOD)

PGOOD is an open-drain type output and requires a pull-up resistor. PGOOD is actively held low in soft-start, standby, and shutdown. It is released when the output voltage rises above 90% of nominal regulation point. The PGOOD signal goes low if the output is turned off or is 10% below its nominal regulation point.

Under-Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage. When under voltage protection is enabled, both UGATE and LGATE gate drivers will be forced low if the output is less than 33% of its set voltage threshold. The UVP will be ignored for at least 3ms (typ.) after start up or a rising edge on the EN threshold. Toggle EN threshold or cycle V_{IN} to reset the UVP fault latch and restart the controller.

Over-Current Protection (OCP)

The RT8071D provides over-current protection by detecting high-side MOSFET peak inductor current. If the sensed peak inductor current is over the current limit threshold, the OCP will be triggered. When OCP is tripped, the RT8071D will keep the over current threshold level until the over current condition is removed.

Thermal Shutdown (OTP)

The device implements an internal thermal shutdown function when the junction temperature exceeds 150°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal shutdown threshold. Once the die temperature decreases below the hysteresis of 20°C, the device reinstates the power up sequence.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-10L 3x3 package, the thermal resistance, θ_{JA}, is 70°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.429W for WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance. The derating curve in Figure 2 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

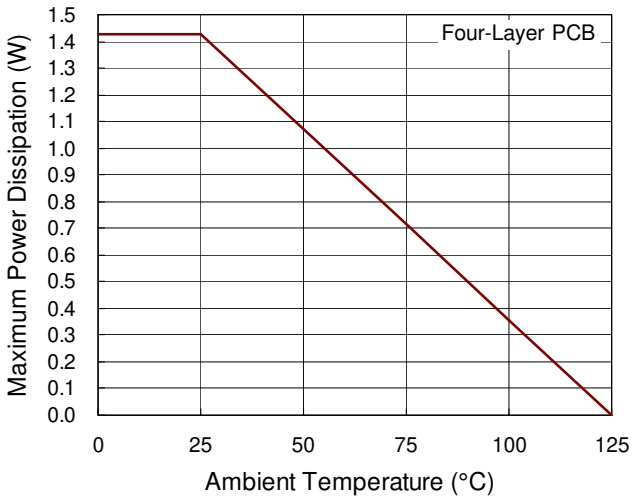


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout. Certain points must be considered before starting a layout using the RT8071D.

- Make the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (V_{IN} and GND).
- SW node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the SW node to prevent stray capacitive noise pick-up.
- Ensure all feedback network connections are short and direct. Place the feedback network as close to the chip as possible.
- The GND pin and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.
- An example of PCB layout guide is shown in Figure 3 for reference.

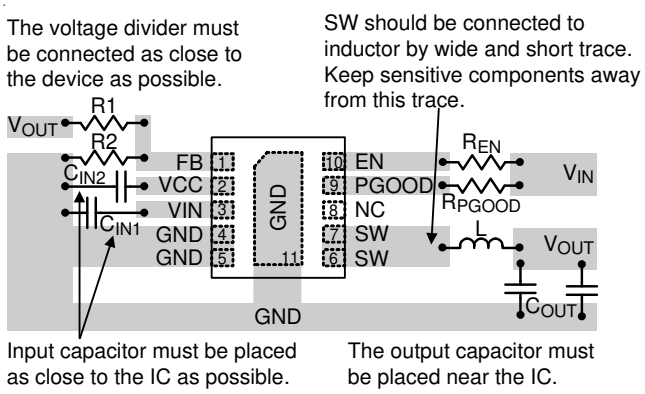
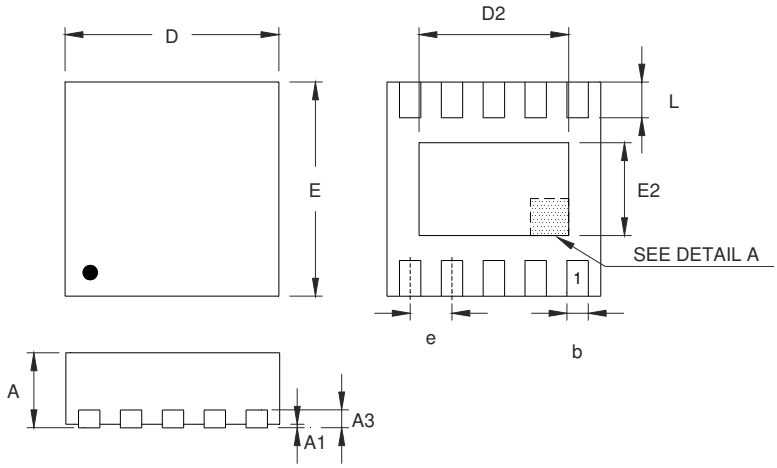
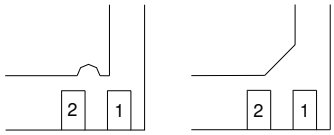


Figure 3. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

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