

# **FDB8878**

# N-Channel Logic Level PowerTrench<sup>®</sup> MOSFET 30V, 48A, $14m\Omega$

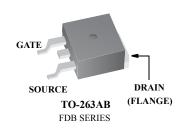
# **General Descriptions**

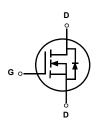
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(ON)}$  and fast switching speed.

# **Features**

- $r_{DS(ON)} = 14m\Omega$ ,  $V_{GS} = 10V$ ,  $I_D = 40A$
- $r_{DS(ON)} = 18m\Omega$ ,  $V_{GS} = 4.5V$ ,  $I_D = 36A$
- High performance trench technology for extremely low rds(ON)
- Low gate charge
- High power and current handling capability
- RoHS Compliant







# MOSFET Maximum Ratings TA = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units	
V <sub>DSS</sub>	Drain to Source Voltage		30	V	
V <sub>GS</sub>	Gate to Source Voltage		±20	V	
I <sub>D</sub>	Drain Current				
	Continuous ( $T_C = 25^{\circ}C$ , $V_{GS} = 10V$ )	48	Α		
	Continuous ( $T_C = 25^{\circ}C$ , $V_{GS} = 4.5V$ )		42	А	
	Pulsed	(Note 4)	170	Α	
E <sub>AS</sub>	Single Pulse Avalanche Energy (Note 1)	L = 1mH, I <sub>AS</sub> = 11A	60	mJ	
		$L = 0.03 \text{mH}, I_{AS} = 38 \text{A}$	21		
P <sub>D</sub>	Power dissipation		47.3	W	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature	-55 to 175	°C		

# **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2)	3.7	°C/W
R <sub>e,IA</sub>	Thermal Resistance, Junction to Ambient at 1000 seconds (Note 3)	43	°C/W

# **Package Marking and Ordering Information**

	Device Marking	Device	Package	Reel Size	Tape Width	Quantity
	FDB8878	FDB8878	TO-263	13"	24mm	800 units
1-						

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics				U.	L
B <sub>VDSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V	30	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temp. Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C		21		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 24V$ $V_{GS} = 0V$ $T_A = 150^{\circ}C$	-	-	1 250	μА
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20V	-	-	±100	nA
On Chara	cteristics			•		
V <sub>GS(TH)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1.2	1.7	2.5	V
$\frac{\Delta V_{GS(TH)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C		-5		mV/ºC
		I <sub>D</sub> = 40A, V <sub>GS</sub> = 10V	-	12	14	
r	Drain to Source On Posistance	$I_D = 36A, V_{GS} = 4.5V$	-	15	18	m()
r <sub>DS(ON)</sub>	Drain to Source On Resistance	I <sub>D</sub> = 40, V <sub>GS</sub> = 10V, T <sub>A</sub> = 175°C	-	19	21	mΩ
Dynamic	Characteristics					
C <sub>ISS</sub>	Input Capacitance	1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1	-	927	1235	pF
C <sub>OSS</sub>	Output Capacitance	→V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, → f = 1MHz	-	188	250	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance	- IMH2	-	117	175	pF
R <sub>G</sub>	Gate Resistance	f = 1MHz		3.0		Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS}$ = 0V to 10V $V_{DD}$ = 15V	-	17.1	23	nC
Q <sub>g(5)</sub>	Total Gate Charge at 5V	$V_{GS} = 0V \text{ to } 5V \mid I_D = 40A$	-	9.2	12	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	I <sub>g</sub> = 1.0mA	-	2.6	-	nC
Q <sub>gs2</sub>	Gate Charge Threshold to Plateau	7	-	1.7	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		-	3.7	-	nC
Switching	Characteristics (V <sub>GS</sub> = 10V)					
t <sub>ON</sub>	Turn-On Time		-	255	383	ns
t <sub>d(ON)</sub>	Turn-On Delay Time	7	-	11.1		ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 15V, I <sub>D</sub> = 40A	-	244		ns
t <sub>d(OFF)</sub>	Turn-Off Delay Time	$V_{GS} = 10V, R_{GS} = 16\Omega$	-	14.8		ns
t <sub>f</sub>	Fall Time	7	-	35.3		ns
t <sub>OFF</sub>	Turn-Off Time		-	50	75	ns
Drain-Soເ	urce Diode Characteristics					
V	Source to Drain Diode Voltage	I <sub>SD</sub> = 40A	-	1.1	1.25	V
$V_{SD}$	Source to Drain Diode voltage	I <sub>SD</sub> = 3.2A	-	0.85	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	$I_{SD} = 40A, dI_{SD}/dt = 100A/\mu s$	-	14.4	18.8	ns
Q <sub>RR</sub>	Reverse Recovered Charge	I <sub>SD</sub> = 40A, dI <sub>SD</sub> /dt=100A/μs	-	5.1	6.7	nC

Notes:
 Starting T<sub>J</sub> = 25°C, V<sub>DD</sub> = 30V, V<sub>GS</sub> = 10V
 R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θJA</sub> is determined by the user's board design.
 R<sub>θJA</sub> is measured with 1.0 in² copper on FR-4 board
 Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%</li>



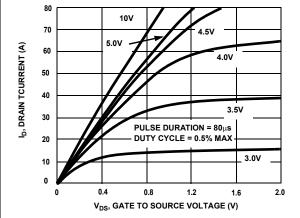


Figure 1. On Region Characteristics

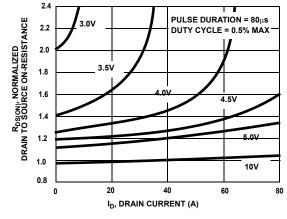


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

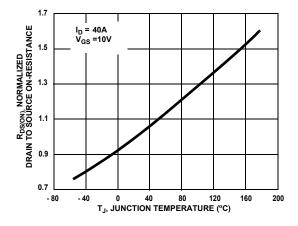


Figure 3. On Resistance Variation with Temperature

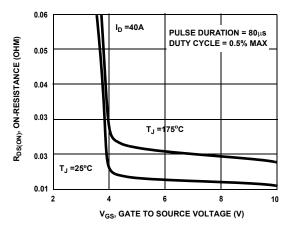


Figure 4. On-Resistance Variation with Gate-to-Source Votlage

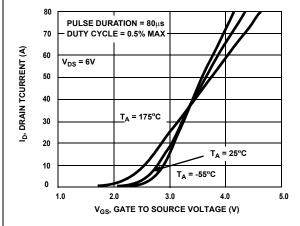


Figure 5. Transfer Characteristics

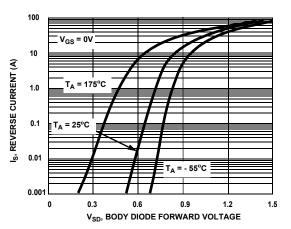


Figure 6. Body Diode Forward Voltage Variation With Source Current and Temperature

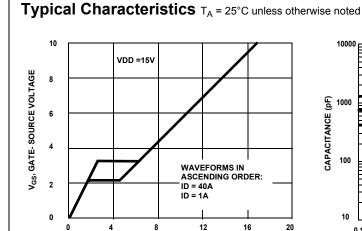


Figure 7. Gate Charge Characteristics

Q<sub>q</sub>, GATE CHARGE (nC)

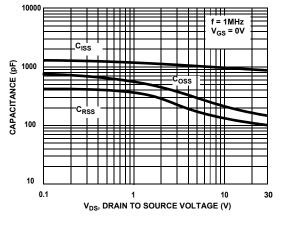


Figure 8. Capacitance Characteristics

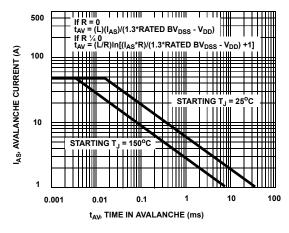


Figure 9. Unclamped Inductive Switching Capability

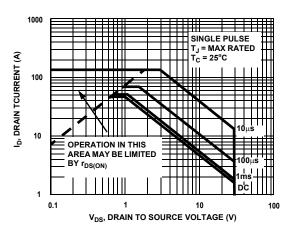


Figure 10. Safe Operating Area

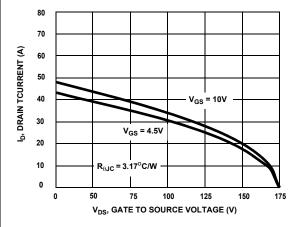


Figure 11. Maximum Continuous Drain Current vs Case Temperature

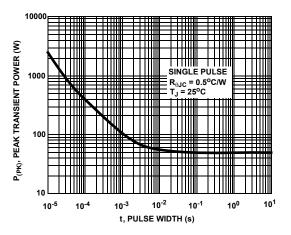


Figure 12. Single Pulse Maximum Power Dissipation

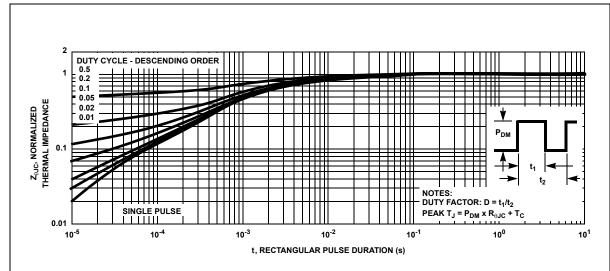


Figure 13. Transient Thermal Response Curve

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