ADS850-EVM

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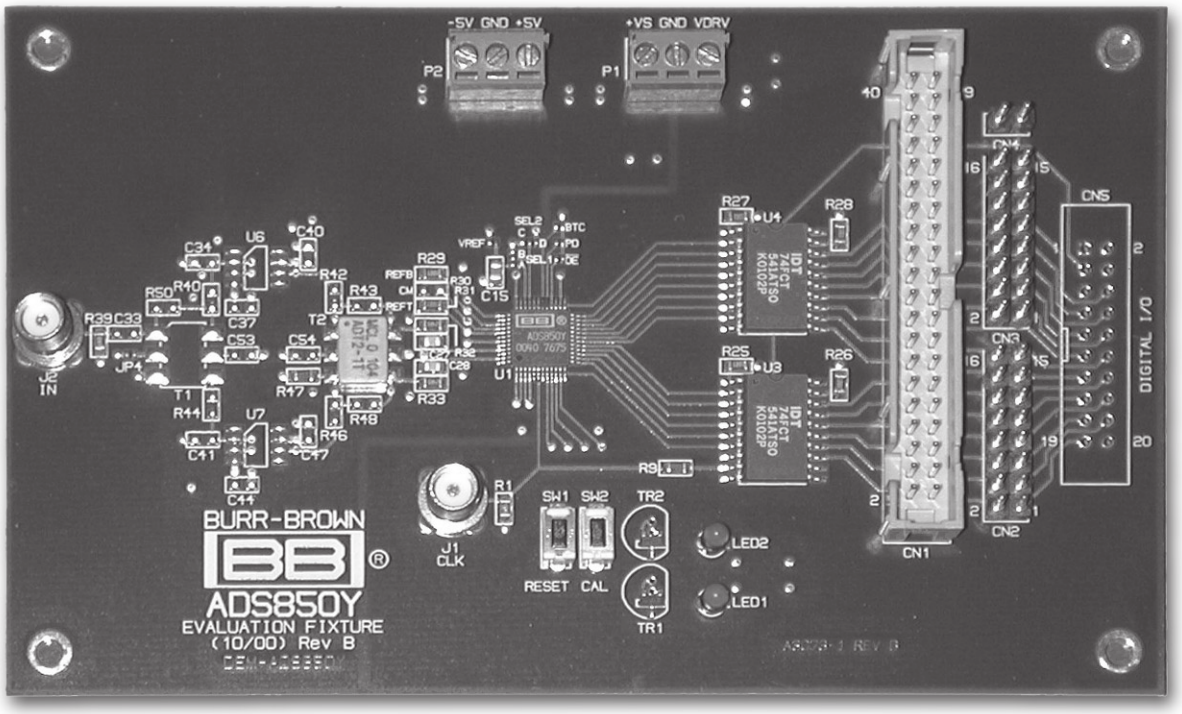

FEATURES

- **PROVIDES FAST AND EASY PERFORMANCE TESTING FOR THE ADS850Y**
- **SINGLE-ENDED DC COUPLED INPUT**
- **SELECTABLE EXTERNAL OR INTERNAL REFERENCE OPERATION**
- **OPTIONAL INPUT FILTER CIRCUIT**

DESCRIPTION

The ADS850-EVM is designed for ease of use when evaluating the ADS850Y high-speed Analog-to-Digital Converter (ADC). The ADS850Y offers 14 bits of resolution at sampling rates of up to 10MHz. The evaluation module offers the user the ability to populate and utilize an active filter circuit at the input of the ADS850Y to help with signal acquisition. The data outputs from the ADS850Y converter are isolated from the output connector by CMOS octal buffers.

INITIAL CONFIGURATION

The ADS850-EVM is designed to apply a differential signal to the ADC by utilizing a single-ended input coupled through a transformer. The input range of the ADC, which is set by the value of the reference and the SEL pin, can then be configured by placing the proper solder switches between JP5, JP6, and JP7. Table I shows the connections needed for the different input ranges.

INPUT RANGE	SEL	VREF	JUMPER CONNECTIONS
2V	V_{REF}	SEL	JP6-A
4V	GND	NC	JP6-B

TABLE I. Jumper Connections.

POWER SUPPLY

The evaluation module requires +5V and –5V power-supply voltages. Two separate power connectors are on the board. Connector P2, labeled with –5V, GND, and +5V, is the analog front-end supply connection. Connector P1, labeled with VDRV, GND, and +5V, is the converter supply connection. The VDRV connector is tied to pin 26 of the ADS850Y. Adjusting the voltage on this pin between +3V and +5V will vary the data-output voltage levels. If the optional analog front-end circuit is not used, there is no need for any connections to be made to P2.

SIGNAL INPUT CONFIGURATION

The standard configuration to the ADS850-EVM utilizes a transformer to change the single-ended input applied to J2, to a differential input into the ADS850Y. There are provisions on the board for a different type of input circuit. The schematic shows the optional circuit, however, the board must be populated in order to utilize the circuit. More information on the circuit can be found in the OPA687 data sheet (SBOS065). Only R39, R47, and T2 of the input circuitry are populated on the ADS850-EVM; all other components must be provided by the end user.

CLOCK INPUT

The ADS850-EVM evaluation board requires an external clock applied to connector J1. This input represents a 50Ω impedance to the clock source. In order to preserve the specified performance of the ADS850Y converter, the clock should contain very low jitter. This is particularly important if the device will be used in the evaluation of an undersampled system. It should also be noted that the clock signal should have rise and fall times no faster than 2ns.

RESET AND CALIBRATION

The ADS850-EVM evaluation fixture is provided with RESET and CALIBRATION push buttons. When the RESET is activated, the memory of the ADS850Y will be cleared. Adequate time must be given to collect and transmit valid data due to the data latency inherent to the ADS850Y.

When the CALIBRATION push-button is pressed, the ADS850Y will enter the calibration mode. LED2 will be active to show that the device is in the calibration process. Refer to the ADS850 data sheet (SBAS154) for further explanation on the calibration sequence.

OVER RANGE INDICATOR

The OVR indicator is used to show when the input to the ADS850Y is over the set input range. LED1 will become active when this happens. Refer to the ADS850 data sheet (SBAS154) for a further explanation on the OVR indicator.

DATA OUTPUT

The data output is provided at CMOS logic levels. The ADS850Y uses Straight Offset Binary coding. The option of Binary Two's Compliment is available by connecting the solder switch located at JP4. The data outputs of the converter are buffered from the data bus by CMOS octal buffers.

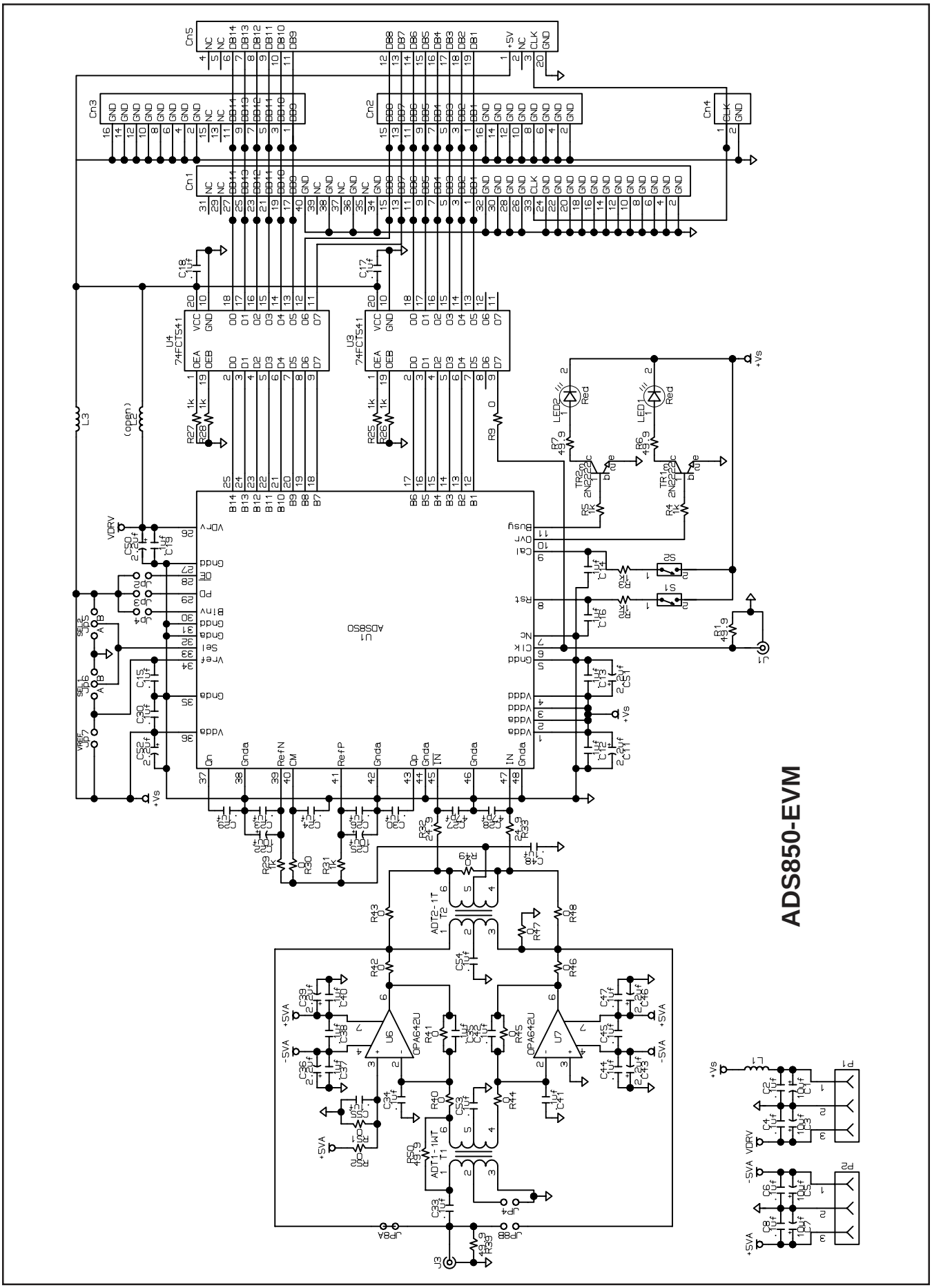

FIGURE 1. ADS850-EVM Schematic.

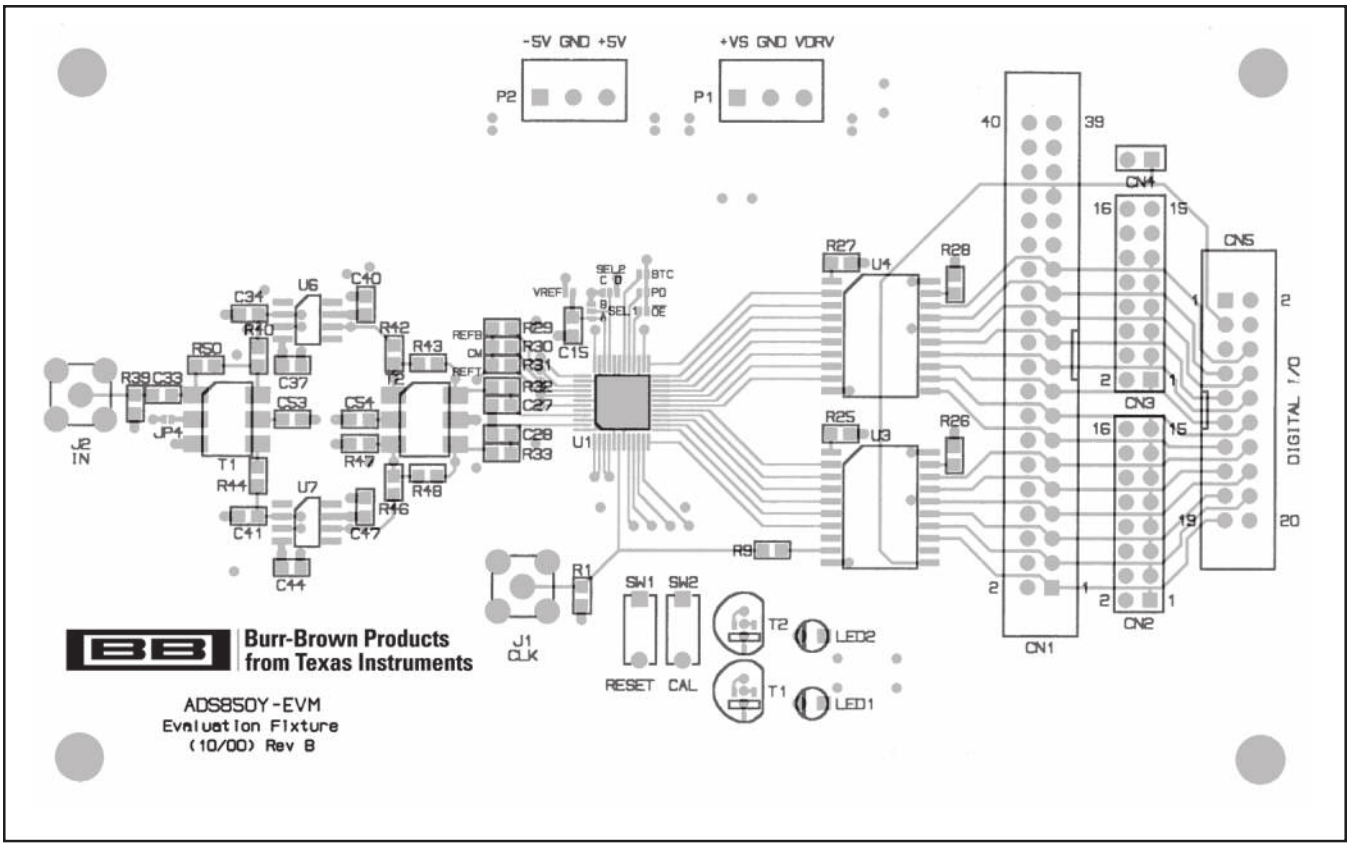

FIGURE 2. Top Layer with Silkscreen.

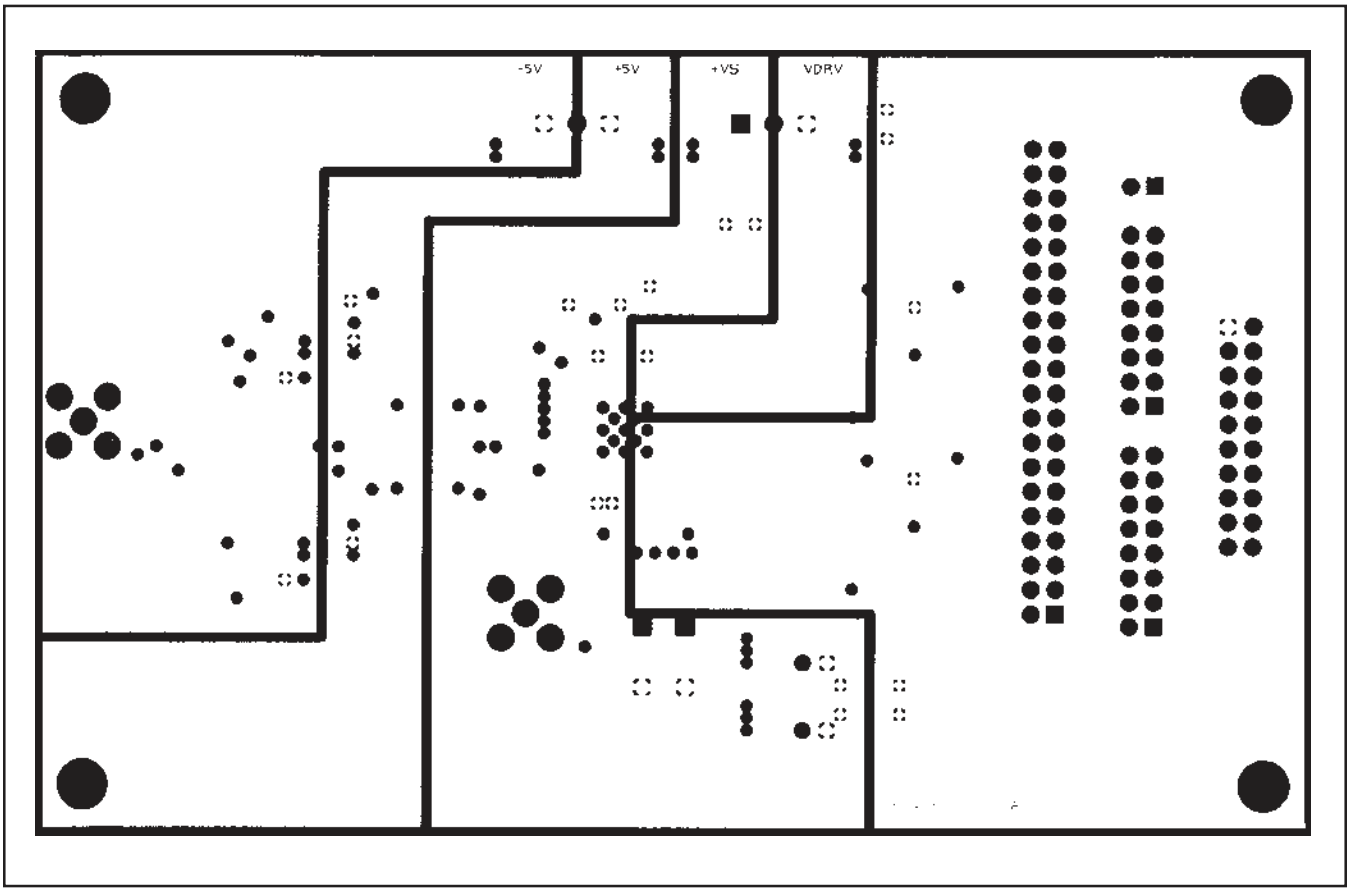

FIGURE 3. Power Plane.

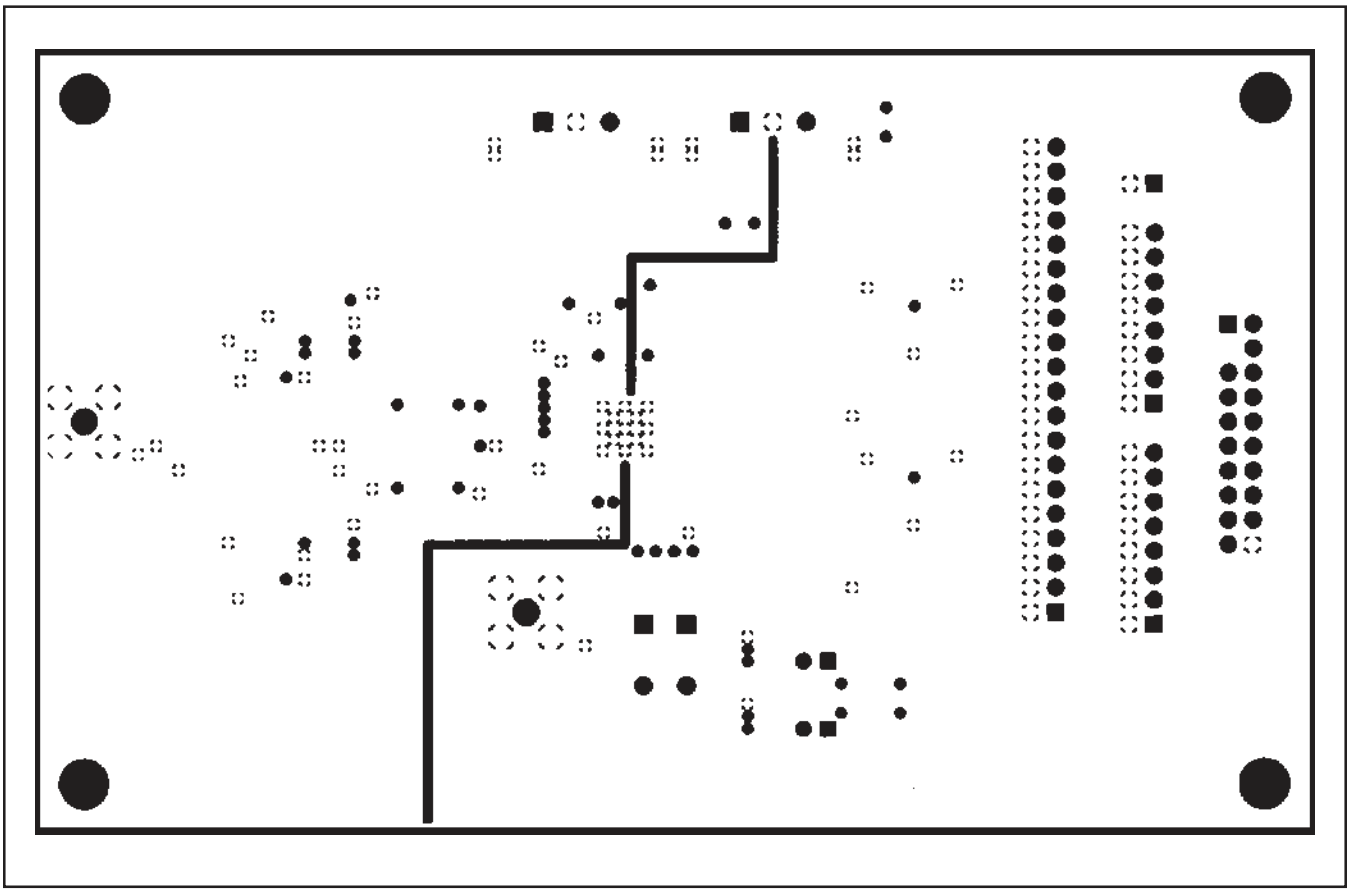

FIGURE 4. Ground Plane

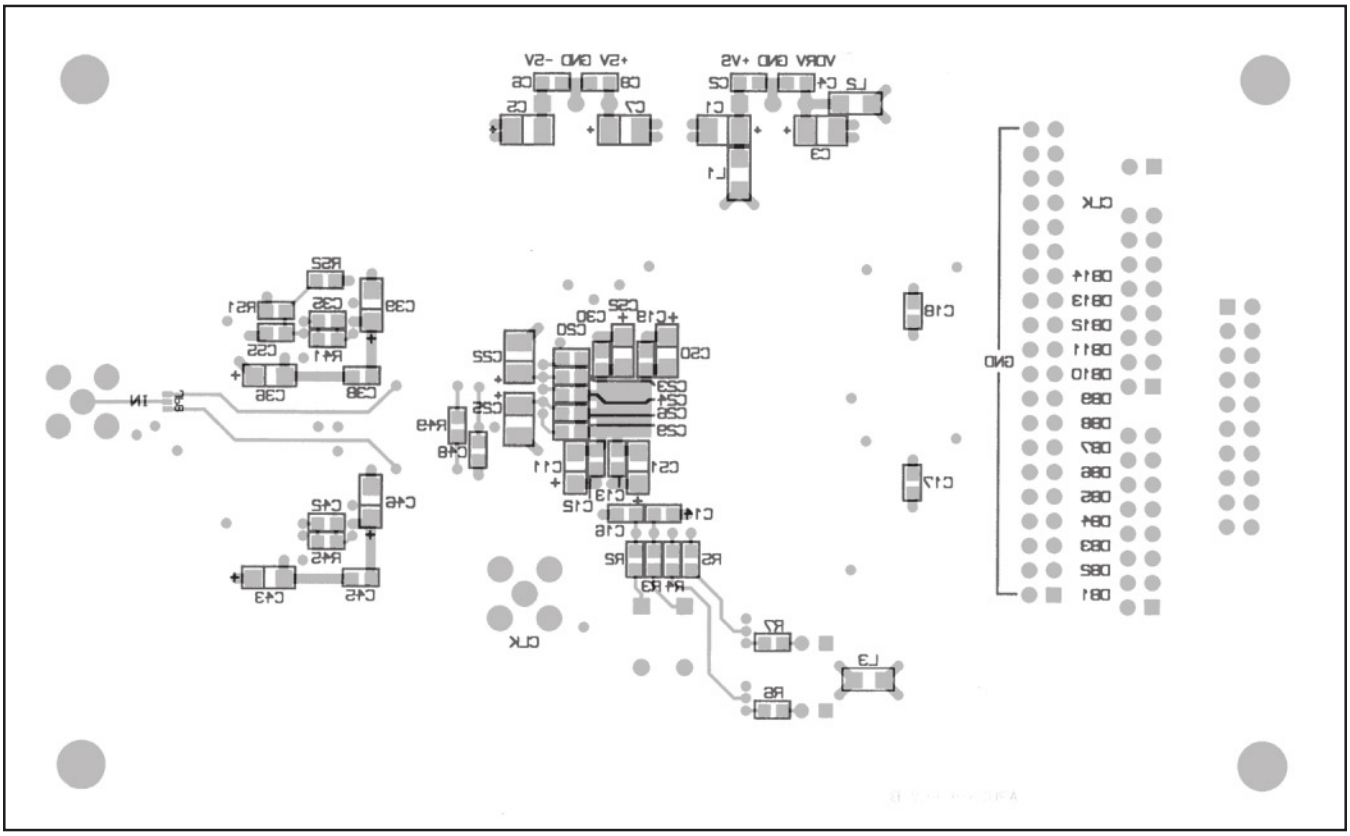

FIGURE5. Bottom Layer with Silkscreen.

COMPONENT LIST

REFERENCE	QTY	COMPONENT (P/N)	DESCRIPTION	MANUFACTURER
U1	1	ADS850Y	14-Bit 10MSPS ADC SE/Diff Input, Int/Ext Ref. Self Cal	Texas Instruments
U3, U4	2	IDT74FCT541ATSO	Fast CMOS Octal Buffer/Line Driver	IDT
T2	1	ADT2-1T	Transformer, 2Ω Wideband RF	Mini-Circuits
R1, R6, R7, R39	4	CRCW080549R9F	49.9Ω, MF0805 Chip Resistor, 1%	Dale
R9, R47	2	CRCW08050R0F	0Ω, MF0805 Chip Resistor, 1%	Dale
R2-R5, R25-28, R29, R31	10	CRCW08051001F	1kΩ, MF0805 Chip Resistor, 1%	Dale
R32, R33	2	CRCW080524R9F	24.9Ω, MF0805 Chip Resistor, 1%	Dale
C1, C3, C5, C7, C22, C25	6	293D106x9010A2T	10.0µF, 10V, 10% Tantalum Capacitor	Sprague
C2, C4, C6, C8, C12-C20, C23, C24, C26, C29, C30, C48	19	C0805C104K050AS	0.1µF, 50V, X7R 0805 Ceramic Capacitor	Kemet
C11, C50-C52	4	T491A225K010AS	2.2µF, 10V, Size A Tantalum Capacitor	Kemet
C27, C28	2	C0805C470J1GAC	47pF, 100V, 0805 Ceramic Capacitor	Kemet
SW1, SW2	2	P8058S-ND	Switch Lt Tuch 6X3.5 160GF	Digi-Key
TR1, TR2	2	MMBT2222ADICT-ND	SMD Transistor NPN 40V, 350mW SOT-23	Digi-Key
LED1, LED2	2	HLMP 1600	LED	HP
L1, L3	2	LI1206B900R	90Ω at 100MHz Chip Inductor	Steward
P1, P2	2	ED1515-ND	Terminal Block 3Pos 3.5mm Straight	Digi-Key
CN1	1	3595-6002	3m Straight 40-Pin Header	3M
CN2, CN3, CN4		TS-132-G-A-2	Terminal Strip-1 Row, 32-Pin, Gold	Samtec
J1, J2	2	142-0701-201	SMA PCB Connector, Straight	EF Johnson
Feet	4	1-SJ5003-0-N	Rubber Feet, Black, 0.44x0.2	Digi-Key
Board	1	A3073	Evaluation Fixture, ADS850-EVM rev B	Texas Instruments

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