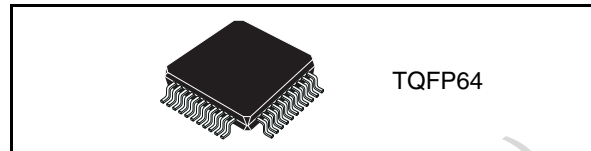


## Multi-channel digital audio processor with DDX™

### Features

- 8 channels of 24-bit DDX®
- >100 dB SNR and dynamic range
- Selectable 32 kHz - 192 kHz input sample rates
- 6 channels of DSD/SACD input
- Digital gain/attenuation +58 dB to -100 dB in 0.5 dB steps
- Soft volume update
- Individual channel and master gain/attenuation plus channel trim (-10 dB to +10 dB)
- Up to 10 independent 32-bit user programmable biquads (EQ) per channel
- Bass/treble tone control
- Pre and post EQ full 8-channel input mix on all 8 channels
- Dual independent limiters/compressors
- Dynamic range compression or anti-clipping modes
- AutoModes:
  - 5-band graphic EQ
  - 32 preset EQ curves (rock, jazz, pop, etc.)
  - Automatic volume controlled loudness
  - 5.1 to 2-channel downmix
  - Simultaneous 5.1- and 2-channel downmix outputs
  - 3 preset volume curves
  - 2 preset anti-clipping modes
  - Preset movie nighttime listening mode
  - Preset TV channel/commercial AGC mode
  - 5.1, 2.1 bass management configurations
  - AM frequency automatic output PWM frequency shifting
  - 8 preset crossover filters
- Individual channel and master soft/hard mute
- Automatic zero-detect and invalid input mute
- Automatic invalid input detect mute



- Advanced PopFree operation
- Advanced AM interference frequency switching and noise suppression modes
- I<sup>2</sup>S output channel mapping function
- Independent channel volume and DSP bypass
- Channel mapping of any input to any processing/DDX® channel
- DC blocking selectable high-pass filter
- Selectable per-channel DDX® damped ternary or binary PWM output
- Max power correction for lower full-power THD
- Variable per channel DDX® output delay control
- 192 kHz internal processing sample rate, 24-bit to 36-bit precision

### Description

The STA308A is a single chip solution for digital audio processing and control in multi-channel applications. It provides output capabilities for DDX® (direct digital amplification). In conjunction with a DDX® power device, it provides high-quality, high-efficiency, all digital amplification. The device is extremely versatile, allowing for input of most digital formats including 6.1/7.1-channel and 192 kHz, 24-bit DVD-audio, DSD/SACD. In 5.1 application the additional 2 channels can be used for audio line-out or headphone drive. In speaker mode, with 8 channel outputs in parallel, the STA308A can deliver 1 W (maximum).

**Table 1. Device summary**

| Order code | Package |
|------------|---------|
| STA308A    | TQFP64  |

# Contents

|          |                                                               |           |
|----------|---------------------------------------------------------------|-----------|
| <b>1</b> | <b>Block diagram</b> .....                                    | <b>8</b>  |
| <b>2</b> | <b>Pin connections</b> .....                                  | <b>9</b>  |
| <b>3</b> | <b>Electrical specification</b> .....                         | <b>12</b> |
| 3.1      | Absolute maximum ratings .....                                | 12        |
| 3.2      | Thermal data .....                                            | 12        |
| 3.3      | Recommended operating condition .....                         | 12        |
| 3.4      | Electrical specifications .....                               | 13        |
| <b>4</b> | <b>Pin description</b> .....                                  | <b>14</b> |
| <b>5</b> | <b>I<sup>2</sup>C bus operation</b> .....                     | <b>15</b> |
| 5.1      | Communication protocol .....                                  | 15        |
| 5.1.1    | Data transition or change .....                               | 15        |
| 5.1.2    | Start condition .....                                         | 15        |
| 5.1.3    | Stop condition .....                                          | 15        |
| 5.1.4    | Data input .....                                              | 15        |
| 5.2      | Device addressing .....                                       | 15        |
| 5.3      | Write operation .....                                         | 16        |
| 5.3.1    | Byte write .....                                              | 16        |
| 5.3.2    | Multi-byte write .....                                        | 16        |
| <b>6</b> | <b>Application reference schematic</b> .....                  | <b>17</b> |
| <b>7</b> | <b>Registers</b> .....                                        | <b>18</b> |
| 7.1      | Register summary .....                                        | 18        |
| 7.2      | Register description .....                                    | 21        |
| 7.2.1    | Configuration register A (0x00) .....                         | 21        |
| 7.2.2    | Configuration register B (0x01) - serial input formats .....  | 23        |
| 7.2.3    | Configuration register C (0x02) - serial output formats ..... | 25        |
| 7.2.4    | Configuration register D (0x03) .....                         | 26        |
| 7.2.5    | Configuration register E (0x04) .....                         | 27        |
| 7.2.6    | Configuration register F (0x05) .....                         | 27        |

|        |                                                            |    |
|--------|------------------------------------------------------------|----|
| 7.2.7  | Configuration register G (0x06)                            | 29 |
| 7.2.8  | Configuration register H (0x07)                            | 30 |
| 7.2.9  | Configuration register I (0x08)                            | 31 |
| 7.2.10 | Master mute register (0x09)                                | 32 |
| 7.2.11 | Master volume register (0x0A)                              | 32 |
| 7.2.12 | Channel 1 volume (0x0B)                                    | 32 |
| 7.2.13 | Channel 2 volume (0x0C)                                    | 32 |
| 7.2.14 | Channel 3 volume (0x0D)                                    | 32 |
| 7.2.15 | Channel 4 volume (0x0E)                                    | 32 |
| 7.2.16 | Channel 5 volume (0x0F)                                    | 33 |
| 7.2.17 | Channel 6 volume (0x10)                                    | 33 |
| 7.2.18 | Channel 7 volume (0x11)                                    | 33 |
| 7.2.19 | Channel 8 volume (0x12)                                    | 33 |
| 7.2.20 | Channel 1 volume trim, mute, bypass (0x13)                 | 33 |
| 7.2.21 | Channel 2 volume trim, mute, bypass (0x14)                 | 33 |
| 7.2.22 | Channel 3 volume trim, mute, bypass (0x15)                 | 33 |
| 7.2.23 | Channel 4 volume trim, mute, bypass (0x16)                 | 34 |
| 7.2.24 | Channel 5 volume trim, mute, bypass (0x17)                 | 34 |
| 7.2.25 | Channel 6 volume trim, mute, bypass (0x18)                 | 34 |
| 7.2.26 | Channel 7 volume trim, mute, bypass (0x19)                 | 34 |
| 7.2.27 | Channel 8 volume trim, mute, bypass (0x1A)                 | 34 |
| 7.2.28 | Channel input mapping channels 1 and 2 (0x1B)              | 36 |
| 7.2.29 | Channel input mapping channels 3 and 4 (0x1C)              | 36 |
| 7.2.30 | Channel input mapping channels 5 and 6 (0x1D)              | 36 |
| 7.2.31 | Channel input mapping channels 7 and 8 (0x1E)              | 36 |
| 7.2.32 | AUTO1 - AutoModes EQ, volume, GC (0x1F)                    | 37 |
| 7.2.33 | AUTO2 - AutoModes bass management2 (0x20)                  | 38 |
| 7.2.34 | AUTO3 - AutoMode AM/pre-Scale/bass management scale (0x21) | 39 |
| 7.2.35 | PREEQ - Preset EQ settings (0x22)                          | 40 |
| 7.2.36 | AGEQ - graphic EQ 80-Hz band (0x23)                        | 41 |
| 7.2.37 | BGEQ - graphic EQ 300-Hz band (0x24)                       | 41 |
| 7.2.38 | CGEQ - graphic EQ 1-kHz band (0x25)                        | 41 |
| 7.2.39 | DGEQ - graphic EQ 3-kHz band (0x26)                        | 41 |
| 7.2.40 | EGEQ - graphic EQ 8-kHz band (0x27)                        | 42 |
| 7.2.41 | Biquad internal channel loop-through (0x28)                | 42 |
| 7.2.42 | Mix internal channel loop-through (0x29)                   | 43 |
| 7.2.43 | EQ bypass (0x2A)                                           | 43 |

|        |                                                                           |    |
|--------|---------------------------------------------------------------------------|----|
| 7.2.44 | Tone control bypass (0x2B) . . . . .                                      | 43 |
| 7.2.45 | Tone control (0x2C) . . . . .                                             | 44 |
| 7.2.46 | Channel limiter select channels 1,2,3,4 (0x2D) . . . . .                  | 44 |
| 7.2.47 | Channel limiter select channels 5,6,7,8 (0x2E) . . . . .                  | 44 |
| 7.2.48 | Limiter 1 attack/release rate (0x2F) . . . . .                            | 44 |
| 7.2.49 | Limiter 1 attack/release threshold (0x30) . . . . .                       | 45 |
| 7.2.50 | Limiter 2 attack/release rate (0x31) . . . . .                            | 45 |
| 7.2.51 | Limiter 2 attack/release threshold (0x32) . . . . .                       | 45 |
| 7.2.52 | Bit description . . . . .                                                 | 45 |
| 7.2.53 | Channel 1 and 2 output timing (0x33) . . . . .                            | 49 |
| 7.2.54 | Channel 3 and 4 output timing (0x34) . . . . .                            | 49 |
| 7.2.55 | Channel 5 and 6 output timing (0x35) . . . . .                            | 49 |
| 7.2.56 | Channel 7 and 8 output timing (0x36) . . . . .                            | 50 |
| 7.2.57 | Channel I <sup>2</sup> S output mapping channels 1 and 2 (0x37) . . . . . | 50 |
| 7.2.58 | Channel I <sup>2</sup> S output mapping channels 3 and 4 (0x38) . . . . . | 50 |
| 7.2.59 | Channel I <sup>2</sup> S output mapping channels 5 and 6 (0x39) . . . . . | 50 |
| 7.2.60 | Channel I <sup>2</sup> S output mapping channels 7 and 8 (0x3A) . . . . . | 51 |
| 7.2.61 | Coefficient address register 1 (0x3B) . . . . .                           | 51 |
| 7.2.62 | Coefficient address register 2 (0x3C) . . . . .                           | 51 |
| 7.2.63 | Coefficient b1 data register, bits 23:16 (0x3D) . . . . .                 | 51 |
| 7.2.64 | Coefficient b1 data register, bits 15:8 (0x3E) . . . . .                  | 52 |
| 7.2.65 | Coefficient b1 data register, bits 7:0 (0x3F) . . . . .                   | 52 |
| 7.2.66 | Coefficient b2 data register, bits 23:16 (0x40) . . . . .                 | 52 |
| 7.2.67 | Coefficient b2 data register, bits 15:8 (0x41) . . . . .                  | 52 |
| 7.2.68 | Coefficient b2 data register, bits 7:0 (0x42) . . . . .                   | 52 |
| 7.2.69 | Coefficient a1 data register, bits 23:16 (0x43) . . . . .                 | 52 |
| 7.2.70 | Coefficient a1 data register, bits 15:8 (0x44) . . . . .                  | 52 |
| 7.2.71 | Coefficient a1 data register, bits 7:0 (0x45) . . . . .                   | 53 |
| 7.2.72 | Coefficient a2 data register, bits 23:16 (0x46) . . . . .                 | 53 |
| 7.2.73 | Coefficient a2 data register, bits 15:8 (0x47) . . . . .                  | 53 |
| 7.2.74 | Coefficient a2 data register, bits 7:0 (0x48) . . . . .                   | 53 |
| 7.2.75 | Coefficient b0 data register, bits 23:16 (0x49) . . . . .                 | 53 |
| 7.2.76 | Coefficient b0 data register, bits 15:8 (0x4A) . . . . .                  | 53 |
| 7.2.77 | Coefficient b0 data register, bits 7:0 (0x4B) . . . . .                   | 53 |
| 7.2.78 | Coefficient write control register (0x4C) . . . . .                       | 54 |
| 7.3    | Reading a coefficient from RAM . . . . .                                  | 54 |
| 7.4    | Reading a set of coefficients from RAM . . . . .                          | 54 |

|           |                                                          |           |
|-----------|----------------------------------------------------------|-----------|
| 7.5       | Writing a single coefficient to RAM .....                | 55        |
| 7.6       | Writing a set of coefficients to RAM .....               | 55        |
| <b>8</b>  | <b>Equalization and mixing .....</b>                     | <b>56</b> |
| 8.1       | Post-scale .....                                         | 56        |
| 8.2       | Variable max power correction .....                      | 58        |
| 8.2.1     | MPCC1-2 (0x4D, 0x4E) .....                               | 58        |
| 8.3       | Variable distortion compensation .....                   | 58        |
| 8.3.1     | DCC1-2 (0x4F, 0x50) .....                                | 58        |
| 8.4       | PSCorrect registers .....                                | 59        |
| 8.4.1     | PSC1-2: ripple correction value (RCV) (0x51, 0x52) ..... | 59        |
| 8.4.2     | PSC3: correction normalization value (CNV) (0x53) .....  | 59        |
| <b>9</b>  | <b>Package information .....</b>                         | <b>60</b> |
| <b>10</b> | <b>Trademarks and other acknowledgements .....</b>       | <b>61</b> |
| <b>11</b> | <b>Revision history .....</b>                            | <b>62</b> |

Obsolete Product(s) - Obsolete Product(s)

## List of tables

|           |                                                             |    |
|-----------|-------------------------------------------------------------|----|
| Table 1.  | Device summary . . . . .                                    | 1  |
| Table 2.  | Pin description . . . . .                                   | 7  |
| Table 3.  | Absolute maximum ratings . . . . .                          | 10 |
| Table 4.  | Thermal data. . . . .                                       | 10 |
| Table 5.  | Recommended operating condition . . . . .                   | 10 |
| Table 6.  | General interface electrical characteristics . . . . .      | 11 |
| Table 7.  | DC electrical characteristics: 3.3-V buffers. . . . .       | 11 |
| Table 8.  | Register summary. . . . .                                   | 16 |
| Table 9.  | RAM block for biquads, mixing, and bass management. . . . . | 54 |
| Table 10. | Document revision history . . . . .                         | 60 |

Obsolete Product(s) - Obsolete Product(s)

## List of figures

|           |                                                                 |    |
|-----------|-----------------------------------------------------------------|----|
| Figure 1. | Block diagram                                                   | 6  |
| Figure 2. | Channel signal flow                                             | 6  |
| Figure 3. | Pin connection (Top view)                                       | 7  |
| Figure 4. | Write mode sequence                                             | 14 |
| Figure 5. | Read mode sequence                                              | 14 |
| Figure 6. | Reference schematic for STA308A-based application               | 15 |
| Figure 7. | Basic limiter and volume flow diagram                           | 44 |
| Figure 8. | Channel mixer                                                   | 54 |
| Figure 9. | TQFP64 (10 x 10 x 1.4mm) mechanical data and package dimensions | 58 |

Obsolete Product(s) - Obsolete Product(s)

# 1 Block diagram

Figure 1. Block diagram

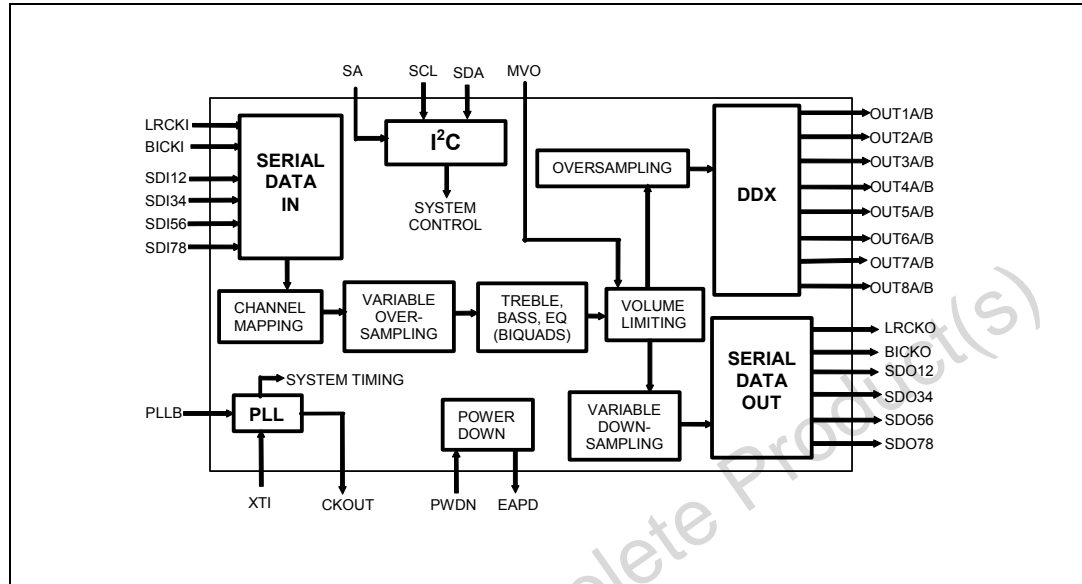
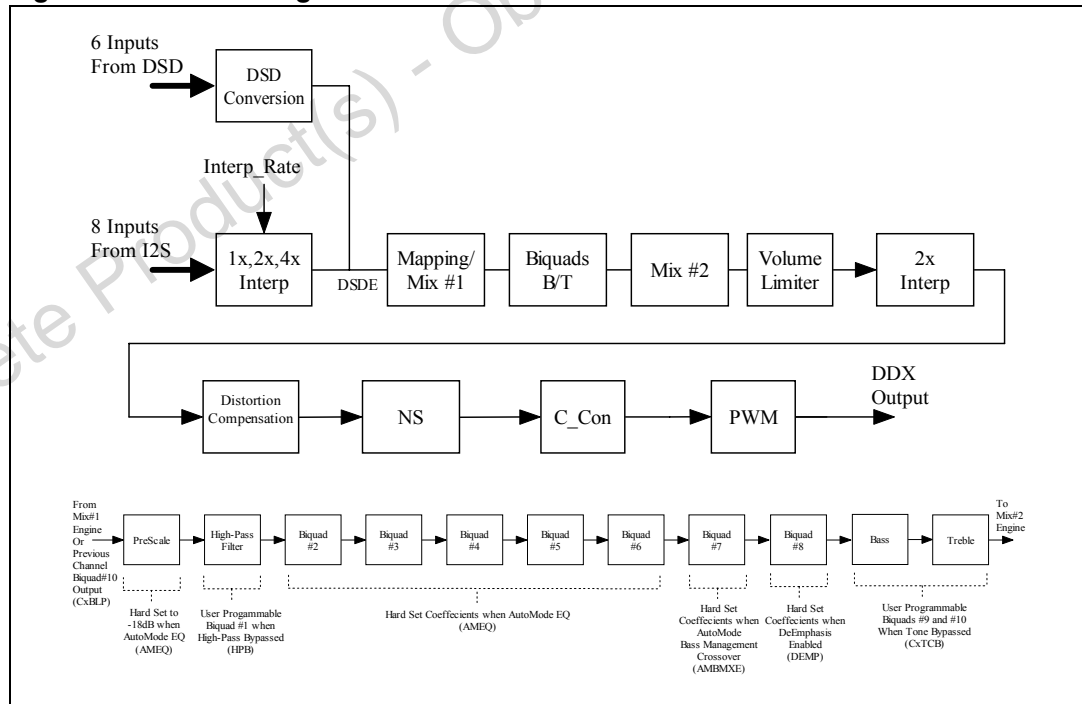


Figure 2. Channel signal flow





## 2 Pin connections

Figure 3. Pin connection (Top view)

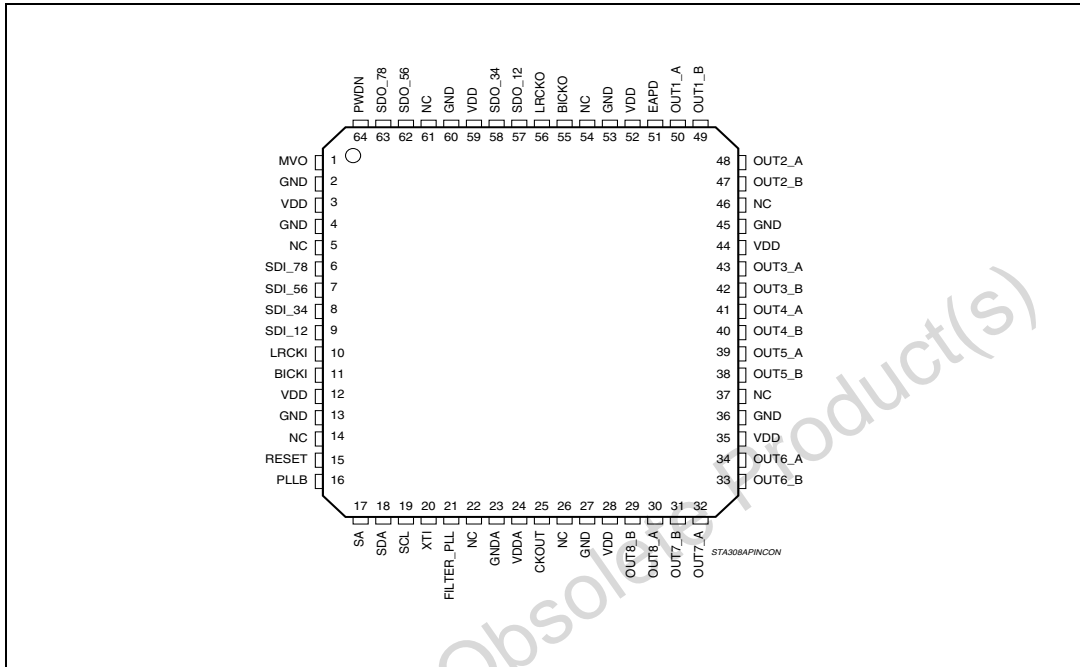


Table 2. Pin description

| Pin | Type                                          | Name         | Description                                              |
|-----|-----------------------------------------------|--------------|----------------------------------------------------------|
| 1   | 5-V tolerant TTL input buffer                 | MVO/DSD_CLK  | Master volume override/<br>DSD input clock               |
| 6   | 5-V tolerant TTL input buffer                 | SDI_78/DSD_6 | Input serial data channels 7 & 8/<br>DSD input channel 6 |
| 7   | 5-V tolerant TTL input buffer                 | SDI_56/DSD_5 | Input serial data channels 5 & 6/<br>DSD input channel 5 |
| 8   | 5-V tolerant TTL input buffer                 | SDI_34/DSD_4 | Input serial data channels 3 & 4/<br>DSD input channel 4 |
| 9   | 5-V tolerant TTL input buffer                 | SDI_12/DSD_3 | Input serial data channels 1 & 2/<br>DSD input channel 3 |
| 10  | 5-V tolerant TTL input buffer                 | LRCKI/DSD_2  | Input left/right clock/<br>DSD input channel 2           |
| 11  | 5-V tolerant TTL input buffer                 | BICKI/DSD_1  | Input serial clock/<br>DSD input channel 1               |
| 15  | 5-V tolerant TTL schmitt trigger input buffer | RESET        | Global reset                                             |
| 16  | CMOS input buffer with pull-down              | PLL_BYPASS   | Bypass phase locked loop                                 |

**Table 2. Pin description (continued)**

| Pin | Type                                                                                                         | Name       | Description                            |
|-----|--------------------------------------------------------------------------------------------------------------|------------|----------------------------------------|
| 17  | CMOS input buffer with pull-down                                                                             | SA         | Select address (I <sup>2</sup> C)      |
| 18  | Bidirectional buffer: 5-V tolerant TTL schmitt trigger input; 3.3-V capable 2mA slew-rate controlled output. | SDA        | Serial data (I <sup>2</sup> C)         |
| 19  | 5-V tolerant TTL schmitt trigger input buffer                                                                | SCL        | Serial clock (I <sup>2</sup> C)        |
| 20  | 5-V tolerant TTL schmitt trigger input buffer                                                                | XTI        | Crystal oscillator input (clock input) |
| 21  | Analog pad                                                                                                   | FILTER_PLL | PLL filter                             |
| 23  | Analog ground                                                                                                | GNDA       | PLL ground                             |
| 24  | 3.3V analog supply voltage                                                                                   | VDDA       | PLL supply                             |
| 25  | 3.3-V capable TTL tristate 4mA output buffer                                                                 | CKOUT      | Clock output                           |
| 29  | 3.3-V capable TTL 2mA output buffer                                                                          | OUT8B      | PWM channel 8 output B                 |
| 30  | 3.3-V capable TTL 2mA output buffer                                                                          | OUT8A      | PWM channel 8 output A                 |
| 31  | 3.3-V capable TTL 2mA output buffer                                                                          | OUT7B      | PWM channel 7 output B                 |
| 32  | 3.3-V capable TTL 2mA output buffer                                                                          | OUT7A      | PWM channel 7 output A                 |
| 33  | 3.3-V capable TTL 2mA output buffer                                                                          | OUT6B      | PWM channel 6 output B                 |
| 34  | 3.3-V capable TTL 2mA output buffer                                                                          | OUT6A      | PWM channel 6 output A                 |
| 38  | 3.3-V capable TTL 2mA output buffer                                                                          | OUT5B      | PWM channel 5 output B                 |
| 39  | 3.3-V capable TTL 2mA output buffer                                                                          | OUT5A      | PWM channel 5 output A                 |
| 40  | 3.3-V capable TTL 2mA output buffer                                                                          | OUT4B      | PWM channel 4 output B                 |
| 41  | 3.3-V capable TTL 2mA output buffer                                                                          | OUT4A      | PWM channel 4 output A                 |
| 42  | 3.3-V capable TTL 2mA output buffer                                                                          | OUT3B      | PWM channel 3 output B                 |
| 43  | 3.3-V capable TTL 2mA output buffer                                                                          | OUT3A      | PWM channel 3 output A                 |
| 47  | 3.3-V capable TTL 2mA output buffer                                                                          | OUT2B      | PWM channel 2 output B                 |

Table 2. Pin description (continued)

| Pin                        | Type                                          | Name   | Description                     |
|----------------------------|-----------------------------------------------|--------|---------------------------------|
| 48                         | 3.3-V capable TTL 2mA output buffer           | OUT2A  | PWM channel 2 output A          |
| 49                         | 3.3-V capable TTL 2mA output buffer           | OUT1B  | PWM channel 1 output B          |
| 50                         | 3.3-V capable TTL 2mA output buffer           | OUT1A  | PWM channel 1 output A          |
| 51                         | 3.3-V capable TTL 4mA output buffer           | EAPD   | Ext. amp power-down             |
| 55                         | 3.3-V capable TTL 2mA output buffer           | BICKO  | Output serial clock             |
| 56                         | 3.3-V capable TTL 2mA output buffer           | LRCKO  | Output left/right clock         |
| 57                         | 3.3-V capable TTL 2mA output buffer           | SDO_12 | Output serial data channels 1&2 |
| 58                         | 3.3-V capable TTL 2mA output buffer           | SDO_34 | Output serial data channels 3&4 |
| 62                         | 3.3-V capable TTL 2mA output buffer           | SDO_56 | Output serial data channels 5&6 |
| 63                         | 3.3-V capable TTL 2mA output buffer           | SDO_78 | Output serial data channels 7&8 |
| 64                         | 5-V tolerant TTL schmitt trigger input buffer | PWDN   | Device power-down               |
| 3,12,28,35,44,52,59        | 3.3-V digital supply voltage                  | VDD    | 3.3-V supply                    |
| 2,4,13,27,36,45,53,60      | Digital ground                                | GND    | Ground                          |
| 5, 14, 22, 26,37,46,54, 61 |                                               | NC     | Not connected                   |

### 3 Electrical specification

#### 3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

| Symbol           | Parameter                     | Min  | Typ | Max                   | Unit |
|------------------|-------------------------------|------|-----|-----------------------|------|
| V <sub>DD</sub>  | 3.3-V I/O power supply        | -0.5 |     | 4                     | V    |
| V <sub>DDA</sub> | 3.3-V logic power supply      | -0.5 |     | 4                     | V    |
| V <sub>i</sub>   | Voltage on input pins         | -0.5 |     | V <sub>DD</sub> + 0.5 | V    |
| V <sub>o</sub>   | Voltage on output pins        | -0.5 |     | V <sub>DD</sub> + 0.3 | V    |
| T <sub>stg</sub> | Storage temperature           | -40  |     | 150                   | °C   |
| T <sub>amb</sub> | Ambient operating temperature | -40  |     | 90                    | °C   |

#### 3.2 Thermal data

Table 4. Thermal data

| Symbol               | Parameter                               | Min | Typ | Max | Unit |
|----------------------|-----------------------------------------|-----|-----|-----|------|
| R <sub>thj-amb</sub> | Thermal resistance, junction to ambient |     | 85  |     | °C/W |

#### 3.3 Recommended operating condition

Table 5. Recommended operating condition

| Symbol           | Parameter                      | Min | Typ | Max | Unit |
|------------------|--------------------------------|-----|-----|-----|------|
| V <sub>DD</sub>  | I/O power supply               | 3.0 |     | 3.6 | V    |
| V <sub>DDA</sub> | Logic power supply             | 3.0 |     | 3.6 | V    |
| T <sub>j</sub>   | Operating junction temperature | -40 |     | 125 | °C   |

### 3.4 Electrical specifications

The following specifications are valid for  $V_{DD} = 3.3V \pm 0.3V$ ,  $V_{DDA} = 3.3V \pm 0.3V$  and  $T_{amb} = 0$  to  $70\text{ }^{\circ}\text{C}$ , unless otherwise stated

**Table 6. General interface electrical specifications**

| Symbol    | Parameter                                    | Conditions               | Min  | Typ | Max              | Unit          |
|-----------|----------------------------------------------|--------------------------|------|-----|------------------|---------------|
| $I_{ij}$  | Low-level input no pull-up                   | $V_i = 0V$               |      |     | 1 <sup>(1)</sup> | $\mu\text{A}$ |
| $I_{ih}$  | High-level input no pull-down                | $V_i = V_{DD}$           |      |     | 2                | $\mu\text{A}$ |
| $I_{OZ}$  | Tristate output leakage without pull-up/down | $V_i = V_{DD}$           |      |     | 2                | $\mu\text{A}$ |
| $V_{esd}$ | Electrostatic protection (human body model)  | Leakage $< 1\mu\text{A}$ | 2000 |     |                  | V             |

1. The leakage currents are generally very small,  $< 1\text{ nA}$ . The values given here are maximum after an electrostatic stress on the pin.

**Table 7. DC electrical characteristics: 3.3-V buffers**

| Symbol       | Parameter                  | Conditions                 | Min            | Typ | Max  | Unit |
|--------------|----------------------------|----------------------------|----------------|-----|------|------|
| $V_{IL}$     | Low-level input voltage    |                            |                |     | 0.8  | V    |
| $V_{IH}$     | High-level input voltage   |                            | 2.0            |     |      | V    |
| $V_{ILhyst}$ | Low-level threshold        | Input falling              | 0.8            |     | 1.35 | V    |
| $V_{IHhyst}$ | High-level threshold       | Input rising               | 1.3            |     | 2.0  | V    |
| $V_{hyst}$   | Schmitt trigger hysteresis |                            | 0.3            |     | 0.8  | V    |
| $V_{ol}$     | Low-level output           | $I_{ol} = 100\mu\text{A}$  |                |     | 0.2  | V    |
| $V_{oh}$     | High-level output          | $I_{oh} = -100\mu\text{A}$ | $V_{DD} - 0.2$ |     |      | V    |
|              |                            | $I_{oh} = -2\text{mA}$     | 2.4            |     |      | V    |

## 4 Pin description

### Master volume override (MVO)

This pin enables the user to bypass the volume control on all channels. When MVO is pulled high, the master volume register is set to 0x00, which corresponds to its full scale setting. The master volume register setting offsets the individual channel volume settings, which default to 0 dB.

### Serial data in (SDI\_12, SDI\_34, SDI\_56, SDI\_78)

Audio information enters the device here. Six format choices are available including I<sup>2</sup>S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

### RESET

Driving this pin low turns off the outputs and returns all settings to their defaults.

### I<sup>2</sup>C bus

The SA, SDA and SCL pins operate per the Phillips I<sup>2</sup>C specification. See Section 5.

### Phase locked loop (PLL)

The phase locked loop section provides the system timing signals and CKOUT.

### Clock output (CKOUT)

System synchronization and master clocks are provided by the CKOUT.

### PWM outputs (OUT1 through OUT8)

The PWM outputs provide the input signal for the power devices.

### External amplifier power-down (EAPD)

This signal can be used to control the power-down of DDX power devices.

### Serial data out (SDO\_12, SDO\_34, SDO\_56, SDO\_78)

These are the outputs for audio information. Six different formats are available including I<sup>2</sup>S, left- or right-justified, LSB or MSB first, with word widths of 16, 18, 20 and 24 bits.

### Device power-down (PWDN)

Pulling PWDN low begins the power-down sequence which puts the STA308A into a low-power state. EAPD (pin 51) goes low approximately 30 ms later.

## 5 I<sup>2</sup>C bus operation

The STA308A supports the I<sup>2</sup>C protocol via the input ports SCL and SDA\_IN (master to slave) and the output port SDA\_OUT (slave to master).

This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver.

The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA308A is always a slave device in all of its communications.

### 5.1 Communication protocol

#### 5.1.1 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

#### 5.1.2 Start condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

#### 5.1.3 Stop condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between STA308A and the bus master.

#### 5.1.4 Data input

During the data input the STA308A samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

### 5.2 Device addressing

To start communication between the master and the Omega DDX core, the master must initiate with a start condition. Following this, the master sends 8 bits onto the SDA line (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I<sup>2</sup>C bus definition. In the STA308A the I<sup>2</sup>C interface has two device addresses depending on the SA port configuration, 0x40 or 0100000x when SA = 0, and 0x42 or 0100001x when SA = 1.

The 8<sup>th</sup> bit (LSB) identifies read or write operation RW, this bit is set to 1 in read mode and 0 for write mode. After a START condition the STA308A identifies on the bus the device

address and if a match is found, it acknowledges the identification on SDA bus during the 9<sup>th</sup>-bit time. The byte following the device identification byte is the internal space address.

### 5.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA308A acknowledges this and the writes for the byte of internal address.

After receiving the internal byte address the STA308A again responds with an acknowledgement.

#### 5.3.1 Byte write

In the byte write mode the master sends one data byte, this is acknowledged by the Omega DDX core. The master then terminates the transfer by generating a STOP condition.

#### 5.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Figure 4. Write mode sequence

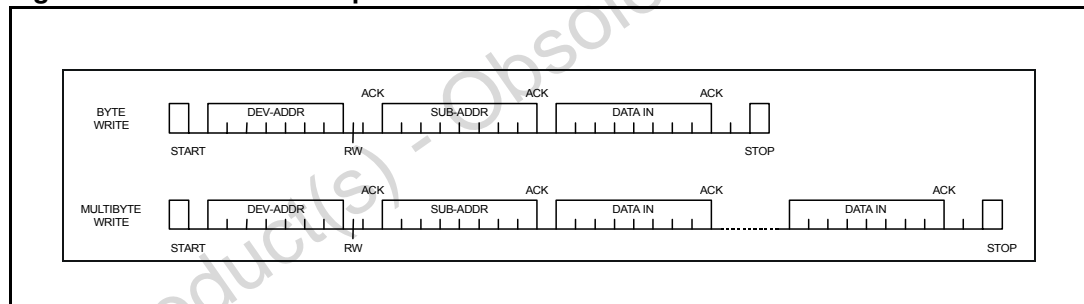
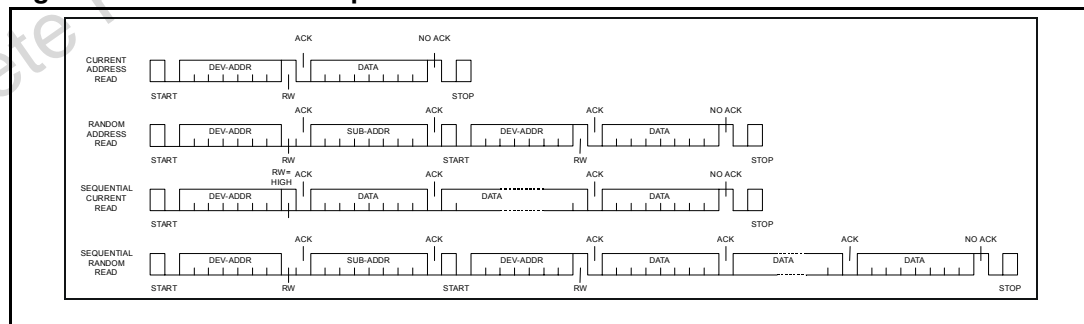


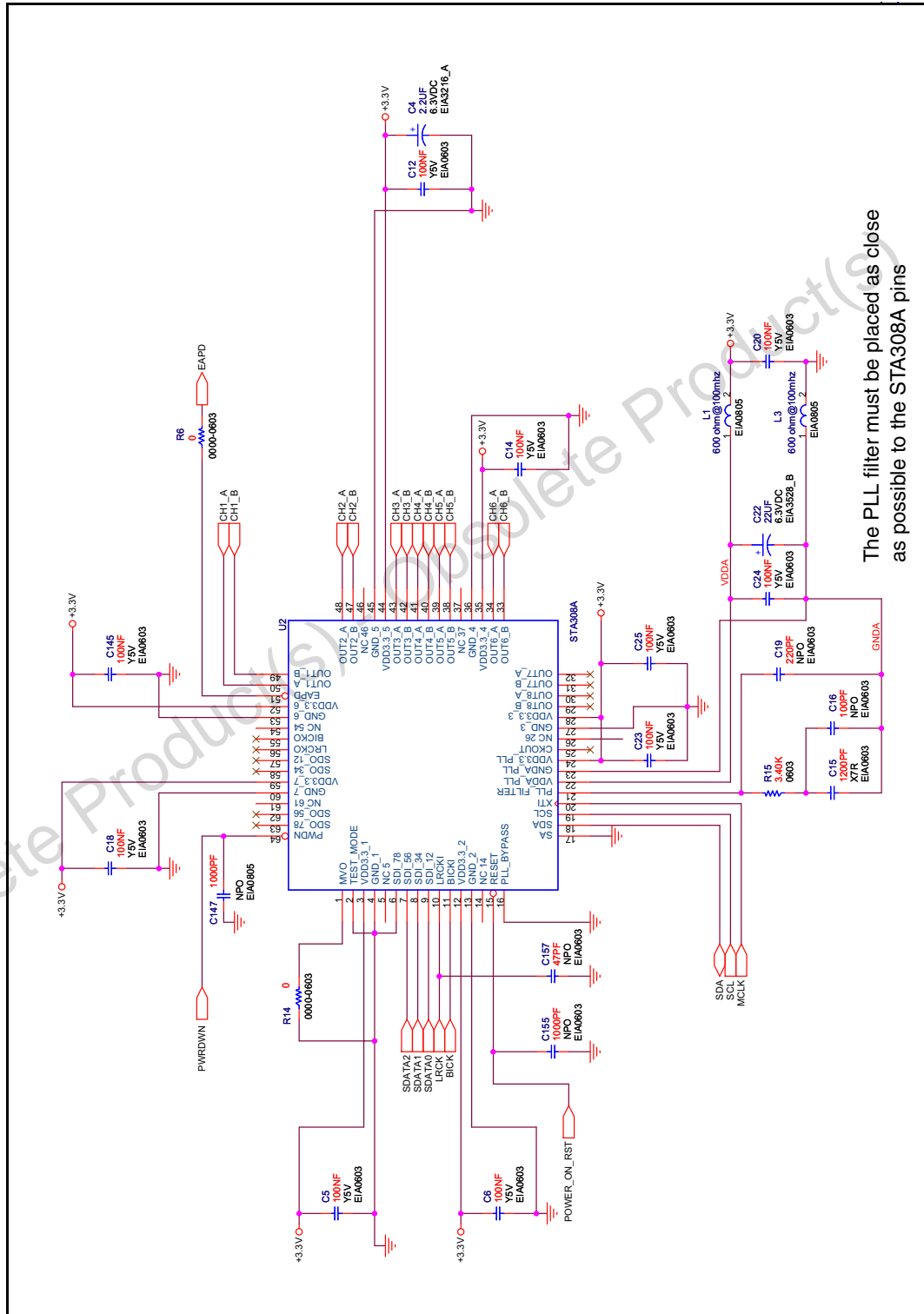
Figure 5. Read mode sequence





# 6 Application reference schematic

Figure 6. Reference schematic for STA308A-based application



The PLL filter must be placed as close as possible to the STA308A pins

## 7 Registers

### 7.1 Register summary

Table 8. Register summary

| Addr           | Name   | D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|----------------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| Configuration  |        |       |       |       |       |       |       |       |       |
| 0x00           | CONFA  | COS1  | COS0  | DSPB  | IR1   | IR0   | MCS2  | MCS1  | MCS0  |
| 0x01           | ConfB  |       |       |       | SAIFB | SAI3  | SAI2  | SAI1  | SAI0  |
| 0x02           | ConfC  |       |       |       | SAOFB | SAO3  | SAO2  | SAO1  | SAO0  |
| 0x03           | ConfD  | MPC   | CSZ4  | CSZ3  | CSZ2  | CSZ1  | CSZ0  | OM1   | OM0   |
| 0x04           | ConfE  | C8BO  | C7BO  | C6BO  | C5BO  | C4BO  | C3BO  | C2BO  | C1BO  |
| 0x05           | ConfF  | PWMS2 | PWMS1 | PWMS0 | BQL   | PSL   | DEMP  | DRC   | HPB   |
| 0x06           | ConfG  | MPCV  | DCCV  | HPE   | AM2E  | AME   | COD   | SID   | PWMD  |
| 0x07           | ConfH  | ECLE  | LDTE  | BCLE  | IDE   | ZDE   | SVE   | ZCE   | NSBW  |
| 0x08           | ConfI  | EAPD  |       |       |       |       |       |       | PSCE  |
| Volume control |        |       |       |       |       |       |       |       |       |
| 0x09           | MMUTE  |       |       |       |       |       |       |       | MMUTE |
| 0x0A           | Mvol   | MV7   | MV6   | MV5   | MV4   | MV3   | MV2   | MV1   | MV0   |
| 0x0B           | C1Vol  | C1V7  | C1V6  | C1V5  | C1V4  | C1V3  | C1V2  | C1V1  | C1V0  |
| 0x0C           | C2Vol  | C2V7  | C2V6  | C2V5  | C2V4  | C2V3  | C2V2  | C2V1  | C2V0  |
| 0x0D           | C3Vol  | C3V7  | C3V6  | C3V5  | C3V4  | C3V3  | C3V2  | C3V1  | C3V0  |
| 0x0E           | C4Vol  | C4V7  | C4V6  | C4V5  | C4V4  | C4V3  | C4V2  | C4V1  | C4V0  |
| 0x0F           | C5Vol  | C5V7  | C5V6  | C5V5  | C5V4  | C5V3  | C5V2  | C5V1  | C5V0  |
| 0x10           | C6Vol  | C6V7  | C6V6  | C6V5  | C6V4  | C6V3  | C6V2  | C6V1  | C6V0  |
| 0x11           | C7Vol  | C7V7  | C7V6  | C7V5  | C7V4  | C7V3  | C7V2  | C7V1  | C7V0  |
| 0x12           | C8Vol  | C8V7  | C8V6  | C8V5  | C8V4  | C8V3  | C8V2  | C8V1  | C8V0  |
| 0x13           | C1VTMB | C1M   | C1VBP |       | C1VT4 | C1VT3 | C1VT2 | C1VT1 | C1VT0 |
| 0x14           | C2VTMB | C2M   | C2VBP |       | C2VT4 | C2VT3 | C2VT2 | C2VT1 | C2VT0 |
| 0x15           | C3VTMB | C3M   | C3VBP |       | C3VT4 | C3VT3 | C3VT2 | C3VT1 | C3VT0 |
| 0x16           | C4VTMB | C4M   | C4VBP |       | C4VT4 | C4VT3 | C4VT2 | C4VT1 | C4VT0 |
| 0x17           | C5VTMB | C5M   | C5VBP |       | C5VT4 | C5VT3 | C5VT2 | C5VT1 | C5VT0 |
| 0x18           | C6VTMB | C6M   | C6VBP |       | C6VT4 | C6VT3 | C6VT2 | C6VT1 | C6VT0 |
| 0x19           | C7VTMB | C7M   | C7VBP |       | C7VT4 | C7VT3 | C7VT2 | C7VT1 | C7VT0 |
| 0x1A           | C8VTMB | C8M   | C8VBP |       | C8VT4 | C8VT3 | C8VT2 | C8VT1 | C8VT0 |
| Input mapping  |        |       |       |       |       |       |       |       |       |
| 0x1B           | C12im  |       | C2IM2 | C2IM1 | C2IM0 |       | C1IM2 | C1IM1 | C1IM0 |

**Table 8. Register summary (continued)**

| Addr                                    | Name    | D7     | D6     | D5     | D4     | D3     | D2     | D1     | D0     |
|-----------------------------------------|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0x1C                                    | C34im   |        | C4IM2  | C4IM1  | C4IM0  |        | C3IM2  | C3IM1  | C3IM0  |
| 0x1D                                    | C56im   |        | C6IM2  | C6IM1  | C6IM0  |        | C5IM2  | C5IM1  | C5IM0  |
| 0x1E                                    | C78im   |        | C8IM2  | C8IM1  | C8IM0  |        | C7IM2  | C7IM1  | C7IM0  |
| AutoMode                                |         |        |        |        |        |        |        |        |        |
| 0x1F                                    | Auto1   | AMDM   | AMGC2  | AMGC1  | AMGC0  | AMV1   | AMV0   | AMEQ1  | AMEQ0  |
| 0x20                                    | Auto2   | SUB    | RSS1   | RSS0   | CSS1   | CSS0   | FSS    | AMBMXE | AMBMME |
| 0x21                                    | Auto3   | AMAM2  | AMAM1  | AMAM0  | AMAME  |        |        | MSA    | AMPS   |
| 0x22                                    | PreEQ   | XO2    | XO1    | XO0    | PEQ4   | PEQ3   | PEQ2   | PEQ1   | PEQ0   |
| 0x23                                    | Ageq    |        |        |        | AGEQ4  | AGEQ3  | AGEQ2  | AGEQ1  | AGEQ0  |
| 0x24                                    | Bgeq    |        |        |        | BGEQ4  | BGEQ3  | BGEQ2  | BGEQ1  | BGEQ0  |
| 0x25                                    | Cgeq    |        |        |        | CGEQ4  | CGEQ3  | CGEQ2  | CGEQ1  | CGEQ0  |
| 0x26                                    | Dgeq    |        |        |        | DGEQ4  | DGEQ3  | DGEQ2  | DGEQ1  | DGEQ0  |
| 0x27                                    | Egeq    |        |        |        | EGEQ4  | EGEQ3  | EGEQ2  | EGEQ1  | EGEQ0  |
| Processing loop                         |         |        |        |        |        |        |        |        |        |
| 0x28                                    | BQlp    | C8BLP  | C7BLP  | C6BLP  | C5BLP  | C4BLP  | C3BLP  | C2BLP  | C1BLP  |
| 0x29                                    | MXlp    | C8MXLP | C7MXLP | C6MXLP | C5MXLP | C4MXLP | C3MXLP | C2MXLP | C1MXLP |
| Processing pypass                       |         |        |        |        |        |        |        |        |        |
| 0x2A                                    | EQbp    | C8EQBP | C7EQBP | C6EQBP | C5EQBP | C4EQBP | C3EQBP | C2EQBP | C1EQBP |
| 0x2B                                    | ToneBP  | C8TCB  | C7TCB  | C6TCB  | C5TCB  | C4TCB  | C3TCB  | C2TCB  | C1TCB  |
| Tone control                            |         |        |        |        |        |        |        |        |        |
| 0x2C                                    | Tone    | TTC3   | TTC2   | TTC1   | TTC0   | BTC3   | BTC2   | BTC1   | BTC0   |
| Dynamics control                        |         |        |        |        |        |        |        |        |        |
| 0x2D                                    | C1234ls | C4LS1  | C4LS0  | C3LS1  | C3LS0  | C2LS1  | C2LS0  | C1LS1  | C1LS0  |
| 0x2E                                    | C5678ls | C8LS1  | C8LS0  | C7LS1  | C7LS0  | C6LS1  | C6LS0  | C5LS1  | C5LS0  |
| 0x2F                                    | L1ar    | L1A3   | L1A2   | L1A1   | L1A0   | L1R3   | L1R2   | L1R1   | L1R0   |
| 0x30                                    | L1atrt  | L1AT3  | L1AT2  | L1AT1  | L1AT0  | L1RT3  | L1RT2  | L1RT1  | L1RT0  |
| 0x31                                    | L2ar    | L2A3   | L2A2   | L2A1   | L2A0   | L2R3   | L2R2   | L2R1   | L2R0   |
| 0x32                                    | L2atrt  | L2AT3  | L2AT2  | L2AT1  | L2AT0  | L2RT3  | L2RT2  | L2RT1  | L2RT0  |
| PWM output timing                       |         |        |        |        |        |        |        |        |        |
| 0x33                                    | C12ot   |        | C2OT2  | C2OT1  | C2OT0  |        | C1OT2  | C1OT1  | C1OT0  |
| 0x34                                    | C34ot   |        | C4OT2  | C4OT1  | C4OT0  |        | C3OT2  | C3OT1  | C3OT0  |
| 0x35                                    | C56ot   |        | C6OT2  | C6OT1  | C6OT0  |        | C5OT2  | C5OT1  | C5OT0  |
| 0x36                                    | C78ot   |        | C8OT2  | C8OT1  | C8OT0  |        | C7OT2  | C7OT1  | C7OT0  |
| I <sup>2</sup> S output channel mapping |         |        |        |        |        |        |        |        |        |
| 0x37                                    | C12om   |        | C2OM2  | C2OM1  | C2OM0  |        | C1OM2  | C1OM1  | C1OM0  |

Table 8. Register summary (continued)

| Addr                         | Name    | D7     | D6     | D5     | D4     | D3     | D2     | D1    | D0    |
|------------------------------|---------|--------|--------|--------|--------|--------|--------|-------|-------|
| 0x38                         | C34om   |        | C4OM2  | C4OM1  | C4OM0  |        | C3OM2  | C3OM1 | C3OM0 |
| 0x39                         | C56om   |        | C6OM2  | C6OM1  | C6OM0  |        | C5OM2  | C5OM1 | C5OM0 |
| 0x3A                         | C78om   |        | C8OM2  | C8OM1  | C8OM0  |        | C7OM2  | C7OM1 | C7OM0 |
| User-defined coefficient RAM |         |        |        |        |        |        |        |       |       |
| 0x3B                         | Cfaddr1 |        |        |        |        |        |        | CFA9  | CFA8  |
| 0x3C                         | Cfaddr2 | CFA7   | CFA6   | CFA5   | CFA4   | CFA3   | CFA2   | CFA1  | CFA0  |
| 0x3D                         | B1cf1   | C1B23  | C1B22  | C1B21  | C1B20  | C1B19  | C1B18  | C1B17 | C1B16 |
| 0x3E                         | B1cf2   | C1B15  | C1B14  | C1B13  | C1B12  | C1B11  | C1B10  | C1B9  | C1B8  |
| 0x3F                         | B1cf3   | C1B7   | C1B6   | C1B5   | C1B4   | C1B3   | C1B2   | C1B1  | C1B0  |
| 0x40                         | B2cf1   | C2B23  | C2B22  | C2B21  | C2B20  | C2B19  | C2B18  | C2B17 | C2B16 |
| 0x41                         | B2cf2   | C2B15  | C2B14  | C2B13  | C2B12  | C2B11  | C2B10  | C2B9  | C2B8  |
| 0x42                         | B2cf3   | C2B7   | C2B6   | C2B5   | C2B4   | C2B3   | C2B2   | C2B1  | C2B0  |
| 0x43                         | A1cf1   | C3B23  | C3B22  | C3B21  | C3B20  | C3B19  | C3B18  | C3B17 | C3B16 |
| 0x44                         | A1cf2   | C3B15  | C3B14  | C3B13  | C3B12  | C3B11  | C3B10  | C3B9  | C3B8  |
| 0x45                         | A1cf3   | C3B7   | C3B6   | C3B5   | C3B4   | C3B3   | C3B2   | C3B1  | C3B0  |
| 0x46                         | A2cf1   | C4B23  | C4B22  | C4B21  | C4B20  | C4B19  | C4B18  | C4B17 | C4B16 |
| 0x47                         | A2cf2   | C4B15  | C4B14  | C4B13  | C4B12  | C4B11  | C4B10  | C4B9  | C4B8  |
| 0x48                         | A2cf3   | C4B7   | C4B6   | C4B5   | C4B4   | C4B3   | C4B2   | C4B1  | C4B0  |
| 0x49                         | B0cf1   | C5B23  | C5B22  | C5B21  | C5B20  | C5B19  | C5B18  | C5B17 | C5B16 |
| 0x4A                         | B0cf2   | C5B15  | C5B14  | C5B13  | C5B12  | C5B11  | C5B10  | C5B9  | C5B8  |
| 0x4B                         | B0cf3   | C5B7   | C5B6   | C5B5   | C5B4   | C5B3   | C5B2   | C5B1  | C5B0  |
| 0x4C                         | Cfud    |        |        |        |        |        |        | WA    | W1    |
| 0x4D                         | MPCC1   | MPCC15 | MPCC14 | MPCC13 | MPCC12 | MPCC11 | MPCC10 | MPCC9 | MPCC8 |
| 0x4E                         | MPCC2   | MPCC7  | MPCC6  | MPCC5  | MPCC4  | MPCC3  | MPCC2  | MPCC1 | MPCC0 |
| 0x4F                         | DCC1    | DCC15  | DCC14  | DCC13  | DCC12  | DCC11  | DCC10  | DCC9  | DCC8  |
| 0x50                         | DCC2    | DCC7   | DCC6   | DCC5   | DCC4   | DCC3   | DCC2   | DCC1  | DCC0  |
| 0x51                         | PSC1    | RCV11  | RCV10  | RCV9   | RCV8   | RCV7   | RCV6   | RCV5  | RCV4  |
| 0x52                         | PSC2    | RCV3   | RCV2   | RCV1   | RCV0   | CNV11  | CNV10  | CNV9  | CNV8  |
| 0x53                         | PSC3    | CNV7   | CNV6   | CNV5   | CNV4   | CNV3   | CNV2   | CNV1  | CNV0  |

## 7.2 Register description

### 7.2.1 Configuration register A (0x00)

| D7   | D6   | D5   | D4  | D3  | D2   | D1   | D0   |
|------|------|------|-----|-----|------|------|------|
| COS1 | COS0 | DSPB | IR1 | IR0 | MCS2 | MCS1 | MCS0 |
| 1    | 0    | 0    | 0   | 0   | 0    | 1    | 1    |

| Bit | RW | RST | Name | Description                                                                                                     |
|-----|----|-----|------|-----------------------------------------------------------------------------------------------------------------|
| 0   | RW | 1   | MCS0 | Master clock select: selects the ratio between the input I <sup>2</sup> S sample frequency and the input clock. |
| 1   | RW | 1   | MCS1 |                                                                                                                 |
| 2   | RW | 0   | MCS2 |                                                                                                                 |

The DDX8000 supports sample rates of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz, and 2.8224 MHz DSD. Therefore the internal clocks are:

- 65.536 MHz for 32 kHz
- 90.3168 MHz for 44.1 kHz, 88.2 kHz, 176.4 kHz, and DSD
- 98.304 MHz for 48 kHz, 96 kHz, and 192 kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency ( $f_s$ ). The relationship between the input clock and the input sample rate is determined by both the MCSn and the IRn (input rate) register bits. The MCSn bits determine the PLL factor generating the internal clock and the IRn bits determine the oversampling ratio used internally.

| Input sample rate<br>$f_s$ (kHz) | IR | MCS[2:0]    |             |             |             |             |
|----------------------------------|----|-------------|-------------|-------------|-------------|-------------|
|                                  |    | 1XX         | 011         | 010         | 001         | 000         |
| 32, 44.1, 48                     | 00 | 128 * $f_s$ | 256 * $f_s$ | 384 * $f_s$ | 512 * $f_s$ | 768 * $f_s$ |
| 88.2, 96                         | 01 | 64 * $f_s$  | 128 * $f_s$ | 192 * $f_s$ | 256 * $f_s$ | 384 * $f_s$ |
| 176.4, 192                       | 10 | 64 * $f_s$  | 128 * $f_s$ | 192 * $f_s$ | 256 * $f_s$ | 384 * $f_s$ |
| DSD                              | 11 | 2 * $f_s$   | 4 * $f_s$   | 6 * $f_s$   | 8 * $f_s$   | 10 * $f_s$  |

#### Interpolation ratio select

| Bit | RW | RST | Name | Description                                                                                                       |
|-----|----|-----|------|-------------------------------------------------------------------------------------------------------------------|
| 3   | RW | 0   | IR0  | Interpolation ratio select: selects internal interpolation ratio based on input I <sup>2</sup> S sample frequency |
| 4   | RW | 0   | IR1  |                                                                                                                   |

The STA308A has variable interpolation (oversampling) settings such that internal processing and DDX output rates remain consistent. The first processing block interpolates by either 4 times, 2 times, or 1 time (pass-through).

The oversampling ratio of this interpolation is determined by the IR bits.

| IR[1,0] | Input sample rate<br>$F_s$ (kHz) | 1 <sup>st</sup> stage interpolation ratio |
|---------|----------------------------------|-------------------------------------------|
| 00      | 32                               | 4-times oversampling                      |
| 00      | 44.1                             | 4-times oversampling                      |
| 00      | 48                               | 4-times oversampling                      |
| 01      | 88.2                             | 2-times oversampling                      |
| 01      | 96                               | 2-times oversampling                      |
| 10      | 176.4                            | Pass-through                              |
| 10      | 192                              | Pass-through                              |
| 11      | DSD                              | DSD to 176.4 kHz conversion               |

| Bit | RW | RST | Name | Description                                                                             |
|-----|----|-----|------|-----------------------------------------------------------------------------------------|
| 0   | RW | 0   | DSPB | DSP bypass bit:<br>0: normal operation<br>1: bypass of biquad and bass/treble functions |

Setting the DSPB bit bypasses the biquad function of the Omega DDX core.

| COS[1,0] | CKOUT frequency |
|----------|-----------------|
| 00       | PLL output      |
| 01       | PLL output / 4  |
| 10       | PLL output / 8  |
| 11       | PLL output / 16 |

**7.2.2 Configuration register B (0x01) - serial input formats**

| D7 | D6 | D5 | D4    | D3   | D2   | D1   | D0   |
|----|----|----|-------|------|------|------|------|
|    |    |    | SAIFB | SAI3 | SAI2 | SAI1 | SAI0 |
|    |    |    | 0     | 0    | 0    | 0    | 0    |

| Bit | RW | RST | Name | Description                                                                                                       |
|-----|----|-----|------|-------------------------------------------------------------------------------------------------------------------|
| 0   | RW | 0   | SAI0 | Serial audio input interface format: determines the interface format of the input serial digital audio interface. |
| 1   | RW | 0   | SAI1 |                                                                                                                   |
| 2   | RW | 0   | SAI2 |                                                                                                                   |
| 3   | RW | 0   | SAI3 |                                                                                                                   |

**Serial data interface**

The STA308A audio serial input interfaces with standard digital audio components and accepts a number of serial data formats. STA308A always acts a slave when receiving audio input from standard digital audio components. Serial data for eight channels is provided using 6 input pins: left/right clock LRCKI (pin 10), serial clock BICKI (pin 11), serial data 1 and 2 SDI12 (pin 9), serial data 3 and 4 SDI34 (pin 8), serial data 5 and 6 SDI56 (pin 7), and serial data 7 and 8 SDI78 (pin 6). The SAI/SAIFB register (Configuration Register B, address 0x01) is used to specify the serial data format. The default serial data format is I<sup>2</sup>S, MSB-first. Available formats are shown in the tables and figure that follow.

| Bit | RW | RST | Name  | Description                                                                      |
|-----|----|-----|-------|----------------------------------------------------------------------------------|
| 4   | RW | 0   | SAIFB | Determines MSB or LSB first for all SAO formats:<br>0: MSB first<br>1: LSB first |

*Note: Serial input and output formats are specified separately*

For example, SAI = 1110 and SAIFB = 1 would specify right-justified 16-bit data, LSB-first.

The table below lists the serial audio input formats supported by STA308A as related to  $BICKI = 32 * fs, 48 * fs, 64 * fs$ , where sampling rate,  $fs = 32, 44.1, 48, 88.2, 96, 176.4, 192$  kHz.

| BICKI   | SAI [3:0] | SAIFB | Interface format                       |
|---------|-----------|-------|----------------------------------------|
| 32 * fs | 1100      | X     | I <sup>2</sup> S 15-bit data           |
|         | 1110      | X     | Left/right-justified 16-bit data       |
| 48 * fs | 0100      | X     | I <sup>2</sup> S 23-bit data           |
|         | 0100      | X     | I <sup>2</sup> S 20-bit data           |
|         | 1000      | X     | I <sup>2</sup> S 18-bit data           |
|         | 0100      | 0     | MSB-first I <sup>2</sup> S 16-bit data |
|         | 1100      | 1     | LSB-first I <sup>2</sup> S 16-bit data |
|         | 0001      | X     | Left-justified 24-bit data             |
|         | 0101      | X     | Left-justified 20-bit data             |
|         | 1001      | X     | Left-justified 18-bit data             |
|         | 1101      | X     | Left-justified 16-bit data             |
|         | 0010      | X     | Right-justified 24-bit data            |
|         | 0110      | X     | Right-justified 20-bit data            |
|         | 1010      | X     | Right-justified 18-bit data            |
|         | 1110      | X     | Right-justified 16-bit data            |
| 64 * fs | 0000      | X     | I <sup>2</sup> S 24-bit data           |
|         | 0100      | X     | I <sup>2</sup> S 20-bit data           |
|         | 1000      | X     | I <sup>2</sup> S 18-bit data           |
|         | 0000      | 0     | MSB-first I <sup>2</sup> S 16-bit data |
|         | 1100      | 1     | LSB-first I <sup>2</sup> S 16-bit data |
|         | 0001      | X     | Left-justified 24-bit data             |
|         | 0101      | X     | Left-justified 20-bit data             |
|         | 1001      | X     | Left-justified 18-bit data             |
|         | 1101      | X     | Left-justified 16-bit data             |
|         | 0010      | X     | Right-justified 24-bit data            |
|         | 0110      | X     | Right-justified 20-bit data            |
|         | 1010      | X     | Right-justified 18-bit data            |
|         | 1110      | X     | Right-justified 16-bit data            |



7.2.3 Configuration register C (0x02) - serial output formats

| D7 | D6 | D5 | D4    | D3   | D2   | D1   | D0   |
|----|----|----|-------|------|------|------|------|
|    |    |    | SAOFB | SAO3 | SAO2 | SAIO | SAO0 |
|    |    |    | 0     | 0    | 0    | 0    | 0    |

| Bit | RW | RST | Name | Description                                                                                                         |
|-----|----|-----|------|---------------------------------------------------------------------------------------------------------------------|
| 0   | RW | 0   | SAO0 | Serial audio output interface format: determines the interface format of the output serial digital audio interface. |
| 1   | RW | 0   | SAO1 |                                                                                                                     |
| 2   | RW | 0   | SAO2 |                                                                                                                     |
| 3   | RW | 0   | SAO3 |                                                                                                                     |

The STA308A features a serial audio output interface that consists of 8 channels. The serial audio output always acts as a slave to the serial audio input interface and, therefore, all output clocks are synchronous with the input clocks. The output sample frequency (fs) is also equivalent to the input sample frequency. In the case of SACD/DSD input, the serial audio output acts as a master with an output sampling frequency of 176.4 kHz. The output serial format can be selected independently from the input format and is done via the SAO and SAOFB bits.

| Bit | RW | RST | Name  | Description                                                                      |
|-----|----|-----|-------|----------------------------------------------------------------------------------|
| 4   | RW | 0   | SAOFB | Determines MSB or LSB first for all SAO formats:<br>0: MSB first<br>1: LSB first |

| BICKI = BICKO | SAO[3:0]                    | Interface data format            |
|---------------|-----------------------------|----------------------------------|
| 32 * fs       | 0111                        | I <sup>2</sup> S data            |
|               | 1111                        | Left/right-justified 16-bit data |
| 48 * fs       | 1110                        | I <sup>2</sup> S data            |
|               | 0001                        | Left-justified data              |
|               | 1010                        | Right-justified 24-bit data      |
|               | 1011                        | Right-justified 20-bit data      |
|               | 1100                        | Right-justified 18-bit data      |
| 64 * fs       | 1101                        | Right-justified 16-bit data      |
|               | 0000                        | I <sup>2</sup> S data            |
|               | 0001                        | Left-justified data              |
|               | 0010                        | Right-justified 24-bit data      |
|               | 0011                        | Right-justified 20-bit data      |
|               | 0100                        | Right-justified 18-bit data      |
| 0101          | Right-justified 16-bit data |                                  |

7.2.4 Configuration register D (0x03)

| D7  | D6   | D5   | D4   | D3   | D2   | D1  | D0  |
|-----|------|------|------|------|------|-----|-----|
| MPC | CSZ4 | CSZ3 | CSZ2 | CSZ1 | CSZ0 | OM1 | OM0 |
| 1   | 1    | 0    | 0    | 0    | 0    | 1   | 0   |

| Bit | RW | RST | Name | Description                                                 |
|-----|----|-----|------|-------------------------------------------------------------|
| 0   | RW | 0   | OM0  | DDX power output mode: selects configuration of DDX output. |
| 1   | RW | 1   | OM1  |                                                             |

The DDX power output mode selects how the DDX output timing is configured. Different power devices use different output modes. The STA50x recommended use is OM = 10.

| OM[1,0] | Output stage - mode                          |
|---------|----------------------------------------------|
| 00      | STA50x/STA51xB - drop compensation           |
| 01      | Discrete output stage - tapered compensation |
| 10      | STA50x/STA51xB - full power mode             |
| 11      | Variable drop compensation (CSZn bits)       |

| Bit | RW | RST | Name | Description                                                                                                                                      |
|-----|----|-----|------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | RW | 0   | CSZ0 | Contra size register: when OM[1,0] = 11, this register determines the size of the DDX compensating pulse from 0 clock ticks to 31 clock periods. |
| 3   | RW | 0   | CSZ1 |                                                                                                                                                  |
| 4   | RW | 0   | CSZ2 |                                                                                                                                                  |
| 5   | RW | 0   | CSZ3 |                                                                                                                                                  |
| 6   | RW | 1   | CSZ4 |                                                                                                                                                  |

| CSZ[4:0] | Compensating pulse size                 |
|----------|-----------------------------------------|
| 00000    | 0 clock period compensating pulse size  |
| 00001    | 1 clock period compensating pulse size  |
| ...      | ...                                     |
| 11111    | 31 clock period compensating pulse size |

| Bit | RW | RST | Name | Description                                                                                               |
|-----|----|-----|------|-----------------------------------------------------------------------------------------------------------|
| 7   | RW | 1   | MPC  | Max power correction: setting of 1 enables STA50x correction for THD reduction near maximum power output. |

Setting the MPC bit turns on special processing that corrects the STA50x power device at high power. This mode should lower the THD+N of a full STA50x DDX system at maximum power output and slightly below. This mode will only be operational in OM[1,0] = 01.

**7.2.5 Configuration register E (0x04)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C8BO | C7BO | C6BO | C5BO | C4BO | C3BO | C2BO | C1BO |
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

| Bit | RW | RST | Name | Description                                                                                                                                                             |
|-----|----|-----|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | RW | 0   | C1BO | Channels 1, 2, 3, 4, 5, 6, 7, and 8 binary output mode enable bits. A setting of 0 indicates ordinary DDX tristate output. A setting of 1 indicates binary output mode. |
| 1   | RW | 0   | C2BO |                                                                                                                                                                         |
| 2   | RW | 0   | C3BO |                                                                                                                                                                         |
| 3   | RW | 0   | C4BO |                                                                                                                                                                         |
| 4   | RW | 0   | C5BO |                                                                                                                                                                         |
| 5   | RW | 0   | C6BO |                                                                                                                                                                         |
| 6   | RW | 0   | C7BO |                                                                                                                                                                         |
| 7   | RW | 0   | C8BO |                                                                                                                                                                         |

Each individual channel output can be set to output a binary PWM stream. In this mode output A of a channel will be considered the positive output and output B is negative inverse.

**7.2.6 Configuration register F (0x05)**

| D7    | D6    | D5    | D4  | D3  | D2   | D1  | D0  |
|-------|-------|-------|-----|-----|------|-----|-----|
| PWMS2 | PWMS1 | PWMS0 | BQL | PSL | DEMP | DRC | HPB |
| 0     | 0     | 0     | 0   | 0   | 0    | 0   | 0   |

| Bit | RW | RST | Name | Description                                                                                        |
|-----|----|-----|------|----------------------------------------------------------------------------------------------------|
| 0   | RW | 0   | HPB  | High-pass filter bypass bit: setting of one bypasses internal AC coupling digital high-pass filter |

The STA308A features an internal digital high-pass filter for the purpose of AC coupling. The purpose of this filter is to prevent DC signals from passing through a DDX amplifier. DC signals can cause speaker damage.

If HPB = 1, then the filter that the high-pass filter utilizes is made available as user-programmable biquad#1.

| Bit | RW | RST | Name | Description                                                                                                                           |
|-----|----|-----|------|---------------------------------------------------------------------------------------------------------------------------------------|
| 1   | RW | 0   | DRC  | Dynamic range compression/anti-clipping<br>0: limiters act in anti-clipping mode<br>1: limiters act in dynamic range compression mode |

Both limiters can be used in one of two ways, anti-clipping or dynamic range compression. When used in anti-clipping mode the limiter threshold values are constant and dependent on the limiter settings.

In dynamic range compression mode the limiter threshold values vary with the volume settings allowing a nighttime listening mode that provides a reduction in the dynamic range regardless of the volume level.

| Bit | RW | RST | Name | Description                                         |
|-----|----|-----|------|-----------------------------------------------------|
| 2   | RW | 0   | DEMP | De-emphasis:<br>0: no de-emphasis<br>1: de-emphasis |

By setting this bit to one de-emphasis will implemented on all channels. When this is used it takes the place of biquad #7 in each channel and any coefficients using biquad #1 will be ignored. DSPB (DSP bypass) bit must be set to 0 for de-emphasis to function.

| Bit | RW | RST | Name | Description                                                                                                             |
|-----|----|-----|------|-------------------------------------------------------------------------------------------------------------------------|
| 3   | RW | 0   | PSL  | Post-scale link:<br>0: each channel uses individual post-scale value<br>1: each channel uses channel 1 post-scale value |

Post-Scale functionality can be used for power-supply error correction. For multi-channel applications running off the same power-supply, the post-scale values can be linked to the value of channel 1 for ease of use and update the values faster.

| Bit | RW | RST | Name | Description                                                                                                  |
|-----|----|-----|------|--------------------------------------------------------------------------------------------------------------|
| 4   | RW | 0   | BQL  | Biquad link:<br>0: each channel uses coefficient values<br>1: each channel uses channel 1 coefficient values |

For ease of use, all channels can use the biquad coefficients loaded into the channel 1 Coefficient RAM space by setting the BQL bit to 1. Therefore, any EQ updates only have to be performed once.

| Bit | RW | RST | Name      | Description          |
|-----|----|-----|-----------|----------------------|
| 7:5 | RW | 00  | PWMS[2:0] | PWM speed selection: |

| PWMS[1:0] | PWM output speed                                         |
|-----------|----------------------------------------------------------|
| 000       | Normal speed (384 kHz) (all channels)                    |
| 001       | Half-speed (192 kHz) (all channels)                      |
| 010       | Double-speed (768 kHz) (all channels)                    |
| 011       | Normal speed (channels 1-6), double-speed (channels 7-8) |
| 100       | Odd speed (341.3 kHz) (all channels)                     |

7.2.7 Configuration register G (0x06)

| D7   | D6   | D5  | D4   | D3  | D2  | D1  | D0   |
|------|------|-----|------|-----|-----|-----|------|
| MPCV | DCCV | HPE | AM2E | AME | COD | SID | PWMD |
| 0    | 0    | 0   | 0    | 0   | 0   | 0   | 0    |

| Bit | RW | RST | Name | Description                                                                                                            |
|-----|----|-----|------|------------------------------------------------------------------------------------------------------------------------|
| 0   | RW | 0   | PWMD | PWM output disable:<br>0: PWM output normal<br>1: no PWM output                                                        |
| 1   | RW | 0   | SID  | Serial interface (I <sup>2</sup> S out) disable:<br>0: I <sup>2</sup> S output normal<br>1: no I <sup>2</sup> S output |
| 2   | RW | 0   | COD  | Clock output disable:<br>0: clock output normal<br>1: no clock output                                                  |

| Bit | RW | RST | Name | Description                                                                        |
|-----|----|-----|------|------------------------------------------------------------------------------------|
| 3   | RW | 0   | AME  | AM mode enable:<br>0: normal DDX operation.<br>1: AM reduction mode DDX operation. |

The STA308A features a DDX processing mode that minimizes the amount of noise generated in frequency range of AM radio. This mode is intended for use when DDX is operating in a device with an AM tuner active. The SNR of the DDX processing is reduced to ~83 dB in this mode, which is still greater than the SNR of AM radio.

| Bit | RW | RST | Name | Description                                                                          |
|-----|----|-----|------|--------------------------------------------------------------------------------------|
| 4   | RW | 0   | AM2E | AM2 mode enable:<br>0: normal DDX operation.<br>1: AM2 reduction mode DDX operation. |

The STA308A features a 2 DDX processing modes that minimize the amount of noise generated in frequency range of AM radio. This second mode is intended for use when DDX is operating in a device with an AM tuner active. This mode eliminates the noise-shaper.

| Bit | RW | RST | Name | Description                                                                                                  |
|-----|----|-----|------|--------------------------------------------------------------------------------------------------------------|
| 5   | RW | 0   | HPE  | DDX headphone enable:<br>0: channels 7 and 8 normal DDX operation<br>1: channels 7 and 8 headphone operation |

Channels 7 and 8 can be configured to be processed and output in such a manner that headphones can be driven using an appropriate output device. This signal is a differential 3-wire drive called DDX Headphone.

| Bit | RW | RST | Name | Description                                                                                            |
|-----|----|-----|------|--------------------------------------------------------------------------------------------------------|
| 6   | RW | 0   | DCCV | Distortion compensation variable enable:<br>0: uses preset DC coefficient.<br>1: uses DCC coefficient. |

| Bit | RW | RST | Name | Description                                                                                               |
|-----|----|-----|------|-----------------------------------------------------------------------------------------------------------|
| 7   | RW | 0   | MPCV | Max power correction variable:<br>0: use standard MPC coefficient<br>1: use MPCC bits for MPC coefficient |

### 7.2.8 Configuration register H (0x07)

| D7   | D6   | D5   | D4  | D3  | D2  | D1  | D0   |
|------|------|------|-----|-----|-----|-----|------|
| ECLE | LDTE | BCLE | IDE | ZDE | SVE | ZCE | NSBW |
| 0    | 1    | 1    | 1   | 1   | 1   | 1   | 0    |

| Bit | RW | RST | Name | Description                                                                                     |
|-----|----|-----|------|-------------------------------------------------------------------------------------------------|
| 0   | RW | 0   | NSBW | Noise-shaper bandwidth selection:<br>1: 3 <sup>rd</sup> order NS<br>0: 4 <sup>th</sup> order NS |

| Bit | RW | RST | Name | Description                                                                                                                                     |
|-----|----|-----|------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | RW | 1   | ZCE  | Zero-crossing volume enable:<br>1: volume adjustments will only occur at digital zero-crossings<br>0: volume adjustments will occur immediately |

The ZCE bit enables zero-crossing volume adjustments. When volume is adjusted on digital zero-crossings no clicks will be audible.

| Bit | RW | RST | Name | Description                                                                                             |
|-----|----|-----|------|---------------------------------------------------------------------------------------------------------|
| 2   | RW | 1   | SVE  | Soft volume enable:<br>1: volume adjustments use soft volume<br>0: volume adjustments occur immediately |

| Bit | RW | RST | Name | Description                                                                  |
|-----|----|-----|------|------------------------------------------------------------------------------|
| 3   | RW | 1   | ZDE  | Zero-detect mute enable: setting of 1 enables the automatic zero-detect mute |

Setting the ZDE bit enables the zero-detect automatic mute. The zero-detect circuit looks at the input data to each processing channel after the channel-mapping block. If any channel receives 2048 consecutive zero value samples (regardless of fs) then that individual channel is muted if this function is enabled.

| Bit | RW | RST | Name | Description                                                                            |
|-----|----|-----|------|----------------------------------------------------------------------------------------|
| 4   | RW | 1   | IDE  | Invalid input detect mute enable:<br>1: enable the automatic invalid input detect mute |

Setting the IDE bit enables this function, which looks at the input I<sup>2</sup>S data and will automatically mute if the signals are perceived as invalid.

| Bit | RW | RST | Name | Description                                    |
|-----|----|-----|------|------------------------------------------------|
| 5   | RW | 1   | BCLE | Binary output mode clock loss detection enable |

Detects loss of input MCLK in binary mode and will output 50% duty cycle.

| Bit | RW | RST | Name | Description                            |
|-----|----|-----|------|----------------------------------------|
| 6   | RW | 1   | LDTE | LRCLK double trigger protection enable |

Actively prevents double trigger of LRCLK.

| Bit | RW | RST | Name | Description             |
|-----|----|-----|------|-------------------------|
| 7   | RW | 0   | ECLE | Auto EAPD on clock loss |

When active will issue a device power down signal (EAPD) on clock loss detection

### 7.2.9 Configuration register I (0x08)

| D7   | D6 | D5 | D4 | D3 | D2 | D1 | D0   |
|------|----|----|----|----|----|----|------|
| EAPD |    |    |    |    |    |    | PSCE |
| 0    |    |    |    |    |    |    | 0    |

This feature utilizes an ADC on SDI78 that provides power supply ripple information for correction. Registers PSC1, PSC2, PSC3 are utilized in this mode.

| Bit | RW | RST | Name | Description                                                                             |
|-----|----|-----|------|-----------------------------------------------------------------------------------------|
| 0   | RW | 0   | PSCE | Power supply ripple correction enable:<br>0: normal operation<br>1: PSCorrect operation |

| Bit | RW | RST | Name | Description                                                                                        |
|-----|----|-----|------|----------------------------------------------------------------------------------------------------|
| 7   | RW | 0   | EAPD | External amplifier power down:<br>0: external power stage power down active<br>1: normal operation |

**7.2.10 Master mute register (0x09)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0    |
|----|----|----|----|----|----|----|-------|
|    |    |    |    |    |    |    | MMUTE |
|    |    |    |    |    |    |    | 0     |

**7.2.11 Master volume register (0x0A)**

| D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| MV7 | MV6 | MV5 | MV4 | MV3 | MV2 | MV1 | MV0 |
| 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

Note: Value of volume derived from MVOL is dependent on AMV AutoMode volume settings.

**7.2.12 Channel 1 volume (0x0B)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C1V7 | C1V6 | C1V5 | C1V4 | C1V3 | C1V2 | C1V1 | C1V0 |
| 0    | 1    | 1    | 0    | 0    | 0    | 0    | 0    |

**7.2.13 Channel 2 volume (0x0C)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C2V7 | C2V6 | C2V5 | C2V4 | C2V3 | C2V2 | C2V1 | C2V0 |
| 0    | 1    | 1    | 0    | 0    | 0    | 0    | 0    |

**7.2.14 Channel 3 volume (0x0D)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C3V7 | C3V6 | C3V5 | C3V4 | C3V3 | C3V2 | C3V1 | C3V0 |
| 0    | 1    | 1    | 0    | 0    | 0    | 0    | 0    |

**7.2.15 Channel 4 volume (0x0E)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C4V7 | C4V6 | C4V5 | C4V4 | C4V3 | C4V2 | C4V1 | C4V0 |
| 0    | 1    | 1    | 0    | 0    | 0    | 0    | 0    |



**7.2.16 Channel 5 volume (0x0F)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C5V7 | C5V6 | C5V5 | C5V4 | C5V3 | C5V2 | C5V1 | C5V0 |
| 0    | 1    | 1    | 0    | 0    | 0    | 0    | 0    |

**7.2.17 Channel 6 volume (0x10)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C6V7 | C6V6 | C6V5 | C6V4 | C6V3 | C6V2 | C6V1 | C6V0 |
| 0    | 1    | 1    | 0    | 0    | 0    | 0    | 0    |

**7.2.18 Channel 7 volume (0x11)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C7V7 | C7V6 | C7V5 | C7V4 | C7V3 | C7V2 | C7V1 | C7V0 |
| 0    | 1    | 1    | 0    | 0    | 0    | 0    | 0    |

**7.2.19 Channel 8 volume (0x12)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C8V7 | C8V6 | C8V5 | C8V4 | C8V3 | C8V2 | C8V1 | C8V0 |
| 0    | 1    | 1    | 0    | 0    | 0    | 0    | 0    |

**7.2.20 Channel 1 volume trim, mute, bypass (0x13)**

| D7  | D6    | D5 | D4    | D3    | D2    | D1    | D0    |
|-----|-------|----|-------|-------|-------|-------|-------|
| C1M | C1VBP |    | C1VT4 | C1VT3 | C1VT2 | C1VT1 | C1VT0 |
| 0   | 0     | 0  | 1     | 0     | 0     | 0     | 0     |

**7.2.21 Channel 2 volume trim, mute, bypass (0x14)**

| D7  | D6    | D5 | D4    | D3    | D2    | D1    | D0    |
|-----|-------|----|-------|-------|-------|-------|-------|
| C2M | C2VBP |    | C2VT4 | C2VT3 | C2VT2 | C2VT1 | C2VT0 |
| 0   | 0     | 0  | 1     | 0     | 0     | 0     | 0     |

**7.2.22 Channel 3 volume trim, mute, bypass (0x15)**

| D7  | D6    | D5 | D4    | D3    | D2    | D1    | D0    |
|-----|-------|----|-------|-------|-------|-------|-------|
| C3M | C3VBP |    | C3VT4 | C3VT3 | C3VT2 | C3VT1 | C3VT0 |
| 0   | 0     | 0  | 1     | 0     | 0     | 0     | 0     |

**7.2.23 Channel 4 volume trim, mute, bypass (0x16)**

| D7  | D6    | D5 | D4    | D3    | D2    | D1    | D0    |
|-----|-------|----|-------|-------|-------|-------|-------|
| C4M | C4VBP |    | C4VT4 | C4VT3 | C4VT2 | C4VT1 | C4VT0 |
| 0   | 0     | 0  | 1     | 0     | 0     | 0     | 0     |

**7.2.24 Channel 5 volume trim, mute, bypass (0x17)**

| D7  | D6    | D5 | D4    | D3    | D2    | D1    | D0    |
|-----|-------|----|-------|-------|-------|-------|-------|
| C5M | C5VBP |    | C5VT4 | C5VT3 | C5VT2 | C5VT1 | C5VT0 |
| 0   | 0     | 0  | 1     | 0     | 0     | 0     | 0     |

**7.2.25 Channel 6 volume trim, mute, bypass (0x18)**

| D7  | D6    | D5 | D4    | D3    | D2    | D1    | D0    |
|-----|-------|----|-------|-------|-------|-------|-------|
| C6M | C6VBP |    | C6VT4 | C6VT3 | C6VT2 | C6VT1 | C6VT0 |
| 0   | 0     | 0  | 1     | 0     | 0     | 0     | 0     |

**7.2.26 Channel 7 volume trim, mute, bypass (0x19)**

| D7  | D6    | D5 | D4    | D3    | D2    | D1    | D0    |
|-----|-------|----|-------|-------|-------|-------|-------|
| C7M | C7VBP |    | C7VT4 | C7VT3 | C7VT2 | C7VT1 | C7VT0 |
| 0   | 0     | 0  | 1     | 0     | 0     | 0     | 0     |

**7.2.27 Channel 8 volume trim, mute, bypass (0x1A)**

| D7  | D6    | D5 | D4    | D3    | D2    | D1    | D0    |
|-----|-------|----|-------|-------|-------|-------|-------|
| C8M | C8VBP |    | C8VT4 | C8VT3 | C8VT2 | C8VT1 | C8VT0 |
| 0   | 0     | 0  | 1     | 0     | 0     | 0     | 0     |

The volume structure of the STA308A consists of individual volume registers for each channel and a master volume register that provides an offset to each channels volume setting. There is also an additional offset for each channel called the channel volume trim. The individual channel volumes are adjustable in 0.5 dB steps from +48 dB to -78 dB. As an example if C5V = 0xXX or +XXX dB and MV = 0xXX or -XX dB, then the total gain for channel 5 = XX dB. The channel volume trim is adjustable independently on each channel from -10 dB to +10 dB in 1 dB steps. The master mute when set to 1 will mute all channels at once, whereas the individual channel mutes (CnM) will mute only that channel. Both the master mute and the channel mutes provide a "soft mute" with the volume ramping down to mute in 8192 samples from the maximum volume setting at the internal processing rate (~192 kHz). A "hard mute" can be obtained by commanding a value of 0xFF (255) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register any channel that whose total volume is less than -91 dB will be muted. All changes in volume take place at zero-crossings when ZCE = 1 (configuration register H) on a per channel basis as this creates the smoothest possible volume transitions.

When ZCE = 0, volume updates occur immediately. Each channel also contains an individual channel volume bypass. If a particular channel has volume bypassed via the CnVBP = 1 register then only the channel volume setting for that particular channel affects the volume setting, the master volume setting will not affect that channel. Each channel also contains a channel mute. If CnM = 1 a soft mute is performed on that channel.

| MV[7:0] | Volume offset from channel value |
|---------|----------------------------------|
| 0x00    | 0 dB                             |
| 0x01    | -0.5 dB                          |
| 0x02    | -1 dB                            |
| ...     | ...                              |
| 0x4C    | -38 dB                           |
| ...     | ...                              |
| 0xFE    | -127 dB                          |
| 0xFF    | Hardware channel mute            |

| CnV[7:0] | Volume                |
|----------|-----------------------|
| 0x00     | +48 dB                |
| 0x01     | +47.5 dB              |
| 0x02     | +47 dB                |
| ...      | ...                   |
| 0x5F     | +0.5 dB               |
| 0x60     | 0 dB                  |
| 0x61     | -0.5 dB               |
| ...      | ...                   |
| 0xFE     | -79.5 dB              |
| 0xFF     | Hardware channel mute |

| CnVT[4:0]    | Volume |
|--------------|--------|
| 0x00 to 0x06 | +10 dB |
| 0x07         | +9 dB  |
| ...          | ...    |
| 0x0F         | +1 dB  |
| 0x10         | 0 dB   |
| 0x11         | -1 dB  |
| ...          | ...    |
| 0x19         | -9 dB  |
| 0x1A to 0x1F | -10 dB |

**7.2.28 Channel input mapping channels 1 and 2 (0x1B)**

| D7 | D6    | D5    | D4    | D3 | D2    | D1    | D0    |
|----|-------|-------|-------|----|-------|-------|-------|
|    | C2IM2 | C2IM1 | C2IM0 |    | C1IM2 | C1IM1 | C1IM0 |
|    | 0     | 0     | 1     |    | 0     | 0     | 0     |

**7.2.29 Channel input mapping channels 3 and 4 (0x1C)**

| D7 | D6    | D5    | D4    | D3 | D2    | D1    | D0    |
|----|-------|-------|-------|----|-------|-------|-------|
|    | C4IM2 | C4IM1 | C4IM0 |    | C3IM2 | C3IM1 | C3IM0 |
|    | 0     | 1     | 1     |    | 0     | 1     | 0     |

**7.2.30 Channel input mapping channels 5 and 6 (0x1D)**

| D7 | D6    | D5    | D4    | D3 | D2    | D1    | D0    |
|----|-------|-------|-------|----|-------|-------|-------|
|    | C6IM2 | C6IM1 | C6IM0 |    | C5IM2 | C5IM1 | C5IM0 |
|    | 1     | 0     | 1     |    | 1     | 0     | 0     |

**7.2.31 Channel input mapping channels 7 and 8 (0x1E)**

| D7 | D6    | D5   | D4    | D3 | D2    | D1    | D0    |
|----|-------|------|-------|----|-------|-------|-------|
|    | C8IM2 | C8M1 | C8IM0 |    | C7IM2 | C7IM1 | C7IM0 |
|    | 1     | 1    | 1     |    | 1     | 1     | 0     |

Each channel received via I<sup>2</sup>S can be mapped to any internal processing channel via the channel input mapping registers. This allows for flexibility in processing, simplifies output stage designs, and enables the ability to perform crossovers. The default settings of these registers map each I<sup>2</sup>S input channel to its corresponding processing channel.

| CnIM[2:0] | Serial input from |
|-----------|-------------------|
| 000       | Channel 1         |
| 001       | Channel 2         |
| 010       | Channel 3         |
| 011       | Channel 4         |
| 100       | Channel 5         |
| 101       | Channel 6         |
| 110       | Channel 7         |
| 111       | Channel 8         |

7.2.32 AUTO1 - AutoModes EQ, volume, GC (0x1F)

| D7   | D6    | D5    | D4    | D3   | D2   | D1    | D0    |
|------|-------|-------|-------|------|------|-------|-------|
| AMDM | AMGC2 | AMGC1 | AMGC0 | AMV1 | AMV0 | AMEQ1 | AMEQ0 |
| 0    | 0     | 0     | 0     | 0    | 0    | 0     | 0     |

| Bit | RW | RST | Name      | Description                                                                                                                                         |
|-----|----|-----|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0 | RW | 0   | AMEQ[1:0] | Biquad 2-6 mode is:<br>00: user programmable<br>01: preset EQ - PEQ bits<br>10: graphic EQ - xGEQ bits<br>11: auto volume controlled loudness curve |

By setting AMEQ to any setting other than 00 enables AutoMode EQ, biquads 1-5 are not user programmable. Any coefficient settings for these biquads will be ignored. Also when AutoMode EQ is used the pre-scale value for channels 1-6 becomes hard-set to -18 dB.

| Bit | RW | RST | Name      | Description                                                                                                                                                                                                                                                                   |
|-----|----|-----|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:2 | RW | 0   | AMV[1:0]  | AutoMode volume mode (MVOL) is:<br>00: MVOL 0.5 dB 256 steps (standard)<br>01: MVOL auto curve 30 steps<br>10: MVOL auto curve 40 steps<br>11: MVOL auto curve 50 steps                                                                                                       |
| 6:4 | RW | 0   | AMGC[2:0] | AutoMode gain compression/limiters mode is:<br>000: user programmable GC<br>001: AC no clipping<br>010: AC limited clipping (10%)<br>011: DRC nighttime listening mode<br>100: DRC TV commercial/channel AGC<br>101: AC 5.1 no clipping<br>110: AC 5.1 limited clipping (10%) |

| Bit | RW | RST | Name | Description                                                                                           |
|-----|----|-----|------|-------------------------------------------------------------------------------------------------------|
| 7   | RW | 0   | AMDM | AutoMode 5.1 downmix:<br>0: normal operation<br>1: channels 7-8 are 2-channel downmix of channels 1-6 |

AutoMode downmix setting uses channels 7-8 of Mix#1 engine and therefore these channels of this function are fixed and not allowed to be user set when in this mode.

Channels 1-6 must be arranged via channel mapping (registers CnIM) if necessary in the following manner for this operation:

- Channel 1: left
- Channel 2: right
- Channel 3: left surround
- Channel 4: right surround
- Channel 5: center
- Channel 6: LFE.

**7.2.33 AUTO2 - AutoModes bass management2 (0x20)**

| D7  | D6   | D5   | D4   | D3   | D2  | D1     | D0     |
|-----|------|------|------|------|-----|--------|--------|
| SUB | RSS1 | RSS0 | CSS1 | CSS0 | FSS | AMBMXE | AMBMME |
| 1   | 0    | 0    | 0    | 0    | 0   | 0      | 0      |

| Bit | RW | RST | Name   | Description                                                                         |
|-----|----|-----|--------|-------------------------------------------------------------------------------------|
| 0   | RW | 0   | AMBMME | 0: AutoMode bass management mix disabled<br>1: AutoMode bass management mix enabled |

| Bit | RW | RST | Name   | Description                                                                                     |
|-----|----|-----|--------|-------------------------------------------------------------------------------------------------|
| 1   | RW | 0   | AMBMXE | 0: AutoMode bass management crossover disabled<br>1: AutoMode bass management crossover enabled |

Setting the AMBMME bit enables the proper mixing to take place for various preset bass management configurations. Setting the AMBMXE bit enables the proper crossover filtering in biquad #7 to take place. The crossover for bass management is always 2<sup>nd</sup> order (24 dB/oct) and the crossover frequency is determined by register bits PREEQ.XO[2:0].

All configurations of Dolby Bass Management can be performed in the IC. These different configurations are selected as they would be by the end-user.

The AutoMode bass management settings utilize channels 1-6 on the Mix #1 engine, Channels 1-6 biquad #6, and channels 1-2 on the mix #2 engine in configuration #2. These functions cannot be user programmed while the bass management automode is active.

Not all settings are valid as some configurations are unlikely and do not have to be supported by Dolby specification.

Automatic crossover settings are provided or custom crossovers can be implemented using the available programmable biquads.

Input channels must be mapped using channel-mapping feature in the following manner for bass management to be performed properly.

- 1: left front
- 2: right front
- 3: left rear
- 4: right rear
- 5: center
- 6: LFE

| Bitfield                  | 10  | 01    | 00    |
|---------------------------|-----|-------|-------|
| CSS - center speaker size | Off | Large | Small |
| RSS - rear speaker size   | Off | Large | Small |

| Bitfield                 | 1     | 0     |
|--------------------------|-------|-------|
| FSS - front speaker size | Large | Small |
| SUB - subwoofer          | On    | Off   |

When AMBMXE = 1, biquad #7 on channels 1-6 are utilized for bass-management crossover filter, this biquad is not user programmable in this mode. The XO settings determine the crossover frequency used, the crossover is 2<sup>nd</sup> order for both high-pass and low-pass with a -3 dB cross point. Higher order filters can be obtained by programming coefficients in other biquads if desired.

It is recommended to use settings of 120-160 Hz when using small, single driver satellite speakers as the frequency response of these speakers normally are limited to this region.

### 7.2.34 AUTO3 - AutoMode AM/pre-Scale/bass management scale (0x21)

| D7    | D6    | D5    | D4    | D3 | D2 | D1  | D0   |
|-------|-------|-------|-------|----|----|-----|------|
| AMAM2 | AMAM1 | AMAM0 | AMAME |    |    | MSA | AMPS |
| 0     | 0     | 0     | 0     |    |    | 0   | 0    |

| Bit | RW | RST | Name | Description                                                                                                   |
|-----|----|-----|------|---------------------------------------------------------------------------------------------------------------|
| 0   | RW | 0   | AMPS | AutoMode pre-scale<br>0: -18 dB used for pre-scale when AMEQ = 00<br>1: user defined pre-scale when AMEQ = 00 |

| Bit | RW | RST | Name | Description                                                                                                                                      |
|-----|----|-----|------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | RW | 0   | MSA  | Bass management mix scale adjustment<br>0: -12 dB scaling on satellite channels in Config #1<br>1: no scaling on satellite channels in Config #1 |

| Bit | RW | RST | Name  | Description                                                                                                                    |
|-----|----|-----|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 4   | RW | 0   | AMAME | AutoMode AM enable<br>0: switching frequency determined by PWMS settings<br>1: switching frequency determined by AMAM settings |

| AMAM[2:0] | 48 kHz/96 kHz input Fs | 44.1 / 88.2 kHz input Fs |
|-----------|------------------------|--------------------------|
| 000       | 0.535 MHz - 0.720 MHz  | 0.535 MHz - 0.670 MHz    |
| 001       | 0.721 MHz - 0.900 MHz  | 0.671 MHz - 0.800 MHz    |
| 010       | 0.901 MHz - 1.100 MHz  | 0.801 MHz - 1.000 MHz    |
| 011       | 1.101 MHz - 1.300 MHz  | 1.001 MHz - 1.180 MHz    |
| 100       | 1.301 MHz - 1.480 MHz  | 1.181 MHz - 1.340 MHz    |
| 101       | 1.481 MHz - 1.600 MHz  | 1.341 MHz - 1.500 MHz    |
| 110       | 1.601 MHz - 1.700 MHz  | 1.501 MHz - 1.700 MHz    |

## 7.2.35 PREEQ - Preset EQ settings (0x22)

| D7  | D6  | D5  | D4   | D3   | D2   | D1   | D0   |
|-----|-----|-----|------|------|------|------|------|
| XO2 | XO1 | XO0 | PEQ4 | PEQ3 | PEQ2 | PEQ1 | PEQ0 |
| 1   | 0   | 1   | 0    | 0    | 0    | 0    | 0    |

| XO[2:0] | Bass management crossover frequency |
|---------|-------------------------------------|
| 000     | 70 Hz                               |
| 001     | 80 Hz                               |
| 010     | 90 Hz                               |
| 011     | 100 Hz                              |
| 100     | 110 Hz                              |
| 101     | 120 Hz                              |
| 110     | 140 Hz                              |
| 111     | 160 Hz                              |

| PEQ[4:0] | Mode / setting |
|----------|----------------|
| 00000    | Flat           |
| 00001    | Rock           |
| 00010    | Soft Rock      |
| 00011    | Jazz           |
| 00100    | Classical      |
| 00101    | Dance          |
| 00110    | Pop            |
| 00111    | Soft           |
| 01000    | Hard           |
| 01001    | Party          |
| 01010    | Vocal          |
| 01011    | Hip-Hop        |
| 01100    | Dialog         |
| 01101    | Bass-boost #1  |
| 01110    | Bass-boost #2  |
| 01111    | Bass-boost #3  |
| 10000    | Loudness 1     |
| 10001    | Loudness 2     |
| 10010    | Loudness 3     |
| 10011    | Loudness 4     |



|       |             |
|-------|-------------|
| 10100 | Loudness 5  |
| 10101 | Loudness 6  |
| 10110 | Loudness 7  |
| 10111 | Loudness 8  |
| 11000 | Loudness 9  |
| 11001 | Loudness 10 |
| 11010 | Loudness 11 |
| 11011 | Loudness 12 |
| 11100 | Loudness 13 |
| 11101 | Loudness 14 |
| 11110 | Loudness 15 |
| 11111 | Loudness 16 |

**7.2.36 AGEQ - graphic EQ 80-Hz band (0x23)**

| D7 | D6 | D5 | D4    | D3    | D2    | D1    | D0    |
|----|----|----|-------|-------|-------|-------|-------|
|    |    |    | AGEQ4 | AGEQ3 | AGEQ2 | AGEQ1 | AGEQ0 |
|    |    |    | 0     | 1     | 1     | 1     | 1     |

**7.2.37 BGEQ - graphic EQ 300-Hz band (0x24)**

| D7 | D6 | D5 | D4    | D3    | D2    | D1    | D0    |
|----|----|----|-------|-------|-------|-------|-------|
|    |    |    | BGEQ4 | BGEQ3 | BGEQ2 | BGEQ1 | BGEQ0 |
|    |    |    | 0     | 1     | 1     | 1     | 1     |

**7.2.38 CGEQ - graphic EQ 1-kHz band (0x25)**

| D7 | D6 | D5 | D4    | D3    | D2    | D1    | D0    |
|----|----|----|-------|-------|-------|-------|-------|
|    |    |    | CGEQ4 | CGEQ3 | CGEQ2 | CGEQ1 | CGEQ0 |
|    |    |    | 0     | 1     | 1     | 1     | 1     |

**7.2.39 DGEQ - graphic EQ 3-kHz band (0x26)**

| D7 | D6 | D5 | D4    | D3    | D2    | D1    | D0    |
|----|----|----|-------|-------|-------|-------|-------|
|    |    |    | DGEQ4 | DGEQ3 | DGEQ2 | DGEQ1 | DGEQ0 |
|    |    |    | 0     | 1     | 1     | 1     | 1     |

**7.2.40 EGEQ - graphic EQ 8-kHz band (0x27)**

| D7 | D6 | D5 | D4    | D3    | D2    | D1    | D0    |
|----|----|----|-------|-------|-------|-------|-------|
|    |    |    | EGEQ4 | EGEQ3 | EGEQ2 | EGEQ1 | EGEQ0 |
|    |    |    | 0     | 1     | 1     | 1     | 1     |

| xGEQ[4:0] | Boost / cut |
|-----------|-------------|
| 11111     | +16         |
| 11110     | +15         |
| 11101     | +14         |
| ...       | ...         |
| 10000     | +1          |
| 01111     | 0           |
| 01110     | -1          |
| ...       | ...         |
| 00001     | -14         |
| 00000     | -15         |

**7.2.41 Biquad internal channel loop-through (0x28)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C8BLP | C7BLP | C6BLP | C5BLP | C4BLP | C3BLP | C2BLP | C1BLP |
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

Each internal processing channel can receive two possible inputs at the input to the biquad block. The input can come either from the output of that channel's MIX#1 engine or from the output of the bass/treble (Biquad#10) of the previous channel. In this scenario, channel 1 receives channel 8. This enables the use of more than 10 biquads on any given channel at the loss of the number of separate internal processing channels.

| Bit | RW | RST | Name  | Description                                                                                                                                            |
|-----|----|-----|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | RW | 0   | CnBLP | For n = 1 to 8:<br>0: input from channel n MIX#1 engine output - normal operation<br>1: input from channel (n - 1) biquad #10 output - loop operation. |

**7.2.42 Mix internal channel loop-through (0x29)**

| D7     | D6     | D5     | D4     | D3     | D2     | D1     | D0     |
|--------|--------|--------|--------|--------|--------|--------|--------|
| C8MXLP | C7MXLP | C6MXLP | C5MXLP | C4MXLP | C3MXLP | C2MXLP | C1MXLP |
| 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      |

Each internal processing channel can receive two possible sets of inputs at the inputs to the Mix#1 block. The inputs can come from the outputs of the interpolation block as normally occurs (CnMXLP = 0) or they can come from the outputs of the Mix#2 block. This enables the use of additional filtering after the second mix block at the expense of losing this processing capability on the channel.

| Bit | RW | RST | Name   | Description                                                                                                                                                                             |
|-----|----|-----|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | RW | 0   | CnMXLP | For n = 1 to 8:<br>0: inputs to channel n MIX#1 engine from interpolation outputs - normal operation<br>1: inputs to channel n MIX#1 engine from MIX#2 engine outputs - loop operation. |

**7.2.43 EQ bypass (0x2A)**

| D7     | D6     | D5     | D4     | D3      | D2     | D1     | D0     |
|--------|--------|--------|--------|---------|--------|--------|--------|
| C8EQBP | C7EQBP | C6EQBP | C5EQBP | C4EQCBP | C3EQBP | C2EQBP | C1EQBP |
| 0      | 0      | 0      | 0      | 0       | 0      | 0      | 0      |

EQ control can be bypassed on a per channel basis. If EQ control is bypassed on a given channel the prescale and all 10 filters (high-pass, biquads, de-emphasis, bass management cross-over, bass, treble in any combination) are bypassed for that channel.

| Bit | RW | RST | Name   | Description                                                                                    |
|-----|----|-----|--------|------------------------------------------------------------------------------------------------|
| 7:0 | RW | 0   | CnEQBP | For n = 1 to 8:<br>0: perform EQ on channel n - normal operation<br>1: bypass EQ on channel n. |

**7.2.44 Tone control bypass (0x2B)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C8TCB | C7TCB | C6TCB | C5TCB | C4TCB | C3TCB | C2TCB | C1TCB |
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

Tone control (bass/treble) can be bypassed on a per channel basis. If tone control is bypassed on a given channel the two filters that tone control utilizes are made available as user programmable biquads #9 and #10.

**7.2.45 Tone control (0x2C)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| TTC3 | TTC2 | TTC1 | TTC0 | BTC3 | BTC2 | BTC1 | BTC0 |
| 0    | 1    | 1    | 1    | 0    | 1    | 1    | 1    |

This is the tone control boost / cut as a function of BTC and TTC bits.

| BTC[3:0] / TTC[3:0] | Boost / cut |
|---------------------|-------------|
| 0000                | -12 dB      |
| 0001                | -12 dB      |
| ...                 | ...         |
| 0111                | -4 dB       |
| 0110                | -2 dB       |
| 0111                | 0 dB        |
| 1000                | +2 dB       |
| 1001                | +4 dB       |
| ...                 | ...         |
| 1101                | +12 dB      |
| 1110                | +12 dB      |
| 1111                | +12dB       |

**7.2.46 Channel limiter select channels 1,2,3,4 (0x2D)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C4LS1 | C4LS0 | C3LS1 | C3LS0 | C2LS1 | C2LS0 | C1LS1 | C1LS0 |
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**7.2.47 Channel limiter select channels 5,6,7,8 (0x2E)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C8LS1 | C8LS0 | C7LS1 | C7LS0 | C6LS1 | C6LS0 | C5LS1 | C5LS0 |
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**7.2.48 Limiter 1 attack/release rate (0x2F)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| L1A3 | L1A2 | L1A1 | L1A0 | L1R3 | L1R2 | L1R1 | L1R0 |
| 0    | 1    | 1    | 0    | 1    | 0    | 1    | 0    |

**7.2.49 Limiter 1 attack/release threshold (0x30)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| L1AT3 | L1AT2 | L1AT1 | L1AT0 | L1RT3 | L1RT2 | L1RT1 | L1RT0 |
| 0     | 1     | 1     | 0     | 1     | 0     | 0     | 1     |

**7.2.50 Limiter 2 attack/release rate (0x31)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| L2A3 | L2A2 | L2A1 | L2A0 | L2R3 | L2R2 | L2R1 | L2R0 |
| 0    | 1    | 1    | 0    | 1    | 0    | 1    | 0    |

**7.2.51 Limiter 2 attack/release threshold (0x32)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| L2AT3 | L2AT2 | L2AT1 | L2AT0 | L2RT3 | L2RT2 | L2RT1 | L2RT0 |
| 0     | 1     | 1     | 0     | 1     | 0     | 0     | 1     |

**7.2.52 Bit description**

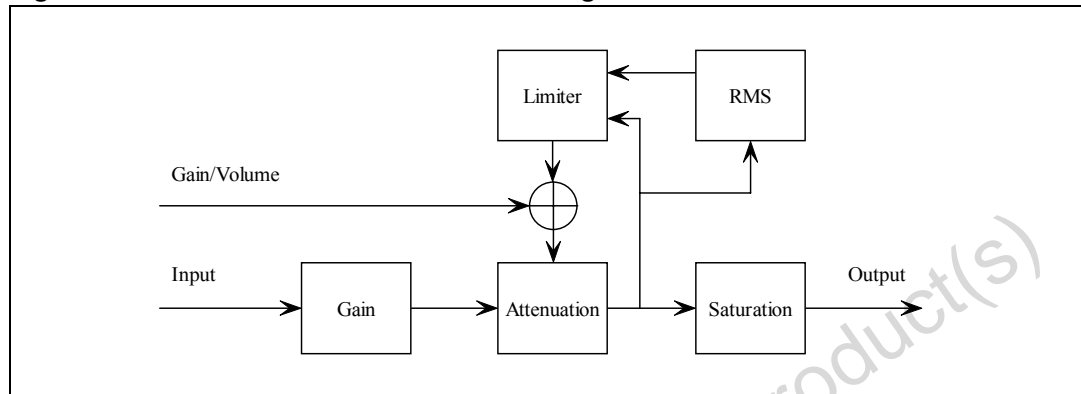
The STA308A includes two independent limiter blocks. The purpose of the limiters is to automatically reduce the dynamic range of a recording to prevent the outputs from clipping in anti-clipping mode or to actively reduce the dynamic range for a better listening environment such as a night-time listening mode which is often needed for DVDs. The two modes are selected via the DRC bit in Configuration Register B, bit 7 address 0x02. Each channel can be mapped to either limiter or not mapped, meaning that channel will clip when 0 dBFS is exceeded. Each limiter will look at the present value of each channel that is mapped to it, select the maximum absolute value of all these channels, perform the limiting algorithm on that value, and then if needed adjust the gain of the mapped channels in unison.

The limiter attack thresholds are determined by the LnAT registers. It is recommended in anti-clipping mode to set this to 0 dBFS, which corresponds to the maximum unclipped output power of a DDX amplifier. Since gain can be added digitally within the STA308A it is possible to exceed 0 dBFS or any other LnAT setting, when this occurs, the limiter, when active, will automatically start reducing the gain. The rate at which the gain is reduced when the attack threshold is exceeded is dependent upon the attack rate register setting for that limiter. The gain reduction occurs on a peak-detect algorithm.

The release of limiter, when the gain is again increased, is dependent on a RMS-detect algorithm. The output of the volume/limiter block is passed through a RMS filter. The output of this filter is compared to the release threshold, determined by the Release Threshold register. When the RMS filter output falls below the release threshold, the gain is again increased at a rate dependent upon the Release Rate register. The gain can never be increased past it's set value and therefore the release will only occur if the limiter has already reduced the gain. The release threshold value can be used to set what is effectively a minimum dynamic range, this is helpful as over-limiting can reduce the dynamic range to virtually zero and cause program material to sound lifeless.

In AC mode the attack and release thresholds are set relative to full-scale. In DRC mode the attack threshold is set relative to the maximum volume setting of the channels mapped to that limiter and the release threshold is set relative to the maximum volume setting plus the attack threshold.

**Figure 7. Basic limiter and volume flow diagram**



| CnLS[1,0] | Channel limiter mapping         |
|-----------|---------------------------------|
| 00        | Channel has limiting disabled   |
| 01        | Channel is mapped to limiter #1 |
| 10        | Channel is mapped to limiter #2 |

| LnA[3:0] | Attack rate (dB/ms) |
|----------|---------------------|
| 0000     | 3.1584 (fast)       |
| 0001     | 2.7072              |
| 0010     | 2.2560              |
| 0011     | 1.8048              |
| 0100     | 1.3536              |
| 0101     | 0.9024              |
| 0110     | 0.4512              |
| 0111     | 0.2256              |
| 1000     | 0.1504              |
| 1001     | 0.1123              |
| 1010     | 0.0902              |
| 1011     | 0.0752              |
| 1100     | 0.0645              |
| 1101     | 0.0564              |
| 1110     | 0.0501              |
| 1111     | 0.0451 (slow)       |

| <b>LnR[3:0]</b> | <b>Release rate (dB/ms)</b> |
|-----------------|-----------------------------|
| 0000            | 0.5116 (fast)               |
| 0001            | 0.1370                      |
| 0010            | 0.0744                      |
| 0011            | 0.0499                      |
| 0100            | 0.0360                      |
| 0101            | 0.0299                      |
| 0110            | 0.0264                      |
| 0111            | 0.0208                      |
| 1000            | 0.0198                      |
| 1001            | 0.0172                      |
| 1010            | 0.0147                      |
| 1011            | 0.0137                      |
| 1100            | 0.0134                      |
| 1101            | 0.0117                      |
| 1110            | 0.0110                      |
| 1111            | 0.0104 (slow)               |

| <b>LnAT[3:0]</b> | <b>Anti-clipping (AC)<br/>(dB relative to FS)</b> |
|------------------|---------------------------------------------------|
| 0000             | -12                                               |
| 0001             | -10                                               |
| 0010             | -8                                                |
| 0011             | -6                                                |
| 0100             | -4                                                |
| 0101             | -2                                                |
| 0110             | 0                                                 |
| 0111             | +2                                                |
| 1000             | +3                                                |
| 1001             | +4                                                |
| 1010             | +5                                                |
| 1011             | +6                                                |
| 1100             | +7                                                |
| 1101             | +8                                                |
| 1110             | +9                                                |
| 1111             | +10                                               |

| <b>LnRT[3:0]</b> | <b>Anti-clipping (AC)<br/>(dB relative to FS)</b> |
|------------------|---------------------------------------------------|
| 0000             | -∞                                                |
| 0001             | -29 dB                                            |
| 0010             | -20 dB                                            |
| 0011             | -16 dB                                            |
| 0100             | -14 dB                                            |
| 0101             | -12 dB                                            |
| 0110             | -10 dB                                            |
| 0111             | -8 dB                                             |
| 1000             | -7 dB                                             |
| 1001             | -6 dB                                             |
| 1010             | -5 dB                                             |
| 1011             | -4 dB                                             |
| 1100             | -3 dB                                             |
| 1101             | -2 dB                                             |
| 1110             | -1 dB                                             |
| 1111             | -0 dB                                             |

| <b>LnAT[3:0]</b> | <b>Dynamic range compression (DRC)<br/>(dB relative to volume)</b> |
|------------------|--------------------------------------------------------------------|
| 0000             | -31                                                                |
| 0001             | -29                                                                |
| 0010             | -27                                                                |
| 0011             | -25                                                                |
| 0100             | -23                                                                |
| 0101             | -21                                                                |
| 0110             | -19                                                                |
| 0111             | -17                                                                |
| 1000             | -16                                                                |
| 1001             | -15                                                                |
| 1010             | -14                                                                |
| 1011             | -13                                                                |
| 1100             | -12                                                                |
| 1101             | -10                                                                |
| 1110             | -7                                                                 |
| 1111             | -4                                                                 |



| LnRT[3:0] | Dynamic range compression (DRC)<br>(db relative to volume + LnAT) |
|-----------|-------------------------------------------------------------------|
| 0000      | -∞                                                                |
| 0001      | -38 dB                                                            |
| 0010      | -36 dB                                                            |
| 0011      | -33 dB                                                            |
| 0100      | -31 dB                                                            |
| 0101      | -30 dB                                                            |
| 0110      | -28 dB                                                            |
| 0111      | -26 dB                                                            |
| 1000      | -24 dB                                                            |
| 1001      | -22 dB                                                            |
| 1010      | -20 dB                                                            |
| 1011      | -18 dB                                                            |
| 1100      | -15 dB                                                            |
| 1101      | -12 dB                                                            |
| 1110      | -9 dB                                                             |
| 1111      | -6 dB                                                             |

**7.2.53 Channel 1 and 2 output timing (0x33)**

| D7 | D6    | D5    | D4    | D3 | D2    | D1    | D0    |
|----|-------|-------|-------|----|-------|-------|-------|
|    | C2OT2 | C2OT1 | C2OT0 |    | C1OT2 | C1OT1 | C1OT0 |
|    | 1     | 0     | 0     |    | 0     | 0     | 0     |

**7.2.54 Channel 3 and 4 output timing (0x34)**

| D7 | D6    | D5    | D4    | D3 | D2    | D1    | D0    |
|----|-------|-------|-------|----|-------|-------|-------|
|    | C4OT2 | C4OT1 | C4OT0 |    | C3OT2 | C3OT1 | C3OT0 |
|    | 1     | 1     | 0     |    | 0     | 1     | 0     |

**7.2.55 Channel 5 and 6 output timing (0x35)**

| D7 | D6    | D5    | D4    | D3 | D2    | D1    | D0    |
|----|-------|-------|-------|----|-------|-------|-------|
|    | C6OT2 | C6OT1 | C6OT0 |    | C5OT2 | C5OT1 | C5OT0 |
|    | 1     | 0     | 1     |    | 0     | 0     | 1     |

### 7.2.56 Channel 7 and 8 output timing (0x36)

| D7 | D6    | D5    | D4    | D3 | D2    | D1    | D0    |
|----|-------|-------|-------|----|-------|-------|-------|
|    | C8OT2 | C8OT1 | C8OT0 |    | C7OT2 | C7OT1 | C7OT0 |
|    | 1     | 1     | 1     |    | 0     | 1     | 1     |

The centering of the individual channel PWM output periods can be adjusted by the output timing registers. PWM slot settings can be chosen to insure that pulse transitions do not occur at the same time on different channels using the same power device. There are 8 possible settings, the appropriate setting varying based on the application and connections to the DDX power devices.

| CnOT[2:0] | PWM slot |
|-----------|----------|
| 000       | 1        |
| 001       | 2        |
| 010       | 3        |
| 011       | 4        |
| 100       | 5        |
| 101       | 6        |
| 110       | 7        |
| 111       | 8        |

### 7.2.57 Channel I<sup>2</sup>S output mapping channels 1 and 2 (0x37)

| D7 | D6    | D5    | D4    | D3 | D2    | D1    | D0    |
|----|-------|-------|-------|----|-------|-------|-------|
|    | C2OM2 | C2OM1 | C2OM0 |    | C1OM2 | C1OM1 | C1OM0 |
|    | 0     | 0     | 1     |    | 0     | 0     | 0     |

### 7.2.58 Channel I<sup>2</sup>S output mapping channels 3 and 4 (0x38)

| D7 | D6    | D5    | D4    | D3 | D2    | D1    | D0    |
|----|-------|-------|-------|----|-------|-------|-------|
|    | C4OM2 | C4OM1 | C4OM0 |    | C3OM2 | C3OM1 | C3OM0 |
|    | 0     | 1     | 1     |    | 0     | 1     | 0     |

### 7.2.59 Channel I<sup>2</sup>S output mapping channels 5 and 6 (0x39)

| D7 | D6    | D5    | D4    | D3 | D2    | D1    | D0    |
|----|-------|-------|-------|----|-------|-------|-------|
|    | C6OM2 | C6OM1 | C6OM0 |    | C5OM2 | C5OM1 | C5OM0 |
|    | 1     | 0     | 1     |    | 1     | 0     | 0     |

**7.2.60 Channel I<sup>2</sup>S output mapping channels 7 and 8 (0x3A)**

| D7 | D6    | D5   | D4    | D3 | D2    | D1    | D0    |
|----|-------|------|-------|----|-------|-------|-------|
|    | C8OM2 | C8M1 | C8OM0 |    | C7OM2 | C7OM1 | C7OM0 |
|    | 1     | 1    | 1     |    | 1     | 1     | 0     |

Each I<sup>2</sup>S output channel can receive data from any channel output of the volume block. Which channel a particular I<sup>2</sup>S output receives is dependent upon that channels CnOM register bits.

| CnOM[2:0] | Serial output from |
|-----------|--------------------|
| 000       | Channel 1          |
| 001       | Channel 2          |
| 010       | Channel 3          |
| 011       | Channel 4          |
| 100       | Channel 5          |
| 101       | Channel 6          |
| 110       | Channel 7          |
| 111       | Channel 8          |

**7.2.61 Coefficient address register 1 (0x3B)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1   | D0   |
|----|----|----|----|----|----|------|------|
|    |    |    |    |    |    | CFA9 | CFA8 |
|    |    |    |    |    |    | 0    | 0    |

**7.2.62 Coefficient address register 2 (0x3C)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| CFA7 | CFA6 | CFA5 | CFA4 | CFA3 | CFA2 | CFA1 | CFA0 |
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

**7.2.63 Coefficient b1 data register, bits 23:16 (0x3D)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C1B23 | C1B22 | C1B21 | C1B20 | C1B19 | C1B18 | C1B17 | C1B16 |
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**7.2.64 Coefficient b1 data register, bits 15:8 (0x3E)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1   | D0   |
|-------|-------|-------|-------|-------|-------|------|------|
| C1B15 | C1B14 | C1B13 | C1B12 | C1B11 | C1B10 | C1B9 | C1B8 |
| 0     | 0     | 0     | 0     | 0     | 0     | 0    | 0    |

**7.2.65 Coefficient b1 data register, bits 7:0 (0x3F)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C1B7 | C1B6 | C1B5 | C1B4 | C1B3 | C1B2 | C1B1 | C1B0 |
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

**7.2.66 Coefficient b2 data register, bits 23:16 (0x40)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C2B23 | C2B22 | C2B21 | C2B20 | C2B19 | C2B18 | C2B17 | C2B16 |
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**7.2.67 Coefficient b2 data register, bits 15:8 (0x41)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1   | D0   |
|-------|-------|-------|-------|-------|-------|------|------|
| C2B15 | C2B14 | C2B13 | C2B12 | C2B11 | C2B10 | C2B9 | C2B8 |
| 0     | 0     | 0     | 0     | 0     | 0     | 0    | 0    |

**7.2.68 Coefficient b2 data register, bits 7:0 (0x42)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C2B7 | C2B6 | C2B5 | C2B4 | C2B3 | C2B2 | C2B1 | C2B0 |
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

**7.2.69 Coefficient a1 data register, bits 23:16 (0x43)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C1B23 | C1B22 | C1B21 | C1B20 | C1B19 | C1B18 | C1B17 | C1B16 |
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**7.2.70 Coefficient a1 data register, bits 15:8 (0x44)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1   | D0   |
|-------|-------|-------|-------|-------|-------|------|------|
| C3B15 | C3B14 | C3B13 | C3B12 | C3B11 | C3B10 | C3B9 | C3B8 |
| 0     | 0     | 0     | 0     | 0     | 0     | 0    | 0    |

**7.2.71 Coefficient a1 data register, bits 7:0 (0x45)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C3B7 | C3B6 | C3B5 | C3B4 | C3B3 | C3B2 | C3B1 | C3B0 |
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

**7.2.72 Coefficient a2 data register, bits 23:16 (0x46)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C4B23 | C4B22 | C4B21 | C4B20 | C4B19 | C4B18 | C4B17 | C4B16 |
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**7.2.73 Coefficient a2 data register, bits 15:8 (0x47)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1   | D0   |
|-------|-------|-------|-------|-------|-------|------|------|
| C4B15 | C4B14 | C4B13 | C4B12 | C4B11 | C4B10 | C4B9 | C4B8 |
| 0     | 0     | 0     | 0     | 0     | 0     | 0    | 0    |

**7.2.74 Coefficient a2 data register, bits 7:0 (0x48)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C4B7 | C4B6 | C4B5 | C4B4 | C4B3 | C4B2 | C4B1 | C4B0 |
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

**7.2.75 Coefficient b0 data register, bits 23:16 (0x49)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C5B23 | C5B22 | C5B21 | C5B20 | C5B19 | C5B18 | C5B17 | C5B16 |
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**7.2.76 Coefficient b0 data register, bits 15:8 (0x4A)**

| D7    | D6    | D5    | D4    | D3    | D2    | D1   | D0   |
|-------|-------|-------|-------|-------|-------|------|------|
| C5B15 | C5B14 | C5B13 | C5B12 | C5B11 | C5B10 | C5B9 | C5B8 |
| 0     | 0     | 0     | 0     | 0     | 0     | 0    | 0    |

**7.2.77 Coefficient b0 data register, bits 7:0 (0x4B)**

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| C5B7 | C5B6 | C5B5 | C5B4 | C5B3 | C5B2 | C5B1 | C5B0 |
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

### 7.2.78 Coefficient write control register (0x4C)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    | WA | W1 |
|    |    |    |    |    |    | 0  | 0  |

Coefficients for EQ and Bass Management are handled internally in the STA308A via RAM. Access to this RAM is available to the user via an I<sup>2</sup>C register interface.

A collection of I<sup>2</sup>C registers are dedicated to this function. One contains a coefficient base address, five sets of three store the values of the 24-bit coefficients to be written or that were read, and one contains bits used to control the write of the coefficient(s) to RAM. The following are instructions for reading and writing coefficients.

### 7.3 Reading a coefficient from RAM

1. write top 2-bits of address to I<sup>2</sup>C register 0x3B
2. write bottom 8-bits of address to I<sup>2</sup>C register 0x3C
3. read top 8-bits of coefficient in I<sup>2</sup>C address 0x3D
4. read middle 8-bits of coefficient in I<sup>2</sup>C address 0x3E
5. read bottom 8-bits of coefficient in I<sup>2</sup>C address 0x3F

### 7.4 Reading a set of coefficients from RAM

1. write top 2-bits of address to I<sup>2</sup>C register 0x3B
2. write bottom 8-bits of address to I<sup>2</sup>C register 0x3C
3. read top 8-bits of coefficient in I<sup>2</sup>C address 0x3D
4. read middle 8-bits of coefficient in I<sup>2</sup>C address 0x3E
5. read bottom 8-bits of coefficient in I<sup>2</sup>C address 0x3F
6. read top 8-bits of coefficient b2 in I<sup>2</sup>C address 0x40
7. read middle 8-bits of coefficient b2 in I<sup>2</sup>C address 0x41
8. read bottom 8-bits of coefficient b2 in I<sup>2</sup>C address 0x42
9. read top 8-bits of coefficient a1 in I<sup>2</sup>C address 0x43
10. read middle 8-bits of coefficient a1 in I<sup>2</sup>C address 0x44
11. read bottom 8-bits of coefficient a1 in I<sup>2</sup>C address 0x45
12. read top 8-bits of coefficient a2 in I<sup>2</sup>C address 0x46
13. read middle 8-bits of coefficient a2 in I<sup>2</sup>C address 0x47
14. read bottom 8-bits of coefficient a2 in I<sup>2</sup>C address 0x48
15. read top 8-bits of coefficient b0 in I<sup>2</sup>C address 0x49
16. read middle 8-bits of coefficient b0 in I<sup>2</sup>C address 0x4A
17. read bottom 8-bits of coefficient b0 in I<sup>2</sup>C address 0x4B

## 7.5 Writing a single coefficient to RAM

1. write top 2-bits of address to I<sup>2</sup>C register 0x3B
2. write bottom 8-bits of address to I<sup>2</sup>C register 0x3C
3. write top 8-bits of coefficient in I<sup>2</sup>C address 0x3D
4. write middle 8-bits of coefficient in I<sup>2</sup>C address 0x3E
5. write bottom 8-bits of coefficient in I<sup>2</sup>C address 0x3F
6. write 1 to W1 bit in I<sup>2</sup>C address 0x4C

## 7.6 Writing a set of coefficients to RAM

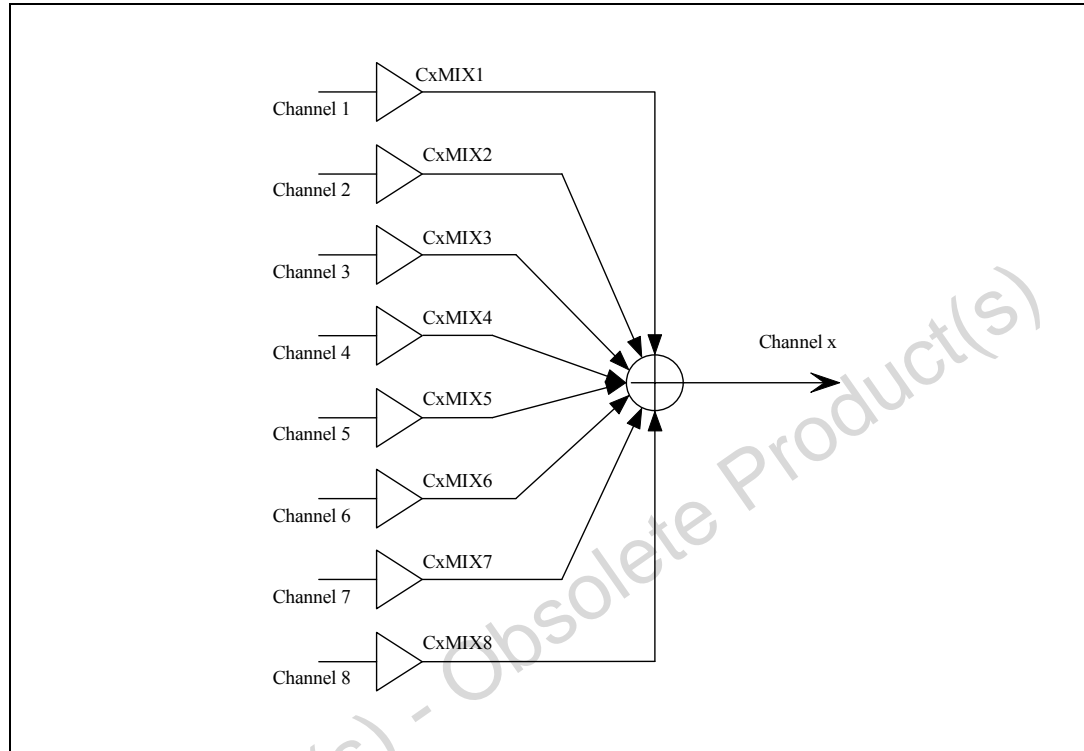
1. write top 2-bits of starting address to I<sup>2</sup>C register 0x3B
2. write bottom 8-bits of starting address to I<sup>2</sup>C register 0x3C
3. write top 8-bits of coefficient b1 in I<sup>2</sup>C address 0x3D
4. write middle 8-bits of coefficient b1 in I<sup>2</sup>C address 0x3E
5. write bottom 8-bits of coefficient b1 in I<sup>2</sup>C address 0x3F
6. write top 8-bits of coefficient b2 in I<sup>2</sup>C address 0x40
7. write middle 8-bits of coefficient b2 in I<sup>2</sup>C address 0x41
8. write bottom 8-bits of coefficient b2 in I<sup>2</sup>C address 0x42
9. write top 8-bits of coefficient a1 in I<sup>2</sup>C address 0x43
10. write middle 8-bits of coefficient a1 in I<sup>2</sup>C address 0x44
11. write bottom 8-bits of coefficient a1 in I<sup>2</sup>C address 0x45
12. write top 8-bits of coefficient a2 in I<sup>2</sup>C address 0x46
13. write middle 8-bits of coefficient a2 in I<sup>2</sup>C address 0x47
14. write bottom 8-bits of coefficient a2 in I<sup>2</sup>C address 0x48
15. write top 8-bits of coefficient b0 in I<sup>2</sup>C address 0x49
16. write middle 8-bits of coefficient b0 in I<sup>2</sup>C address 0x4A
17. write bottom 8-bits of coefficient b0 in I<sup>2</sup>C address 0x4B
18. write 1 to WA bit in I<sup>2</sup>C address 0x4C

The mechanism for writing a set of coefficients to RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoid possible unpleasant acoustic side-effects.

When using this technique, the 10-bit address would specify the address of the biquad b1 coefficient (for example, decimals 0, 5, 10, 15, ..., 100, ... 395), and the STA308A will generate the RAM addresses as offsets from this base value to write the complete set of coefficient data.

## 8 Equalization and mixing

Figure 8. Channel mixer



### 8.1 Post-scale

The STA308A provides one additional multiplication after the last interpolation stage and before the distortion compensation on each channel. This is a 24-bit signed fractional multiply.

The scale factor for this multiply is loaded into RAM using the same I<sup>2</sup>C registers as the biquad coefficients and the bass-management.

This post-scale factor can be used in conjunction with an ADC equipped micro-controller to perform power-supply error correction. All channels can use the channel 1 by setting the post-scale link bit.

Table 9. RAM block for biquads, mixing, and bass management

| Index (decimal) | Index (hex) |                      | Coefficient  | Default  |
|-----------------|-------------|----------------------|--------------|----------|
| 0               | 0x00        | Channel 1 - Biquad 1 | C1H10 (b1/2) | 0x000000 |
| 1               | 0x01        |                      | C1H11 (b2)   | 0x000000 |
| 2               | 0x02        |                      | C1H12 (a1/2) | 0x000000 |
| 3               | 0x03        |                      | C1H13 (a2)   | 0x000000 |



**Table 9. RAM block for biquads, mixing, and bass management (continued)**

| Index (decimal) | Index (hex) |                        | Coefficient  | Default    |
|-----------------|-------------|------------------------|--------------|------------|
| 4               | 0x04        |                        | C1H14 (b0/2) | 0x400000   |
| 5               | 0x05        | Channel 1 - Biquad 2   | C1H20        | 0x000000   |
| ...             | ...         | ...                    | ...          | ...        |
| 49              | 0x31        | Channel 1 - Biquad 10  | C1HA4        | 0x400000   |
| 50              | 0x32        | Channel 2 - Biquad 1   | C2H10        | 0x000000   |
| 51              | 0x33        |                        | C2H11        | 0x000000   |
| ...             | ...         | ...                    | ...          | ...        |
| 99              | 0x63        | Channel 2 - Biquad 10  | C2HA4        | 0x4000000  |
| 100             | 0x64        | Channel 3 - Biquad 1   | C3H10        | 0x000000   |
| ...             | ...         | ...                    | ...          | ...        |
| 399             | 0x18F       | Channel 8 - Biquad 10  | C8HA4        | 0x400000   |
| 400             | 0x190       | Channel 1 - Pre-Scale  | C1PreS       | 0x7FFFFFFF |
| 401             | 0x191       | Channel 2 - Pre-Scale  | C2PreS       | 0x7FFFFFFF |
| 402             | 0x192       | Channel 3 - Pre-Scale  | C3PreS       | 0x7FFFFFFF |
| ...             | ...         | ...                    | ...          | ...        |
| 407             | 0x197       | Channel 8 - Pre-Scale  | C8PreS       | 0x7FFFFFFF |
| 408             | 0x198       | Channel 1 - Post-Scale | C1PstS       | 0x7FFFFFFF |
| 409             | 0x199       | Channel 2 - Post-Scale | C2PstS       | 0x7FFFFFFF |
| ...             | ...         | ...                    | ...          | ...        |
| 415             | 0x19F       | Channel 8 - Post-Scale | C8PstS       | 0x7FFFFFFF |
| 416             | 0x1A0       | Channel 1 - Mix#1 1    | C1MX11       | 0x7FFFFFFF |
| 417             | 0x1A1       | Channel 1 - Mix#1 2    | C1MX12       | 0x000000   |
| ...             | ...         | ...                    | ...          | ...        |
| 423             | 0x1A7       | Channel 1 - Mix#1 8    | C1MX18       | 0x000000   |
| 424             | 0x1A8       | Channel 2 - Mix#1 1    | C2MX11       | 0x000000   |
| 425             | 0x1A9       | Channel 2 - Mix#1 2    | C2MX12       | 0x7FFFFFFF |
| ...             | ...         | ...                    | ...          | ...        |
| 463             | 0x1CF       | Channel 8 - Mix#1 8    | C8MX18       | 0x7FFFFFFF |
| 464             | 0x1D0       | Channel 1 - Mix#2 1    | C1MX21       | 0x7FFFFFFF |
| 465             | 0x1D1       | Channel 1 - Mix#2 2    | C1MX22       | 0x000000   |
| ...             | ...         | ...                    | ...          | ...        |
| 471             | 0x1D7       | Channel 1 - Mix#2 8    | C1MX28       | 0x000000   |
| 472             | 0x1D8       | Channel 2 - Mix#2 1    | C2MX21       | 0x000000   |
| 473             | 0x1D9       | Channel 2 - Mix#2 2    | C2MX22       | 0x7FFFFFFF |

**Table 9. RAM block for biquads, mixing, and bass management (continued)**

| Index (decimal) | Index (hex) |                     | Coefficient | Default   |
|-----------------|-------------|---------------------|-------------|-----------|
| ...             | ...         | ...                 | ...         | ...       |
| 527             | 0x20F       | Channel 8 - Mix#2 8 | C8MX28      | 0x7FFFFFF |
|                 |             |                     |             |           |
|                 |             |                     |             |           |

## 8.2 Variable max power correction

### 8.2.1 MPCC1-2 (0x4D, 0x4E)

MPCC bits determine the 16 MSBs of the MPC compensation coefficient. This coefficient is used in place of the default coefficient when MPCV = 1.

| D7     | D6     | D5     | D4     | D3     | D2     | D1    | D0    |
|--------|--------|--------|--------|--------|--------|-------|-------|
| MPCC15 | MPCC14 | MPCC13 | MPCC12 | MPCC11 | MPCC10 | MPCC9 | MPCC8 |
| 0      | 0      | 1      | 0      | 1      | 1      | 0     | 1     |

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| MPCC7 | MPCC6 | MPCC5 | MPCC4 | MPCC3 | MPCC2 | MPCC1 | MPCC0 |
| 1     | 1     | 0     | 0     | 0     | 0     | 0     | 0     |

## 8.3 Variable distortion compensation

### 8.3.1 DCC1-2 (0x4F, 0x50)

DCC bits determine the 16 MSBs of the distortion compensation coefficient. This coefficient is used in place of the default coefficient when DCCV = 1.

| D7    | D6    | D5    | D4    | D3    | D2    | D1   | D0   |
|-------|-------|-------|-------|-------|-------|------|------|
| DCC15 | DCC14 | DCC13 | DCC12 | DCC11 | DCC10 | DCC9 | DCC8 |
| 1     | 1     | 1     | 1     | 0     | 0     | 1    | 1    |

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| DCC7 | DCC6 | DCC5 | DCC4 | DCC3 | DCC2 | DCC1 | DCC0 |
| 0    | 0    | 1    | 1    | 0    | 0    | 1    | 1    |

## 8.4 PSCorrect registers

ADC is used to input ripple data to SDI78. The left channel (7) is used internally. No audio data can therefore be used on these channels. Though all channel mapping and mixing from other inputs to channels 7 and 8 internally are still valid.

### 8.4.1 PSC1-2: ripple correction value (RCV) (0x51, 0x52)

Equivalent to negative maximum ripple peak as a percentage of Vcc (MPR), scaled by the inverse of maximum ripple p-p as percentage of full-scale analog input to ADC. Represented as a 1.11 signed fractional number.

| D7    | D6    | D5   | D4   | D3   | D2   | D1   | D0   |
|-------|-------|------|------|------|------|------|------|
| RCV11 | RCV10 | RCV9 | RCV8 | RCV7 | RCV6 | RCV5 | RCV4 |
| 0     | 0     | 0    | 0    | 0    | 0    | 0    | 0    |

| D7   | D6   | D5   | D4   | D3    | D2    | D1   | D0   |
|------|------|------|------|-------|-------|------|------|
| RCV3 | RCV2 | RCV1 | RCV0 | CNV11 | CNV10 | CNV9 | CNV8 |
| 0    | 0    | 0    | 0    | 1     | 1     | 1    | 1    |

### 8.4.2 PSC3: correction normalization value (CNV) (0x53)

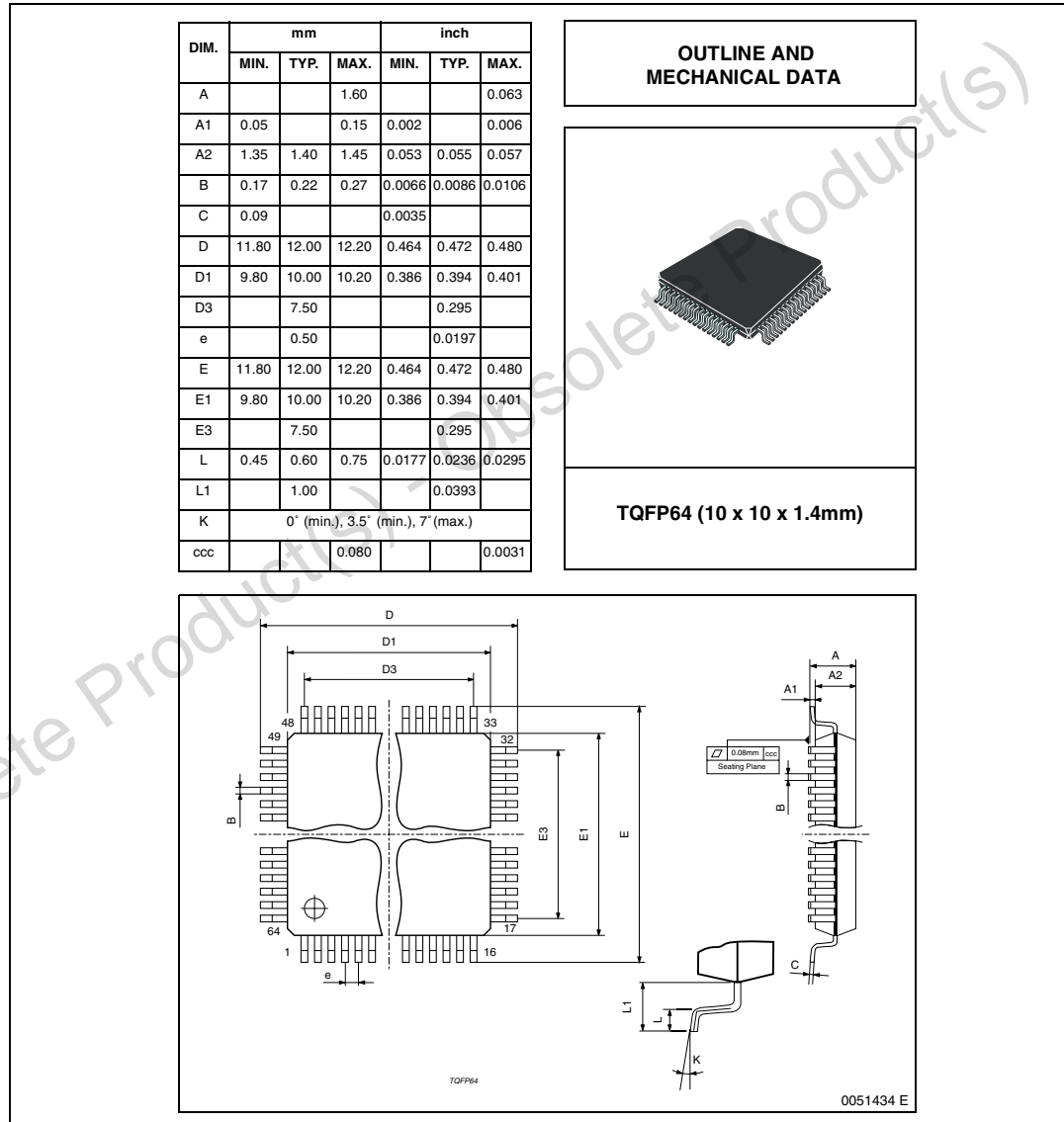
Equivalent to  $1 / (1+MPR)$  expressed as a 0.12 unsigned fractional number.

| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|------|------|------|------|------|------|------|------|
| CNV7 | CNV6 | CNV5 | CNV4 | CNV3 | CNV2 | CNV1 | CNV0 |
| 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |

# 9 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 9. TQFP64 (10 x 10 x 1.4mm) mechanical data and package dimensions**



## 10 Trademarks and other acknowledgements

DDX is a registered trademark of Apogee Technology Inc.

ECOPACK is a registered trademark of STMicroelectronics.

Obsolete Product(s) - Obsolete Product(s)

## 11 Revision history

**Table 10. Document revision history**

| Date      | Revision | Changes                                                                                                                                                                                     |
|-----------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| May-2004  | 1        | Initial release.                                                                                                                                                                            |
| Nov-2005  | 2        | Changed in page 4 value $T_{amb}$ and $T_j$ .                                                                                                                                               |
| June-2006 | 3        | Changed in Figure 4 and Table 2 the name of the pins 22 and 24.                                                                                                                             |
| July-2007 | 4        | Updated cover page<br>Added chapter 6, Application reference schematic<br>Removed reserved registers from chapter 7<br>Updated register descriptions in chapter 7<br>Various minor changes. |

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2007 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)