10-Bit Monitor and Control System with ADC, DACs, Temperature Sensor, and GPIOs

Data Sheet **AD7292**

FEATURES

- 10-bit SAR ADC
  - 8 multiplexed analog input channels
  - Single-ended mode of operation
  - Differential mode of operation
  - 5 V analog input range
  - V_{REF}, 2 × V_{REF}, or 4 × V_{REF} input ranges
  - Input measured with respect to A_{GND} or V_{DD}
- 4 monotonic, 10-bit, 5 V DACs
  - 2 µs settling time
  - Power-on reset to 0 V
  - 10 mA sink and source capability
- Internal temperature sensor
  - ±1°C accuracy
- 12 general-purpose digital I/O pins
- Internal 1.25 V reference
- Built-in monitoring features
  - Minimum and maximum value register for each channel
  - Programmable alert thresholds
  - Programmable hysteresis
- SPI interface
- Temperature range: −40°C to +125°C
- Package type: 36-lead LFCSP

APPLICATIONS

- Base station power amplifier (PA) monitoring and control
- RF control loops
- Optical communication system control
- General-purpose system monitoring and control

FUNCTIONAL BLOCK DIAGRAM

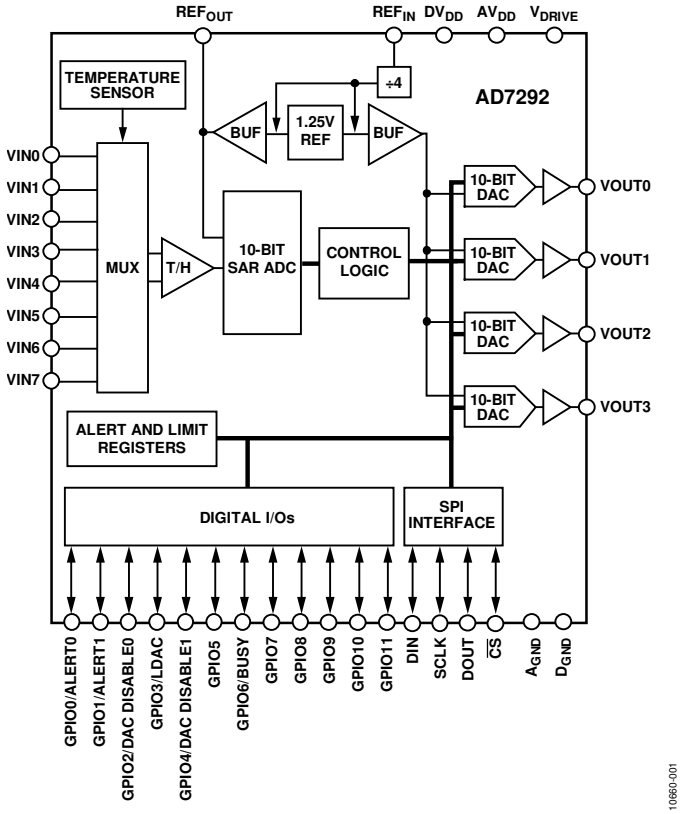

Figure 1.

GENERAL DESCRIPTION

The AD7292 contains all the functionality required for general-purpose monitoring of analog signals and control of external devices, integrated into a single-chip solution. The AD7292 features an 8-channel, 10-bit SAR ADC, four 10-bit DACs, a ±1°C accurate internal temperature sensor, and 12 GPIOs to aid system monitoring and control.

The 10-bit, high speed, low power successive approximation register (SAR) ADC is designed to monitor a variety of single-ended input signals. Differential operation is also available by configuring VIN0 and VIN1 to operate as a differential pair.

The AD7292 offers a register programmable ADC sequencer, which enables the selection of a programmable sequence of channels for conversion.

Four 10-bit digital-to-analog converters (DACs) provide outputs from 0 V to 5 V. An internal, high accuracy, 1.25 V reference provides a separately buffered reference source for both the ADC and the DACs.

A high accuracy band gap temperature sensor is monitored and digitized by the 10-bit ADC to give a resolution of 0.03125°C. The AD7292 also features built-in limit and alarm functions.

The AD7292 is a highly integrated solution offered in a 36-lead LFCSP package with an operating temperature range of −40°C to +125°C.

Rev. A Document Feedback

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REVISION HISTORY

9/14—Rev. 0 to Rev. A

Changes to Figure 2 ... 6
Changed t_{11} from 4 ns max to 4 ns min and Removed Endnote 4; Table 5 ... 21
Changes to Figure 35 ... 18
Changes to Table 15 ... 21
Changes to VIN Filter Subregister (Address 0x13) Section, Conversion Delay Control Subregister (Address 0x14) Section, Table 23, and Table 24 ... 26
Changes to VIN ALERT0 Routing and VIN ALERT1 Routing Subregisters (Address 0x15 and Address 0x16) Section, Table 25, and Table 26 ... 27
Changes to Figure 40 and Figure 41 ... 35
Changes to Figure 42 ... 36

10/12—Revision 0: Initial Version

SPECIFICATIONS

ADC SPECIFICATIONS

AV_{DD} = 4.75 V to 5.25 V, DV_{DD} = 1.8 V to 5.25 V, V_{REF} = 1.25 V internal, V_{DRIVE} = 1.8 V to 5.25 V, A_{GND} = 0 V, T_A = −40°C to +125°C, unless otherwise noted. Specifications apply to single-ended mode only, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY					
Resolution	10			Bits	
Integral Nonlinearity (INL)[1]		±0.11	±0.5	LSB	
			±0.6	LSB	(AV_{DD} − 4 × V_{REF}) to AV_{DD} input range
Differential Nonlinearity (DNL)[1]		±0.1	±0.99	LSB	
Offset Error		±3	±8	mV	
			±12	mV	(AV_{DD} − 4 × V_{REF}) to AV_{DD} input range
Offset Error Matching		0.5	±1	mV	
Offset Error Drift		±0.22		ppm/°C	
Gain Error		±0.09	±0.25	% FS	
			±0.36	% FS	(AV_{DD} − 4 × V_{REF}) to AV_{DD} input range
Gain Error Matching		±0.5		% FS	
Gain Error Drift		±4.17		ppm/°C	
DYNAMIC PERFORMANCE[1]					f_{IN} = 10 kHz sine wave
Signal-to-Noise Ratio (SNR)		61.5		dB	
Signal-to-Noise-and-Distortion (SINAD) Ratio		61.5		dB	
Total Harmonic Distortion (THD)		−84		dB	
Spurious-Free Dynamic Range (SFDR)		84.5		dB	
Channel-to-Channel Isolation		−80		dB	f_{IN} = 3 kHz to 1000 kHz
Full Power Bandwidth		60		MHz	At −3 dB (0 V to V_{REF} input range)
		3		MHz	At −0.1 dB (0 V to V_{REF} input range)
CONVERSION RATE					
Conversion Time		900		ns	See Table 5
Track-and-Hold Acquisition Time			45	ns	
Throughput Rate			625	kSPS	ADC only; temperature sensor disabled
			150	kSPS	ADC and temperature sensor
ANALOG INPUT					
Single-Ended Input Range					
With Respect to A_{GND}	0		4 × V_{REF}	V	
	0		2 × V_{REF}	V	
	0		V_{REF}	V	
With Respect to AV_{DD}	AV_{DD} − 4 × V_{REF}		AV_{DD}	V	
Fully Differential Input Range	−4 × V_{REF}		+4 × V_{REF}	V	VIN0 and VIN1 inputs only
	−2 × V_{REF}		+2 × V_{REF}	V	
	−V_{REF}		+V_{REF}	V	
Input Capacitance		23		pF	0 V to V_{REF} input range
		18		pF	0 V to 2 × V_{REF} input range
		15		pF	0 V to 4 × V_{REF} input range
DC Input Leakage Current			±1	µA	
INTERNAL REFERENCE					
Reference Output Voltage	1.245	1.25	1.255	V	At 25°C
Reference Temperature Coefficient		±13		ppm/°C	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
EXTERNAL REFERENCE					
Reference Input Voltage	4.75		AV_{DD}	V	Internal reference used to calibrate temperature sensor
Input Resistance		100		kΩ	

[1] Specifications also apply to differential mode.

DAC SPECIFICATIONS

AV_{DD} = 4.75 V to 5.25 V, DV_{DD} = 1.8 V to 5.25 V, V_{REF} = 1.25 V internal, V_{DRIVE} = 1.8 V to 5.25 V, A_{GND} = 0 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY					
Resolution	10			Bits	
Integral Nonlinearity (INL)		±0.2	±1	LSB	
Differential Nonlinearity (DNL)		±0.1	±0.3	LSB	Guaranteed monotonic
Zero-Scale Error		4.8	±10	mV	All 0s loaded to DAC register
Full-Scale Error		±0.1	±0.5	% FS	All 1s loaded to DAC register
Offset Error		±1.62	±10	mV	Measured in the linear region, T_A = −40°C to +125°C
Offset Error Drift		±4.4		ppm/°C	Measured in the linear region, T_A = 25°C
Gain Error		±0.35	±0.5	% FS	
Gain Error Drift		±2.6		ppm/°C	
DC Power Supply Rejection Ratio (PSRR)		−50		dB	f_{RIPPLE} up to 100 kHz
DC Crosstalk		5		μV	
DAC OUTPUT CHARACTERISTICS					
Output Voltage Range	0		$4 \times V_{REF}$	V	
Short-Circuit Current		±30		mA	
Load Current		±10		mA	Sink/source current; within ±200 mV of supply
Resistive Load to A_{GND}		500		Ω	
Capacitive Load Stability			1	nF	
DC Output Impedance		1		Ω	
AC CHARACTERISTICS[1]					
Output Voltage Settling Time		1	2	μs	¼ to ¾ scale step change within 1 LSB, measured from last SCLK edge
Overshoot		200		mV	¼ to ¾ scale step change within 1 LSB, measured from last SCLK edge; C_L = 200 pF, R_L = 25 kΩ
Slew Rate	9	12		V/μs	
Digital-to-Analog Glitch Impulse		4		nV-sec	
Digital Feedthrough		0.4		nV-sec	
DAC-to-DAC Crosstalk		2		nV-sec	
Output Noise Spectral Density		730		nV/√Hz	DAC code = midscale, 1 kHz
Output Noise		28		μV rms	0.1 Hz to 10 Hz
Output Transient Response During Power-Up		5		mV	AV_{DD} ramp of 1 ms with 100 kΩ load

[1] The DAC buffer output level is undefined until 30 μs after all supplies reach their minimum specified operating voltages.

GENERAL SPECIFICATIONS

AV_{DD} = 4.75 V to 5.25 V, DV_{DD} = 1.8 V to 5.25 V, V_{REF} = 1.25 V internal, V_{DRIVE} = 1.8 V to 5.25 V, A_{GND} = 0 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
Input High Voltage, V_{IH}	$0.7 \times V_{DRIVE}$			V	V_{DRIVE} = 2.3 V to 5.25 V
	$0.8 \times V_{DRIVE}$			V	V_{DRIVE} = 1.8 V to 1.95 V
Input Low Voltage, V_{IL}			$0.3 \times V_{DRIVE}$	V	V_{DRIVE} = 2.3 V to 5.25 V
			$0.2 \times V_{DRIVE}$	V	V_{DRIVE} = 1.8 V to 1.95 V
Input Leakage Current, I_{IN}			±1	µA	
Input Capacitance, C_{IN}		3		pF	
Input Hysteresis, V_{HYST}		$0.05 \times V_{DRIVE}$		V	
GPIO OUTPUTS					
I_{SINK}/I_{SOURCE}		1.6		mA	
Output High Voltage, V_{OH}	DV_{DD} − 0.2			V	I_{SINK}/I_{SOURCE} = 1.6 mA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK}/I_{SOURCE} = 1.6 mA
POWER REQUIREMENTS					
AV_{DD}	4.75		5.25	V	
DV_{DD}	1.8		5.25	V	
V_{DRIVE}	1.8		5.25	V	
Static Current					
I_{AVDD}		4.2	5.4	mA	
I_{DVDD}		0.65	1.3	mA	
I_{DRIVE}		0.12	0.35	mA	
Total Static Current		4.97		mA	$AV_{DD} + DV_{DD} + V_{DRIVE}$
Dynamic Current					
I_{AVDD}		6.45	8.5	mA	
I_{DVDD}		0.65	1.3	mA	
I_{DRIVE}		0.12	0.35	mA	
Total Dynamic Current		7.22		mA	$AV_{DD} + DV_{DD} + V_{DRIVE}$, DAC outputs loaded and converting at full scale, continuous conversion on ADC inputs
Power Dissipation					
Static		26	34.125	mW	
Dynamic		37.9	50.925	mW	

TEMPERATURE SENSOR SPECIFICATIONS

AV_{DD} = 4.75 V to 5.25 V, DV_{DD} = 1.8 V to 5.25 V, V_{REF} = 1.25 V internal, V_{DRIVE} = 1.8 V to 5.25 V, A_{GND} = 0 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INTERNAL TEMPERATURE SENSOR					
Operating Range	−40		+125	°C	
Accuracy		±1	±3	°C	T_A = −40°C to +125°C
		±1	±2	°C	T_A = 0°C to +125°C
		0.5	±1.5	°C	T_A = 25°C
Resolution		0.03125		°C	Digital filter enabled
Update Rate		1.25		ms	

TIMING SPECIFICATIONS

AV_{DD} = 4.75 V to 5.25 V, DV_{DD} = 1.8 V to 5.25 V, V_{REF} = 1.25 V internal, V_{DRIVE} = 1.8 V to 5.25 V, A_{GND} = 0 V, C_L = 27 pF, T_A = −40°C to +125°C, unless otherwise noted.[1]

Table 5.

		Limit at T_{MIN}/T_{MAX}		
Parameter	**Description**	**V_{DRIVE} = 1.8 V**	**V_{DRIVE} = 2.7 V to 5.25 V**	**Unit**
$t_{CONVERT}$	ADC conversion time/BUSY high time			
	Temperature sensor disabled	950	950	ns max
	Temperature sensor enabled	5.85	5.85	µs max
t_{ACQ}	ADC acquisition time	50	50	ns max
f_{SCLK}	Frequency of serial read clock[2]	15	25	MHz max
t_1	SCLK period	66	40	ns min
t_2	SCLK low	33	20	ns min
t_3	SCLK high	33	20	ns min
t_4	$\overline{CS}$ falling edge to SCLK rising edge	4	4	ns min
t_5	DIN setup time to SCLK falling edge	4	4	ns min
t_6[3]	DIN hold time after SCLK falling edge	2	2	ns max
t_7	SCLK falling edge to $\overline{CS}$ rising edge	5	5	ns min
t_8	$\overline{CS}$ high	5	5	ns min
t_9	SCLK to output data valid delay time	30	19	ns max
t_{10}	SCLK to output data valid hold time	7	5	ns min
t_{11}[4]	$\overline{CS}$ rising edge to SCLK rising edge	4	4	ns min
t_{12}	$\overline{CS}$ rising edge to DOUT high impedance	15	15	ns max

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DRIVE}).
[2] For V_{DRIVE} = 2.5 V, f_{SCLK} = 22 MHz maximum.
[3] Time required for the output to cross 0.2 × V_{DRIVE} and 0.8 × V_{DRIVE} when V_{DRIVE} = 1.8 V; time required for the output to cross 0.3 × V_{DRIVE} and 0.7 × V_{DRIVE} when V_{DRIVE} = 2.7 V to 5.25 V.
[4] Guaranteed by design.

Timing Diagram

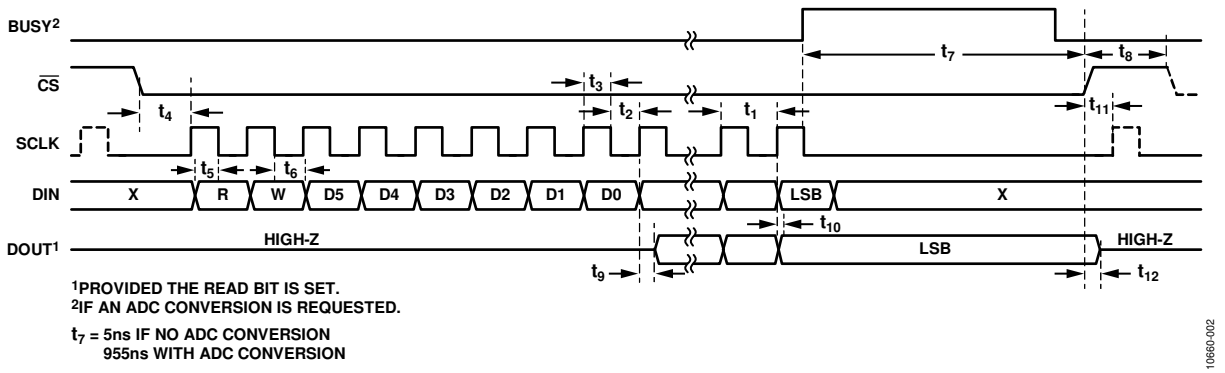


Figure 2. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
AV_{DD} to A_{GND}	−0.3 V to +6 V
DV_{DD} to D_{GND}	−0.3 V to +6 V
V_{DRIVE} to D_{GND}	−0.3 V to +6 V
VINx to A_{GND}	−0.3 V to AV_{DD} + 0.3 V
VOUTx to A_{GND}	−0.3 V to AV_{DD} + 0.3 V
Digital Inputs/Outputs to D_{GND}	−0.3 V to DV_{DD} + 0.3 V
$\overline{CS}$, SCLK, DIN, DOUT to D_{GND}	−0.3 V to V_{DRIVE} + 0.3 V
REF_{OUT} to A_{GND}	−0.3 V to +2.2 V
REF_{IN} to A_{GND}	−0.3 V to AV_{DD} + 0.3 V
D_{GND} to A_{GND}	0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
ESD, Human Body Model	2.5 kV
Reflow Soldering Peak Temperature	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 7. Thermal Resistance

Package Type	θ_{JA}	Unit
36-Lead LFCSP	54.1	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

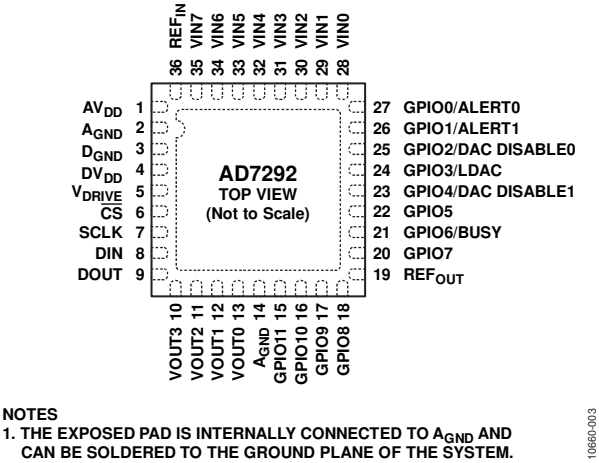


Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AV_{DD}	Supply Pin. This pin should be decoupled to A_{GND} with a 0.1 µF decoupling capacitor.
2, 14	A_{GND}	Analog Ground. Ground reference point for all analog circuitry on the AD7292. All analog signals should be referred to A_{GND}. Both the A_{GND} and D_{GND} pins should be connected to the ground plane of the system.
3	D_{GND}	Digital Ground. Ground reference point for all digital circuitry on the AD7292. All digital signals should be referred to D_{GND}. Both the D_{GND} and A_{GND} pins should be connected to the ground plane of the system.
4	DV_{DD}	Sets the GPIO voltage level. This pin should be decoupled to D_{GND} with a 0.1 µF decoupling capacitor.
5	V_{DRIVE}	This pin sets the reference level of the SPI bus from 1.8 V to 5.25 V. This pin should be decoupled to D_{GND} with a 0.1 µF decoupling capacitor.
6	$\overline{CS}$	Chip Select Signal. This active low logic input signal is used to frame the serial data input.
7	SCLK	SPI Clock Input.
8	DIN	SPI Serial Data Input. Serial data to be loaded into the registers of the AD7292 is provided on this pin. Data is clocked into the serial interface on the falling edge of SCLK.
9	DOUT	SPI Serial Data Output. Serial data to be read from the registers of the AD7292 is provided on this pin. Data is clocked out on the rising edge of SCLK. DOUT is high impedance when it is not outputting data.
10 to 13	VOUT3 to VOUT0	Buffered DAC Analog Outputs. Each DAC analog output is driven from an output amplifier and has a maximum output voltage span of 5 V. Each DAC is capable of sourcing and sinking 10 mA and driving a 1 nF load.
15 to 18	GPIO11 to GPIO8	General-Purpose Input/Output Pins.
19	REF_{OUT}	ADC Internal Reference Output. Decouple the internal ADC reference buffer to A_{GND} with a 0.1 µF decoupling capacitor.
20	GPIO7	General-Purpose Input/Output Pin.
21	GPIO6/BUSY	General-Purpose Input/Output Pin (GPIO6). Busy Output Pin (BUSY). When a conversion starts, this output pin transitions high and remains high until the conversion is completed.
22	GPIO5	General-Purpose Input/Output Pin.
23	GPIO4/ DAC DISABLE1	General-Purpose Input/Output Pin (GPIO4). DAC Disable Pin 1 (DAC DISABLE1). When this pin is activated, the selected DAC outputs are disabled. Select the DAC channels to be disabled by this pin using the GPIO4/DAC DISABLE1 subregister within the configuration register bank (see Table 30).
24	GPIO3/LDAC	General-Purpose Input/Output Pin (GPIO3). LDAC Input Pin (LDAC). When this input is taken high, the DAC registers are updated.
25	GPIO2/ DAC DISABLE0	General-Purpose Input/Output Pin (GPIO2). DAC Disable Pin 0 (DAC DISABLE0). When this pin is activated, the selected DAC outputs are disabled. Select the DAC channels to be disabled by this pin using the GPIO2/DAC DISABLE0 subregister within the configuration register bank (see Table 29).

Pin No.	Mnemonic	Description
26	GPIO1/ALERT1	General-Purpose Input/Output Pin (GPIO1). Alert Pin 1 (ALERT1). When configured as an alert, this pin acts as an out-of-range indicator and becomes active when the conversion result violates the high or low limit stored in the alert limits register bank. The polarity of the alert signal is controlled using the general subregister within the configuration register bank.
27	GPIO0/ALERT0	General-Purpose Input/Output Pin (GPIO0). Alert Pin 0 (ALERT0). When configured as an alert, this pin acts as an out-of-range indicator and becomes active when the conversion result violates the high or low limit stored in the alert limits register bank. The polarity of the alert signal is controlled using the general subregister within the configuration register bank.
28 to 35	VIN0 to VIN7	Analog Inputs. The eight single-ended analog inputs of the AD7292 are multiplexed into the on-chip track-and-hold amplifier. Each input channel can accept analog inputs from 0 V to 5 V. Any unused input channels should be connected to A_{GND} to avoid noise pickup.
36	REF_{IN}	Voltage Reference Input. An external reference for the AD7292 can be applied to this pin. If this pin is unused, connect it to A_{GND}.
EPAD	EPAD	The exposed pad is internally connected to A_{GND} and can be soldered to the ground plane of the system.

TYPICAL PERFORMANCE CHARACTERISTICS

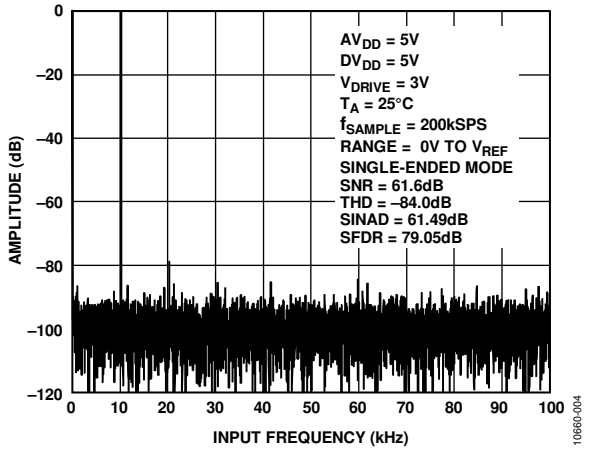


Figure 4. ADC FFT, 200 kSPS, f_{IN} = 10 kHz, Single-Ended Mode

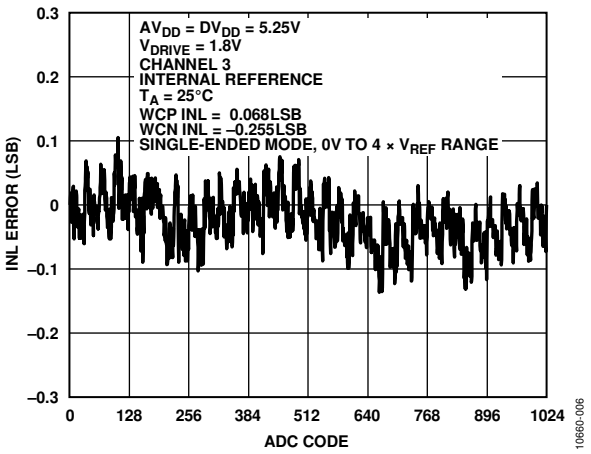


Figure 5. Typical ADC INL, Single-Ended Mode

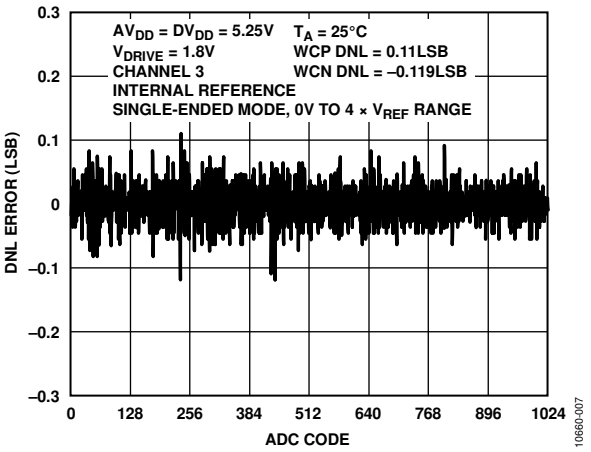


Figure 6. Typical ADC DNL, Single-Ended Mode

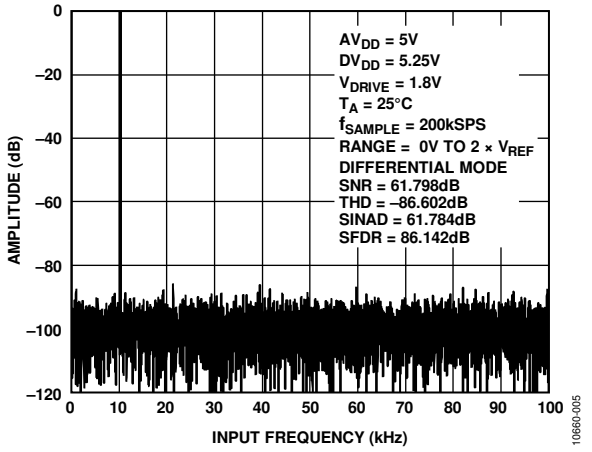


Figure 7. ADC FFT, 200 kSPS, f_{IN} = 10 kHz, Differential Mode

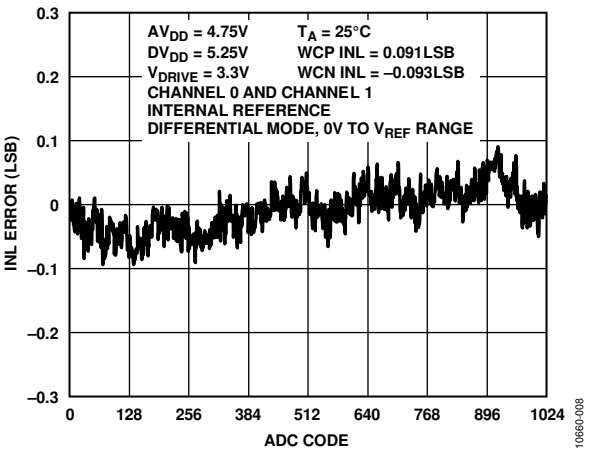


Figure 8. Typical ADC INL, Differential Mode

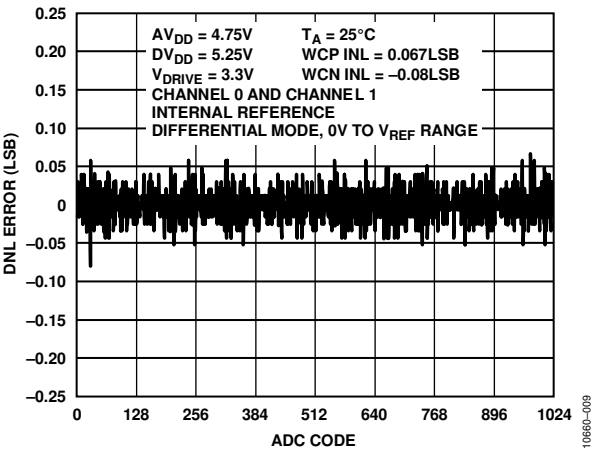


Figure 9. Typical ADC DNL, Differential Mode

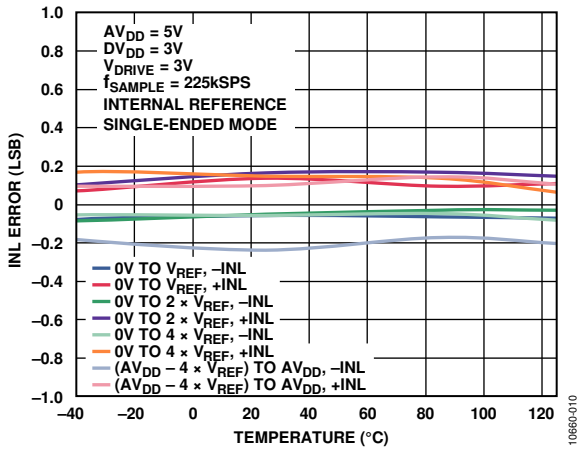


Figure 10. ADC INL vs. Temperature

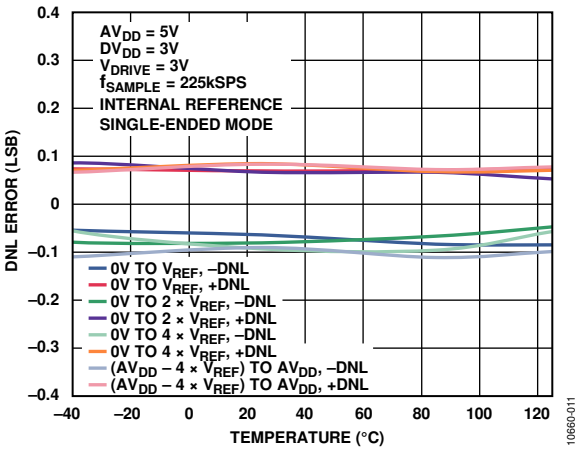


Figure 13. ADC DNL vs. Temperature

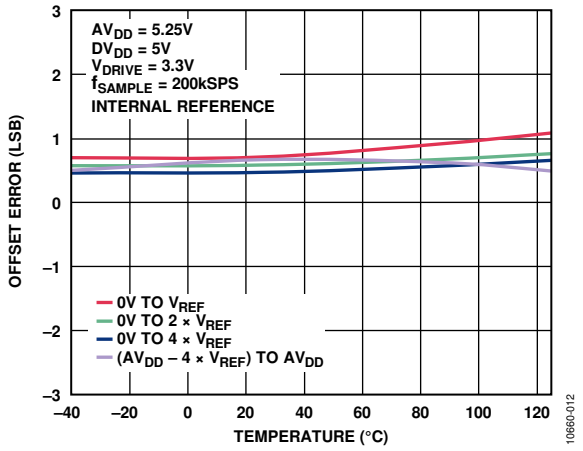


Figure 11. Offset Error vs. Temperature, Single-Ended and Differential Modes

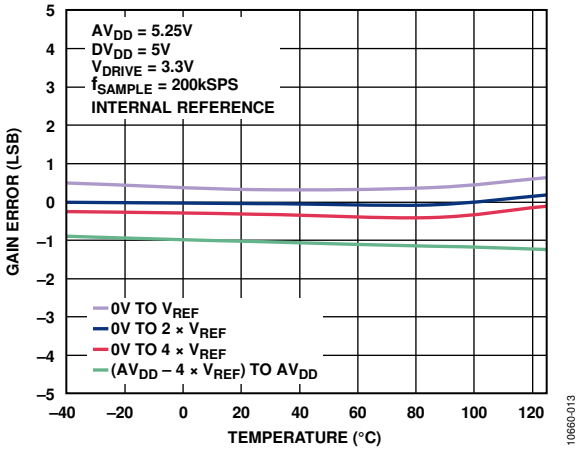


Figure 14. ADC Gain Error vs. Temperature, Single-Ended and Differential Modes

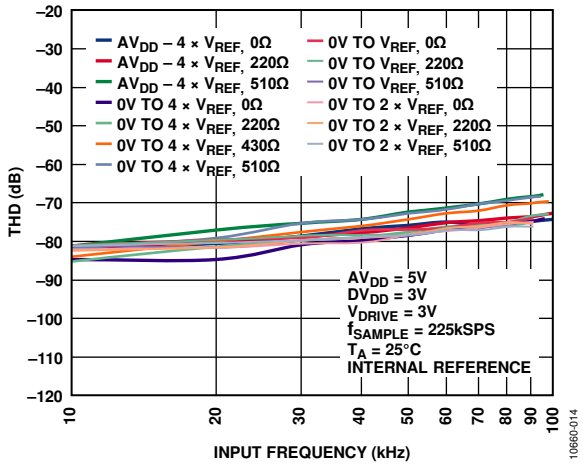


Figure 12. THD vs. Input Frequency for Various Source Impedances, Single-Ended Mode

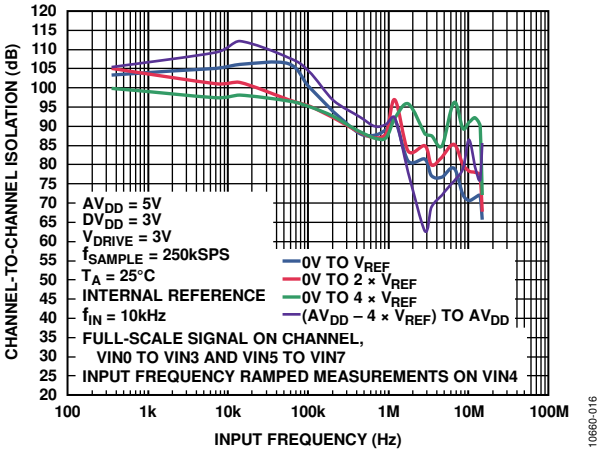


Figure 15. ADC Channel-to-Channel Isolation

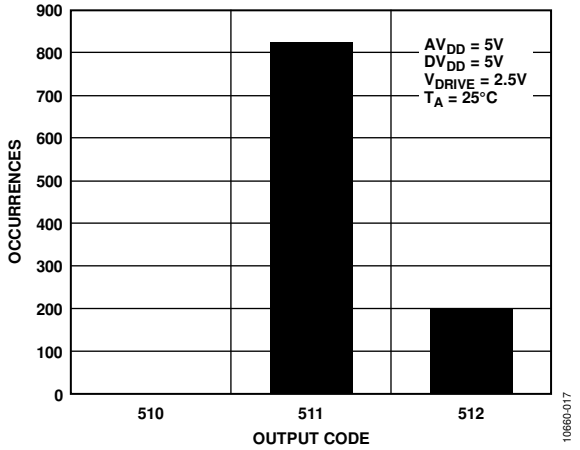


Figure 16. Histogram of Codes

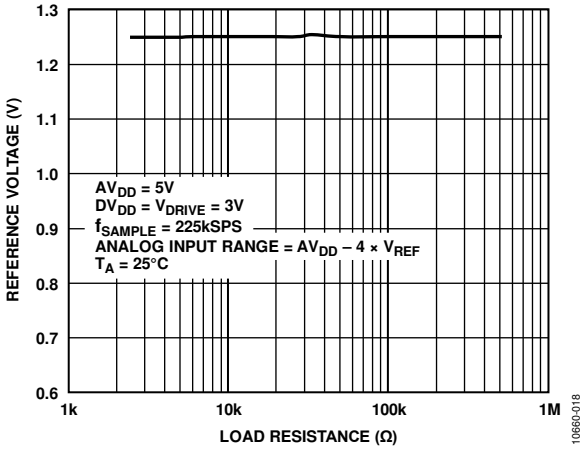


Figure 19. Reference Voltage vs. Load Resistance

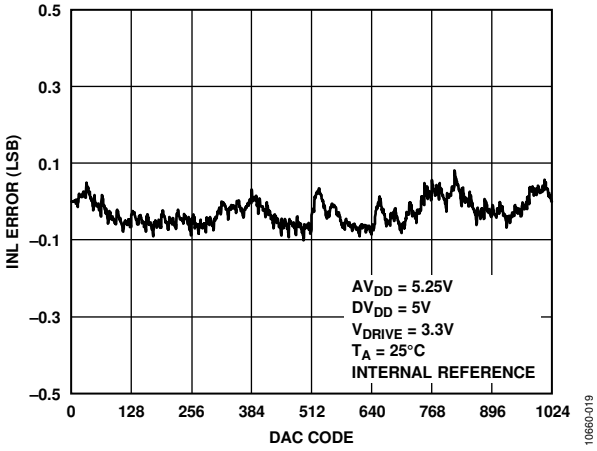


Figure 17. Typical DAC INL vs. Output Code

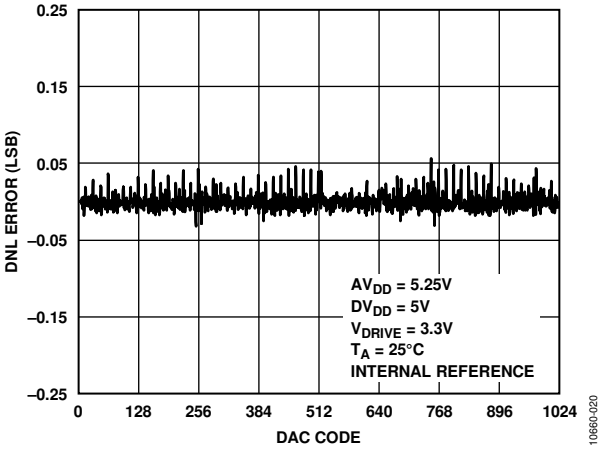


Figure 20. Typical DAC DNL vs. Output Code

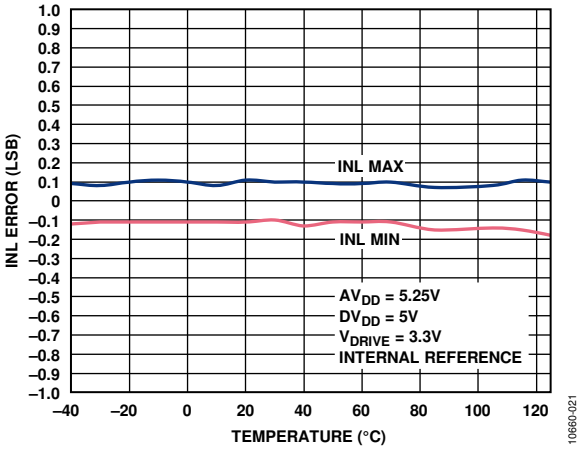


Figure 18. DAC INL vs. Temperature

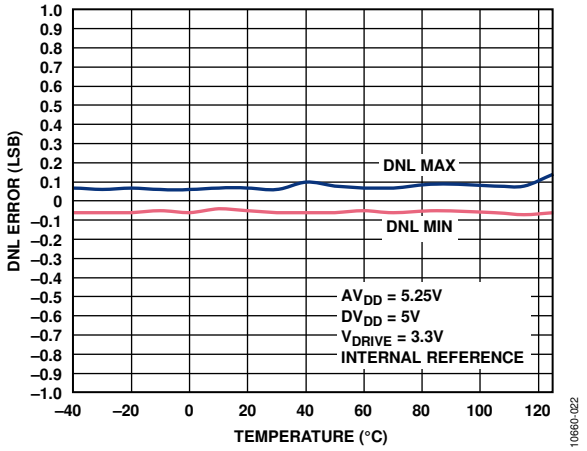


Figure 21. DAC DNL vs. Temperature

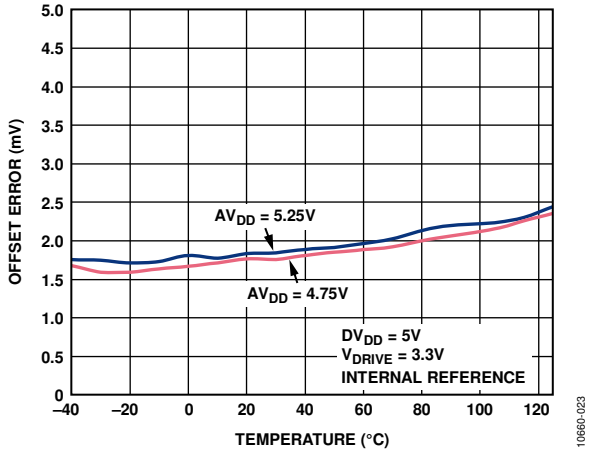


Figure 22. DAC Offset Error vs. Temperature

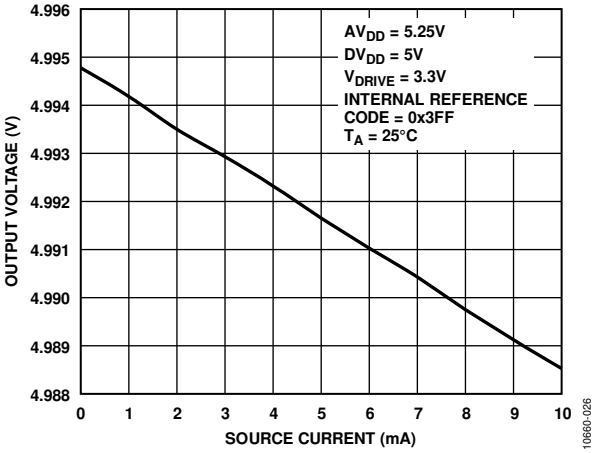


Figure 23. DAC Source Current (Full Scale)

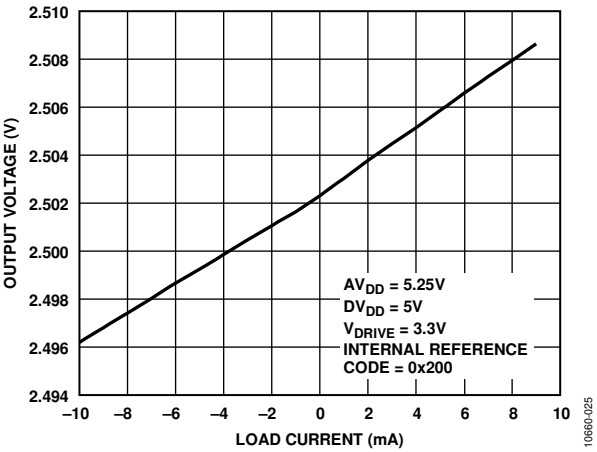


Figure 24. DAC Output Voltage vs. Load Current (Midscale)

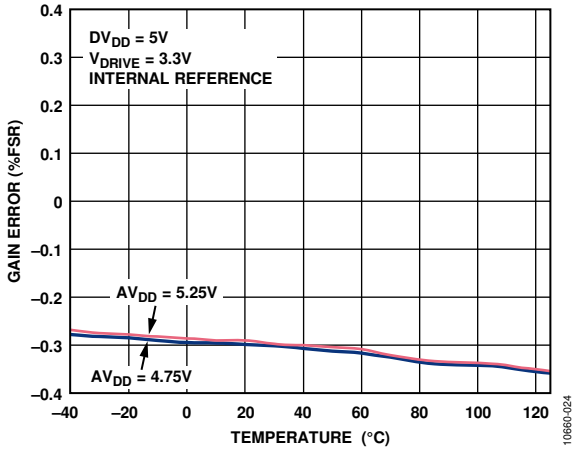


Figure 25. DAC Gain Error vs. Temperature

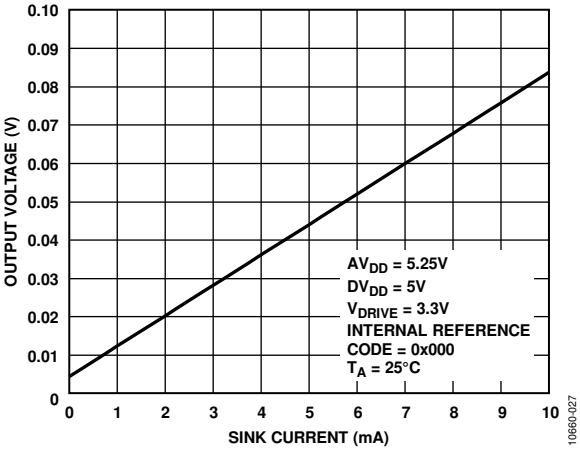


Figure 26. DAC Sink Current (Zero Scale)

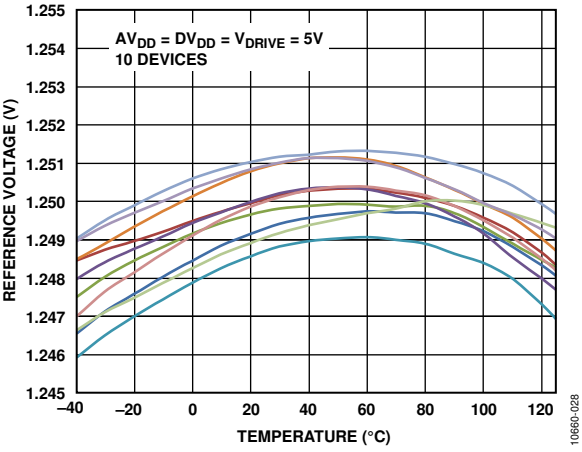


Figure 27. Reference Voltage vs. Temperature

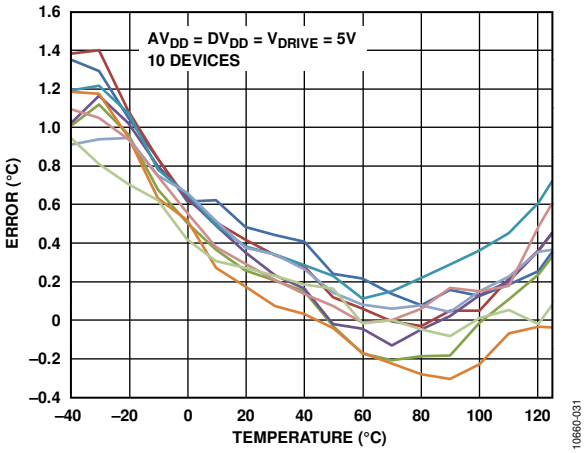


Figure 28. Temperature Sensor Error vs. Temperature

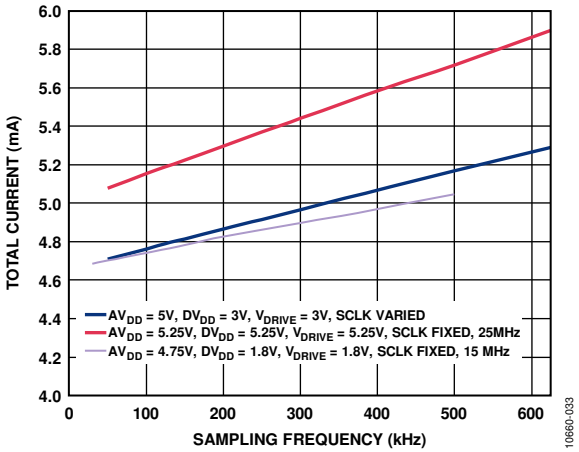


Figure 30. Total Supply Current vs. Throughput Rate

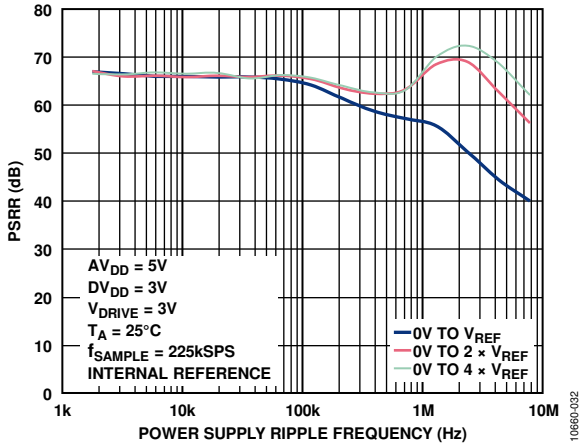


Figure 29. PSRR vs. Power Supply Ripple Frequency

THEORY OF OPERATION

ANALOG INPUTS

The AD7292 has eight analog input channels. By default, these channels are configured as single-ended inputs. Differential operation is also available by configuring VIN0 and VIN1 to operate as a differential pair.

Single-Ended Mode

In applications where the signal source has high impedance, it is recommended that the analog input be buffered before it is applied to the ADC.

The analog input range is programmed to one of these values: 0 V to V_{REF}, 0 V to 2 × V_{REF}, or 0 V to 4 × V_{REF}. For information about programming the input range, see the VIN RANGE0 and VIN RANGE1 Subregisters (Address 0x10 and Address 0x11) section.

In 0 V to 2 × V_{REF} mode, the input is scaled by a factor of 2 before the conversion takes place. In 0 V to 4 × V_{REF} mode, the input is scaled by a factor of 4 before the conversion takes place. Note that the voltage with respect to A_{GND} on the ADC analog input pins cannot exceed AV_{DD}.

If the analog input signal to be sampled is bipolar, the internal reference of the ADC can be used to externally bias this signal up so that it is correctly formatted for the ADC. Figure 31 shows a typical connection diagram when operating the ADC in single-ended mode with a bipolar ±0.625 V input signal.

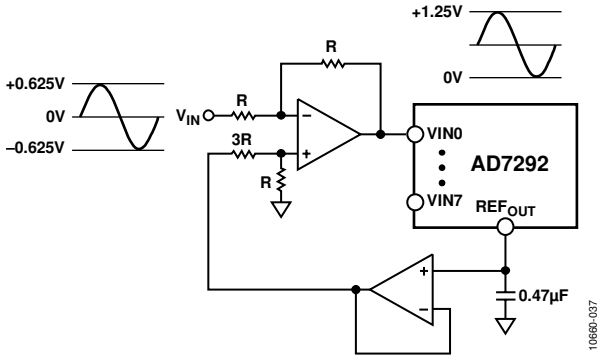


Figure 31. Interfacing to a Bipolar Input Signal

Differential Mode

The AD7292 can be configured to have one differential analog input pair (VIN0 and VIN1). Differential signals have some benefits over single-ended signals, including noise immunity based on the common-mode rejection of the device and improvements in distortion performance. Figure 32 shows the fully differential analog input of the AD7292.

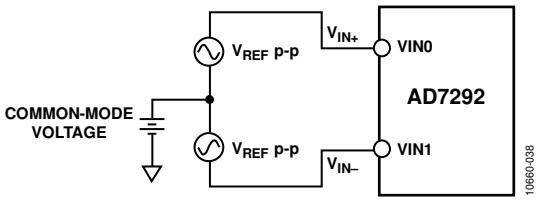


Figure 32. Differential Analog Input

The amplitude of the differential signal is the difference between the signals applied to the input pins of the differential pair, VIN0 and VIN1. The resulting converted data is stored in straight binary format in the ADC data register. VIN0 and VIN1 should be simultaneously driven by two signals that are 180° out of phase; each signal should be of maximum amplitude V_{REF}, 2 × V_{REF}, or 4 × V_{REF}, depending on the selected range.

Therefore, if the 0 V to V_{REF} range is selected, the amplitude of the differential signal is –V_{REF} to +V_{REF} peak-to-peak (2 × V_{REF}), regardless of the common-mode voltage (V_{CM}).

The common-mode voltage is the average of the two signals.

$$V_{CM} = (V_{IN+} + V_{IN-})/2$$

The common-mode voltage is, therefore, the voltage on which the two inputs are centered; the resulting span for each input is V_{CM} ± V_{REF}/2. This voltage must be set up externally. When the inputs are driven with an amplifier, the actual common-mode range is determined by the output voltage swing of the amplifier and the input common-mode range of the AD7292. The common-mode voltage must be in this range to guarantee the functionality of the AD7292 (see Figure 33). When a conversion takes place, the common-mode voltage is rejected, resulting in a virtually noise-free signal of amplitude –V_{REF} to +V_{REF}.

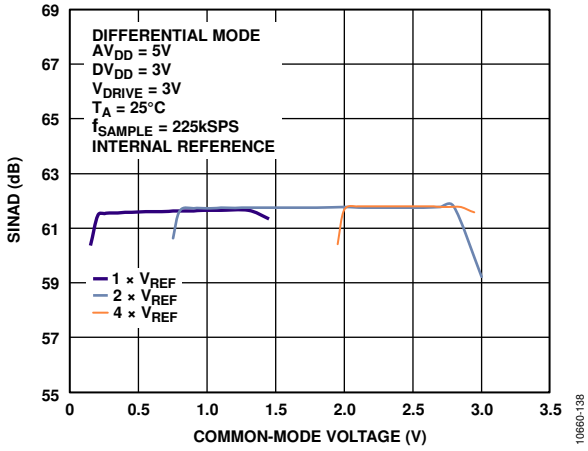


Figure 33. Common-Mode Voltage (Dependent on Input Range)

ADC TRANSFER FUNCTIONS

The output coding of the AD7292 is 10-bit straight binary for the analog input channels. The designated code transitions occur at successive LSB values.

To select the input range, set the appropriate bits in the VIN RANGE1 and VIN RANGE0 subregisters of the configuration register bank (see Table 10).

The LSB size depends on the input range selected (see Table 9).

Table 9. Input Range and LSB Size

Input Range	LSB Size
0 V to V_{REF}	$V_{REF}/2^{10}$
0 V to 2 × V_{REF}	$2V_{REF}/2^{10}$
0 V to 4 × V_{REF}	$4V_{REF}/2^{10}$

The ideal transfer function for the AD7292 when operating with an input range of 0 V to V_{REF} is shown in Figure 34.

Table 10. Analog Input Range Selection

Subregister Bit Settings[1]		Sample with Respect to A_{GND}		Sample with Respect to AV_{DD}[2]
VIN RANGE1	VIN RANGE0	Single-Ended Input Range (VIN0 to VIN7)	Differential Input Range (VIN0 and VIN1 Only)	Single-Ended Input Range (VIN0 to VIN7)
0	0	0 V to 4 × V_{REF}	−4 × V_{REF} to +4 × V_{REF}	(AV_{DD} − 4 × V_{REF}) to AV_{DD}
0	1	0 V to 2 × V_{REF}	−2 × V_{REF} to +2 × V_{REF}	Not applicable
1	0	0 V to 2 × V_{REF}	−2 × V_{REF} to +2 × V_{REF}	Not applicable
1	1	0 V to V_{REF}	−V_{REF} to +V_{REF}	Not applicable

[1] For more information, see the ADC Sampling Mode Subregister (Address 0x12) section.
[2] The contents of the VIN RANGE0 and VIN RANGE1 subregisters are ignored when the AD7292 is configured to sample with respect to AV_{DD}; the only input range allowed when sampling with respect to AV_{DD} is from (AV_{DD} − 4 × V_{REF}) to AV_{DD}.

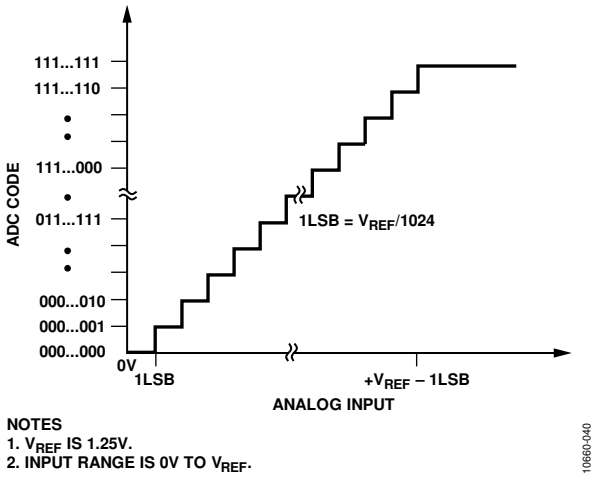


Figure 34. Straight Binary Transfer Characteristic Corresponding to Single-Ended Input Range of 0 V to V_{REF}

Table 11. Output Codes and Ideal Input Voltages (AV_{DD} = 5 V)

	Analog Input Range							
	Single-Ended Mode of Operation				Differential Mode of Operation			
Description	0 V to 4 × V_{REF}	0 V to 2 × V_{REF}	0 V to V_{REF}	(AV_{DD} − 4 × V_{REF}) to AV_{DD}	−4 × V_{REF} to +4 × V_{REF}	−2 × V_{REF} to +2 × V_{REF}	−V_{REF} to +V_{REF}	Digital Output Code (Hex)
+FSR − 1 LSB	4.995117 V	2.497559 V	1.248779 V	4.995117 V	4.990234 V	2.495117 V	1.247559 V	0x3FF
Midscale + 1 LSB	2.504883 V	1.252441 V	0.626221 V	2.504883 V	0.009766 V	0.004883 V	0.002441 V	0x201
Midscale	2.5 V	1.25 V	0.625 V	2.5 V	0 V	0 V	0 V	0x200
Midscale − 1 LSB	2.495117 V	1.247559 V	0.623779 V	2.495117 V	−0.009766 V	−0.004883 V	−0.002441 V	0x1FF
−FSR + 1 LSB	0.004883 V	0.002441 V	0.001221 V	0.004883 V	4.995117 V	−2.495117 V	−1.247559 V	0x001
−FSR	0 V	0 V	0 V	0 V	−5 V	−2.5 V	−1.25 V	0x000

TEMPERATURE SENSOR

The AD7292 contains one local temperature sensor. The on-chip, band gap temperature sensor measures the temperature of the AD7292 die. The temperature sensor input gathers data and computes a value over a period of several hundred microseconds. The temperature measurement takes place continuously in the background, leaving the user free to perform conversions on the other channels.

After a temperature value is computed, a signal passes to the control logic to initiate a conversion automatically. If an ADC conversion is in progress, the temperature sensor conversion is performed as soon as the ADC conversion is completed. If the ADC is idle, the temperature sensor conversion takes place immediately.

The T_{SENSE} conversion result register stores the result of the last conversion on the temperature channel; this result can be read at any time provided that the temperature sensor is enabled via the temperature sensor subregister within the configuration register bank (see the Temperature Sensor Subregister (Address 0x20) section).

Temperature readings from the ADC are stored in the T_{SENSE} conversion result register. Results are in 14-bit straight binary format and accommodate both positive and negative temperature measurements. Bit D0 and Bit D1 hold alert flags; Bit D2 stores the LSB, which corresponds to 0.03125°C if the digital filter is enabled.

Table 12 provides examples of temperature sensor data. An output of all 0s is equal to −256°C; this value is output by the AD7292 until the first measurement is completed. Note that when digital filtering is disabled, Bit D3 and Bit D2 of the T_{SENSE} conversion result register are set to 0, producing a 12-bit straight binary result with an LSB of 0.125°C. When the T_{SENSE} conversion result is read via the ADC data register (Address 0x01), the temperature sensor result is a 10-bit result with an LSB that equates to 0.5°C.

Table 12. Temperature Sensor Data Format

Temperature (°C)	T_{SENSE} Conversion Result Register, Bits[D15:D2]
−40	01 1011 0000 0000
−25	01 1100 1110 0000
−10	01 1110 1100 0000
−0.03125	01 1111 1111 1111
0	10 0000 0000 0000
+0.03125	10 0000 0000 0001
+10	10 0001 0100 0000
+25	10 0011 0010 0000
+50	10 0110 0100 0000
+75	10 1001 0110 0000
+100	10 1100 1000 0000
+125	10 1111 1010 0000

DAC OPERATION

The four DACs of the AD7292 provide digital control with 10 bits of resolution. DAC outputs VOUT0 to VOUT3 feature an output voltage range up to 5 V (LSB of 4.88 mV).

The DAC output buffer can be controlled via software using the GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 subregisters within the configuration register bank, or via hardware using the GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 pins.

DIGITAL I/O PINS

To aid in system monitoring, the AD7292 features 12 digital I/O pins. All 12 pins can be configured as GPIO pins. Six of the digital I/O pins can be configured for other functionality; on power-up, the non-GPIO functionality of these six pins is enabled by default. For more information, see the Digital Output Driver Subregister (Address 0x01) section and the Digital I/O Function Subregister (Address 0x02) section.

GPIO0/ALERT0 and GPIO1/ALERT1 Pins

When Pin 27 and Pin 26 (GPIO0/ALERT0 and GPIO1/ALERT1, respectively) are configured as alert pins, they act as out-of-range indicators that become active when the selected conversion result exceeds the high or low limit stored in the alert limits register bank. The polarity of the alert output pins can be set to active high or active low via the general subregister within the configuration register bank (see the General Subregister (Address 0x08) section).

GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 Pins

When Pin 25 and Pin 23 (GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1, respectively) are configured as DAC disable pins, they can be used to power down the selected DAC outputs, as determined by the contents of the GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 subregisters within the configuration register bank. For more information, see the GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 Subregisters (Address 0x30 and Address 0x31) section.

GPIO3/LDAC Pin

When Pin 24 (GPIO3/LDAC) is configured as an LDAC pin, the DAC registers are updated when this input pin is taken high.

GPIO6/BUSY Pin

Pin 21 (GPIO6/BUSY) can be configured as a general-purpose input/output or as a busy output pin. When configured as a busy output pin, this pin transitions high when a conversion starts and remains high until the conversion is completed.

SERIAL PORT INTERFACE (SPI)

The AD7292 serial port interface (SPI) allows the user to configure the device for specific functions and operations through an internal structured register space. The interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT. The SPI reference level is set by Pin 5 (V_{DRIVE}) to a level in the range of 1.8 V to 5.25 V.

SCLK is the serial clock input for the device; all data transfers on DIN or DOUT take place with respect to SCLK. The chip select input pin ($\overline{CS}$) is an active low control that initiates the data transfer and conversion process.

Data is clocked into the AD7292 on the SCLK falling edge. Data is loaded into the device MSB first. The length of each frame can vary and depends on the command being sent. Data is clocked out of the AD7292 on DOUT in the same frame as the read command, on the rising edge of SCLK while $\overline{CS}$ is low. When $\overline{CS}$ is high, the SCLK and DIN signals are ignored and the DOUT line becomes high impedance.

INTERFACE PROTOCOL

When reading from or writing to the AD7292, the first byte contains the address pointer (see Table 13). Bit D7 and Bit D6 of the address pointer are the read and write bits, respectively. Bit D5 to Bit D0 of the address pointer specify the register address for the read or write operation. A register can be simultaneously read from and written to by setting both Bit D7 and Bit D6 to 1.

Table 13. Address Pointer

D7	D6	D5	D4	D3	D2	D1	D0
R	W	Register select					

After the address pointer, subsequent data for writing to the part is supplied in bytes (see Figure 36). Some registers are located within register banks and, therefore, require both a pointer address and a subpointer address. The subpointer address is specified in the first byte following the pointer address (see Figure 37). Figure 36 through Figure 38 show the read and write data formats. These figures show read operations; for a write to a register or subregister, the write bit is set and the DOUT line remains high impedance.

If neither the read nor write bit is set (Bit D7 and Bit D6 of the address pointer are set to 0), the address pointer is updated but no data is read or written. Note that writing this command also reinitializes the ADC sequencer (see the ADC Conversion Control section).

On completion of a read or write, the AD7292 is ready to accept a new pointer address; alternatively, the $\overline{CS}$ pin can be taken high to terminate the operation.

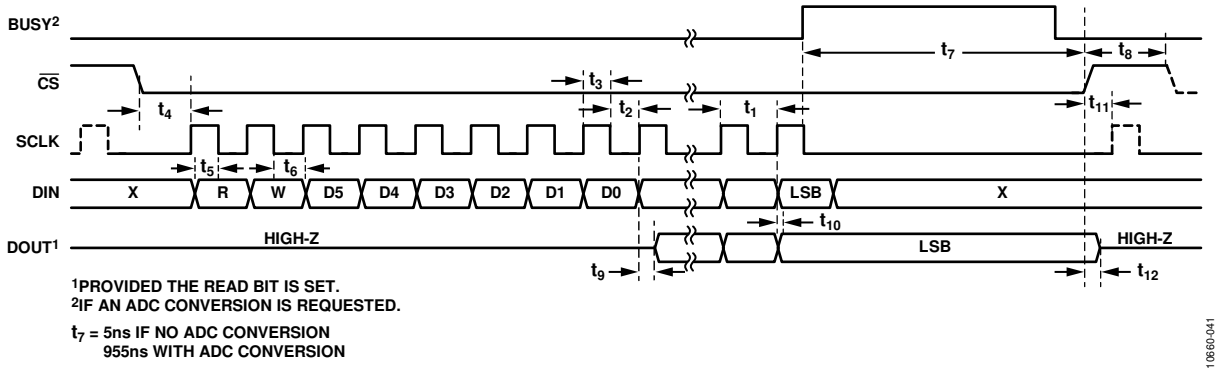


Figure 35. Serial Interface Timing Diagram

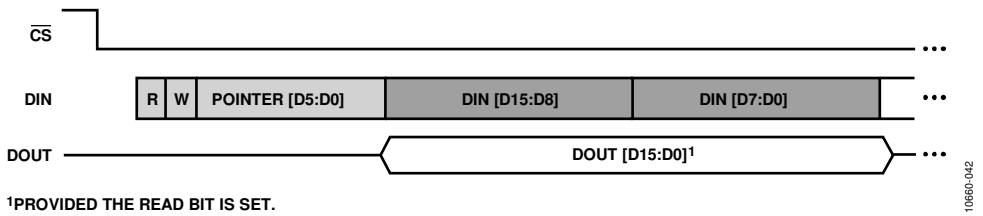


Figure 36. Accessing a 16-Bit Register

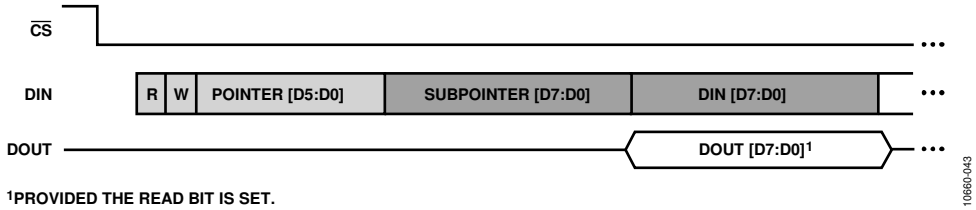


Figure 37. Accessing an 8-Bit Subregister Within a Register Bank

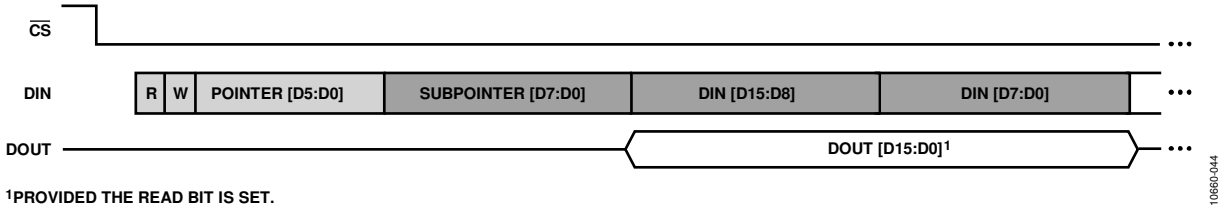


Figure 38. Accessing a 16-Bit Subregister Within a Register Bank

REGISTER STRUCTURE

The AD7292 contains internal registers that store conversion results, high and low conversion limits, and information to configure and control the device (see Figure 39). Each register has an address; the address pointer register points to the address when communicating with the register. Some registers and sub-registers contain reserved bits. The AD7292 allows either a 0 or a 1 to be written to these reserved bits.

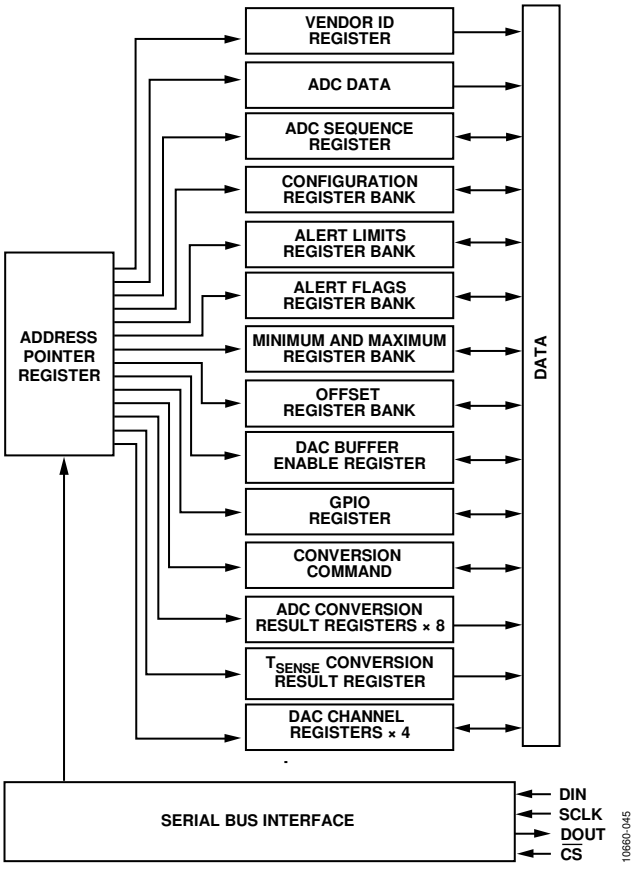


Figure 39. AD7292 Register Structure

Table 14 lists each register and specifies whether the register has read access or read and write access.

Table 14. AD7292 Registers

Address	Register Name	Access[1]	Data Format
0x00	Vendor ID register	R	Figure 36
0x01	ADC data register	R	Figure 36
0x03	ADC sequence register	R/W	Figure 36
0x05	Configuration register bank	R/W	Figure 38
0x06	Alert limits register bank	R/W	Figure 38
0x07	Alert flags register bank	R/W	Figure 38
0x08	Minimum and maximum register bank	R/W	Figure 38
0x09	Offset register bank	R/W	Figure 37
0x0A	DAC buffer enable register	R/W	Figure 36
0x0B	GPIO register	R/W	Figure 36
0x0E	Conversion command[2]	N/A	N/A
0x10	ADC conversion result register, Channel 0	R	Figure 36
0x11	ADC conversion result register, Channel 1	R	Figure 36
0x12	ADC conversion result register, Channel 2	R	Figure 36
0x13	ADC conversion result register, Channel 3	R	Figure 36
0x14	ADC conversion result register, Channel 4	R	Figure 36
0x15	ADC conversion result register, Channel 5	R	Figure 36
0x16	ADC conversion result register, Channel 6	R	Figure 36
0x17	ADC conversion result register, Channel 7	R	Figure 36
0x20	T_{SENSE} conversion result register	R	Figure 36
0x30	DAC Channel 0 register	R/W	Figure 36
0x31	DAC Channel 1 register	R/W	Figure 36
0x32	DAC Channel 2 register	R/W	Figure 36
0x33	DAC Channel 3 register	R/W	Figure 36

[1] R is read only; R/W is read/write.
[2] See the ADC Conversion Command section for more information.

REGISTER DESCRIPTIONS

VENDOR ID REGISTER (ADDRESS 0x00)

The 16-bit, read-only vendor ID register stores the Analog Devices vendor ID, 0x0018. The vendor ID register is provided to identify the AD7292 to an SPI master such as a microcontroller.

ADC DATA REGISTER (ADDRESS 0x01)

The 16-bit, read-only ADC data register provides read access to the most recent ADC conversion result. This register provides 10 bits of conversion data, four channel identifier bits, and two alert bits (see the ADC Conversion Control section).

ADC SEQUENCE REGISTER (ADDRESS 0x03)

The 16-bit, read/write ADC sequence register allows the user to specify a preprogrammed sequence of ADC channels for conversion. The ADC converts on each of the specified ADC channels in turn. For more information, see the ADC Conversion Control section. Table 16 describes the register bit functions. Bit D15 is the first bit in the data stream. On power-up, the ADC sequence register contains all 0s by default.

Temperature sensor results can be inserted into the sequence by writing a 1 to Bit D8 of the ADC sequence register, provided that the temperature sensor has been enabled in the temperature sensor subregister within the configuration register bank (see the Temperature Sensor Subregister (Address 0x20) section).

CONFIGURATION REGISTER BANK (ADDRESS 0x05)

The configuration register bank subregisters are listed in Table 15. On power-up, the subregisters within the configuration register bank contain all 0s by default.

Table 15. Configuration Register Bank Subregisters

Subaddress (Hex)	Subregister Name[1]
0x01	Digital output driver
0x02	Digital I/O function
0x08	General
0x10	VIN RANGE0
0x11	VIN RANGE1
0x12	ADC sampling mode
0x13	VIN filter
0x14	Conversion delay control
0x15	VIN ALERT0 routing
0x16	VIN ALERT1 routing
0x20	Temperature sensor
0x21	Temperature sensor alert routing
0x30	GPIO2/DAC DISABLE0
0x31	GPIO4/DAC DISABLE1

[1] All subregisters in the configuration register bank are read/write.

Table 16. ADC Sequence Register, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D9]	Reserved	R/W	Reserved
D8	T_{SENSE} readback enable	R/W	0 = disable T_{SENSE} readback 1 = enable T_{SENSE} readback
D7	ADC Channel 7 convert	R/W	0 = disable conversion of Channel 7 1 = enable conversion of Channel 7
D6	ADC Channel 6 convert	R/W	0 = disable conversion of Channel 6 1 = enable conversion of Channel 6
D5	ADC Channel 5 convert	R/W	0 = disable conversion of Channel 5 1 = enable conversion of Channel 5
D4	ADC Channel 4 convert	R/W	0 = disable conversion of Channel 4 1 = enable conversion of Channel 4
D3	ADC Channel 3 convert	R/W	0 = disable conversion of Channel 3 1 = enable conversion of Channel 3
D2	ADC Channel 2 convert	R/W	0 = disable conversion of Channel 2 1 = enable conversion of Channel 2
D1	ADC Channel 1 convert	R/W	0 = disable conversion of Channel 1 1 = enable conversion of Channel 1
D0	ADC Channel 0 convert	R/W	0 = disable conversion of Channel 0 1 = enable conversion of Channel 0

Digital Output Driver Subregister (Address 0x01)

The 16-bit digital output driver subregister enables the output drivers of the digital I/O pins. Setting Bits[D11:D0] to 1 enables the corresponding digital I/O output driver. Six of the 12 digital I/O pins offer mixed functionality (see Table 18). When a digital I/O pin is configured as a GPIO pin and its output is enabled, its value is controlled by the GPIO register (see the GPIO Register (Address 0x0B) section).

Digital I/O Function Subregister (Address 0x02)

Six of the 12 GPIO pins offer dual functionality. To enable standard GPIO functionality, write a 1 to the corresponding bit in the 16-bit digital I/O subregister. To enable the alternative functionality, write a 0 to the appropriate bit (see Table 18). For example, to configure the GPIO6/BUSY pin as an ADC busy pin, write a 0 to Bit D6 of Address 0x02.

Table 17. Digital Output Driver Subregister, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D12]	Reserved	R/W	Reserved
D11	GPIO11 output	R/W	0 = disable GPIO11 output driver; 1 = enable GPIO11 output driver
D10	GPIO10 output	R/W	0 = disable GPIO10 output driver; 1 = enable GPIO10 output driver
D9	GPIO9 output	R/W	0 = disable GPIO9 output driver; 1 = enable GPIO9 output driver
D8	GPIO8 output	R/W	0 = disable GPIO8 output driver; 1 = enable GPIO8 output driver
D7	GPIO7 output	R/W	0 = disable GPIO7 output driver; 1 = enable GPIO7 output driver
D6	GPIO6 output	R/W	0 = disable GPIO6 output driver; 1 = enable GPIO6/BUSY output driver
D5	GPIO5 output	R/W	0 = disable GPIO5 output driver; 1 = enable GPIO5 output driver
D4	GPIO4 output	R/W	0 = disable GPIO4 output driver; 1 = enable GPIO4/DAC DISABLE1 output driver
D3	GPIO3 output	R/W	0 = disable GPIO3 output driver; 1 = enable GPIO3/LDAC output driver
D2	GPIO2 output	R/W	0 = disable GPIO2 output driver; 1 = enable GPIO4/DAC DISABLE0 output driver
D1	GPIO1 output	R/W	0 = disable GPIO1 output driver; 1 = enable GPIO1/ALERT1 output driver
D0	GPIO0 output	R/W	0 = disable GPIO0 output driver; 1 = enable GPIO1/ALERT0 output driver

Table 18. Digital I/O Function Subregister, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D12]	Reserved	R/W	Reserved
D11	GPIO11	R/W	0 = reserved 1 = enable the GPIO11 function
D10	GPIO10	R/W	0 = reserved 1 = enable the GPIO10 function
D9	GPIO9	R/W	0 = reserved 1 = enable the GPIO9 function
D8	GPIO8	R/W	0 = reserved 1 = enable the GPIO8 function
D7	GPIO7	R/W	0 = reserved 1 = enable the GPIO7 function
D6	GPIO6/BUSY	R/W	0 = enable the ADC busy output function 1 = enable the GPIO6 function
D5	GPIO5	R/W	0 = reserved 1 = enable the GPIO5 function
D4	GPIO4/DAC DISABLE1	R/W	0 = enable the DAC DISABLE1 input function 1 = enable the GPIO4 function
D3	GPIO3/LDAC	R/W	0 = enable the LDAC input function 1 = enable the GPIO3 function
D2	GPIO2/DAC DISABLE0	R/W	0 = enable the DAC DISABLE0 input function 1 = enable the GPIO2 function
D1	GPIO1/ALERT1	R/W	0 = enable the ALERT1 output function 1 = enable the GPIO1 function
D0	GPIO0/ALERT0	R/W	0 = enable the ALERT0 output function 1 = enable the GPIO0 function

General Subregister (Address 0x08)

When the GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 pins are configured as DAC disable pins (via the digital I/O function subregister), Bits[D2:D1] of the 16-bit general subregister control the power disable mode of these two pins. Table 19 shows the four power disable modes. The GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 subregisters determine which DAC outputs are controlled by the GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 pins (see Table 29 and Table 30).

Bit D5 and Bit D4 of the general subregister are used to configure the polarity of the ALERT output pins when the GPIO1/ALERT1 and GPIO0/ALERT0 pins are configured as alert outputs (see the Digital Output Driver Subregister (Address 0x01) section and the Digital I/O Function Subregister (Address 0x02) section).

Bit D8 is used to select the source of the voltage reference used for the AD7292. When this bit is set to 1, the external reference is used. When this bit is set to 0, the internal reference is used.

Table 19. General Subregister, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D9]	Reserved	R/W	Reserved.
D8	Reference mode	R/W	This bit specifies whether the internal reference or an external reference is used. 0 = internal reference used (default). 1 = external reference used.
[D7:D6]	Reserved	R/W	Reserved.
D5	ALERT1 polarity	R/W	When the GPIO1/ALERT1 pin is configured to function as an alert, this bit sets the polarity of the ALERT1 pin. 0 = active low (default). 1 = active high.
D4	ALERT0 polarity	R/W	When the GPIO0/ALERT0 pin is configured to function as an alert, this bit sets the polarity of the ALERT0 pin. 0 = active low (default). 1 = active high.
D3	Reserved	R/W	Reserved.
[D2:D1]	DAC disable mode	R/W	These bits control the disable mode of the GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 pins when these pins are configured to function as DAC disable pins. 00 = 1 kΩ and 100 kΩ resistors in parallel to ground (default). 01 = 100 kΩ resistor to ground. 10 = 1 kΩ resistor to ground. 11 = high impedance.
D0	Reserved	R/W	Reserved.

VIN RANGE0 and VIN RANGE1 Subregisters (Address 0x10 and Address 0x11)

The 16-bit VIN RANGE0 and VIN RANGE1 subregisters specify a divide-by-2 factor for each analog input channel, VIN0 to VIN7. A divide-by-2 factor from both the VIN RANGE0 and VIN RANGE1 subregisters can be applied to each channel; that is, setting Bit D0 of VIN RANGE1 and Bit D0 of VIN RANGE0 enables a divide-by-4 factor for the VIN0 input range. The settings of the VIN RANGE0 and VIN RANGE1 bits are ignored if samples are with respect to AV_{DD} (see the ADC Sampling Mode Subregister (Address 0x12) section).

Table 20. VIN RANGE0 and VIN RANGE1 Subregisters, Bit Function Descriptions (Default = 0)

Bits	Bit Name	R/W	Description
[D15:D8]	Reserved	R/W	Reserved
D7	VIN7 range	R/W	Analog input range for VIN7 (see Table 21)
D6	VIN6 range	R/W	Analog input range for VIN6 (see Table 21)
D5	VIN5 range	R/W	Analog input range for VIN5 (see Table 21)
D4	VIN4 range	R/W	Analog input range for VIN4 (see Table 21)
D3	VIN3 range	R/W	Analog input range for VIN3 (see Table 21)
D2	VIN2 range	R/W	Analog input range for VIN2 (see Table 21)
D1	VIN1 range	R/W	Analog input range for VIN1 (see Table 21)
D0	VIN0 range	R/W	Analog input range for VIN0 (see Table 21)

Table 21. Analog Input Range Selection

Subregister Bit Settings		Sample with Respect to A_{GND}		Sample with Respect to AV_{DD}
		Single-Ended Input Range	Differential Input Range	Single-Ended Input Range
VIN RANGE1	VIN RANGE0	(VIN0 to VIN7)	(VIN0 and VIN1 Only)	(VIN0 to VIN7)
0	0	0 V to $4 \times V_{REF}$	$-4 \times V_{REF}$ to $+4 \times V_{REF}$	($AV_{DD} - 4 \times V_{REF}$) to AV_{DD}
0	1	0 V to $2 \times V_{REF}$	$-2 \times V_{REF}$ to $+2 \times V_{REF}$	Not applicable
1	0	0 V to $2 \times V_{REF}$	$-2 \times V_{REF}$ to $+2 \times V_{REF}$	Not applicable
1	1	0 V to V_{REF}	$-V_{REF}$ to $+V_{REF}$	Not applicable

ADC Sampling Mode Subregister (Address 0x12)

Table 22 lists the bit function descriptions for the 16-bit ADC sampling mode subregister. Bit D0 allows the user to enable differential input mode for analog input channels VIN0 and VIN1. When enabled and converting on VIN0, the differential input to the ADC is (VIN0, VIN1). When enabled and converting on VIN1, the differential input to the ADC is (VIN1, VIN0). To use differential mode, Bit D0 must be set to 1.

Bits[D15:D8] specify whether the corresponding analog input, VIN7 to VIN0, is measured with respect to AV_{DD} or A_{GND}.

Table 22. ADC Sampling Mode Subregister, Bit Function Descriptions (Default = 0)

Bits	Bit Name	R/W	Description
D15	VIN7 sampling mode	R/W	This bit specifies whether VIN7 is measured with respect to AV_{DD} or A_{GND}. 0 = sample with respect to AV_{DD}. 1 = sample with respect to A_{GND}.
D14	VIN6 sampling mode	R/W	This bit specifies whether VIN6 is measured with respect to AV_{DD} or A_{GND}. 0 = sample with respect to AV_{DD}. 1 = sample with respect to A_{GND}.
D13	VIN5 sampling mode	R/W	This bit specifies whether VIN5 is measured with respect to AV_{DD} or A_{GND}. 0 = sample with respect to AV_{DD}. 1 = sample with respect to A_{GND}.
D12	VIN4 sampling mode	R/W	This bit specifies whether VIN4 is measured with respect to AV_{DD} or A_{GND}. 0 = sample with respect to AV_{DD}. 1 = sample with respect to A_{GND}.
D11	VIN3 sampling mode	R/W	This bit specifies whether VIN3 is measured with respect to AV_{DD} or A_{GND}. 0 = sample with respect to AV_{DD}. 1 = sample with respect to A_{GND}.
D10	VIN2 sampling mode	R/W	This bit specifies whether VIN2 is measured with respect to AV_{DD} or A_{GND}. 0 = sample with respect to AV_{DD}. 1 = sample with respect to A_{GND}.
D9	VIN1 sampling mode	R/W	This bit specifies whether VIN1 is measured with respect to AV_{DD} or A_{GND}. 0 = sample with respect to AV_{DD}. 1 = sample with respect to A_{GND}.
D8	VIN0 sampling mode	R/W	This bit specifies whether VIN0 is measured with respect to AV_{DD} or A_{GND}. 0 = sample with respect to AV_{DD}. 1 = sample with respect to A_{GND}.
[D7:D1]	Reserved	R/W	Reserved.
D0	VIN0/VIN1 differential mode	R/W	This bit specifies whether VIN0 and VIN1 function as two single-ended inputs or as a differential pair. 0 = single-ended mode. 1 = differential mode.

VIN Filter Subregister (Address 0x13)

The 16-bit VIN filter subregister enables digital filtering of the analog inputs channels. The digital filter consists of a simple low-pass filter function to help reduce unwanted noise on dc signals. Writing a 1 to Bits[D7:D0] in this subregister enables digital filtering of the corresponding analog input channel (see Table 23). On power-up, the VIN filter subregister contains all 0s by default.

Conversion Delay Control Subregister (Address 0x14)

The 16-bit conversion delay control subregister is used to delay the start (including the sample point) of a conversion. The delay is a count of internal ADC clocks following the falling SCLK signal that triggers the start of a conversion.

For example, if the conversion delay control subregister holds the value 0x0003, three ADC clocks are counted before the ADC enters hold mode and the conversion begins. The ADC clock has a period of 40 ns typically.

If the conversion delay control subregister is set to a nonzero value N, the ADC waits for the programmed number of ADC clock periods (N) after a conversion is triggered before sampling the input. If the register holds the default value of 0, there is no delay, and the conversion is started from the falling SCLK that triggers the start of the conversion. When using the conversion delay, the conversion is extended by N + 1 clocks.

Table 23. VIN Filter Subregister, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D8]	Reserved	R/W	Reserved
D7	Enable digital filtering of VIN7	R/W	0 = disable digital filtering of VIN7 1 = enable digital filtering of VIN7
D6	Enable digital filtering of VIN6	R/W	0 = disable digital filtering of VIN6 1 = enable digital filtering of VIN6
D5	Enable digital filtering of VIN5	R/W	0 = disable digital filtering of VIN5 1 = enable digital filtering of VIN5
D4	Enable digital filtering of VIN4	R/W	0 = disable digital filtering of VIN4 1 = enable digital filtering of VIN4
D3	Enable digital filtering of VIN3	R/W	0 = disable digital filtering of VIN3 1 = enable digital filtering of VIN3
D2	Enable digital filtering of VIN2	R/W	0 = disable digital filtering of VIN2 1 = enable digital filtering of VIN2
D1	Enable digital filtering of VIN1	R/W	0 = disable digital filtering of VIN1 1 = enable digital filtering of VIN1
D0	Enable digital filtering of VIN0	R/W	0 = disable digital filtering of VIN0 1 = enable digital filtering of VIN0

Table 24. Conversion Delay Control Subregister, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D0]	Delay value	R/W	These bits specify the 16-bit delay value (0 to 0xFFFF) before the start of a conversion. The delay is a count of internal ADC clocks following the falling SCLK signal.

VIN ALERT0 Routing and VIN ALERT1 Routing Subregisters (Address 0x15 and Address 0x16)

The 16-bit VIN ALERT0 and VIN ALERT1 subregisters enable the routing of alerts from the analog input channels, VIN0 to VIN7, to the GPIO0/ALERT0 and GPIO1/ALERT1 pins (see Table 25 and Table 26.

For information about how to configure the GPIO0/ALERT0 and GPIO1/ALERT1 pins as alert pins, see the Digital I/O Function Subregister (Address 0x02) section and the Digital Output Driver Subregister (Address 0x01) section.

For information about how to enable routing of the temperature sensor alerts, see the Temperature Sensor Alert Routing Subregister (Address 0x21) section.

Table 25. VIN ALERT0 Routing Subregister, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D8]	Reserved	R/W	Reserved
D7	Route VIN7 alerts to ALERT0 pin	R/W	0 = disable routing of VIN7 alerts to the ALERT0 pin 1 = enable routing of VIN7 alerts to the ALERT0 pin
D6	Route VIN6 alerts to ALERT0 pin	R/W	0 = disable routing of VIN6 alerts to the ALERT0 pin 1 = enable routing of VIN6 alerts to the ALERT0 pin
D5	Route VIN5 alerts to ALERT0 pin	R/W	0 = disable routing of VIN5 alerts to the ALERT0 pin 1 = enable routing of VIN5 alerts to the ALERT0 pin
D4	Route VIN4 alerts to ALERT0 pin	R/W	0 = disable routing of VIN4 alerts to the ALERT0 pin 1 = enable routing of VIN4 alerts to the ALERT0 pin
D3	Route VIN3 alerts to ALERT0 pin	R/W	0 = disable routing of VIN3 alerts to the ALERT0 pin 1 = enable routing of VIN3 alerts to the ALERT0 pin
D2	Route VIN2 alerts to ALERT0 pin	R/W	0 = disable routing of VIN2 alerts to the ALERT0 pin 1 = enable routing of VIN2 alerts to the ALERT0 pin
D1	Route VIN1 alerts to ALERT0 pin	R/W	0 = disable routing of VIN1 alerts to the ALERT0 pin 1 = enable routing of VIN1 alerts to the ALERT0 pin
D0	Route VIN0 alerts to ALERT0 pin	R/W	0 = disable routing of VIN0 alerts to the ALERT0 pin 1 = enable routing of VIN0 alerts to the ALERT0 pin

Table 26. VIN ALERT1 Routing Subregister, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D0]	Reserved	R/W	Reserved
D7	Route VIN7 alerts to ALERT1 pin	R/W	0 = disable routing of VIN7 alerts to the ALERT1 pin 1 = enable routing of VIN7 alerts to the ALERT1 pin
D6	Route VIN6 alerts to ALERT1 pin	R/W	0 = disable routing of VIN6 alerts to the ALERT1 pin 1 = enable routing of VIN6 alerts to the ALERT1 pin
D5	Route VIN5 alerts to ALERT1 pin	R/W	0 = disable routing of VIN5 alerts to the ALERT1 pin 1 = enable routing of VIN5 alerts to the ALERT1 pin
D4	Route VIN4 alerts to ALERT1 pin	R/W	0 = disable routing of VIN4 alerts to the ALERT1 pin 1 = enable routing of VIN4 alerts to the ALERT1 pin
D3	Route VIN3 alerts to ALERT1 pin	R/W	0 = disable routing of VIN3 alerts to the ALERT1 pin 1 = enable routing of VIN3 alerts to the ALERT1 pin
D2	Route VIN2 alerts to ALERT1 pin	R/W	0 = disable routing of VIN2 alerts to the ALERT1 pin 1 = enable routing of VIN2 alerts to the ALERT1 pin
D1	Route VIN1 alerts to ALERT1 pin	R/W	0 = disable routing of VIN1 alerts to the ALERT1 pin 1 = enable routing of VIN1 alerts to the ALERT1 pin
D0	Route VIN0 alerts to ALERT1	R/W	0 = disable routing of VIN0 alerts to the ALERT1 pin 1 = enable routing of VIN0 alerts to the ALERT1 pin

Temperature Sensor Subregister (Address 0x20)

The 16-bit temperature sensor subregister enables temperature sensor conversions and digital filtering of the temperature sensor channel. To enable temperature sensor conversions or digital filtering, the corresponding bit in the temperature sensor subregister must be set to 1 (see Table 27). On power-up, the temperature sensor subregister contains all 0s by default.

Temperature Sensor Alert Routing Subregister (Address 0x21)

The 16-bit temperature sensor alert routing subregister enables the routing of alerts from the internal temperature sensor to the GPIO0/ALERT0 and GPIO1/ALERT1 pins (see Table 28).

For information about how to configure the GPIO0/ALERT0 and GPIO1/ALERT1 pins as alert pins, see the Digital I/O Function Subregister (Address 0x02) section and the Digital Output Driver Subregister (Address 0x01) section.

For information about how to enable routing of the analog input channel alerts, see the VIN Filter Subregister (Address 0x13) and Conversion Delay Control Subregister (Address 0x14) section.

Table 27. Temperature Sensor Subregister, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D9]	Reserved	R/W	Reserved.
D8	Enable/disable digital filtering of T_{SENSE}	R/W	This bit specifies whether digital filtering is enabled on the temperature sensor channel. 0 = disable digital filtering of the temperature sensor channel (default). 1 = enable digital filtering of the temperature sensor channel.
[D7:D1]	Reserved	R/W	Reserved.
D0	Enable/disable T_{SENSE} conversions	R/W	This bit enables or disables conversion of the temperature sensor channel. 0 = disable T_{SENSE} conversions (default). 1 = enable T_{SENSE} conversions.

Table 28. Temperature Sensor Alert Routing Subregister, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D9]	Reserved	R/W	Reserved.
D8	Route T_{SENSE} alerts to ALERT1 pin	R/W	This bit specifies whether alerts from the internal temperature sensor are routed to the ALERT1 pin. 0 = disable routing of alerts from the temperature sensor to the ALERT1 pin (default). 1 = enable routing of alerts from the temperature sensor to the ALERT1 pin.
[D7:D1]	Reserved	R/W	Reserved.
D0	Route T_{SENSE} alerts to ALERT0 pin	R/W	This bit specifies whether alerts from the internal temperature sensor are routed to the ALERT0 pin. 0 = disable routing of alerts from the temperature sensor to the ALERT0 pin (default). 1 = enable routing of alerts from the temperature sensor to the ALERT0 pin.

GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 Subregisters (Address 0x30 and Address 0x31)

The 16-bit, read/write GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 subregisters specify which DAC channels are disabled by the GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 pins. For example, when Bit D0 in the GPIO2/DAC DISABLE0 subregister is set to 1, the GPIO2/DAC DISABLE0 pin disables DAC output VOUT0 when the pin is taken high. On power-up, these subregisters contain all 0s by default.

For information about how to enable the DAC disable function on the GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 pins, see the Digital Output Driver Subregister (Address 0x01) section and the Digital I/O Function Subregister (Address 0x02) section.

Table 29. GPIO2/DAC DISABLE0 Subregister, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D4]	Reserved	R/W	Reserved.
D3	Disable VOUT3 pin	R/W	This bit specifies whether the VOUT3 output is disabled when the GPIO2/DAC DISABLE0 pin is high. 0 = disable control of VOUT3 by the GPIO2/DAC DISABLE0 pin (default). 1 = enable control of VOUT3 by the GPIO2/DAC DISABLE0 pin.
D2	Disable VOUT2 pin	R/W	This bit specifies whether the VOUT2 output is disabled when the GPIO2/DAC DISABLE0 pin is high. 0 = disable control of VOUT2 by the GPIO2/DAC DISABLE0 pin (default). 1 = enable control of VOUT2 by the GPIO2/DAC DISABLE0 pin.
D1	Disable VOUT1 pin	R/W	This bit specifies whether the VOUT1 output is disabled when the GPIO2/DAC DISABLE0 pin is high. 0 = disable control of VOUT1 by the GPIO2/DAC DISABLE0 pin (default). 1 = enable control of VOUT1 by the GPIO2/DAC DISABLE0 pin.
D0	Disable VOUT0 pin	R/W	This bit specifies whether the VOUT0 output is disabled when the GPIO2/DAC DISABLE0 pin is high. 0 = disable control of VOUT0 by the GPIO2/DAC DISABLE0 pin (default). 1 = enable control of VOUT0 by the GPIO2/DAC DISABLE0 pin.

Table 30. GPIO4/DAC DISABLE1 Subregister, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D4]	Reserved	R/W	Reserved.
D3	Disable VOUT3 pin	R/W	This bit specifies whether the VOUT3 output is disabled when the GPIO4/DAC DISABLE1 pin is high. 0 = disable control of VOUT3 by the GPIO4/DAC DISABLE1 pin (default). 1 = enable control of VOUT3 by the GPIO4/DAC DISABLE1 pin.
D2	Disable VOUT2 pin	R/W	This bit specifies whether the VOUT2 output is disabled when the GPIO4/DAC DISABLE1 pin is high. 0 = disable control of VOUT2 by the GPIO4/DAC DISABLE1 pin (default). 1 = enable control of VOUT2 by the GPIO4/DAC DISABLE1 pin.
D1	Disable VOUT1 pin	R/W	This bit specifies whether the VOUT1 output is disabled when the GPIO4/DAC DISABLE1 pin is high. 0 = disable control of VOUT1 by the GPIO4/DAC DISABLE1 pin (default). 1 = enable control of VOUT1 by the GPIO4/DAC DISABLE1 pin.
D0	Disable VOUT0 pin	R/W	This bit specifies whether the VOUT0 output is disabled when the GPIO4/DAC DISABLE1 pin is high. 0 = disable control of VOUT0 by the GPIO4/DAC DISABLE1 pin (default). 1 = enable control of VOUT0 by the GPIO4/DAC DISABLE1 pin.

ALERT LIMITS REGISTER BANK (ADDRESS 0x06)

The alert limits register bank comprises subregisters that set the high and low alert limits for the eight analog input channels and the temperature sensor channel (see Table 31). Each subregister is 16 bits in length; values are 10-bit, left-justified (padded with 0s as the 6 LSBs). On power-up, the low limit and hysteresis subregisters contain all 0s, whereas the high limit subregisters are set to 0xFFC0.

If a conversion result exceeds the high or low limit set in the alert limits subregister, the AD7292 signals an alert in one or more of the following ways:

- Via hardware using the GPIO0/ALERT0 and GPIO1/ALERT1 pins (see the Hardware Alert Pins section)
- Via software using the alert flag bits in the conversion result registers (see the ADC Conversion Result Registers, VIN0 to VIN7 (Address 0x10 to Address 0x17) section and the T_{SENSE} Conversion Result Register (Address 0x20) section)
- Via software using the alert bits in the alert flags register bank (see the Alert Flags Register Bank (Address 0x07) section)

Alert High Limit and Alert Low Limit Subregisters

The alert high limit subregisters store the upper limit that activates an alert. If the conversion result is greater than the value in the alert high limit subregister, an alert is triggered. The alert low limit subregister stores the lower limit that activates an alert. If the conversion result is less than the value in the alert low limit subregister, an alert is triggered.

An alert associated with either the alert high limit or alert low limit subregister is cleared automatically after the monitored signal is back in range, that is, when the conversion result returns between the configured high and low limits. The contents of the alert flags subregisters are updated after each conversion (see the Alert Flags Register Bank (Address 0x07) section).

Hysteresis Subregisters

Each channel has an associated hysteresis subregister that stores the hysteresis value, N (see Table 31). The hysteresis subregisters can be used to avoid flicker on the GPIO0/ALERT0 and GPIO1/ALERT1 pins. If the hysteresis function is enabled, the conversion result must return to a value of at least N LSB below the alert high limit subregister value, or N LSB above the alert low limit subregister value for the alert output pins and alert flag bits to be reset (see Figure 46). The value of N is taken from the 10 MSBs of the 16-bit, read/write hysteresis subregister. For more information, see the Hysteresis section.

Table 31. Alert Limits Register Bank Subregisters

Subaddress (Hex)	Subregister Name[1]
0x00	VIN0 alert high limit
0x01	VIN0 alert low limit
0x02	VIN0 hysteresis
0x03	VIN1 alert high limit
0x04	VIN1 alert low limit
0x05	VIN1 hysteresis
0x06	VIN2 alert high limit
0x07	VIN2 alert low limit
0x08	VIN2 hysteresis
0x09	VIN3 alert high limit
0x0A	VIN3 alert low limit
0x0B	VIN3 hysteresis
0x0C	VIN4 alert high limit
0x0D	VIN4 alert low limit
0x0E	VIN4 hysteresis
0x0F	VIN5 alert high limit
0x10	VIN5 alert low limit
0x11	VIN5 hysteresis
0x12	VIN6 alert high limit
0x13	VIN6 alert low limit
0x14	VIN6 hysteresis
0x15	VIN7 alert high limit
0x16	VIN7 alert low limit
0x17	VIN7 hysteresis
0x18 to 0x2F	Reserved
0x30	T_{SENSE} alert high limit
0x31	T_{SENSE} alert low limit
0x32	T_{SENSE} hysteresis
0x33 to 0xFF	Reserved

[1] All subregisters in the alert limits register bank are read/write.

ALERT FLAGS REGISTER BANK (ADDRESS 0x07)

If a conversion result activates an alert (as specified in the alert limits register bank), the alert flags register bank can be read to obtain more information about the alert. This register bank contains the ADC alert flags and T_{SENSE} alert flags subregisters. Both subregisters store flags that are triggered when the minimum or maximum conversion limits, as defined in the alert limits register bank, are exceeded.

Table 32. Alert Flags Register Bank Subregisters

Subaddress (Hex)	Subregister Name[1]
0x00	ADC alert flags subregister
0x01	Reserved
0x02	T_{SENSE} alert flags subregister
0x03 to 0xFF	Reserved

[1] Bits in the alert flags subregisters can be reset by writing 1 to the selected bits.

ADC Alert Flags and T_{SENSE} Alert Flags Subregisters (Address 0x00 and Address 0x02)

The ADC alert flags subregister stores alerts for the analog voltage conversion channels, VIN0 to VIN7. The T_{SENSE} alert flags subregister stores alerts for the temperature sensor channel.

These subregisters contain two status bits per channel: one corresponding to the high limit, and the other corresponding to the low limit. A bit with a status of 1 shows the channel on which the violation occurred and whether the violation occurred on the high or low limit.

If additional alert events occur on any other channels after the first alert is triggered but before the alert flags subregister is read, the corresponding bits for the new alert events are also set. For example, if Bit D14 in the ADC alert flags subregister is set to 1, the low limit on Channel 7 has been exceeded, whereas if Bit D3 is set to 1, the high limit on Channel 1 has been exceeded.

To find out which channel or channels caused the alert flag, the user must read the ADC alert flags subregister or the T_{SENSE} alert flags subregister. If the ADC alert flags subregister or the T_{SENSE} alert flags subregister is accessed with both the read and write bits of the address pointer set to 1, the stored alert flags can be read and reset in one operation. A blanket reset can be performed by writing 0xFFFF to the ADC alert flags subregister, or 0x0003 to the T_{SENSE} alert flags subregister, thus clearing all alert flags.

Table 33. ADC Alert Flags Subregister, Bit Function Descriptions

Bits	Bit Name	R/W	Description
D15	VIN7 high limit flag	R/W	1 = VIN7 high limit exceeded
D14	VIN7 low limit flag	R/W	1 = VIN7 low limit exceeded
D13	VIN6 high limit flag	R/W	1 = VIN6 high limit exceeded
D12	VIN6 low limit flag	R/W	1 = VIN6 low limit exceeded
D11	VIN5 high limit flag	R/W	1 = VIN5 high limit exceeded
D10	VIN5 low limit flag	R/W	1 = VIN5 low limit exceeded
D9	VIN4 high limit flag	R/W	1 = VIN4 high limit exceeded
D8	VIN4 low limit flag	R/W	1 = VIN4 low limit exceeded
D7	VIN3 high limit flag	R/W	1 = VIN3 high limit exceeded
D6	VIN3 low limit flag	R/W	1 = VIN3 low limit exceeded
D5	VIN2 high limit flag	R/W	1 = VIN2 high limit exceeded
D4	VIN2 low limit flag	R/W	1 = VIN2 low limit exceeded
D3	VIN1 high limit flag	R/W	1 = VIN1 high limit exceeded
D2	VIN1 low limit flag	R/W	1 = VIN1 low limit exceeded
D1	VIN0 high limit flag	R/W	1 = VIN0 high limit exceeded
D0	VIN0 low limit flag	R/W	1 = VIN0 low limit exceeded

Table 34. T_{SENSE} Alert Flags Subregister, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D2]	Reserved	R/W	Reserved
D1	T_{SENSE} high limit flag	R/W	1 = T_{SENSE} high limit exceeded
D0	T_{SENSE} low limit flag	R/W	1 = T_{SENSE} low limit exceeded

MINIMUM AND MAXIMUM REGISTER BANK (ADDRESS 0x08)

The minimum and maximum register bank contains the minimum and maximum conversion values for each of the eight analog input channels and the temperature sensor channel. Values are 10-bit, left justified.

The minimum and maximum subregisters are cleared when a value is written to them—that is, they return to their power-up values. This means that if a subregister is accessed with both the read and write bits set, the stored minimum or maximum value can be read and reset in one operation. On power-up, the minimum value subregisters contain 0xFFC0, and the maximum value subregisters contain 0x0000.

Table 35. Minimum and Maximum Register Bank Subregisters

Subaddress (Hex)	Subregister Name[1]
0x00	VIN0 maximum value
0x01	VIN0 minimum value
0x02	VIN1 maximum value
0x03	VIN1 minimum value
0x04	VIN2 maximum value
0x05	VIN2 minimum value
0x06	VIN3 maximum value
0x07	VIN3 minimum value
0x08	VIN4 maximum value
0x09	VIN4 minimum value
0x0A	VIN5 maximum value
0x0B	VIN5 minimum value
0x0C	VIN6 maximum value
0x0D	VIN6 minimum value
0x0E	VIN7 maximum value
0x0F	VIN7 minimum value
0x10 to 0x1F	Reserved
0x20	T_{SENSE} maximum value
0x21	T_{SENSE} minimum value
0x22 to 0xFF	Reserved

[1] Bits in the minimum and maximum subregisters can be reset by writing 1 to the selected bits.

OFFSET REGISTER BANK (ADDRESS 0x09)

The offset register bank contains nine subregisters. Each of the eight analog input channels, as well as the temperature sensor channel, has a corresponding offset register (see Table 36).

Table 36. Offset Register Bank Subregisters

Subaddress (Hex)	Subregister Name[1]
0x00	VIN0 offset
0x01	VIN1 offset
0x02	VIN2 offset
0x03	VIN3 offset
0x04	VIN4 offset
0x05	VIN5 offset
0x06	VIN6 offset
0x07	VIN7 offset
0x10	Temperature sensor offset

[1] All subregisters in the offset register bank are read/write.

Each 8-bit, read/write offset subregister stores data in twos complement format. Values are added to the ADC conversion results. The offset encoding scheme used for the analog input channels and the temperature sensor are shown in Table 39 and Table 40, respectively. The default value for all subregisters in the offset register bank is 0x00.

When bits in these subregisters are set, the offset value is cumulative. Table 37 provides examples of analog input channel values, and Table 38 provides examples of temperature sensor channel values.

Table 37. Examples of Analog Input Channel Offset Values

Offset Subregister Value	Offset Value (LSB)
10000000	−32
11000000	−16
00001000	+2

Table 38. Examples of Temperature Sensor Channel Offset Values

Offset Subregister Value	Offset Value (°C)
10000000	−16
11000000	−8
00001000	+1

Table 39. VIN0 to VIN7 Offset Encoding Scheme

D7	D6	D5	D4	D3	D2	D1	D0
−32 LSB	+16 LSB	+8 LSB	+4 LSB	+2 LSB	+1 LSB	+0.5 LSB	+0.25 LSB

Table 40. Temperature Sensor Offset Encoding Scheme

D7	D6	D5	D4	D3	D2	D1	D0
−16°C	+8°C	+4°C	+2°C	+1°C	+0.5°C	+0.25°C	+0.125°C

DAC BUFFER ENABLE REGISTER (ADDRESS 0x0A)

The 16-bit, read/write DAC buffer enable register enables the DAC output buffers. Setting the appropriate bit to 1 enables the corresponding DAC output buffer (see Table 41). On power-up, the DAC buffer enable register contains all 0s by default.

GPIO REGISTER (ADDRESS 0x0B)

The 16-bit, read/write GPIO register is used to read or write data to the GPIO pins, provided that the GPIO functionality is enabled (see the Digital Output Driver Subregister (Address 0x01) section and the Digital I/O Function Subregister (Address 0x02) section). On power-up, the GPIO register contains all 0s by default.

Table 41. DAC Buffer Enable Register, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D4]	Reserved	R/W	Reserved
D3	Enable DAC 3	R/W	0 = disable DAC 3 output buffer (default) 1 = enable DAC 3 output buffer
D2	Enable DAC 2	R/W	0 = disable DAC 2 output buffer (default) 1 = enable DAC 2 output buffer
D1	Enable DAC 1	R/W	0 = disable DAC 1 output buffer (default) 1 = enable DAC 1 output buffer
D0	Enable DAC 0	R/W	0 = disable DAC 0 output buffer (default) 1 = enable DAC 0 output buffer

Table 42. GPIO Register, Bit Function Descriptions

Bits	Bit Name	R/W	Description
[D15:D12]	Reserved	R/W	Reserved
D11	GPIO11	R/W	0 = low output for write; low input for read 1 = high output for write; high input for read
D10	GPIO10	R/W	0 = low output for write; low input for read 1 = high output for write; high input for read
D9	GPIO9	R/W	0 = low output for write; low input for read 1 = high output for write; high input for read
D8	GPIO8	R/W	0 = low output for write; low input for read 1 = high output for write; high input for read
D7	GPIO7	R/W	0 = low output for write; low input for read 1 = high output for write; high input for read
D6	GPIO6	R/W	0 = low output for write; low input for read 1 = high output for write; high input for read
D5	GPIO5	R/W	0 = low output for write; low input for read 1 = high output for write; high input for read
D4	GPIO4	R/W	0 = low output for write; low input for read 1 = high output for write; high input for read
D3	GPIO3	R/W	0 = low output for write; low input for read 1 = high output for write; high input for read
D2	GPIO2	R/W	0 = low output for write; low input for read 1 = high output for write; high input for read
D1	GPIO1	R/W	0 = low output for write; low input for read 1 = high output for write; high input for read
D0	GPIO0	R/W	0 = low output for write; low input for read 1 = high output for write; high input for read

CONVERSION COMMAND REGISTER (ADDRESS 0x0E)

The conversion command signals the ADC to begin conversions. See the ADC Conversion Control section for more information.

ADC CONVERSION RESULT REGISTERS, VIN0 TO VIN7 (ADDRESS 0x10 TO ADDRESS 0x17)

The 16-bit, read-only ADC conversion result registers store the conversion results of the eight ADC input channels. Bits[D15:D6] store the 10-bit, straight binary result; Bits[D5:D0] contain the channel ID and alert information. Table 43 lists the contents of the two bytes that are read from the ADC conversion result registers. Channel ID numbers 0 to 7 correspond to the analog input channels, VIN0 to VIN7.

T_{SENSE} CONVERSION RESULT REGISTER (ADDRESS 0x20)

The 16-bit, read-only T_{SENSE} conversion result register stores the ADC data generated from the internal temperature sensor. The temperature data is stored in a 14-bit straight binary format. Bit D2 has a weight of 0.03125°C. An output of all 0s is equal to −256°C; this value is output by the AD7292 until the first measurement is completed. An output of 10 0000 0000 0000 corresponds to 0°C.

When digital filtering is disabled, Bit D3 and Bit D2 are set to 0, producing a 12-bit straight binary result with an LSB of 0.125°C. See the Temperature Sensor section for more information.

DAC CHANNEL REGISTERS (ADDRESS 0x30 TO ADDRESS 0x33)

Writing to the DAC channel registers sets the DAC output voltage codes. For more information, see the DAC Output Control section.

Table 43. ADC Conversion Result Register Format

MSB												LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**[D5:D2]**	**D1**	**D0**
B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	4-bit channel ID (0000 to 0111)	T_{SENSE} alert flag	ADC alert flag

Table 44. T_{SENSE} Conversion Result Register Format

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3[1]**	**D2[1]**	**D1**	**D0**
B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	T_{SENSE} alert flag	ADC alert flag

[1] When digital filter is enabled (see the Temperature Sensor Subregister (Address 0x20) section).

Table 45. DAC Channel Register Format

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0	0	Copy	$\overline{\text{LDAC}}$

ADC CONVERSION CONTROL

ADC CONVERSION COMMAND

To initiate an ADC conversion on a channel, the conversion command must be written to the AD7292. The special address pointer byte, 0x8E, consists of the conversion command register (Address 0x0E) with the MSB read bit set to 1 to signify an ADC conversion. When the conversion command is received, the AD7292 uses the current value of the address pointer to determine which channel to convert on.

In Figure 40, the first byte sets the address pointer with both the read and write bits cleared and sets Bits[D5:D0] to point to the selected channel conversion result register. The second byte contains the conversion command with the read bit set. After receiving the conversion command, the AD7292 stays in conversion mode, performing a new ADC conversion at the end of each read, until the $\overline{CS}$ (chip select) input signal is taken high.

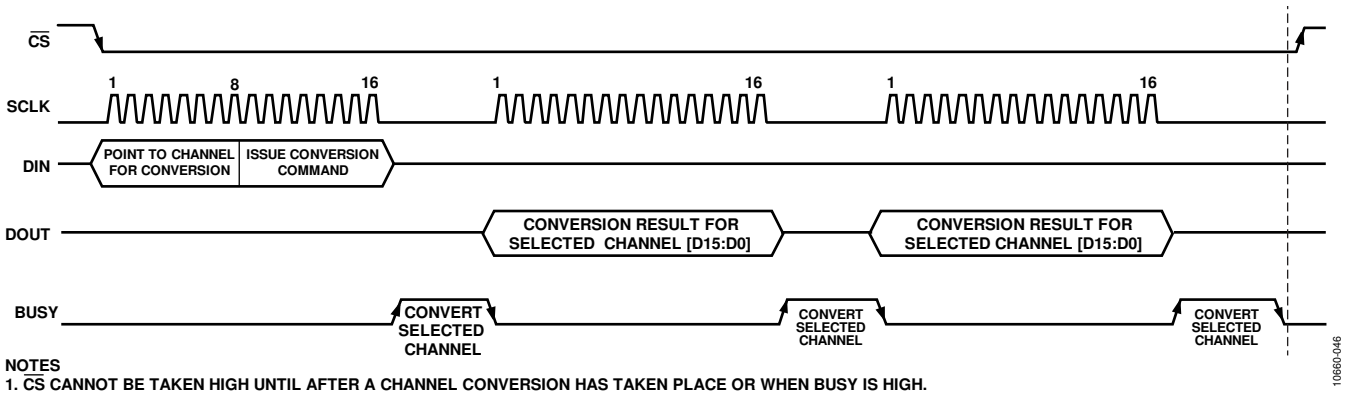
In Figure 41, the address pointer is set to point to the ADC data register (Address 0x01) with both the read and write bits cleared. The conversion command is issued, and the contents of the ADC sequence register specify the sequence of ADC channels for conversion (see the ADC Sequencer section).

In this example, the ADC sequence register is programmed to convert on analog input channels VIN0 and VIN1. The AD7292 stays in conversion mode and performs a new ADC conversion at the end of each read until the $\overline{CS}$ input signal is taken high.

In the examples shown in Figure 40 and Figure 41, an SCLK delay is inserted following the conversion command to allow the ADC to perform the conversion before the data is read. If temperature sensor conversions are requested, a longer delay is necessary (see the Temperature Sensor section).

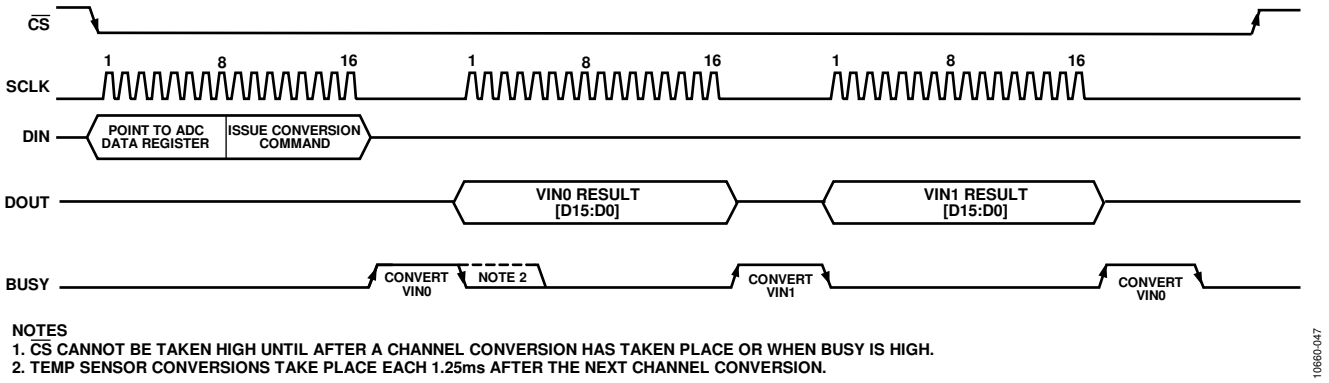
In some applications, the SPI bus master may not allow the serial clock to be held low during a read sequence, and it may be necessary to take $\overline{CS}$ high, as shown in Figure 42. In this case, the $\overline{CS}$ line must remain low while the ADC conversion is in progress to prevent possible corruption of the ADC result.

In the example shown in Figure 42, the address pointer is set to point to the ADC data register (Address 0x01) with both the read and write bits cleared. The conversion command is issued with the read bit set. The $\overline{CS}$ line is taken high after the conversion on VIN0 is completed. The $\overline{CS}$ line is then brought low, and the ADC data register is pointed to with the read bit set. The conversion result is clocked out. The conversion command is reissued before the $\overline{CS}$ line is taken high again, and so on.



NOTES
1. $\overline{CS}$ CANNOT BE TAKEN HIGH UNTIL AFTER A CHANNEL CONVERSION HAS TAKEN PLACE OR WHEN BUSY IS HIGH.

Figure 40. ADC Conversion Command (ADC Sequencer Not Used)



NOTES
1. $\overline{CS}$ CANNOT BE TAKEN HIGH UNTIL AFTER A CHANNEL CONVERSION HAS TAKEN PLACE OR WHEN BUSY IS HIGH.
2. TEMP SENSOR CONVERSIONS TAKE PLACE EACH 1.25ms AFTER THE NEXT CHANNEL CONVERSION.

Figure 41. ADC Conversion Command (ADC Sequencer Used)

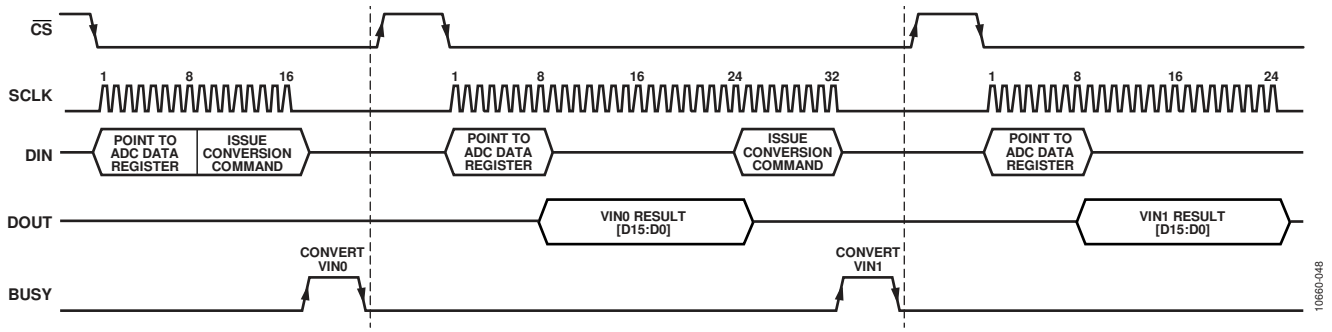


Figure 42. ADC Conversion Command ($\overline{CS}$ Line Taken High After Conversions)

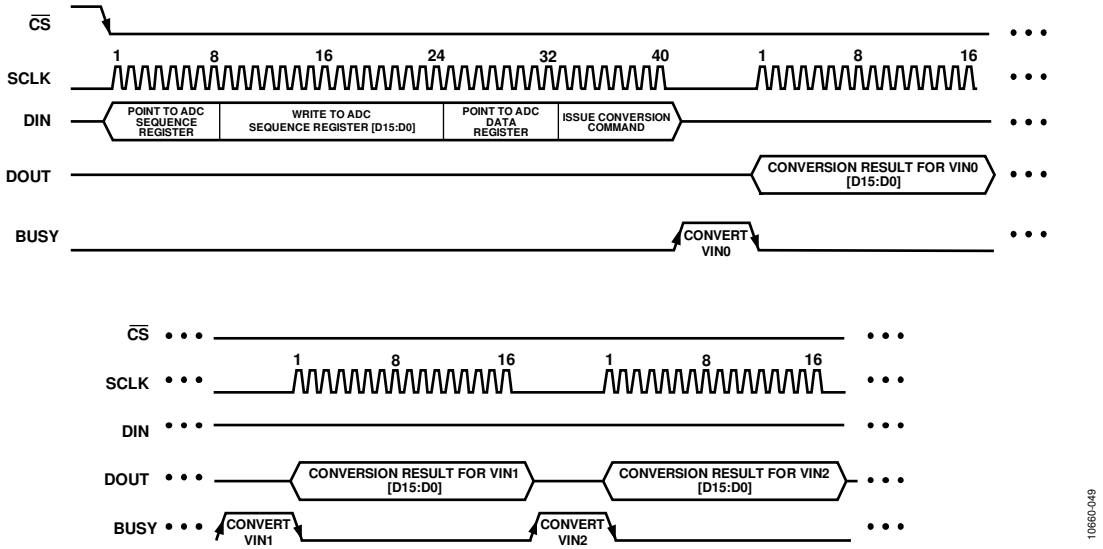


Figure 43. Example of Using the ADC Sequencer

ADC SEQUENCER

The AD7292 provides an ADC sequencer, which enables the selection of a preprogrammable sequence of channels for conversion. Figure 43 shows the operation of the ADC sequencer.

To initiate a write to the ADC sequence register (Address 0x03), point to it in the address pointer register with the write bit set and the read bit cleared. The next two bytes specify the sequence of channels that the ADC converts on (see Table 16). The ADC data register (Address 0x01) is then pointed to and the conversion command is issued. Note that the read bit is set when issuing the conversion command.

When the ADC sequencer is used, ADC conversions are triggered based on the contents of the ADC sequence register; the address pointer reverts to its previous value—in this example, the ADC data register—allowing the conversion results to be read back.

After the first ADC conversion is complete, the first result is read back, which requires 16 serial clocks. The first 10 bits contain the ADC result, the next four bits are the channel identifier, and the last two bits are alert bits (see Table 43). On the last falling edge of the clock, the next ADC conversion begins.

The AD7292 continues converting on the channels specified by the ADC sequence register. On completing the first sequence of conversions, the sequencer loops back and begins the sequence again until $\overline{CS}$ is taken high. The AD7292 is ready to accept a new address pointer after $\overline{CS}$ is taken low. It is recommended that the serial clock be kept low during the ADC conversions to ensure that there is no disturbance of the results.

DAC OUTPUT CONTROL

To set the DAC output voltage codes, the user must write to the DAC channel registers (Address 0x30 to Address 0x33). Figure 44 shows an example of how to set the DAC output voltage codes.

1. The DAC buffer enable register (Address 0x0A) is pointed to with the write bit set.
2. The following two bytes specify which of the four DAC output buffers are enabled.
3. The DAC channel register (DAC Channel 0 register in Figure 44) is pointed to with the write bit set.
4. The following two bytes contain the value to be written to the DAC channel.

On completion of this write, the DAC channel output is immediately updated to the new value, provided that the $\overline{\text{LDAC}}$ bit in the DAC channel register is not set.

Note that the process can be reversed—that is, the user can first write a value to the DAC channel register and then enable the DAC output buffer.

LDAC OPERATION

A write to a DAC channel register (Address 0x30 to Address 0x33) is addressed to the DAC input register; a read from a DAC channel register is addressed to the DAC output register (see Figure 45). The DAC output registers are updated based on the $\overline{\text{LDAC}}$ bit in the DAC channel register or on the polarity of the GPIO3/LDAC pin (if the pin is configured as an LDAC pin).

When the $\overline{\text{LDAC}}$ bit in the DAC channel register is set to 1, the 10-bit DAC value is stored, but the DAC channel output is not updated. When a write to any DAC channel register occurs with the $\overline{\text{LDAC}}$ bit cleared, all DAC channel outputs are updated with the stored values from previous writes.

When the $\overline{\text{LDAC}}$ bit in the DAC channel register is used to control the updating of the DAC output, the LDAC pin function should be disabled, that is, the GPIO3/LDAC pin should be configured as GPIO3.

The GPIO3/LDAC pin can be used to update the DAC outputs with the stored values when the pin is configured as an LDAC pin (see the Digital Output Driver Subregister (Address 0x01) section and the Digital I/O Function Subregister (Address 0x02) section). If the GPIO3/LDAC pin is configured as an LDAC input and is taken high, the DAC output registers are updated; conversely, if this input pin is held low, the DAC value is stored but the channel output is not updated.

SIMULTANEOUS UPDATE OF ALL DAC OUTPUTS

It may be useful to update all four DAC channel registers simultaneously with the same value but not update the DAC outputs ($\overline{\text{LDAC}}$ bit is set to 1; LDAC pin is set to 0). Setting the copy bit (Bit 1) when writing to any DAC channel register instructs the AD7292 to copy the new DAC value to all the DAC input registers.

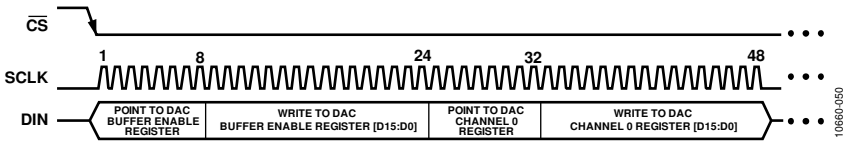
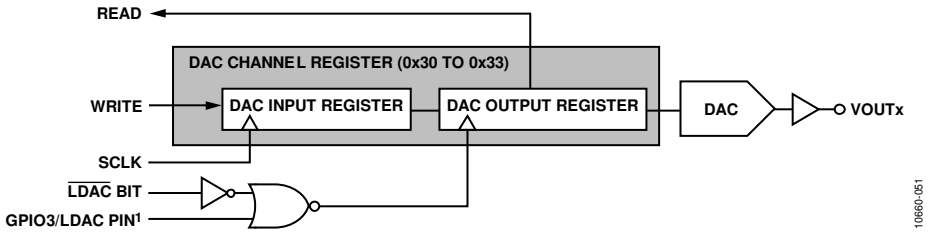


Figure 44. Setting the DAC Output Voltage Code



1PROVIDED THE GPIO3/LDAC PIN IS CONFIGURED AS AN LDAC PIN.

Figure 45. DAC Input and Output Registers

ALERTS AND LIMITS

ALERT LIMIT MONITORING FEATURES

The alert limits register bank comprises subregisters that set the high and low alert limits for the eight analog input channels and the temperature sensor channel (see Table 31). Each subregister is 16 bits in length; values are 10-bit, left-justified (padded with 0s as the 6 LSBs). On power-up, the low limit and hysteresis subregisters contain all 0s, whereas the high limit subregisters are set to 0xFFC0.

The alert high limit subregisters store the upper limit that activates an alert. If the conversion result is greater than the value in the alert high limit subregister, an alert is triggered. The alert low limit subregister stores the lower limit that activates an alert. If the conversion result is less than the value in the alert low limit subregister, an alert is triggered.

If a conversion result exceeds the high or low limit set in the alert limits subregister, the AD7292 signals an alert in one or more of the following ways:

- Via hardware using the GPIO0/ALERT0 and GPIO1/ALERT1 pins
- Via software using the alert flag bits in the conversion result registers
- Via software using the alert bits in the alert flags register bank

Hysteresis

The hysteresis value determines the reset point for the alert pins and alert flags if a violation of the limits occurs. Each channel has an associated hysteresis subregister that stores the hysteresis value, N (see Table 31). If the hysteresis function is enabled, the conversion result must return to a value of at least N LSB below the alert high limit subregister value, or N LSB above the alert low limit subregister value to reset the alert output pins and the alert flag bits (see Figure 46).

The advantage of using the hysteresis subregister associated with each limit subregister is that hysteresis prevents chatter on the alert bits associated with each ADC channel and also prevents flicker on the alert output pins. Figure 46 shows the limit checking operation.

HARDWARE ALERT PINS

Pin 27 and Pin 26 (GPIO0/ALERT0 and GPIO1/ALERT1, respectively) can be configured as alert pins (see the Digital I/O Function Subregister (Address 0x02) section). When these pins are configured as alert pins, they become active when the selected conversion result exceeds the high or low limit stored in the alert limits register bank. The polarity of the alert output pins can be set to active high or active low via the general subregister within the configuration register bank (see the General Subregister (Address 0x08) section).

If an alert pin signals an alert event and the contents of the alert flags subregisters are not read before the next conversion is completed, the contents of the subregister may change if the out-of-range signal returns to the specified range. In this case, the ALERTx pin no longer signals the occurrence of an alert event.

ALERT FLAG BITS IN THE CONVERSION RESULT REGISTERS

The T_{SENSE} alert and ADC alert flag bits in the ADC conversion result and T_{SENSE} conversion result registers indicate whether the conversion result being read or any other channel result has violated the limit registers associated with it. If an alert occurs and the alert bit is set in a conversion result register, the master can read the alert flags register bank to obtain more information about where the alert occurred.

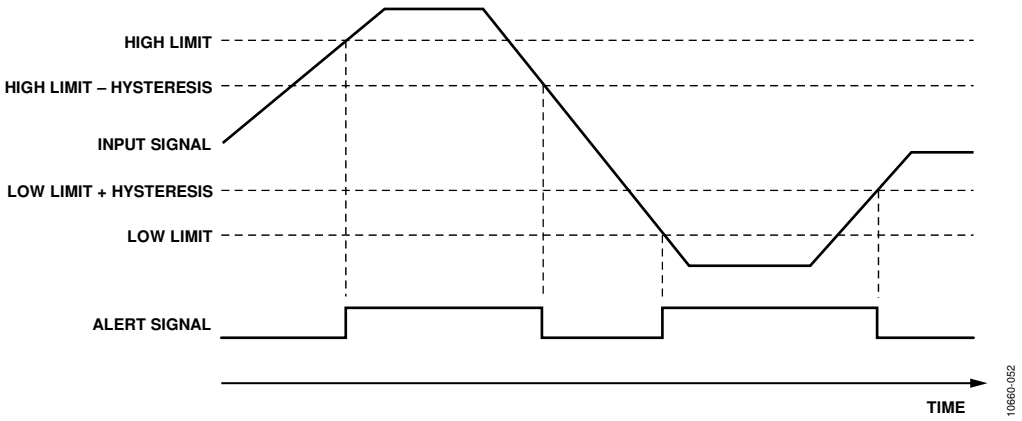


Figure 46. Limit Checking: Alert High Limit, Alert Low Limit, and Hysteresis

ALERT FLAGS REGISTER BANK

The alert flags register bank contains two subregisters: the ADC alert flags subregister and the T_{SENSE} alert flags subregister. The ADC alert flags subregister stores alerts for the analog voltage conversion channels, VIN0 to VIN7. The T_{SENSE} alert flags subregister stores alerts for the temperature sensor channel. These subregisters contain two status bits per channel: one corresponding to the high limit, and the other corresponding to the low limit (see Table 33 and Table 34). A bit with a status of 1 shows the channel on which the violation occurred and whether the violation occurred on the high or low limit.

If additional alert events occur on any other channels after the first alert is triggered but before the alert flags subregister is read, the corresponding bits for the new alert events are also set. For example, if Bit D14 in the ADC alert flags subregister is set to 1, the low limit on Channel 7 has been exceeded, whereas if Bit D3 is set to 1, the high limit on Channel 1 has been exceeded.

An alert associated with either the alert high limit or alert low limit subregister is cleared automatically after the monitored signal is back in range, that is, when the conversion result returns between the configured high and low limits. The contents of the alert flags subregister are updated after each conversion.

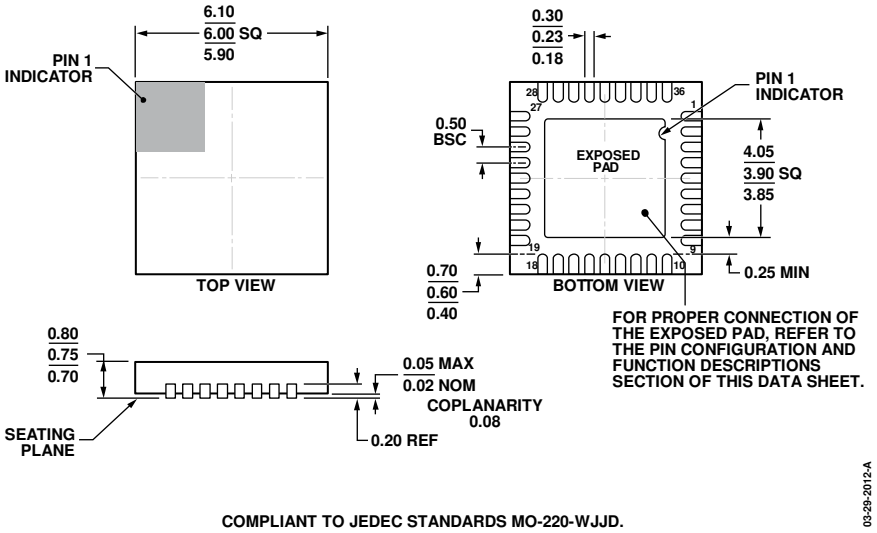
To find out which channel or channels caused the alert flag, the user must read the ADC alert flags subregister or the T_{SENSE} alert flags subregister. If the ADC alert flags subregister or the T_{SENSE} alert flags subregister is accessed with both the read and write bits of the address pointer set to 1, the stored alert flags can be read and reset in one operation. A blanket reset can be performed by writing 0xFFFF to the ADC alert flags subregister, or 0x0003 to the T_{SENSE} alert flags subregister, thus clearing all alert flags.

MINIMUM AND MAXIMUM CONVERSION RESULTS

The read-only minimum/maximum register bank contains the minimum and maximum conversion values for each of the eight analog input channels and the temperature sensor channel. Values are 10-bit, left justified.

The minimum and maximum subregisters are cleared when a value is written to them—that is, they return to their power-up values. This means that if a subregister is accessed with both the read and write bits set, the stored minimum or maximum value can be read and reset in one operation. On power-up, the minimum value subregisters contain 0xFFC0, and the maximum value subregisters contain 0x0000.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD.

Figure 47. 36-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-36-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7292BCPZ	−40°C to +125°C	36-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-36-3
AD7292BCPZ-RL	−40°C to +125°C	36-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-36-3
EVAL-AD7292SDZ		Evaluation Board	
EVAL-SDP-CB1Z		System Development Platform	

[1] Z = RoHS Compliant Part.