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February 2016

# FFG3105
# Battery ID and Smart Charge Monitor

## Features

- Two, One-Time-Programmable, 64-Bit Registers for Unique Identifier Codes.
- Precision Voltage and Temperature Measurement enables Smart Charging Topologies
- Low Power: < 2 µA Shutdown Current
  2 µA Standby Current
  < 4.5 µA Average Active Current
- Fully Integrated $I^2C$ Slave with support for Normal and Fast Modes with auto increment.
- Internal BID redundancy for increased robustness
- 6-Ball, 2 x 3, 0.5 mm Pitch - Chip Scale Packaging (WLCSP)

## Applications

- Battery Packs
- Mobile Devices

## Description

The FFG3105 battery ID and smart charge monitor chip is designed for battery packs used in cell phones and other mobile devices. The FFG3105 has two programmable 64-bit registers, which can be used to store a pack's identification code. The FFG3105 monitors the cell voltage and temperature providing precise knowledge of these values. This information can be used in charging applications to ensure optimal performance and safety.

The FFG3105 includes an integrated temperature sensor and battery voltage monitor. The FFG3105 also includes twelve 16-bit registers which can be used to store battery parameters and recent history. A system side fuel gauge like Fairchild's FFG1040 can use these registers to facilitate fast initialization following battery removal and reinsertion or for battery swaps. All registers including temperature and voltage readings can be accessed by the host via $I^2C$ in either Standard-mode or Fast-mode.

Each Battery ID register has an internal redundant copy to improve robustness and protect against potential miss programming.

The FFG3105 utilizes a 2 x 3 ball, 0.5 mm pitch, WLCSP with nominal dimensions of 0.96 x 1.66 $mm^2$.

## Ordering Information

| Part Number | Operating Temperature Range | Package | Packing Method |
|---|---|---|---|
| FFG3105UCX | -40 to 85°C | 0.96 x 1.66 $mm^2$, 6-Ball CSP, 0.5 mm Ball Pitch | Tape and Reel |

## Block Diagram

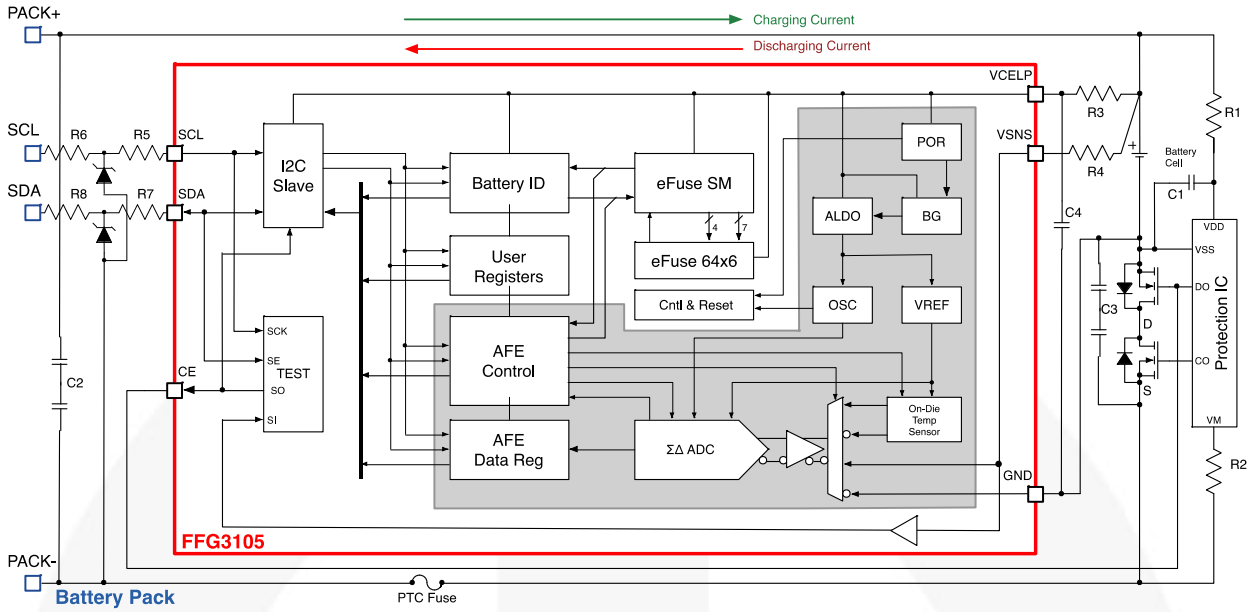



**Figure 1. FFG3105 Block Diagram and Battery Pack**

### Table 1. Recommended External Components

| Component | Description | Typical | Unit |
|---|---|---|---|
| R1 | Protection IC ESD Protection and power fluctuation Resistor (1) | 220 | Ω |
| R2 | Protection IC Protection for reverse connection of charger (1) | 1000 | Ω |
| R3 | VCELP ESD Series Protection Resistor | 300 | Ω |
| R4 | VSNS ESD Series Protection Resistor | 1000 | Ω |
| R5, R6, R7, R8 | SCL and SDA ESD Protection Resistor | 100 | Ω |
| C1 | Decoupling Capacitor for power fluctuation (1) | 0.1 | µF |
| C2(2) | ESD Protection Capacitor | 0.1 | µF |
| C3 | ESD Protection Capacitor(1) | 0.1 | µF |
| C4 | Decoupling Capacitor for power fluctuation | 0.1 | µF |

**Notes:**

1. Please follow the recommendation of the Protection IC vendor for these component values.
2. C2 should consist of two capacitors in series as shown in Figure 1 in the event one of the capacitors were to short circuit.

## Pin Configuration

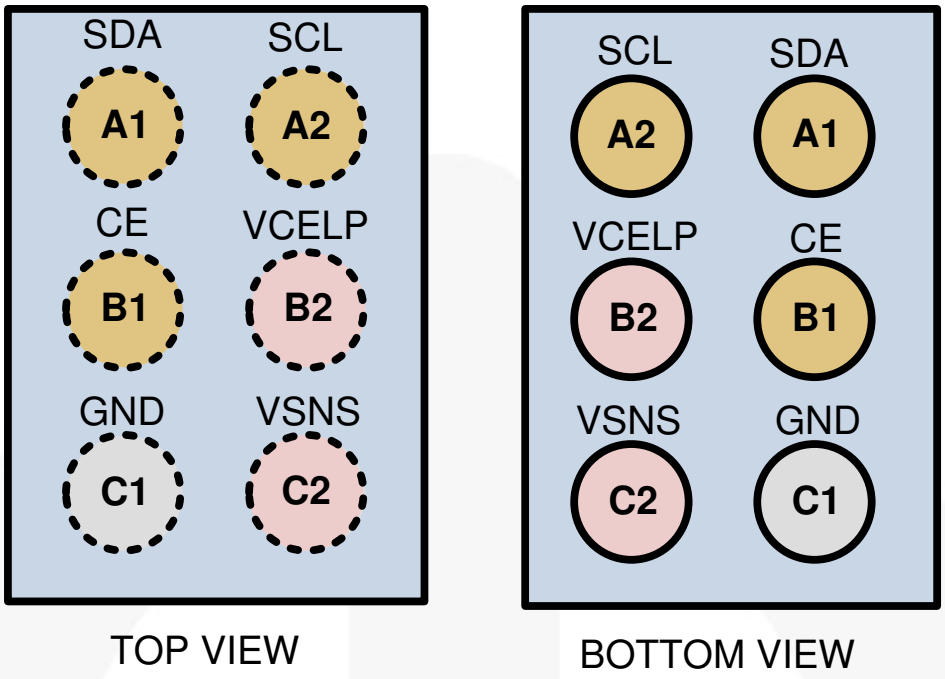



**Figure 2. Ball Assignments**

## Pin Definitions

| Name | Position | Type | Description |
|---|---|---|---|
| CE | B1 | Digital I/O | **Chip Enable**, Connected to Battery Protection IC and used to enable and disable the device. This pin should not be left floating. |
| GND | C1 | Ground | **Device Ground**. Connected to Battery Cell Anode |
| SCL | A2 | Digital I/O | **I$^2$C Serial Clock,** I$^2$C communication clock input. This pin should not be left floating, use with 2-10 k pull up resistor. |
| SDA | A1 | Digital I/O | **I$^2$C Serial Data,** Bi-directional I$^2$C serial data line. This pin should not be left floating, use with 2-10 k pull up resistor. |
| VCELP | B2 | Power | **Power Input**. Decoupled with 0.1 µF to GND and connected to Battery Cell Cathode through a series protection resistor. |
| VSNS | C2 | Sense Input | **Voltage Sense**. Battery Voltage Measurement Sense ADC Input. Connected to Battery Cell Cathode through series protection resistor. |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CELP}$ | Positive Battery Supply Voltages | | $V_{GND}$ - 0.5 | $V_{GND}$ + 6.0 | V |
| $V_{GND}$ | Negative Analog Supply Voltage | | $V_{CELP}$ - 6.0 | $V_{CELP}$ + 0.5 | V |
| $V_{I/O}$ | All Digital Input / Output Signals | | $V_{GND}$ - 0.5 | $V_{GND}$ + 6.0 | V |
| $T_A$ | Operating Free-air Temperature | | -40 | +85 | °C |
| $T_{J\|MAX}$ | Maximum Junction Temperature | | | +150 | °C |
| $T_{STG}$ | Storage Temperature Range | | -65 | +150 | °C |
| $T_L$ | Lead Soldering Temperature, 10 Seconds | | | +260 | °C |
| ESD | Human Body Model, ANSI/ESDA/JEDEC JS-001-2012 | | 2 | | kV |
| | Charged Device Model, JESD22-C101 | | 500 | | V |
| | IEC 6100-4-2 System ESD, Pins VIN[3] | Air Gap | 15 | | kV |
| | | Contact | 8 | | kV |

**Note:**

3. Pins should be protected by external TVS devices when tested for IEC compliance.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings. The recommended operating conditions assume the following: $V_{CELP}$ = 2.5 V to 4.5 V, $T_A$ = -40°C to +85°C, unless otherwise noted.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CELP}$ | Battery Supply Voltage | 2.5 | 4.5 | V |
| | Device Programming Voltage | 5.5 | 6.0 | V |
| $V_{BAT\_SLEW}$ | Battery Supply Voltage Slew Rate | 20 | | V/ms |
| $R_{I2CPU}$ | $I^2C$ Pull up Resistor to $V_{PU}$ (SDA, SCL) | 4.7 | 10 | kΩ |
| $C_b$ | $I^2C$ Bus Capacitance for each pin | | 400 | pF |
| $T_A$ | Operating Free-air Temperature | -40 | +85 | °C |
| $T_J$ | Operating Junction Temperature | -40 | +85 | °C |

## Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature $T_A$.

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-Ambient Thermal Resistance (1in.$^2$ pad of 2 oz. copper) | 70 | °C/W |
| $\theta_{JB}$ | Junction-to-PCB Thermal Resistance | 20 | °C/W |

## DC Electrical Characteristics

The Recommended Operating Conditions for DC Electrical Characteristics assume $V_{CELP}$ = 2.5 V to 4.5 V and $T_A$ = -20°C to 70°C, unless otherwise noted. Typical values are at $T_A$ = 25°C, $V_{CELP}$ = 3.8 V. $V_{PU}$ = $V_{CELP}$. Min. / Max. values are guaranteed by design and/or characterization for process variations and the temperature range of $T_A$= -20°C to 70°C.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{IN}$ | Input Leakage Current on Digital I/O Pins | $0 \le V_{IN} \le V_{CELP}$; $V_{CELP}$ = 2.5 to 4.5 V | | | 0.5 | µA |
| $I_{OFF}$ | Power-Off Leakage Current (Shutdown) | $V_{IN}$ or $V_{OUT}$= 4.5 V; $V_{CELP}$ = 0 | | 0.2 | < 2.0 | µA |
| $I_{CC}$ | Standby Mode Current(4,10) | $V_{IN}$ = 3.6 V; $V_{CELP}$ = 2.5 to 4.5 V | | 2.0 | 4.0 | µA |
| | Active Mode Average Current(4,5,10) | | | 4.3 | 7.0 | |
| **Fast Mode(400 KHz) $I^2C$ Controller SDA, SCL, ($T_A$ = -40°C to 85°C)** | | | | | | |
| $V_{IL}$ | Low-Level Input Voltage(8, 9) | | -0.50 | | 0.65 | V |
| $V_{IH}$ | High-Level Input Voltage(8, 9) | | 1.05 | | 4.50 | V |
| $V_{OL}$ | Low-Level Output Voltage at 3 mA Sink Current (Open Drain)(6,9) | $V_{CELP}$ >2 V | 0 | | 0.4 | V |
| | | $V_{CELP}$ <2 V | | | 0.2 x $V_{CELP}$ | |
| $V_{PU}$ | External Pull Up Voltage Range | | 1.62 | | 4.50 | V |
| $I_I$ | Input Current of Each I/O Pin, Input Voltage 0.26 V to 2.34 V | | -10 | | 10 | µA |
| $C_I$ | Capacitance for Each I/O Pin(10) | | | | 10 | pF |
| **CE ($T_A$ = -40°C to 85°C)** | | | | | | |
| $V_{IL}$ | Low-Level Input Voltage | | -0.5 | | 0.3 x $V_{CELP}$ | V |
| $V_{IH}$ | High-Level Input Voltage | | 0.7 x $V_{CELP}$ | | $V_{CELP}$+0.5 | V |
| $I_I$ | Input Current, Input Voltage 0.26 V to 2.34 V | | -10 | | 10 | µA |
| $C_I$ | Capacitance(10) | | | | 10 | pF |

*Continued on the following page...*

## DC Electrical Characteristics (Continued)

The Recommended Operating Conditions for DC Electrical Characteristics assume $V_{CELP}$ = 2.5 V to 4.5 V and $T_A$ = -20°C to 70°C, unless otherwise noted. Typical values are at $T_A$ = 25°C, $V_{CELP}$ = 3.8 V. $V_{PU}$ = $V_{CELP}$. Min. / Max. values are guaranteed by design and/or characterization for process variations and the temperature range of $T_A$= -20°C to 70°C.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Data Acquisition Performance Parameters** | | | | | | |
| $T_{MIN}$, $T_{MAX}$ | Temperature Range | | -40 | | 85 | °C |
| $G_{TEMP}$ | Temperature Sensor Voltage Gain(10) | | | 2.0 | | mV/°C |
| $T_{DIE}$ | Temperature Measurement Error (10,11) | $V_{CELP}$ = 2.5 to 4.5 V, $T_A$ = + 25°C | -2 | | +2 | °C |
| | | $T_A$ = +0°C | -3 | | +3 | °C |
| | | $T_A$ = +50°C | -3 | | +3 | °C |
| | | $T_A$ = -40°C | -4 | | +4 | °C |
| | | $T_A$ = +80°C | -4 | | +4 | °C |
| LSB | Voltage Sense Least Significant Bit | | | | 122 | µV |
| EVR | Voltage Measurement Resolution | $V_{CELP}$ = 2.5 to 4.5 | | | 1 | mV |
| $V_{GERR}$ | Voltage Gain Error (% of \|VBAT- 3.5 V\|) | $V_{CELP}$ = 2.5 to 4.5 | -0.85 | | +0.85 | % |
| $V_{OS}$ | Voltage Offset Error | $V_{CELP}$ = 2.5 to 4.5 V $T_J$ = -20 °C to +70°C | -20 | | +20 | mV |

**Notes:**

4. Assumes $I^2C$ access at 400 kHz rate.
5. Average active current is based on request for voltage and temperature measurement once per every 2 seconds.
6. The SDA and SCL pins are open drain with external pull-up resistor tied to VPU. Recommended pull-up resistor range is 4.7 kΩ to 10 kΩ.
7. $V_{IH}$(max.) = VPU + 0.5 or 5.5 V which-ever is lower.
8. $V_{IH}$ and $V_{IL}$ have been chosen to be fully compliant to I2C specification at VPU = 1.8V ± 10%. At 2.25 V ≤ VPU ≤ 3.63 V the $V_{IL}$(max.) provides 200 mV of noise margin to the required $V_{OL}$(max.) of the transmitter.
9. Parts may be ordered for enhanced I2C operation in systems where the device I2C pull-up resistors are biased from a voltage greater than 3.6 V. Please contact Fairchild for parts programmed with this feature.
10. Guaranteed by design; not tested in production.
11. Accuracy (expressed in °C) = the difference between the FFG3105 output temperature and the measured temperature.

## AC Electrical Characteristics ($I^2C$ Controller SDA, SCL)

The AC electrical characteristics assume $V_{CELP}$ = 2.5 V to 4.5 V.

| Symbol | Parameter | Fast Mode | | |
|---|---|---|---|---|
| | | Min. | Max. | Unit |
| $f_{SCL}$ | SCL Clock Frequency | 0 | 400 | kHz |
| $t_{HD;STA}$ | Hold Time (Repeated) Start Condition | 0.6 | | µs |
| $t_{LOW}$ | Low Period of SCL Clock | 1.3(12) | | µs |
| $t_{HIGH}$ | High Period of SCL Clock | 0.6 | | µs |
| $t_{SU;STA}$ | Set-up Time for Repeated Start Condition | 0.6 | | µs |
| $t_{HD;DAT}$ | Data Hold Time (*see Figure 3)* | 0 | 0.9 | µs |
| $t_{SU;DAT}$ | Data Set-up Time (*see Figure 3)* | 100(13) | | ns |
| $t_{PS}$ | Set-up Time Required by SDA Input Buffer (Receiving Data) | 0 | | ns |
| $t_{PH}$ | Out Delay Required by SDA Output Buffer (Transmitting Data) | 300 | | ns |
| $t_r$ | Rise Time of SDA and SCL Signals | $20+0.1C_b$(14,15) | 300 | ns |
| $t_f$ | Fall Time of SDA and SCL Signals | $20+0.1C_b$(14,15) | 300 | ns |
| $t_{SU;STO}$ | Set-up Time for Stop Condition | 0.6 | | µs |
| $t_{BUF}$ | Bus Free Time between a Stop and Start Conditions | 1.3 | | µs |
| $t_{SP}$ | Pulse Width of Spikes that Must Be Suppressed by the Input Filter | 0 | 50 | ns |

**Notes:**

12. The FFG3105 can accept clock signals with $t_{LOW}$ as low as 1.1 µs, provided that the received SDA signal $t_{HD;DAT}+ t_{r/f} \leq 1.1$ µs. The FFG3105 features a 0 ns SDA input set-up time; therefore, this parameter is not included in the above equation.
13. A Fast-Mode $I^2C$ Bus® device can be used in a Standard-Mode $I^2C$ bus system, but the requirement that $t_{SU;DAT} \geq 250$ ns must be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\_max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode $I^2C$ Bus specification) before the SCL line is released.
14. $C_b$ equals the total capacitance of one bus line in pF.
15. The FFG3105 ensures that the SDA signal OUT must coincide with SCL LOW for worst-case SCL $t_{f\ max}$ time of 300 ns. This requirement prevents data loss by preventing SDA-OUT transitions during the undefined region of the falling edge of SCL. Consequently, the FFG3105 fulfills the following requirement from the $I^2C$ specification (page 77, Note 2): “A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IHmin}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.”
16. FFG3105 $I^2C$ slave is fully compliant the NXP (Phillips) $I^2C$ specification, Rev. 0.3 UM10204 (2007) for both Standard Mode and Fast Mode.
17. The FFG3105 is tested and qualified for a max speed of 400 Kbps/s, Fast Mode.

## Timing Diagrams

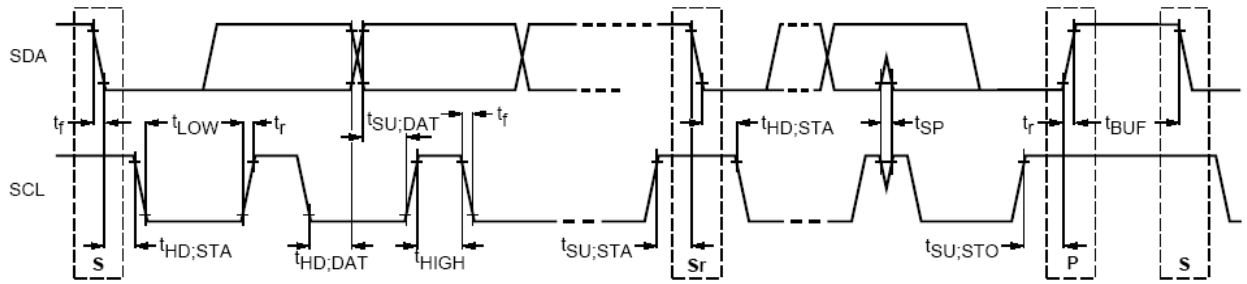



**Figure 3. Definition of Timing for Full-Speed Mode Devices on the $I^2C$ Bus**

## System Applications Diagram

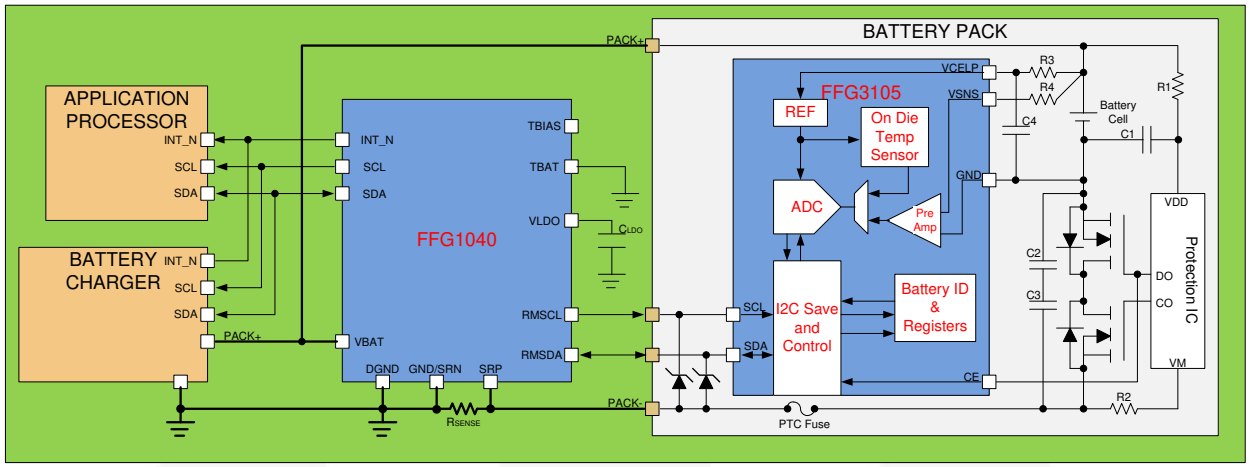



**Figure 4. Systems Applications Diagram**

## Functional Description

### Overview

The FFG3105 includes a 64-bit one-time factory programmable fuse locked register to enable unique battery identification.

The FFG3105 uses an Analog-to-Digital Converter (ADC) to monitor the battery cell voltage and temperature.

### Battery Pack Identification

The FFG3105 has two 64-bits, one-time programmable registers for Battery ID (BID). These registers can be programmed with customized values by battery lot or phone model. With the ability to uniquely identify specific batteries, systems can selectively enable special features after verifying that the system battery is valid.

Each register has an internal redundant copy used to improve robustness and detect potential mismatches.

### Voltage Monitoring

The integrated ADC allows battery terminal voltage monitoring with a high degree of accuracy. The FFG3105 has been designed for integration into the battery pack, which allows it to directly measure the cell voltage. This allows the host system to know what the voltage is at the battery cell. It eliminates the uncertainty introduced by system side gauge measurements, which include series resistance of the protection circuitry, pack terminals and series trace resistance. To achieve optimal charging performance it is important for the host to accurately know the internal cell voltage.

### Temperature Sensing and Reporting

The FFG3105 measures the battery temperature using its on board temperature sensor. This temperature information can be used to improve battery-charging performance. Accurate understanding of the battery temperature is critical to maintain optimal charging rates and to ensure safe operation during high current charging. The FFG3105 temperature sensor is accurate to within ±3°C over the operating ranges that support battery charging.

### User Definable Registers

The FFG3105 includes twelve 16-bit registers, which can be written to and read by the host. These registers are provided to allow important history or other user information to be stored in the battery pack. If used in conjunction with the FFG1040, Fuel Gauge, the FFG3105 registers can be used to support the FFG1040's save and restore feature, by storing critical battery parameters and fuel gauging information. This information is used when a battery is removed and re-inserted or when a user swaps between several batteries.

With the ability to identify the battery and store fuel gauging history, the system side fuel gauge can initialize with zero learning time to achieve optimal accuracy. The FFG3105 is powered directly from the battery pack's internal terminal voltage. Therefore, the values in the FFG3105 registers are retained even when the battery voltage drops below the systems shut down voltage. If the battery voltage drops below the battery protection threshold and the battery is locked out, the FFG3105 loses power and the values in these registers are lost.

## Programming the 64-Bit ID Code

The FFG3105 includes two 64-bit, one-time, eFuse programmable registers to allow for a unique ID code to be permanently stored in this register.

Programming the FFG3105 requires knowledge of the Lock and Unlock keywords. The appropriate lock and unlock 32-bit keyword must be written to the KEYWORD_MSW, KEYWORD_LSW registers before a Lock or Unlock command is issued and programming is attempted.

When programmed, a redundant copy is created. The redundant copy is used when the BID is read back to improve robustness and detect errors.

These register can be programmed and verified by Fairchild before shipping or with the proper procedure be programmed by the customer before the battery cell is attached. Please contact your Fairchild sales representative to set the custom code for your application or to receive detailed information on programming the FFG3105.

## Power Modes

The FFG3105 chip has three power modes, ACTIVE, STANDBY and SHUTDOWN. The FFG3105 moves in and out of these modes automatically based on requests from the Host for voltage and temperature readings and the external chip enable, **CE**.

### Standby Power Mode

During periods of inactivity when the host is not requesting voltage or temperature readings the FFG3015 enters STANDBY mode to save power. In STANDBY, the FFG3105, the $I^2C$ bus, and registers are still available and accessible. The Host may read or write the User Definable registers while in STANDBY.

### Active Power Mode

The FFG3105 enters this mode when the host requests a measurement of the battery voltage or temperature. It takes < 28 ms for the FFG3105 to measure both voltage and temperature and write them into the output registers. The measure automatically moves the device to ACTIVE. After the measurements are made the device returns to STANDBY on its own.

### Shutdown Mode and Chip Enable

The FFG3105 has an active high chip enable, **CE**, which must be high for chip to function in either STANDBY or ACTIVE modes. When the FFG3105 is used internal to the battery pack, this pin is connected to the gate driver of the protection device used to control the discharge FET. This signal is high whenever the battery pack is functioning within acceptable operating range.

When the FET is turned-off to protect the battery cell the FFG3105 is also disabled and goes to its lowest power condition, SHUTDOWN. This helps to reduce the under-voltage discharge the FFG3105 applies to the internal cell. All internal current paths from **VCELP**, the chip supply, to **GND**, which drain the battery cell, are turned off when **CE** = 0 to guarantee a typical quiescent current of ≤ 1 µA.

### Wake and Sleep

The FFG3105 also supports WAKE and SLEEP modes that can be used for system debug. In WAKE mode the entire device is turned on and left on until the SLEEP mode is requested. In WAKE mode the internal Bandgap, Oscillator and LDO are enabled and the current increases.

### Calculating Average Power

Average power consumption of the FFG3105 is a function of the frequency of voltage and temperature read requests. During measurement time the FFG3105 uses 180 µA, when at rest, in STANDBY it uses 2 µA.

Average power consumption can be calculated using the following equation and graphic.

$$Average\ Current \approx (180\mu A \times 0.0256s + 58\mu A \times 0.0005s + 2.0\mu A \times (Tr - 0.0256s - 0.0005s))/Tr \quad (1)$$

where $Tr$ = Time between read requests in seconds (S)

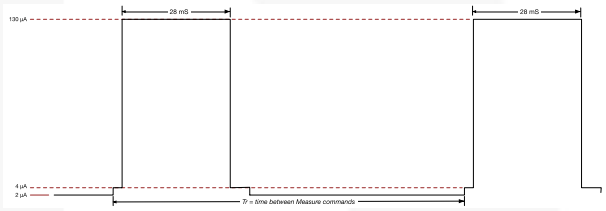



**Figure 5. Timing Relationship Diagram**

For example, if the system were to request voltage and temperature readings from the FFG3105 once every 6 seconds, the average power would be:

$$Average\ Current \approx (180\mu A \times 0.0256s + 58\mu A \times 0.0005s + 2.0\mu A \times (6s - 0.0256s - 0.0005s))/6s \quad (2)$$

$$Average\ Current = 4.9\ \mu A \quad (3)$$

For a case where the Host system requests voltage and temperature once per second, the average current is 6.06 µA. A summary of the active current vs. sampling interval is shown in Figure 6.

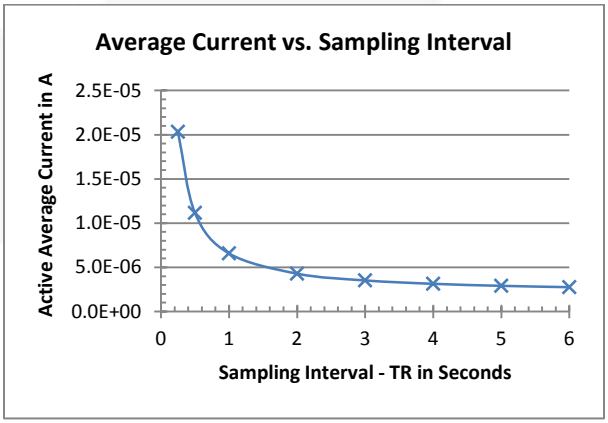



**Figure 6. Average Active Current**

## Battery and Device Protection

### Cell Protection

The FFG3105 has been designed to be integrated directly into a single-cell Lithium-ion battery pack and meet all the necessary safety requirements. This is accomplished by having separate terminals (**VCELP** and **VSNS**) to power the device, and sense the cell voltage respectively. Each of these connections to the battery cell requires a series resistor to limit the current if an internal short occurs. This is needed because the FFG3105 is connected directly to the cell cathode and anode. Additional filter capacitors may also be required. It is recommended that series capacitors be used to eliminate a single capacitor short from shorting out the cell.

### Input ESD Protection

In a removable battery pack, **SCL** and **SDA**, the I2C clock and data pins of the host bus are externally exposed. It is recommended that a protection network consisting of a Zener diode and resistors, or some equivalent, be connected to the serial interface pins to protect the pack from ESD events.

The maximum pull-up voltage of 5.5 V is supported for device programming, so it is recommended that the breakdown voltage of the protection device be > 5.6 V.

The devices needed for cell and ESD protection are represented in the schematic in Figure 1.

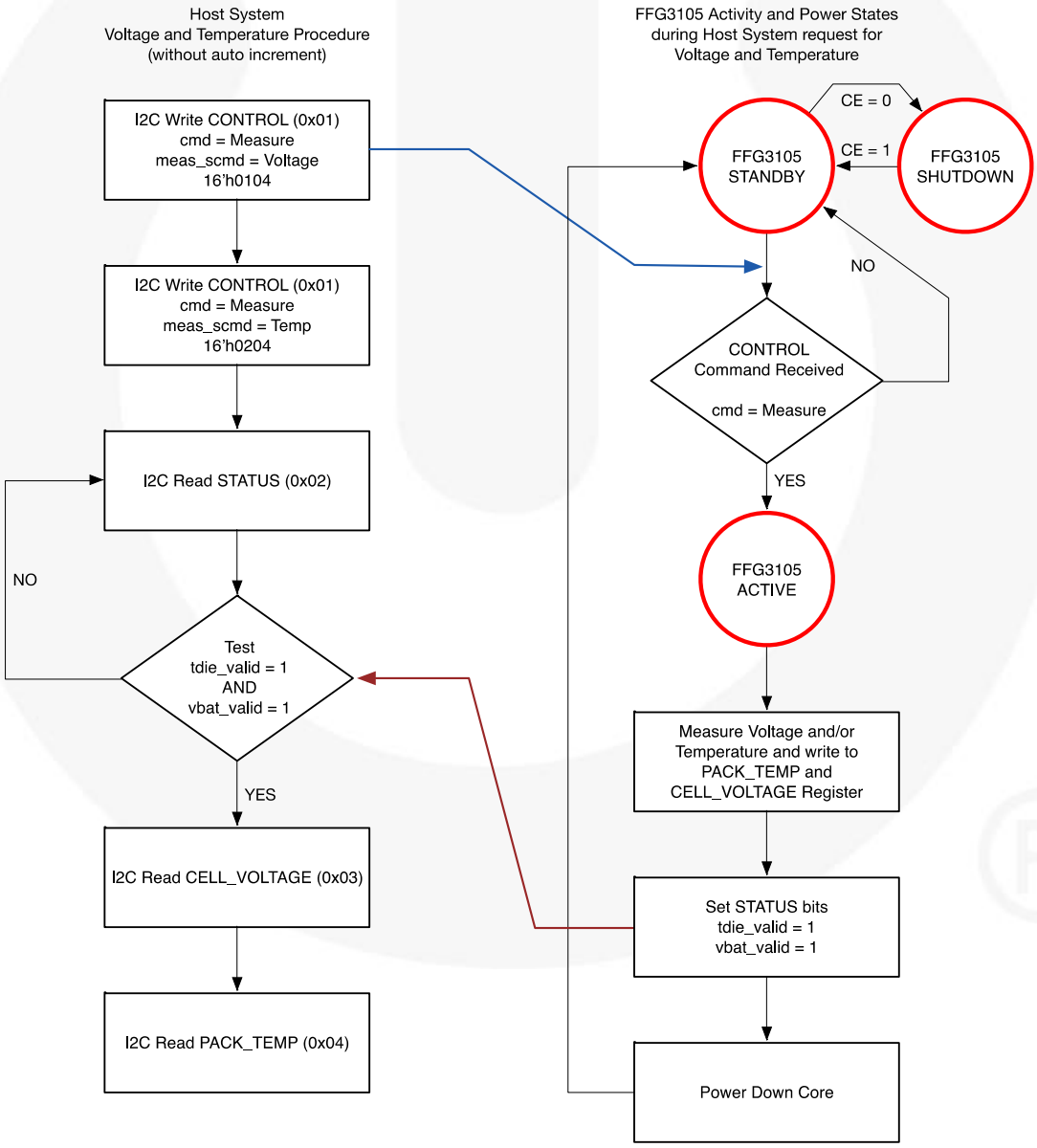



**Figure 7. Voltage and Temperature Data Request**

## Device Programming

The FFG3105 has two 64-bit battery identifications values that can be programmed into the device, This section outlines the procedure that should be followed to program the device.

### Keyword Registers

The device must first be unlocked by writing the 32-bit Keyword with the appropriate value into KEYWORD_MSW and KEYWORD_LSW registers at $I^2C$ addresses 0x06 and 0x07. Next an Unlock command must be written to the CONTROL register to perform the Unlock. This enables the user to write into the BID registers.

### BID Registers

Each BID uses four 16-bit registers that total 64-bits. The first BID, BID0, is located at $I^2C$ address 0x20, 0x21, 0x22, and 0x23. The second BID, BID1 is located at 0x24, 0x25, 0x26, and 0x27. Once unlocked one or both of these BID must be written and then verified by reading it back.

### Programming

Once the BID's have been verified the Program command is issued using an $I^2C$ write to the CONTROL register. Before issuing the Program command the supply voltage, $V_{CELP}$[18], must be increased to 5.5 V. Once programming has been initiated an internal state machine controls the part and completes the programming process. Programming both BID's takes approximately 5.2 ms but the actual time will depend on the number of 1's in the BID codes.

Reading the TEST_STATUS register bit fuse_prgm_done can monitor the status of the programming sequence. Once completed this bit is set to 1.

### Verification

Once programmed, the voltage is lowered back to 3.8 V and reset. After reset the BID's can be read and their internal status checks to determine if the programming was successful.

**Note:**

18. $V_{CELP}$ should be capable of supplying a minimum of 61 mA.

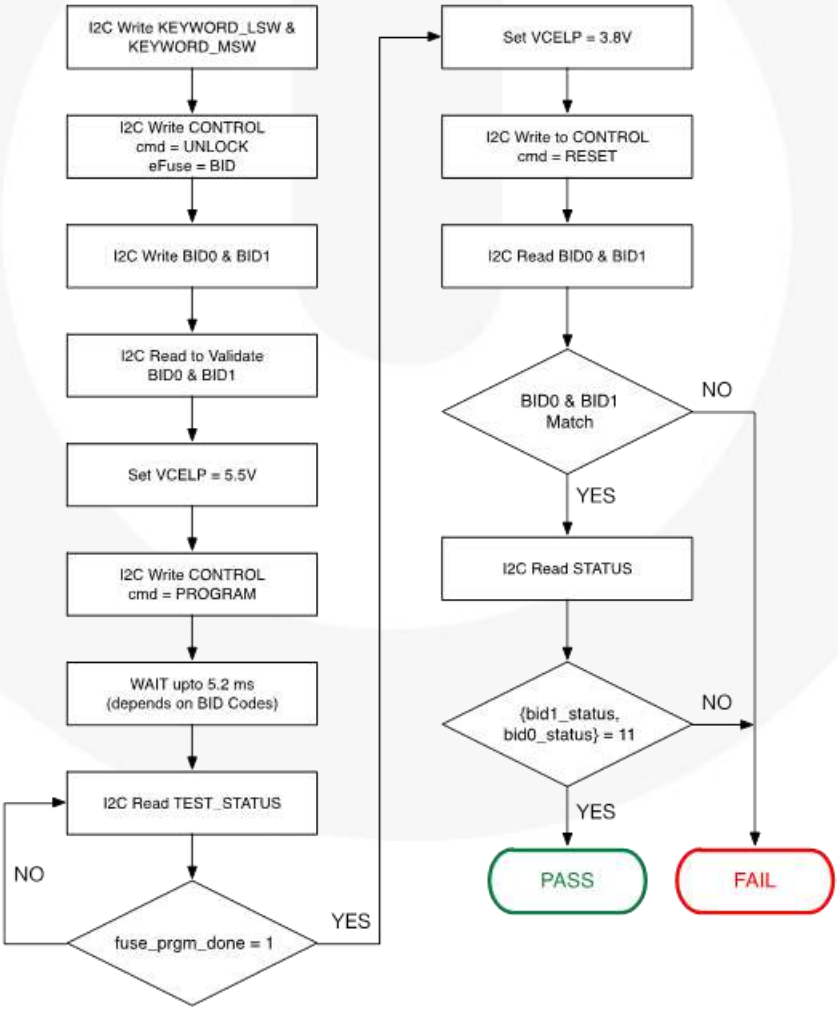



**Figure 8. Device Programming**

## I²C Interface

The I²C interface is slave controllers with a standard 7-bit device address that supports read, incremental read, write and incremental write. This allows an external host to control the FFG3105 and configure it.

The I²C supports:

- 7-Bit Standard Device Address
- 100 kbit/s Standard Mode
- 400 kbit/s Fast Mode
- Auto Increment to support Burst-Reads and Burst-Writes for the most used registers.

The FFG3105's **SCL** line is an input and its SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The **SDA** line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

### Slave Address

The I²C Device ID is 7-bits and is constructed as shown in the table below. There is always an 8th bit, which indicates if the operation being done to the slave is either a read or write. A read is active-high and indicated by '1', the write is active-low and indicated by a '0'.

The slave device ID will be configurable with a device ID at address 8'h6E for write and 8'h6F for read.

**Table 2. I²C Slave Address Byte**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Value | 0 | 1 | 1 | 0 | 1 | 1 | 1 | R/$\overline{W}$ |

Other slave addresses can be accommodated upon request. Contact your Fairchild representative.

### Bus Timing

As shown in Figure 9, data is normally transferred when **SCL** is LOW. Data is clocked in on the rising edge of **SCL**. Typically, data transitions at or shortly after the falling edge of **SCL** to allow ample time for the data to set up before the next SCL rising edge.

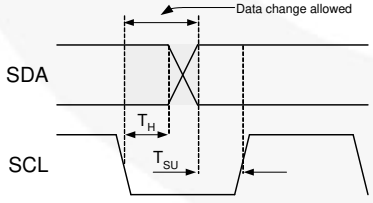



**Figure 9. Data Transfer Timing**

Each bus transaction begins and ends with **SDA** and **SCL** HIGH. A transaction begins with a START condition, which is defined as **SDA** transitioning from 1 to 0 with **SCL** HIGH.

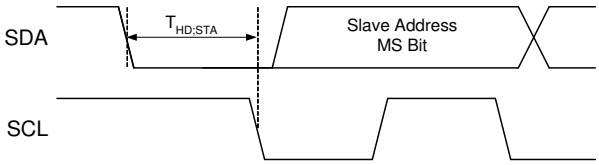



**Figure 10. START Bit**

A transaction ends with a STOP condition, which is defined as **SDA** transitioning from 0 to 1 with **SCL** HIGH.

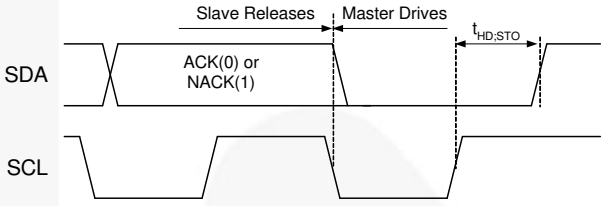



**Figure 11. STOP Bit**

During a read from the FFG3105, the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1-to-0 transition on **SDA** while **SCL** is HIGH.

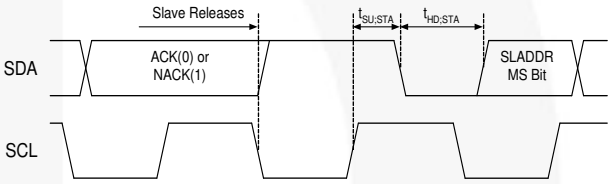



**Figure 12. Repeated STOP Timing**

### Auto–Incrementing

The external host can also utilize auto-increment to do sequential reads or writes of the internal registers.

When the auto-incremented address is not with the supported range of registers one of four responses can be expected.

- If write or read is to an illegal or out of range address the response to the host is a NACK.
- If a write auto increments to an out of range address the response to the host is a NACK.
- If a read auto increment to an out of range address the read returns data with a value of 0xFFFF.

## I²C Read Write Procedures

The following figures illustrate compatible I²C write and read sequences.

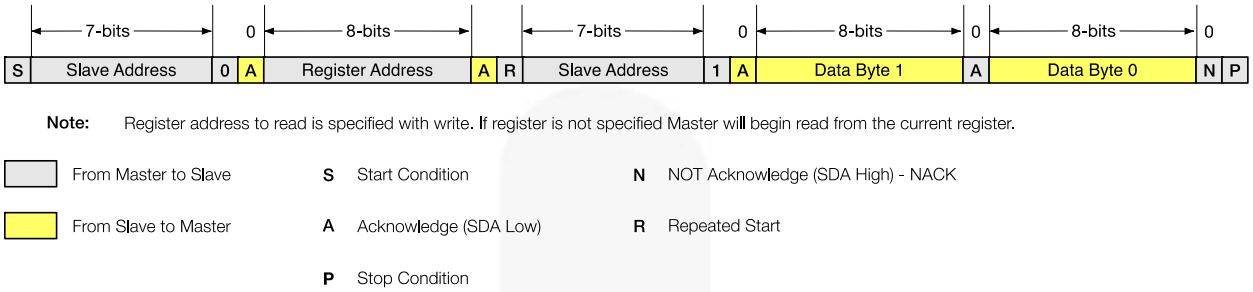



**Figure 13. I²C Read Sequence**

During an I²C read, the master must acknowledge the first byte read for proper operation. Missing or corrupted clocks during an I²C operation, may result in the FFG3105 continuously asserting the SDA line. The I²C master must support the Bus Clear operation in systems where SCL integrity is not guaranteed (for example in systems with a removable battery pack which can result in interrupted I²C transactions).

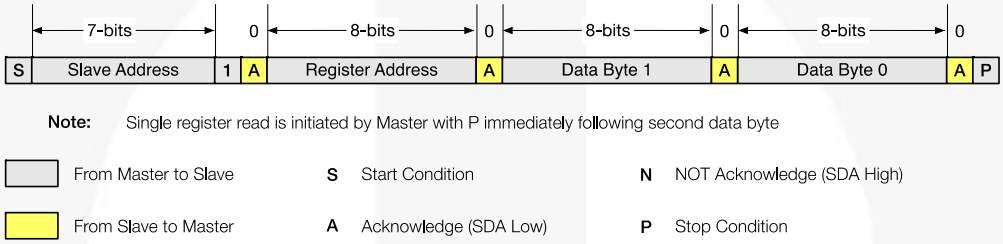



**Figure 14. I²C Write Sequence**

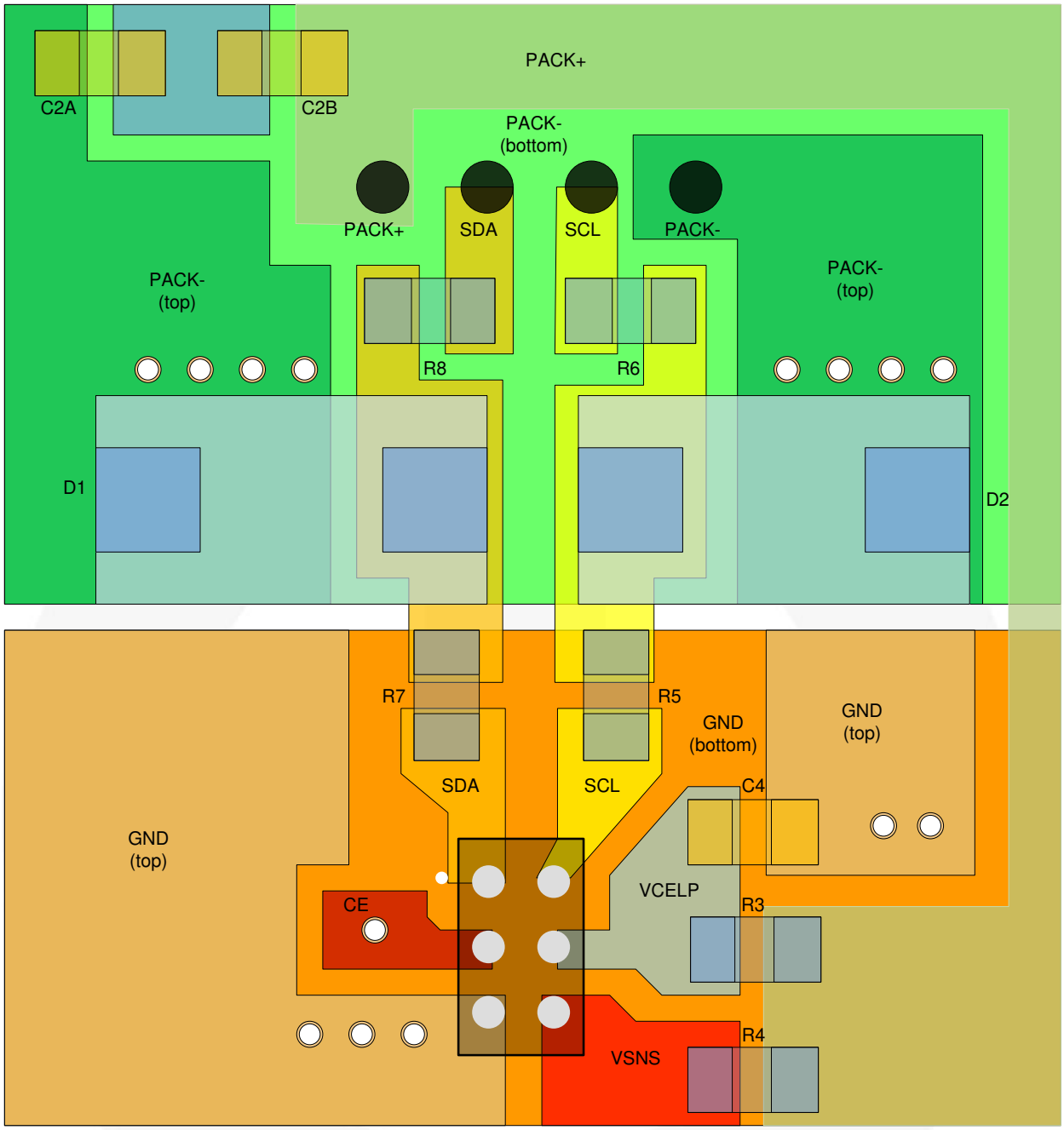



**Figure 15. Recommended Layout**

## Register Information

Any registers or bit fields marked as RESERVED or reserved should be left at their default values and not modified.

**Table 3. Register Map**

| Registers | | | |
|---|---|---|---|
| **Register Name** | **Address** | **Type** | **Description** |
| PART_ID | 0x00 | RO | Part Identification |
| CONTROL | 0x01 | R/W | Control |
| STATUS | 0x02 | RO | Status |
| CELL_VOLTAGE | 0x03 | RO | Cell Voltage Measurement |
| PACK_TEMPERATURE | 0x04 | RO | Pack Temperature |
| CELL_CURRENT | 0x05 | N/A | Reserved for future use |
| KEYWORD_LSW | 0x06 | R/W | Keyword Least Significant Word |
| KEYWORD_MSW | 0x07 | R/W | Keyword Most Significant Word |
| TEST_CONTROL | 0x08 | R/W | Test Control |
| TEST_STATUS | 0x09 | RO | Test Status |
| SPARE | 0x0A | R/W | Spare |
| USER_00 – USER_11 | 0x10-0x1B | R/W | User Configurable |
| BATTERY_ID0 | 0x20-0x23 | R/W | Unique Identification Code 0 |
| BATTERY_ID1 | 0x24-0x27 | R/W | Unique Identification Code 1 |
| RESERVED | 0x30-0x57 | - | Reserved |

## Control and Status Registers for Mission Mode and Test

The registers in this section are used to store information used, created, and maintained by the top level of the chip. They are defined in the address range 0x00 – 0x0A. These registers are powered by the battery and can be written or read when the core is asleep or awake.

**Table 4. PART_ID Register (0x00)**

| Bit Name | Bit | Type | Default | Description |
|---|---|---|---|---|
| rev_id[2:0] | 2:0 | RO | 3'b000 | Device Revision |
| part_id[4:0] | 7:3 | RO | 5'b10000 | Part Identification |
| device_id[7:0] | 15:8 | RO | 8'h6E | $I^2C$ Device ID |

**Table 5. CONTROL Register (0x01)**

| Bit Name | Bit | Type | Default | Description |
|---|---|---|---|---|
| command | 3:0 | R/W/SC | 4'b0000 | Device Command<br>0000 – NOP (used with TEST_CONTROL)<br>0001 – Wake<br>0010 – Sleep<br>0011 – Program (eFuse)<br>0100 – Measure<br>0101 – Lock eFuse Group<br>0110 – Unlock eFuse Group<br>0111 – Reset<br>1000 – Reserved<br>1001 – Reserved<br>1010 – Reserved<br>1011 – Reserved<br>1100 – Reserved<br>1101 – Reserved<br>1110 – Reserved<br>1111 – Test (reserved) |
| eFuse_group | 5:4 | R/W | 2'b00 | Block Group for Lock/Unlock<br>00 – None<br>01 – BID<br>10 – AFE Trim<br>11 – Reserved<br>Note: Only applies with commands 0x5 and 0x6 |
| reserved | 7:6 | R/W | 2'b00 | Reserved |
| The following fields are based on the command chosen | | | | |
| Commands: **NOP**, **Wake**, **Sleep**, **Lock**, **Unlock**, **Reset**, **Program** | | | | |
| reserved | 15:8 | R/W | 8'h00 | N/A |
| Commands: **Measure** | | | | |
| meas_scmd[2:0] | 8 | R/W | 1'b0 | Measure Source Sub Command Bit-0<br>0 – No voltage measurement<br>1 – Measure Voltage |
| | 9 | R/W | 1'b0 | Measure Source Sub Command Bit-1<br>0 – No temperature measurement<br>1 – Measure Temperature |
| | 10 | R/W | 1'b0 | Measure Source Sub Command Bit-2<br>0 – No current measurement<br>1 – Measure Current (Not implemented in FFG3105) |
| meas_scmd[7:3] | 15:11 | R/W | 5'b00000 | Can be treated as "Don't Cares" |
| Commands: **Test** | | | | |
| test_scmd[2:0] | 11:8 | R/W | 4'b0000 | Reserved |
| reserved | 15:12 | R/W | 4'b0000 | Can be treated as "Don't Cares" |

**Table 6. STATUS Register (0x02)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| wake_status | 0 | RO | 1'b0 | Core Power Status<br>0 – AFE core is asleep.<br>1 – AFE core is awake. |
| busy_status | 1 | RO | 1'b0 | Busy Status<br>0 – chip core is not busy<br>1 – chip core is busy |
| keep_awake | 2 | RO | 1'b0 | Keep Awake<br>0 – core is not kept awake<br>1 – core is to be kept awake |
| tdie_valid | 3 | RO | 1'b0 | Die Temperature Measurement Valid<br>0 – current pack temperature invalid<br>1 – current pack temperature valid |
| vbat_valid | 4 | RO | 1'b0 | Battery Voltage Measurement Valid<br>0 – current cell voltage invalid<br>1 – current cell voltage valid |
| ibat_valid<br>(reserved) | 5 | RO | 1'b0 | Battery Current Measurement Valid<br>0 – current cell current invalid<br>1 – current cell current valid |
| bid_lock_status | 6 | RO | 1'b1 | Battery ID Lock Status<br>0 – unlocked<br>1 – locked |
| at_lock_status | 7 | RO | 1'b1 | AFE Trim Lock Status<br>0 – unlocked<br>1 – locked |
| bid0_status | 8 | RO | 1'b0 | BID0 Status<br>0 – BID0 Redundancy Check Failed<br>1 – BID0 Redundancy Check Passed |
| bid1_status | 9 | RO | 1'b0 | BID1 Status<br>0 – BID1 Redundancy Check Failed<br>1 – BID1 Redundancy Check Passed |
| reserved | 15:8 | RO | 8'hXX | Reserved |

**Table 7. CELL_VOLTAGE Register (0x03)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| cell_voltage | 15:0 | RO | 16'h0000 | Battery Voltage Measurement Unsigned Short<br>MSB = a[15] = $2^{2}$ = 4 V<br>LSB = a[0] = $2^{-13}$ = 122.07 µV<br>+FS = 16'b1111111111111111 = 7.99987793 V<br>- FS = 16'b0000000000000000 = 0 V |

**Table 8. PACK_TEMPERATURE Register (0x04)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| pack_temperature | 15:0 | R | 16'h0000 | Temperature Measurement Signed Short<br>MSB = a[15] = $-2^{8}$ = -256 mV<br>LSB = a[4] = $2^{-3}$ = 0.125 mV<br>+FS = 255.9921875 mV<br>-FS = -255.9921875 mV |

**Table 9. CELL_CURRENT Register (0x05)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| cell_current | 15:0 | R | 16'h0000 | Reserved |

**Note:**
19. Not supported in the FFG3105.

**Table 10. KEYWORD_LSW Register (0x06)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| keyword[15:0] | 15:0 | R/W | 16'hFFFF | Protection Keyword Least Significant Word |

**Table 11. KEYWORD_MSW Register (0x07)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| keyword[31:0] | 15:0 | R/W | 16'h0000 | Protection Keyword Most Significant Word |

**Table 12. TEST_CONTROL Register (0x08)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| reserved | 15:0 | R/W | 16'h0000 | Reserved |

**Table 13. TEST_STATUS Register (0x09)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| reserved | 15:0 | RO | 16'h0000 | Reserved |

**Table 14. SPARE Register (0x0A)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| User Defined | 15:0 | R/W | 16'h0000 | Spare scratch pad register |

## User Battery Parameter Registers

The 12 registers in this section can be used to hold the Save/Restore content of the FFG1040. If the FFG3105 is not used with the FFG1040, these become user definable registers. These registers sit in the **VCELP** domain and retain their value if the battery pack has been properly charged and does not experience an over-discharge or over-current condition.

These registers can be written or read when the core is asleep or awake.

**Table 15. USER_00 – USER_011 - Register (0x10 – 0x1B)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| User Defined | 15:0 | R/W | 16'h0000 | 12 User Defined R/W registers |

## Battery Identification Registers

These two sets of four 16-bit registers are assigned to hold two 64-bit battery identifications. These should be concatenated such that BID0[63:0] = {BID_03[15:0], BID_02[15:0], BID_01[15:0], BID_00[15:0]} and BID1[63:0] = {BID_13[15:0], BID_12[15:0], BID_11[15:0], BID_10[15:0]}. These registers can only be written when the core is awake and **wake_status** = 1'b1. They can be read when the core is asleep or awake.

**Table 16. BID_00 Register (0x020)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| bid_data_00[15:0] | 15:0 | RO | 16'h0000 | Battery ID 0 Register – Bytes 0 & 1 |

**Table 17. BID_01 Register (0x021)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| bid_data_01[31:16] | 15:0 | RO | 16'h0000 | Battery ID 0 Register – Bytes 2 & 3 |

**Table 18. BID_02 Register (0x022)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| bid_data_02[47:32] | 15:0 | RO | 16'h0000 | Battery ID 0 Register – Bytes 4 & 5 |

**Table 19. BID_03 Register (0x023)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| bid_data_03[63:48] | 15:0 | RO | 16'h0000 | Battery ID 0 Register – Bytes 6 & 7 |

**Table 20. BID_10 Register (0x024)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| bid_data-10[15:0] | 15:0 | RO | 16'h0000 | Battery ID 1 Register – Bytes 0 & 1 |

**Table 21. BID_11 Register (0x025)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| bid_data_11[31:16] | 15:0 | RO | 16'h0000 | Battery ID 1 Register – Bytes 2 & 3 |

**Table 22. BID_12 Register (0x026)**

| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| bid_data_12[47:32] | 15:0 | RO | 16'h0000 | Battery ID 1 Register – Bytes 4 & 5 |

**Table 23. BID_13 Register (0x027)**

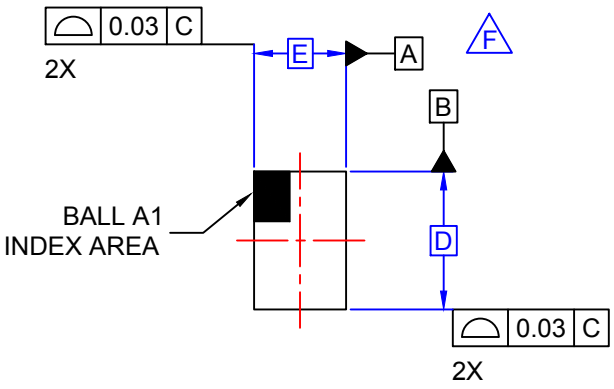
| Type | Bit | Type | Default | Description |
|---|---|---|---|---|
| bid_data_13[63:48] | 15:0 | RO | 16'h0000 | Battery ID 1 Register – Bytes 6 & 7 |

**Notes:**
20. R/W = register value may be read or written.
21. RO = register value that should only be read; attempting a write may cause unpredictable behavior.
22. R/W1CO = register value may be read; writing a 1 clears a bit in another register.

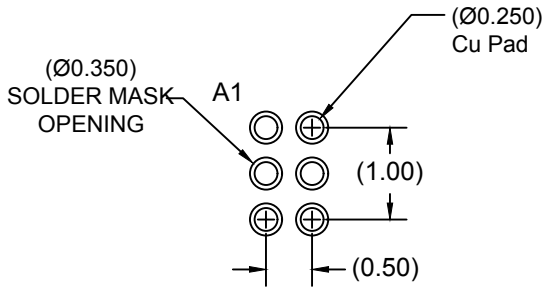
The table below pertains to the Marketing Outline drawing on the following page.

## Product Specific Dimensions

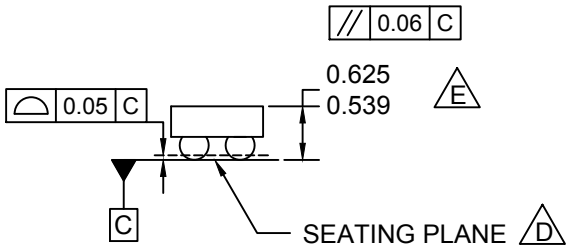
| E (mm) | D (mm) | X (mm) | Y (mm) |
|---|---|---|---|
| 0.960 ± 0.030 | 1.660 ± 0.030 | 0.230 ± 0.018 | 0.330 ± 0.018 |

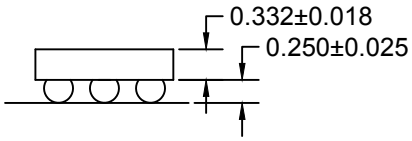



TOP VIEW

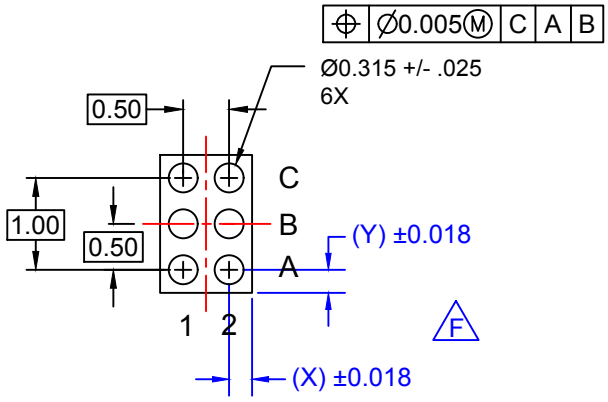



RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)




SIDE VIEWS




BOTTOM VIEW

## NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 582 MICRONS ±43 MICRONS (539-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC006AFrev3.

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