ARM® Cortex®-M0

32-bit Microcontroller

NuMicro® Family
M0519 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro® M0519 Series 32-bit microcontroller is embedded with the newest ARM® Cortex®-M0 core at a cost equivalent to traditional 8-bit microcontroller for industrial control and applications which need high performance.

The NuMicro® M0519 Series embedded with the Cortex®-M0 core runs up to 72 MHz and supports a variety of industrial control and applications which need high CPU performance. The NuMicro® M0519 Series provides 128K/64K bytes embedded flash, 4 Kbytes data flash, 8 Kbytes flash for the ISP, and 16K bytes embedded SRAM. This MCU includes advanced PWM function and input capture timer which are specially designed for motor driving application. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, UART, SPI, I2C, PWM Timer, GPIO, 12-bit ADC, Low Voltage Detector and Brown-out detector. These useful functions make the NuMicro® M0519 Series powerful for a wide range of applications.

In addition, the NuMicro® M0519 Series is equipped with ISP (In-System Programming), ICP (In-Circuit Programming) functions and IAP (In-Application Programming) which allow user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex®-M0 core running up to 72 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode by WFI instructions
  - Single-cycle 32-bit hardware multiplier
  - Supports programmable 4 level priorities of Nested Vectored Interrupt Controller (NVIC)
  - Supports Serial Wire Debug (SWD) support with two watchpoints and four breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5V to 5.5V
- Memory
  - 128K/64K bytes Flash for program memory (APROM)
  - 4KB Flash for data memory (Data Flash)
  - 8KB Flash for loader (LDROM)
  - Supports In-system program (ISP) and In-application program (IAP) application code update
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
  - 16K bytes embedded SRAM
- Clock Control
  - Built-in 22.1184 MHz internal high speed RC oscillator (HIRC) for system operation (variation < 2% at -40˚C ~ +105˚C)
  - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation
  - Built-in 4~24 MHz external high speed crystal oscillator (HXT) for precise timing operation
  - Supports one PLL up to 72 MHz for high performance system operation, sourced from HIRC and HXT
  - Supports clock output
- Hardware divider
  - Supports signed 32-bit dividend, 16-bit divisor operation
- GPIO port
  - Four I/O modes:
  - TTL/Schmitt trigger input selectable
  - Bit control available
  - I/O pin configured as interrupt source with edge/level trigger setting
  - Supports high driver and high sink current I/O (up to 16 mA at 5V)
  - INT0 and INT1 pins with individual interrupt vectors
  - Supports up to 82/51/38 GPIOs for LQFP100/64/48 respectively
- Timers
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Provides One-shot, Periodic, Toggle and Continuous Counting operation modes
  - Supports event counting function to count the event from external pin
- Watchdog Timer
  - Supports multiple clock sources from LIRC(default selection) and HCLK/2048
  - 8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
  - Time-out reset delay period time can be selected
- Window Watchdog Timer

- Supports multiple clock sources from HCLK/2048 (default selection) and LIRC
- Window set by 6-bit counter with 11-bit prescale
- Able to wake up from Power-down or Idle mode

- Basic PWM
  - 1 unit of 16-bit basic PWM, up to 2ch output
  - Alternative function as input capture timer
- Enhanced PWM
  - 2 units of 16-bit enhanced PWM, up to 6ch output with dead-zone control, brake and polarity control for motor drive
  - Default tri-state during any reset
- Enhanced Input Capture
  - Up to 2 units of 24-bit input capture
  - Each unit has 3 inputs: ECAPx_IC0, ECAPx_IC1 and ECAPx_IC2
- UART
  - Up to two 16550 compatible UART devices
  - Programmable baud-rate generator
  - Buffered receiving and transmitting, each with 16 bytes FIFO
  - Supports flow control (TX, RX, CTS and RTS)
  - Supports IrDA(SIR) function
  - Supports RS-485
- SPI
  - Up to three sets of SPI device
  - Supports SPI master/slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Supports Byte Suspend mode in 32-bit transmission
- I^2C
  - Master/Slave up to 1 Mbit/s
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters
  - Programmable clocks allow versatile rate control
  - Multiple address recognition (four slave address with mask option)
- ADC
  - Two A/D converters
  - Each ADC with up to 8 channel, 12-bit resolution with 10-bit accuracy
  - 16 result registers
  - Sampling rate up to 800ksps
  - Two operating modes:
    - Single Sampling mode: Only one specified channel can be sampled at one time.
    - Simultaneous Sampling mode: Allowing two ADC channels to be sampled simultaneously.
  - Two converting result digital comparators
  - Conversion start by software, external pins, or linked with Timer 0~3 or PWM module
- Up to three Analog Comparators
- Up to two OPA (operational amplifier)

- Brown-out detector
  - 4 levels: 4.4V/3.7V/2.7V/2.2V
  - Optional brown-out interrupt or reset
- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Low Voltage Reset
- 96-bit unique ID
- Operating Temperature: -40℃~105℃
- Develop tools: parallel writer or In-Circuit Programming (ICP) writer
- Packages:
  - All Green package (RoHS)
  - LQFP 100/64/48-pin

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output
SPI	Serial Peripheral Interface

SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® M0519 Selection Guide

4.1.1 NuMicro® M0519 Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	LDROM (KB)	I/O	Timer (32-Bit)	Connectivity				Capture	PWM	ADC (12-Bit)	OPA	Comp.	ISP/ICP/IAP	Package
							UART	SPI	I^2C	LIN							
M0519LD3AE	64	16	4	8	38	4	2	1	1	2	-	6	x2, 16-ch	2	2	v	LQFP48
M0519LE3AE	128	16	Config.	8	38	4	2	1	1	2	-	6	x2, 16-ch	2	2	v	LQFP48
M0519SD3AE	64	16	4	8	51	4	2	2	1	2	-	10	x2, 16-ch	2	2	v	LQFP64
M0519SE3AE	128	16	Config.	8	51	4	2	2	1	2	-	10	x2, 16-ch	2	2	v	LQFP64
M0519VE3AE	128	16	Config.	8	82	4	2	3	1	2	6	14	x2, 16-ch	2	3	v	LQFP100

4.1.2 NuMicro® M0519 Naming Rule

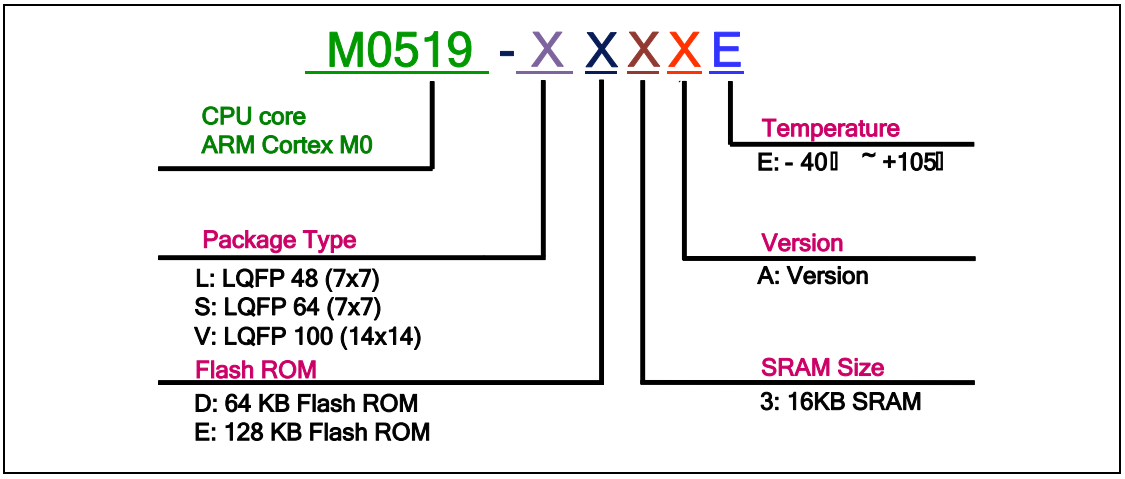


Figure 4-1 NuMicro® M0519 Selection Code

4.2 Pin Configuration

4.2.1 LQFP 100-pin

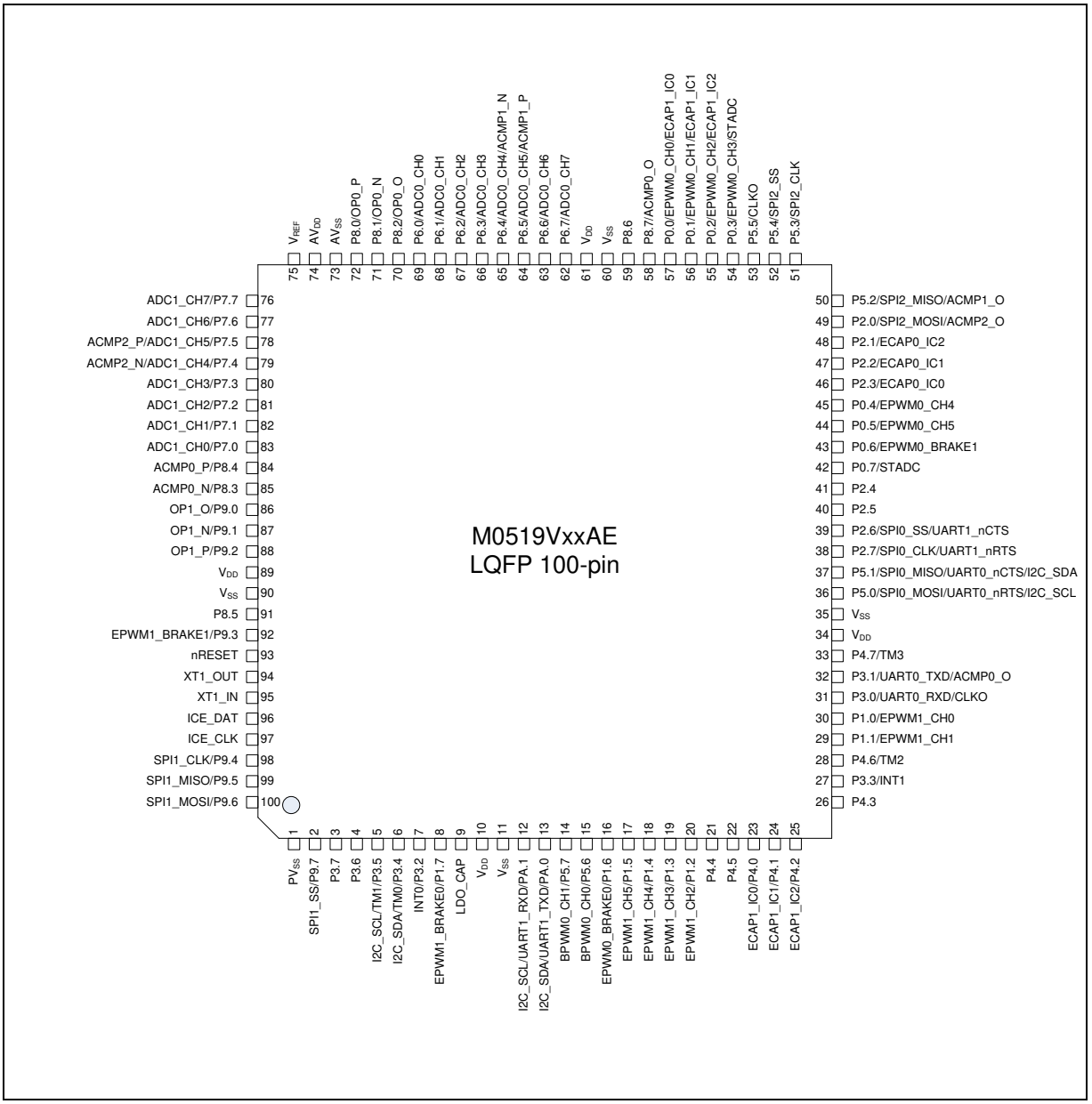


Figure 4-2 NuMicro® M0519VxxAE Series LQFP-100 Pin Diagram

4.2.2 LQFP 64-pin

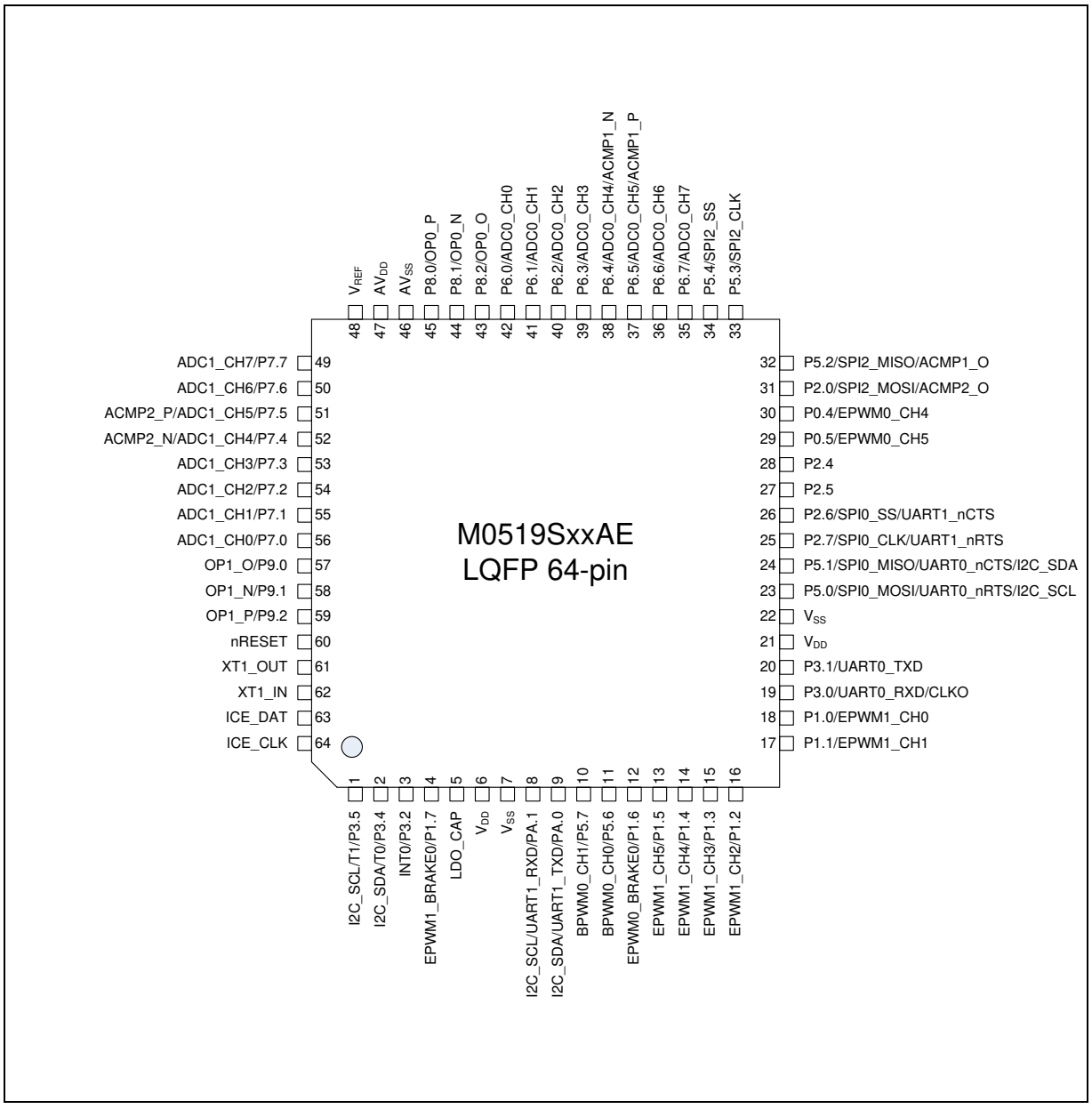


Figure 4-3 NuMicro® M0519SxxAE Series LQFP-64 Pin Diagram

4.2.3 LQFP 48-pin

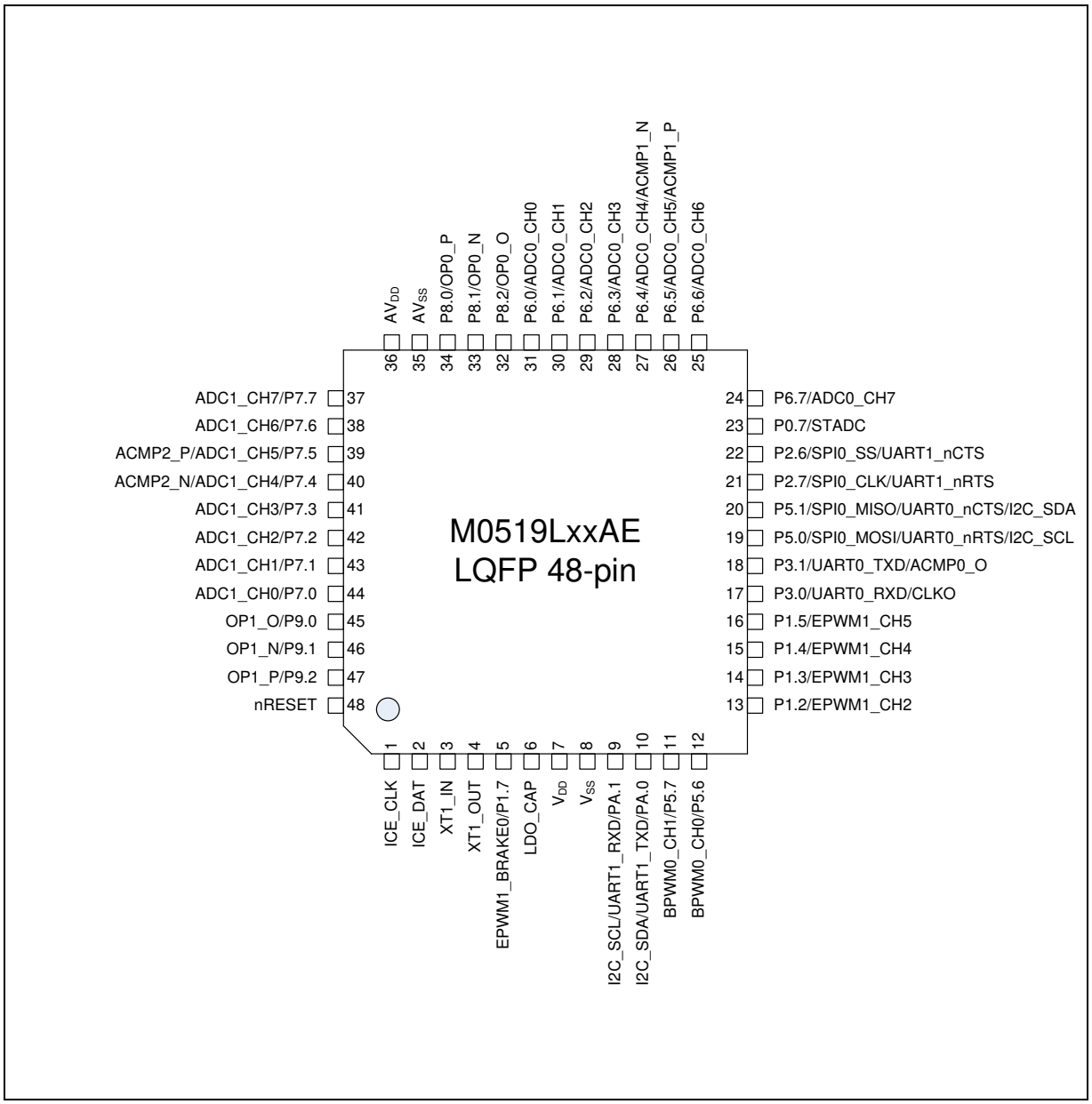


Figure 4-4 NuMicro® M0519LxxAE Series LQFP-48 Pin Diagram

4.3 Pin Description

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
10	6	7	V_{DD}	**P**	**POWER SUPPLY:** Supply voltage **Digital** V_{DD} for operation.
34					
61	21				
89					
11	7	8	V_{SS}	**P**	**GROUND:** Digital Ground potential.
35					
60	22				
90					
9	5	6	LDO_CAP	**P**	**LDO:** LDO output pin **Note: It needs to be connected with a 1uF capacitor.**
1	-	-	PV_{SS}	**P**	**PLL GROUND: PLL** Ground potential.
74	47	36	AV_{DD}	**AP**	Power supply for internal analog circuit
73	46	35	AV_{SS}	**AP**	Ground Pin for analog circuit
75	48	-	V_{REF}	**AP**	Voltage reference input for ADC **Note: It needs to be connected with a 1uF capacitor.**
93	60	48	nRESET	**I (ST)**	**RESET:** nRESET pin is a Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. nRESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
94	61	4	XT1_OUT	**O**	**CRYSTAL OUT:** This is the output pin from the internal inverting amplifier. It emits the inverted signal of XT1_IN.
95	62	3	XT1_IN	**I (ST)**	**CRYSTAL IN:** This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC[1:0] (CONFIG3[1:0]) are both logic 1 by default.
96	63	2	ICE_DAT	**I/O**	Serial Wired Debugger Data pin
97	64	1	ICE_CLK	**I**	Serial Wired Debugger Clock pin
57	-	-	P0.0	**I/O**	General purpose digital I/O pin
			PWM0_CH0	**O**	PWM0 output of PWM Unit 0
			ECAP1_IC0	**I**	Input 0 of Enhanced Input Capture Unit 1
56	-	-	P0.1	**I/O**	General purpose digital I/O pin
			PWM0_CH1	**O**	PWM1 output of PWM Unit 0
			ECAP1_IC1	**I**	Input 1 of Enhanced Input Capture Unit 1
55	-	-	P0.2	**I/O**	General purpose digital I/O pin
			PWM0_CH2	**O**	PWM2 output of PWM Unit 0

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
			ECAP1_IC2	I	Input 2 of Enhanced Input Capture Unit 1
54	-	-	P0.3	I/O	General purpose digital I/O pin
			PWM0_CH3	O	PWM3 output of PWM Unit 0
			STADC	I	ADC external trigger input
45	30	-	P0.4	I/O	General purpose digital I/O pin
			PWM0_CH4	O	PWM4 output of PWM Unit 0
44	29	-	P0.5	I/O	General purpose digital I/O pin
			PWM0_CH5	O	PWM5 output of PWM Unit 0
43	-	-	P0.6	I/O	General purpose digital I/O pin
			PWM0_BRAKE1	I	Brake input pin 1 of PWM Unit 0
42	-	23	P0.7	I/O	General purpose digital I/O pin
			STADC	I	ADC external trigger input
30	18	-	P1.0	I/O	General purpose digital I/O pin
			PWM1_CH0	O	PWM0 output of PWM Unit 1
29	17	-	P1.1	I/O	General purpose digital I/O pin
			PWM1_CH1	O	PWM1 output of PWM Unit 1
20	16	13	P1.2	I/O	General purpose digital I/O pin
			PWM1_CH2	O	PWM2 output of PWM Unit 1
19	15	14	P1.3	I/O	General purpose digital I/O pin
			PWM1_CH3	O	PWM3 output of PWM Unit 1
18	14	15	P1.4	I/O	General purpose digital I/O pin
			PWM1_CH4	O	PWM4 output of PWM Unit 1
17	13	16	P1.5	I/O	General purpose digital I/O pin
			PWM1_CH5	O	PWM5 output of PWM Unit 1
16	12	-	P1.6	I/O	General purpose digital I/O pin
			PWM0_BRAKE0	I	Brake input pin 0 of PWM Unit 0
8	4	5	P1.7	I/O	General purpose digital I/O pin
			PWM1_BRAKE0	I	Brake input pin0 of PWM Unit 1
49	31	-	P2.0	I/O	General purpose digital I/O pin
			SPI2_MOSI	I/O	SPI2 MOSI (Master Out, Slave In) pin
			ACMP2_O	AO	Analog comparator 2 output pin
48	-	-	P2.1	I/O	General purpose digital I/O pin
			ECAP0_IC2	I	Input 2 of Enhanced Input Capture Unit 0

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
47	-	-	P2.2	I/O	General purpose digital I/O pin
			ECAP0_IC1	I	Input 1 of Enhanced Input Capture Unit 0
46	-	-	P2.3	I/O	General purpose digital I/O pin
			ECAP0_IC0	I	Input 0 of Enhanced Input Capture Unit 0
41	28	-	P2.4	I/O	General purpose digital I/O pin
40	27	-	P2.5	I/O	General purpose digital I/O pin
39	26	22	P2.6	I/O	General purpose digital I/O pin
			SPI0_SS	I/O	SPI0 slave select pin
			UART1_nCTS	I	UART1 CTS pin
38	25	21	P2.7	I/O	General purpose digital I/O pin
			SPI0_CLK	I/O	SPI0 serial clock pin
			UART1_nRTS	O	UART1 RTS pin
31	19	17	P3.0	I/O	General purpose digital I/O pin
			UART0_RXD	I	Data Receiver input pin for UART0
32	20	18	P3.1	I/O	General purpose digital I/O pin
			UART0_TXD	O	Data transmitter output pin for UART0
			ACMP0_O	AO	Analog comparator 0 output
7	3	-	P3.2	I/O	General purpose digital I/O pin
			INT0	I	External Interrupt 0 input pin
27	-	-	P3.3	I/O	General purpose digital I/O pin
			INT1	I	External Interrupt 1 input pin
6	2	-	P3.4	I/O	General purpose digital I/O pin
			TM0	I/O	Timer0 external clock
			I2C0_SDA	I/O	I2C0 data input/output pin
5	1	-	P3.5	I/O	General purpose digital I/O pin
			TM1	I/O	Timer1 external clock
			I2C0_SCL	I/O	I2C0 clock output pin
4	-	-	P3.6	I/O	General purpose digital I/O pin
3	-	-	P3.7	I/O	General purpose digital I/O pin
23	-	-	P4.0	I/O	General purpose digital I/O pin
			ECAP1_IC0	I	Input 0 of Enhanced Input Capture Unit 1
24	-	-	P4.1	I/O	General purpose digital I/O pin
			ECAP1_IC1	I	Input 1 of Enhanced Input Capture Unit 1

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
25	-	-	P4.2	I/O	General purpose digital I/O pin
			ECAP1_IC2	I	Input 2 of Enhanced Input Capture Unit 1
26	-	-	P4.3	I/O	General purpose digital I/O pin
21	-	-	P4.4	I/O	General purpose digital I/O pin
22	-	-	P4.5	I/O	General purpose digital I/O pin
28	-	-	P4.6	I/O	General purpose digital I/O pin
			TM2	I/O	Timer2 external clock
33	-	-	P4.7	I/O	General purpose digital I/O pin
			TM3	I/O	Timer3 external clock
36	23	19	P5.0	I/O	General purpose digital I/O pin
			SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin
			UART0_nRTS	O	UART0 RTS pin
37	24	20	P5.1	I/O	General purpose digital I/O pin
			SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin
			UART0_nCTS	I	UART0 CTS pin
50	32	-	P5.2	I/O	General purpose digital I/O pin
			SPI2_MISO	I/O	SPI2 MISO (Master In, Slave Out) pin
			ACMP1_O	AO	Analog comparator 1 output pin
51	33	-	P5.3	I/O	General purpose digital I/O pin
			SPI2_CLK	I/O	SPI2 serial clock pin
52	34	-	P5.4	I/O	General purpose digital I/O pin
			SPI2_SS	I/O	SPI2 slave select pin
53	-	-	P5.5	I/O	General purpose digital I/O pin
			CLKO	O	Frequency Divider output pin
15	11	12	P5.6	I/O	General purpose digital I/O pin
			PWM2_CH0	I/O	PWM0 output of PWM unit 2
14	10	11	P5.7	I/O	General purpose digital I/O pin
			PWM2_CH1	I/O	PWM1 output of PWM unit 2
69	42	31	P6.0	I/O	General purpose digital I/O pin
			ADC0_CH0	AI	ADC analog input 0 for sample-and-hold A
68	41	30	P6.1	I/O	General purpose digital I/O pin
			ADC0_CH1	AI	ADC analog input 1 for sample-and-hold A
67	40	29	P6.2	I/O	General purpose digital I/O pin

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
			ADC0_CH2	AI	ADC analog input 2 for sample-and-hold A
66	39	28	P6.3	I/O	General purpose digital I/O pin
			ADC0_CH3	AI	ADC analog input 3 for sample-and-hold A
65	38	27	P6.4	I/O	General purpose digital I/O pin
			ADC0_CH4	AI	ADC analog input 4 for sample-and-hold A
			ACMP1_N	AI	Analog comparator 1 negative input
64	37	26	P6.5	I/O	General purpose digital I/O pin
			ADC0_CH5	AI	ADC analog input 5 for sample-and-hold A
			ACMP1_P	AI	Analog comparator 1 positive input
63	36	25	P6.6	I/O	General purpose digital I/O pin
			ADC0_CH6	AI	ADC analog input 6 for sample-and-hold A
62	35	24	P6.7	I/O	General purpose digital I/O pin
			ADC0_CH7	AI	ADC analog input 7 for sample-and-hold A
83	56	44	P7.0	I/O	General purpose digital I/O pin
			ADC1_CH0	AI	ADC analog input 0 for sample-and-hold B
82	55	43	P7.1	I/O	General purpose digital I/O pin
			ADC1_CH1	AI	ADC analog input 1 for sample-and-hold B
81	54	42	P7.2	I/O	General purpose digital I/O pin
			ADC1_CH2	AI	ADC analog input 2 for sample-and-hold B
80	53	41	P7.3	I/O	General purpose digital I/O pin
			ADC1_CH3	AI	ADC analog input 3 for sample-and-hold B
79	52	40	P7.4	I/O	General purpose digital I/O pin
			ADC1_CH4	AI	ADC analog input 4 for sample-and-hold B
			ACMP2_N	AI	Analog comparator 2 negative input
78	51	39	P7.5	I/O	General purpose digital I/O pin
			ADC1_CH5	AI	ADC analog input 5 for sample-and-hold B
			ACMP2_P	AI	Analog comparator 2 positive input
77	50	38	P7.6	I/O	General purpose digital I/O pin
			ADC1_CH6	AI	ADC analog input 6 for sample-and-hold B
76	49	37	P7.7	I/O	General purpose digital I/O pin
			ADC1_CH7	AI	ADC analog input 7 for sample-and-hold B
72	45	34	P8.0	I/O	General purpose digital I/O pin
			OP0_P	AI	OP Amplifier 0 positive input

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
71	44	33	P8.1	I/O	General purpose digital I/O pin
			OP0_N	AI	OP Amplifier 0 negative input
70	43	32	P8.2	I/O	General purpose digital I/O pin
			OP0_O	AO	OP Amplifier 0 output
85	-	-	P8.3	I/O	General purpose digital I/O pin
			ACMP0_N	AI	Analog comparator negative input pin
84	-	-	P8.4	I/O	General purpose digital I/O pin
			ACMP0_P	AI	Analog comparator positive input pin
91	-	-	P8.5	I/O	General purpose digital I/O pin
59	-	-	P8.6	I/O	General purpose digital I/O pin
58	-	-	P8.7	I/O	General purpose digital I/O pin
			ACMP0_O	O	Analog comparator output pin
86	57	45	P9.0	I/O	General purpose digital I/O pin
			OP1_O	AO	OP Amplifier 1 output
87	58	46	P9.1	I/O	General purpose digital I/O pin
			OP1_N	AI	OP Amplifier 1 negative input
88	59	47	P9.2	I/O	General purpose digital I/O pin
			OP1_P	AI	OP Amplifier 1 positive input
92	-	-	P9.3	I/O	General purpose digital I/O pin
			PWM1_BRAKE1	I	Brake input pin 1 of PWM Unit 1
98	-	-	P9.4	I/O	General purpose digital I/O pin
			SPI1_CLK	I/O	SPI1 serial clock pin
99	-	-	P9.5	I/O	General purpose digital I/O pin
			SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin
100	-	-	P9.6	I/O	General purpose digital I/O pin
			SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin
2	-	-	P9.7	I/O	General purpose digital I/O pin
			SPI1_SS	I/O	SPI1 slave select pin
13	9	10	PA.0	I/O	General purpose digital I/O pin
			UART1_TXD	O	Data transmitter output pin for UART1
			I2C0_SDA	I/O	I2C0 data input/output pin
12	8	9	PA.1	I/O	General purpose digital I/O pin
			UART1_RXD	I	Data Receiver input pin for UART1

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
			I2C0_SCL	I/O	I2C0 clock output pin

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

5 BLOCK DIAGRAM

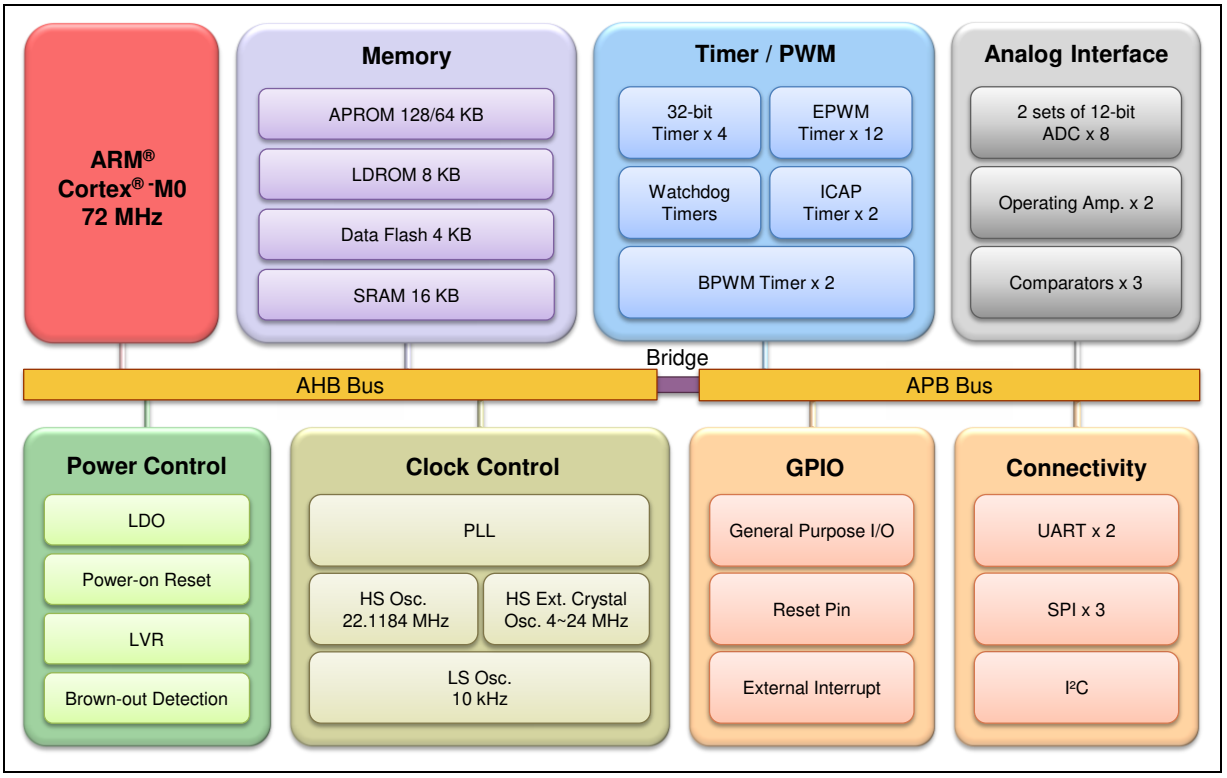


Figure 5-1 NuMicro® M0519 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

Figure 6-1 shows the functional controller of processor.

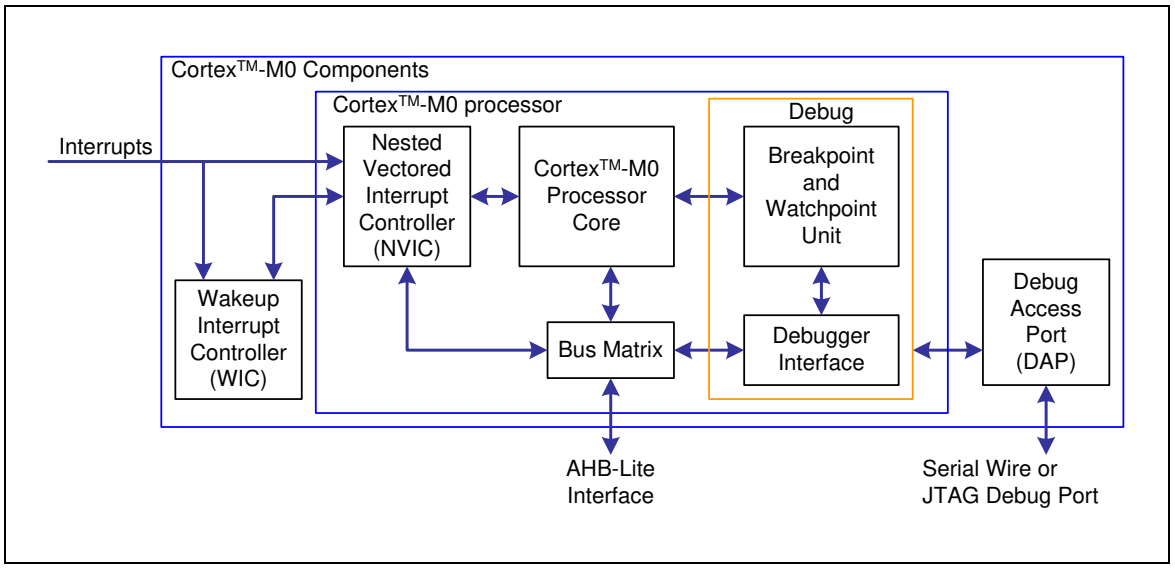


Figure 6-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC:

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode

- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Power Distribution
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Hardware Reset
  - Power-on Reset (POR)
  - Low level on the Reset pin (nRESET)
  - Watchdog Time-out Reset (WDT)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD)
- Software Reset
  - SYS Reset - SYSRESETREQ (AIRCR[2])
  - Cortex®-M0 Core One-shot Reset - CPU_RST (IPRSTC1[1])
  - Chip One-shot Reset - CHIP_RST (IPRSTC1[0])

Power-on Reset or CHIP_RST (IPRST1[0]) reset the whole chip including all peripherals, external crystal circuit and BS (ISPCON[1]) bit.

SYSRESETREQ (AIRCR[2]) reset the whole chip including all peripherals, but does not reset external crystal circuit and BS (ISPCON[1]) bit.

6.2.3 System Power Distribution

In this chip, the power distribution is divided into two segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the I/O pins and internal regulator which provides a fixed 1.8V power for digital operation.

The output of internal voltage regulators, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}).

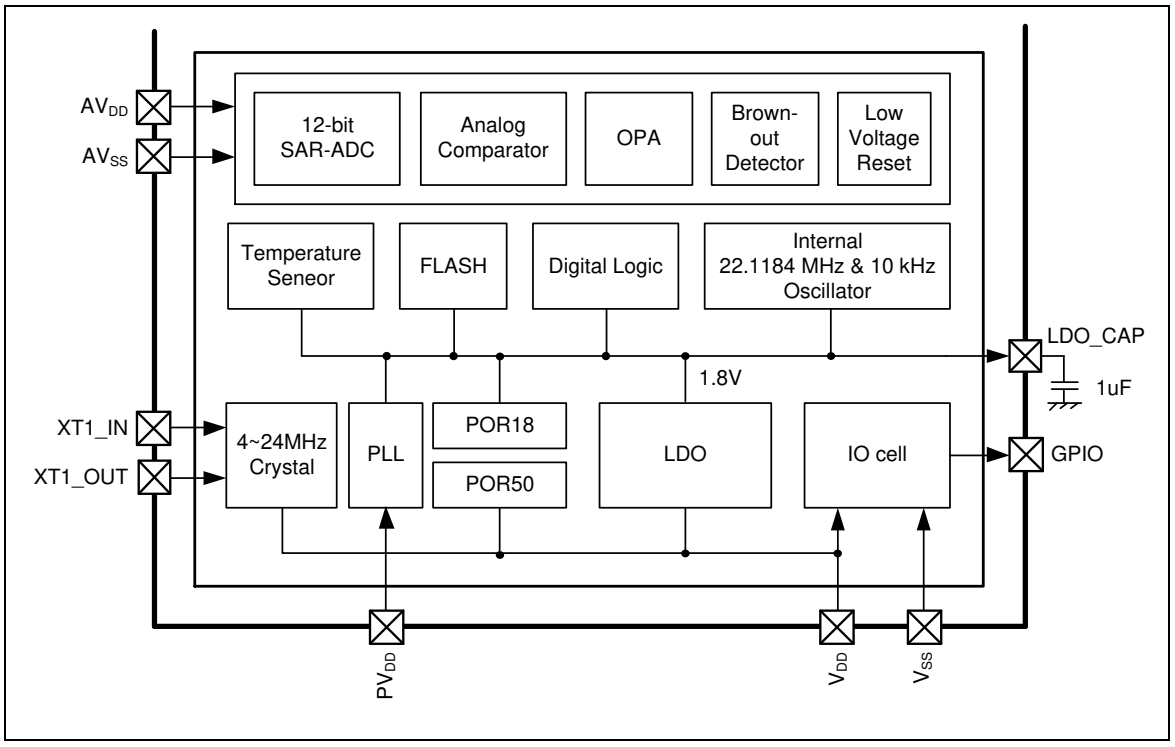


Figure 6-2 NuMicro® M0519 Series Power Distribution Diagram

6.2.4 System Memory Map

The NuMicro® M0519 Series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6-1. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripheral. The NuMicro® M0519 Series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128 KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (16 KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_4000 – 0x5001_7FFF	HDIV_BA	Hardware Divider Register
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_4100 – 0x4000_7FFF	WWDT_BA	Window Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	BPWM0_BA	Basic PWM0 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_3FFF	EADC_BA	Enhanced Analog-Digital-Converter (EADC) Control Registers
0x400F_0000 – 0x400F_3FFF	OPA_BA	Operation Amplifier Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
Reserved	Reserved	Reserved
0x4019_0000 – 0x4019_3FFF	EPWM0_BA	Enhanced PWM0 Control Registers
0x4019_4000 – 0x4019_7FFF	EPWM1_BA	Enhanced PWM1 Control Registers

Address Space	Token	Controllers
0x401B_0000 – 0x401B_3FFF	ECAP0_BA	Enhanced Input Capture 0 Control Registers
0x401B_4000 – 0x401B_7FFF	ECAP1_BA	Enhanced Input Capture 1 Control Registers
Reserved	Reserved	Reserved
Reserved	Reserved	Reserved
Reserved	Reserved	Reserved
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E01F	SYST_BA	System Timer Control Registers
0xE000_E100 – 0xE000_E4EF	NVIC_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED3F	SCS_BA	System Control Registers

Table 6-1 Address Space Assignments for On-Chip Controllers

6.2.5 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.6 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”, which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.6.1 *Exception Model and System Interrupt Map*

Table 6-2 lists the exception model supported by the NuMicro® M0519 Series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0" and the lowest priority is denoted as "3". The default priority of all the user-configurable interrupts is "0". Note that priority "0" is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6-2 Exception Model

Exception Number	Vector Address	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Exception Description	Power Down Wake-Up
1 ~ 15		-	-	-	System exceptions	-
16	0x40	0	**BOD_INT**	Brown-out	Brown-out low voltage detected interrupt	Yes
17	0x44	1	**WDT_INT**	WDT	Watchdog Timer interrupt	Yes
18	0x48	2	**EINT0_INT**	P3.2	External signal interrupt from P3.2 pin	Yes
19	0x4C	3	**EINT1_INT**	P3.3	External signal interrupt from P3.3 pin	Yes
20	0x50	4	**GPG0_INT**	P0~P4 except P3.2 and P3.3	External interrupt from GPIO group 0 (P0~P4) except P3.2 and P3.3	Yes
21	0x54	5	**GPG1_INT**	P5~PA	External interrupt from GPIO group 1 (P5~PA)	Yes
22	0x58	6	**BPWM0_INT**	BPWM0	Basic PWM0 interrupt	No
23	0x5C	7	**EADC0_INT**	EADC0	EADC0 interrupt	No
24	0x60	8	**TMR0_INT**	TMR0	Timer 0 interrupt	No
25	0x64	9	**TMR1_INT**	TMR1	Timer 1 interrupt	No
26	0x68	10	**TMR2_INT**	TMR2	Timer 2 interrupt	No
27	0x6C	11	**TMR3_INT**	TMR3	Timer 3 interrupt	No
28	0x70	12	**UART0_INT**	UART0	UART0 interrupt	Yes

Exception Number	Vector Address	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Exception Description	Power Down Wake-Up
29	0x74	13	**UART1_INT**	UART1	UART1 interrupt	Yes
30	0x78	14	**SPI0_INT**	SPI0	SPI0 interrupt	No
31	0x7C	15	**SPI1_INT**	SPI1	SPI1 interrupt	No
32	0x80	16	**SPI2_INT**	SPI2	SPI2 interrupt	No
33	0x84	17	**Reserved**	Reserved	Reserved	-
33	0x84	17	**Reserved**	Reserved	Reserved	No
34	0x88	18	**I2C0_INT**	I^2C0	I^2C0 interrupt	Yes
35	0x8C	19	**CKD_INT**	CKD	CKD interrupt	No
36	0x90	20	**Reserved**	Reserved	Reserved	-
36	0x90	20	**Reserved**	Reserved	Reserved	-
37	0x94	21	**EPWM0_INT**	EPWM0	Enhanced PWM0 interrupt	No
38	0x98	22	**EPWM1_INT**	EPWM1	Enhanced PWM1 interrupt	No
39	0x9C	23	**ECAP0_INT**	ECAP0	Enhanced input capture 0 interrupt	No
40	0xA0	24	**ECAP1_INT**	ECAP1	Enhanced input capture 1 interrupt	No
41	0xA4	25	**ACMP_INT**	ACMP	Analog Comparator 0 or 1, or OP Amplifier digital output interrupt	Yes (only by analog comparator)
42	0xA8	26	**Reserved**	Reserved	Reserved	-
43	0xAC	27	**Reserved**	Reserved	Reserved	-
42	0xA8	26	**Reserved**	Reserved	Reserved	-
43	0xAC	27	**Reserved**	Reserved	Reserved	-
44	0xB0	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake up from power-down state	-
45	0xB4	29	**EADC1_INT**	EADC1	EADC1 interrupt	No
46	0xB8	30	**EADC2_INT**	EADC2	EADC2 interrupt	No
47	0xBC	31	**EADC3_INT**	EADC3	EADC3 interrupt	No

Table 6-3 System Interrupt Map Vector Table

6.2.6.2 *Vector Table*

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset (Bytes)	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6-4 Vector Table

6.2.6.3 *Operation Description*

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the SLEEPDEEP (SCR[2]) bit is set to 1. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In the Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal oscillator and 22.1184 MHz internal high speed RC oscillator to reduce the overall system power consumption. Figure 6-3 shows the clock generator and the overview of the clock source control.

The clock generator consists of 4 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLL_FOUT), PLL source can be selected from 4~24 MHz external high speed crystal oscillator (HXT) or 22.1184 MHz internal high speed RC oscillator (HIRC)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index (OSC22M_STB(CLKSTATUS[4]), OSC10K_STB(CLKSTATUS[3]), PLL_STB(CLKSTATUS[2]) and XTL12M_STB(CLKSTATUS[0])) are set to 1 after stable counter value reach a define value as Table 6-5. System and peripheral can use these clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index will auto clear when user disables the clock source (OSC10K_EN(PWRCON[3]), OSC22M_EN(PWRCON[2]), XTL12M_EN(PWRCON[0]) and PD(PLLCON[16])). Besides, the clock stable index of HXT, HIRC and PLL will auto clear when chip enter power-down and clock stable counter will re-counting after chip wake-up if correlate clock is enabled.

Clock Source	Clock Stable Count Value
HXT	4096 HXT clock
PLL	6144 PLL source (PLL source is HXT if PLL_SRC(PLLCON[19]) = 0, or HIRC if PLL_SRC(PLLCON[19]) = 1)
HIRC	256 HIRC clock
LIRC	1 LIRC

Table 6-5 Clock Stable Count Value Table

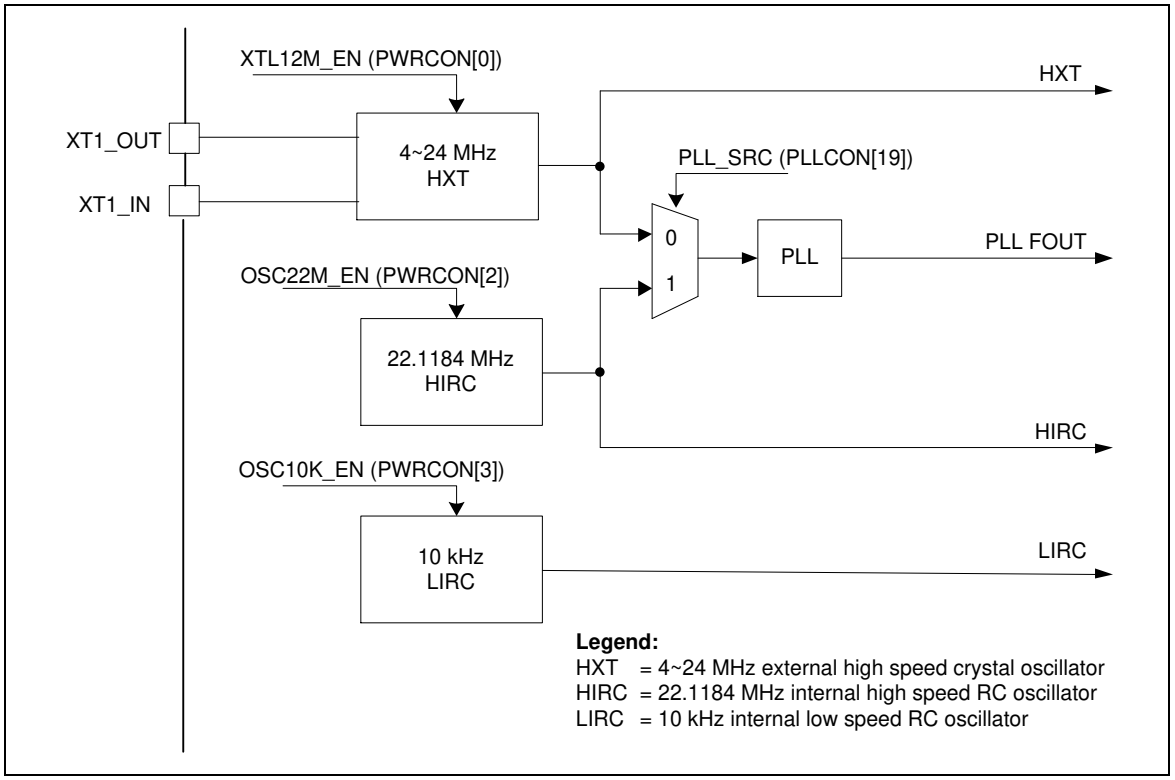
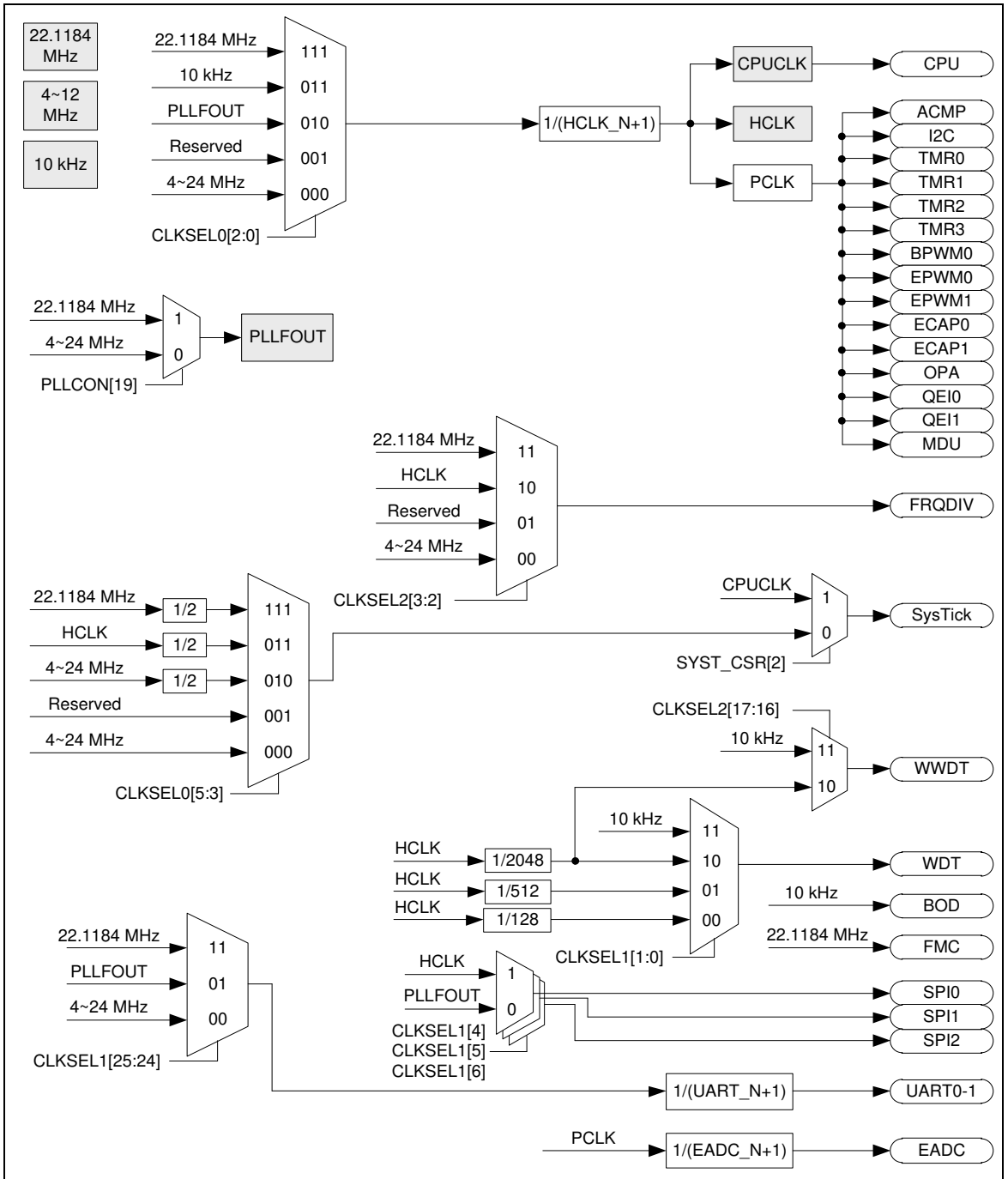


Figure 6-3 Clock Generator Block Diagram



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6-4 Clock Generator Global View Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro® M0519 Series is equipped with 128/64 KB on-chip embedded flash for application program memory (APROM) and data flash, and with 8K bytes for ISP loader program memory (LDROM) that could be programmed boot loader to update APROM and data flash through In System Programming (ISP) procedure. ISP function enables user to update embedded flash when chip is soldered on PCB. After chip is powered on, Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select CBS (Config0[7:6]). By the way, the NuMicro® M0519 Series also provides data flash for user to store some application dependent data before chip power off. For 128 KB APROM device, the data flash is shared with original 128 KB program memory and its start address is configurable in Config1. For 64 KB APROM device, the data flash is fixed at 4K bytes.

6.4.2 Features

- Runs up to 72 MHz and optional up to 50 MHz with zero wait state for continuous address read access
- Supports 512 bytes page erase for all embedded flash
- Supports 128/64 Kbytes application program ROM (APROM)
- Supports 8 KB loader ROM (LDROM)
- Supports 4KB data flash for 64 Kbytes APROM device
- Supports configurable data flash size for 128KB APROM device
- Supports 8 bytes User Configuration block to control system initiation
- Support In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded flash memory

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NuMicro® M0519 Series has up to 82 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 82 pins are arranged in 10 ports named as P0, P1, P2, P3, P4, P5, P6, P7, P8, P9 and PA. The P0/1/2/3/4/5/6/7/8/9 port has the maximum of 8 pins and PA port has the maximum of 2 pins. Each of the 82 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are stay at input mode. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 KΩ for V_{DD} is from 5.0 V to 2.5 V.

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by Px_TYPE[7:0] in Px_MFP[23:16]
- I/O pin configured as interrupt source with edge/level setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling pin interrupt function will also enable the pin wake-up function

6.6 Timer Controller (TIMER)

6.6.1 Overview

The Timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through TDR (TDR[23:0])
- Supports event counting function
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter

6.7 Basic PWM Generator and Capture Timer (BPWM)

6.7.1 Overview

The NuMicro® M0519 series has 1 set of BPWM group (BPWM0), supporting 1 set of BPWM generators that can be configured as 2 independent BPWM outputs, BPWM0_CH0 and BPWM0_CH1, or as 1 complementary BPWM pairs, (BPWM0_CH0, BPWM0_CH1) with programmable dead-zone generator.

The BPWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two BPWM Timers including two clock selectors, two 16-bit BPWM down-counters for BPWM period control, two 16-bit comparators for BPWM duty control and one dead-zone generator. The BPWM generator provides two independent BPWM interrupt flags which are set by hardware when the corresponding BPWM period down counter reaches zero.

Each BPWM interrupt source with its corresponding enable bit can cause CPU to request BPWM interrupt. The BPWM generators can be configured as one-shot mode to produce only one BPWM cycle signal or auto-reload mode to output BPWM waveform continuously. BPWM can be used to trigger EADC when operation in center-aligned mode.

6.7.2 Features

6.7.2.1 BPWM Function:

- Up to 1 BPWM group to support 2 BPWM channels or 1 BPWM paired channels.
- Supports 8-bit prescaler from 1 to 255
- Up to 16-bit resolution BPWM timer
- PWM timer supports edge-aligned and center-aligned operation type
- One-shot or Auto-reload mode BPWM
- PWM Interrupt request synchronized with BPWM period or duty
- Supports dead-zone generator with 8-bit resolution for BPWM paired channels
- Supports trigger EADC

6.7.2.2 Capture Function:

- Supports 2 Capture input channels shared with 2 BPWM output channels
- Supports rising or falling capture condition
- Supports rising or falling capture interrupt

6.8 Enhanced PWM Generator (EPWM)

6.8.1 Overview

This device has two built-in PWM units with the same architecture whose function is specially designed for driving motor control applications.

6.8.2 Features

Each unit supports the features below:

- Three independent 16-bit PWM duty control units with maximum 6 port pins:
  - 3 independent PWM output:
    EPWM0_CH0, EPWM0_CH2 and EPWM0_CH4 for Unit 0
    EPWM1_CH0, EPWM1_CH2 and EPWM1_CH4 for Unit 1
  - 3 complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-time insertion:
    (EPWMx_CH0, EPWMx_CH1), (PWMx_CH2, EPWMx_CH3) and (EPWMx_CH4, EPWMx_CH5) where x=0~1.
  - 3 synchronous PWM pairs, with each pin in a pair in-phase:
    (EPWMx_CH0, EPWMx_CH1), (EPWMx_CH2, EPWMx_CH3) and (EPWMx_CH4, EPWMx_CH5) where x=0~1
- Group control bits:
  EPWMx_CH2 and EPWMx_CH4 are synchronized with EPWMx_CH0
- Supports Edge aligned mode and Center aligned mode
- Programmable dead-time insertion between complementary paired PWMs
- Each pin of EPWMx_CH0 to EPWMx_CH5 has independent polarity setting control
- Mask output control for Electrically Commutated Motor operation
- Tri-state output at reset and brake state
- Hardware brake protection
- Two Interrupt Sources:
  - Interrupt is synchronously requested at PWM frequency when up/down counter comparison matched (edge and center aligned modes) or underflow (center aligned mode).
  - Interrupt is requested when external brake pins asserted
- PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register.
- High Source/Sink current.
- Supports trigger EADC

6.9 Enhanced Input Capture Timer (ECAP)

6.9.1 Overview

This device provides up to two units of Input Capture Timer/Counter which capture function can detect the digital edge changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

6.9.2 Features

- Up to two Input Capture Timer/Counter Units, Input Capture 0 and Input Capture 1.
- Each unit has own interrupt vector
- 24-bit Input Capture up-counting timer/counter
- With noise filter in front end of input ports
- Edge detector with three options
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Each input channel is supported with one capture counter hold register
- Captured event reset/reload capture counter option
- Supports the compare-match function

6.10 Watchdog Timer (WDT)

6.10.1 Overview

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.10.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) and the time-out interval is 1.6 ms ~ 26.214 s if WDT_CLK = 10 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 10 kHz

6.11 Window Watchdog Timer (WWDT)

6.11.1 Overview

The Window Watchdog Timer is used to perform a system reset within a specified window period to prevent software from running to uncontrollable state by any unpredictable condition usually generated by external interferences or unexpected logical conditions.

When the window function is used to trim the watchdog behavior to match the application perfectly, software must refresh the counter before time-out.

6.11.2 Features

- 6-bit down counter value WWDTCVAL (WWDTCVR[5:0]) and 6-bit compare value WINCMP (WWDTCR[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value PERIODSEL (WWDTCR[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.12 Universal Asynchronous Receiver Transmitter (UART)

6.12.1 Overview

The NuMicro® M0519 series provides two channels of Universal Asynchronous Receiver/Transmitters (UART). UART Controller performs Normal Speed UART and supports flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports seven types of interrupts. The UART controller also supports IrDA SIR, RS-485 and LIN.

6.12.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control/flow control function (nCTS, nRTS) and programmable nRTS flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports nCTS wake-up function
- Supports 8-bit receiver buffer time out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UA_TOR [15:8]) register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable data bit length, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
  - Supports 3-/16-bit duration for normal mode
- LIN function mode
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver
- RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software direct enable control provided by nRTS pin

6.13 I²C Serial Interface Controller (I²C)

6.13.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. I²C controller supports Power-down wake-up function.

6.13.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- A built-in a 14-bit time out counter requested the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- External pull-up resistors are needed for high output
- Programmable clocks allow versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)

6.14 Serial Peripheral Interface (SPI)

6.14.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full duplex mode. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NuMicro® M0519 series contains up to three sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be configured as a master or a slave device.

6.14.2 Features

- Up to three sets of SPI controllers
- Supports Master or Slave mode operation
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports the Byte Reorder function
- Supports 3-wire, no slave select signal, bi-direction interface

6.15 Hardware Divider (HDIV)

6.15.1 Overview

The hardware divider is useful to the high performance application. The hardware divider is a signed, integer divider with quotient and remainder outputs.

6.15.2 Features

- Supports Signed (two's complement) integer calculation.
- Supports 32-bit dividend with 16-bit divisor calculation capacity.
- Supports 32-bit quotient and 16-bit remainder outputs.
- Supports divided by 0 warning flag.
- 7 HCLK clocks taken for one cycle calculation.
- Software triggered with finish flag.

6.16 Enhanced Analog-to-Digital Converter (EADC)

6.16.1 Overview

The NuMicro® M0519 Series contains two 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 16 input channels. The two A/D converters ADCA and ADCB can be sampled with Simultaneous or Single Sampling mode. The A/D converters can be started by software, PWM triggers, timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC pulse trigger and external STADC pin input signal.

Note: The analog input port pins must be configured as input type before the EADC function is enabled.

6.16.2 Features

- Analog input voltage range: 0~V_{REF}(Max to 5.0V).
- 12-bit resolution and 10-bit accuracy is guaranteed.
- Up to 16 single-end analog input channels.
- Two SAR ADC converters.
- Four EADC interrupts with individual interrupt vector addresses.
- Maximum EADC clock frequency: 16MHz.
- Up to 1.6M SPS conversion rate, each of ADC converter conversion time less than 1.25μs.
- Two operating modes
  - Single sampling mode: two ADC converters run at normal operation.
  - Simultaneous sampling mode: Allow two ADC converters can be sampled simultaneously.
- An A/D conversion can be started by:
  - Writing 1 to ADST(ADSSTR[n]) bit (n = 0~15) through software
  - External pin STADC
  - Timer0~3 overflow pulse triggers
  - ADINT0, ADINT1 interrupt EOC pulse triggers
  - PWM triggers
- Conversion results are held in 16 data registers with valid and overrun indicators.
- SAMPLEA0~7 ADC control logic modules, each of them is configurable for ADCA converter channel AINA0~7 and trigger source.
- SAMPLEB0~7 ADC control logic modules, each of them is configurable for ADCB converter channel AINB0~7 and trigger source.
- Channel AINA0 supports 2 input sources: external analog voltage and internal OP0 Amplifier output voltage.
- Channel AINB0 supports 2 input sources: external analog voltage and internal OP1 Amplifier output voltage.
- Channel AINA7 supports 4 input sources: external analog voltage, internal fixed band-gap voltage, internal temperature sensor output, and analog ground.

6.17 Analog Comparator (ACMP)

6.17.1 Overview

The NuMicro® M0519 Series contains three comparators. The comparator output is logic 1 when positive input voltage is greater than negative input voltage; otherwise the output is logic 0. Each comparator can be configured to cause an interrupt when the comparator output value changes. The block diagram is shown in **錯誤! 找不到參照來源。**.

6.17.2 Features

- Analog input voltage range: 0~ AV_{DD}
- Supports hysteresis function
- Supports wake-up function
- Supports comparator output inverse function
- Supports the comparator output can be the brake source for EPWM function
- ACMP0 supports
  - 2 positive sources: ACMP0_P and OP0_O
  - 2 negative sources: ACMP0_N and Internal band-gap voltage (V_{BG})
- ACMP1 supports
  - 2 positive sources: ACMP1_P and OP1_O
  - 2 negative sources: ACMP1_N and Internal band-gap voltage (V_{BG})
- ACMP2 supports
  - 1 positive sources: ACMP2_P
  - 2 negative sources: ACMP2_N and Internal band-gap voltage (V_{BG})
- Shares one ACMP interrupt vector for all comparators

6.18 OP Amplifier (OPA)

6.18.1 Overview

This device integrated two operational amplifiers. It can be enabled through OP0_EN (OPACR[0]) and OP1_EN (OPACR[1]) bit. User can measure the output of the OP amplifier through the integrated A/D converter.

6.18.2 Features

- Analog input voltage range: 0~AV_{DD}
- Supports two analog OP amplifiers
- Supports OP output voltage measurement by A/D converter
- Supports Schmitt trigger buffer outputs and generate interrupt
- OP amplifier 0 output can be an optional input source of integrated comparator 0 positive input
- OP amplifier 1 output can be an optional input source of integrated comparator 1 positive input

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+6.3	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	105	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

7.2 DC Electrical Characteristics

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operation voltage	V_{DD}	2.5	-	5.5	V	V_{DD} =2.5V ~ 5.5V				
Power Ground	V_{SS}/ AV_{SS}	-0.3	-	-	V					
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} >= 2.5V				
Analog Operating Voltage	AV_{DD}	2.5	-	V_{DD}	V					
Analog Reference Voltage	V_{REF}	1.2	-	AV_{DD}	V					
Operating Current Normal Run Mode At 72MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD1}		38.7		mA	VDD	HXT	HIRC	PLL	All digital module
						5.5V	12MHz	X	✓	✓
	I_{DD2}		17.9		mA	5.5V	12MHz	X	✓	X
	I_{DD3}		37.2		mA	3.3V	12MHz	X	✓	✓
	I_{DD4}		16.4		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 60MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD5}		32.9		mA	5.5V	12MHz	X	✓	✓
	I_{DD6}		15.5		mA	5.5V	12MHz	X	✓	X
	I_{DD7}		31.4		mA	3.3V	12MHz	X	✓	✓
	I_{DD8}		14.0		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 50MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD9}		29.1		mA	5.5V	12MHz	X	✓	✓
	I_{DD10}		14.5		mA	5.5V	12MHz	X	✓	X
	I_{DD11}		27.6		mA	3.3V	12MHz	X	✓	✓
	I_{DD12}		13.0		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 48MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD13}		28.1		mA	5.5V	12MHz	X	✓	✓
	I_{DD14}		14.0		mA	5.5V	12MHz	X	✓	X
	I_{DD15}		26.6		mA	3.3V	12MHz	X	✓	✓
	I_{DD16}		12.5		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 32MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD17}		19.9		mA	5.5V	12MHz	X	✓	✓
	I_{DD18}		10.4		mA	5.5V	12MHz	X	✓	X
	I_{DD19}		18.4		mA	3.3V	12MHz	X	✓	✓
	I_{DD20}		8.9		mA	3.3V	12MHz	X	✓	X

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operating Current Normal Run Mode At 22.1184MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD21}		11.7		mA	5.5V	X	✓	X	✓
	I_{DD22}		5.3		mA	5.5V	X	✓	X	X
	I_{DD23}		11.6		mA	3.3V	X	✓	X	✓
	I_{DD24}		5.2		mA	3.3V	X	✓	X	X
Operating Current Normal Run Mode At 12MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD25}		8.6		mA	5.5V	12MHz	X	X	✓
	I_{DD26}		4.9		mA	5.5V	12MHz	X	X	X
	I_{DD27}		7.2		mA	3.3V	12MHz	X	X	✓
	I_{DD28}		3.4		mA	3.3V	12MHz	X	X	X
Operating Current Normal Run Mode At 10kHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD29}		0.13		mA	VDD	HXT/ LXT	LIRC	PLL	All digital module
						5.5V	X	10KHz	X	✓
	I_{DD30}		0.12		mA	5.5V	X	10KHz	X	X
	I_{DD31}		0.11		mA	3.3V	X	10KHz	X	✓
	I_{DD32}		0.11		mA	3.3V	X	10KHz	X	X
Operating Current Idle Mode At 72MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE1}		30.1		mA	VDD	HXT	HIRC	PLL	All digital module
						5.5V	12MHz	X	✓	✓
	I_{IDLE2}		9.2		mA	5.5V	12MHz	X	✓	X
	I_{IDLE3}		28.6		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE4}		7.7		mA	3.3V	12MHz	X	✓	X
Operating Current Idle Mode At 60MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE5}		25.7		mA	5.5V	12MHz	X	✓	✓
	I_{IDLE6}		8.2		mA	5.5V	12MHz	X	✓	X
	I_{IDLE7}		24.2		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE8}		6.7		mA	3.3V	12MHz	X	✓	X
Operating Current Idle Mode At 50MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE9}		23.0		mA	5.5V	12MHz	X	✓	✓
	I_{IDLE10}		8.4		mA	5.5V	12MHz	X	✓	X
	I_{IDLE11}		21.5		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE12}		6.9		mA	3.3V	12MHz	X	✓	X

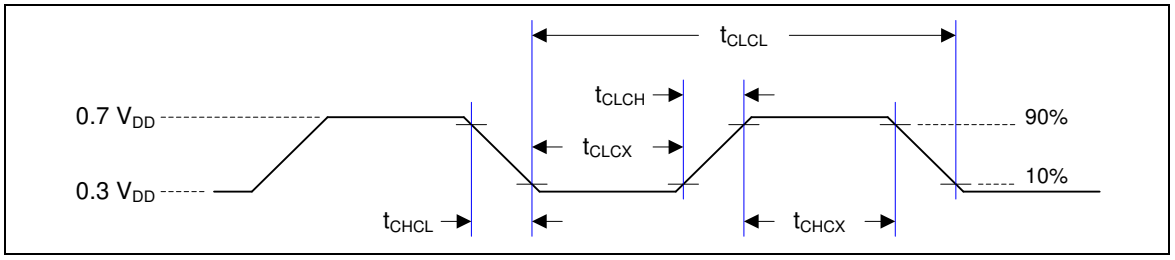
PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operating Current Idle Mode At 48MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE13}		22.3		mA	5.5V	12MHz	X	✓	✓
	I_{IDLE14}		8.1		mA	5.5V	12MHz	X	✓	X
	I_{IDLE15}		20.8		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE16}		6.7		mA	3.3V	12MHz	X	✓	X
Operating Current Idle Mode At 32MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE17}		16.0		mA	5.5V	12MHz	X	✓	✓
	I_{IDLE18}		6.4		mA	5.5V	12MHz	X	✓	X
	I_{IDLE19}		14.5		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE20}		4.9		mA	3.3V	12MHz	X	✓	X
Operating Current Idle Mode At 22.1184MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE21}		8.6		mA	5.5V	X	✓	X	✓
	I_{IDLE22}		2.2		mA	5.5V	X	✓	X	X
	I_{IDLE23}		8.6		mA	3.3V	X	✓	X	✓
	I_{IDLE24}		2.2		mA	3.3V	X	✓	X	X
Operating Current Idle Mode At 12MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE25}		7.2		mA	5.5V	12MHz	X	X	✓
	I_{IDLE26}		3.4		mA	5.5V	12MHz	X	X	X
	I_{IDLE27}		5.7		mA	3.3V	12MHz	X	X	✓
	I_{IDLE28}		1.9		mA	3.3V	12MHz	X	X	X
Operating Current Idle Mode At 10kHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE29}		0.13		mA	VDD	HXT/ LXT	LIRC	PLL	All digital module
						5.5V	X	10KHz	X	✓
	I_{IDLE30}		0.12		mA	5.5V	X	10KHz	X	X
	I_{IDLE31}		0.11		mA	3.3V	X	10KHz	X	✓
	I_{IDLE32}		0.11		mA	3.3V	X	10KHz	X	X
Standby Current Power-down Mode	I_{PWD1}		-		μA	VDD	HXT	HIRC	LIRC	All digital module
						5.5V	✓	X	X	X
	I_{PWD2}		-		μA	5.5V	X	✓	X	X
	I_{PWD3}		-		μA	5.5V	X	X	✓	X
	I_{PWD4}		-		μA	3.3V	✓	X	X	X
	I_{PWD5}		-		μA	3.3V	X	✓	X	X

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
	I_{PWD6}		-		μA	3.3V	X	X	✓	X
Logic 0 Input Current (Quasi-bidirectional mode)	I_{IL}	-	-	-75	μA					
Input Leakage Current (input only)	I_{LK}	-	-	2	μA					
Logic 1 to 0 Transition Current (Quasi-bidirectional mode)	I_{TL}[3]	-	-	-660	μA	V_{DD} = 5.5V, V_{IN}<2.0V				
Internal Pull-High Resistor of /RESET[1]	R_{RST}	15	-	-	kΩ					
Input Low Voltage (TTL input)	V_{IL}	-0.3	-	0.2V_{DD}-0.1	V					
Input Low Voltage (Schmitt input)	V_{IL1}	-0.3		0.3V_{DD}	V					
Input Low Voltage (/RESET, XTAL in)	V_{IL2}	-0.3		0.15V_{DD}	V					
Input High Voltage (TTL input)	V_{IH}	0.2V_{DD}+0.9	-	V_{DD} +0.3	V					
Input High Voltage (Schmitt input, /RESET, XTAL in)	V_{IH1}	0.7V_{DD}	-	V_{DD} +0.3	V					
Hysteresis voltage of (Schmitt input)	V_{HY}	-	0.2V_{DD}	-	V					
Source Current (Quasi-bidirectional Mode)	I_{OH}	-360	-	-	μA	V_{DD} = 4.5V, V_S = 2.4V				
		-60	-	-	μA	V_{DD} = 2.7V, V_S = 2.2V				
		-50	-	-	μA	V_{DD} = 2.5V, V_S = 2.0V				
Source Current (Push-pull Mode)	I_{OH1}	-25	-	-	mA	V_{DD} = 4.5V, V_S = 2.4V				
		-4	-	-	mA	V_{DD} = 2.7V, V_S = 2.2V				
		-3	-	-	mA	V_{DD} = 2.5V, V_S = 2.0V				
Sink Current (Quasi-bidirectional and Push-pull Mode)	I_{OL}	16	-	-	mA	V_{DD} = 4.5V, V_S = 0.45V				
		10	-	-	mA	V_{DD} = 2.7V, V_S = 0.45V				
		9	-	-	mA	V_{DD} = 2.5V, V_S = 0.45V				

Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. I/O pin can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

7.3 AC Electrical Characteristics



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		10	-	-	nS
t_{CLCX}	Clock Low Time		10	-	-	nS
t_{CLCH}	Clock Rise Time		2	-	15	nS
t_{CHCL}	Clock Fall Time		2	-	15	nS

7.3.1 External 4~24MHz Crystal

PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Temperature	-	-40	-	85	℃
Operating Current	12 MHz at V_{DD} = 5V	-	1	-	mA
Clock Frequency	External crystal	4		24	MHz

7.3.1.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20 pF	10~20 pF	without

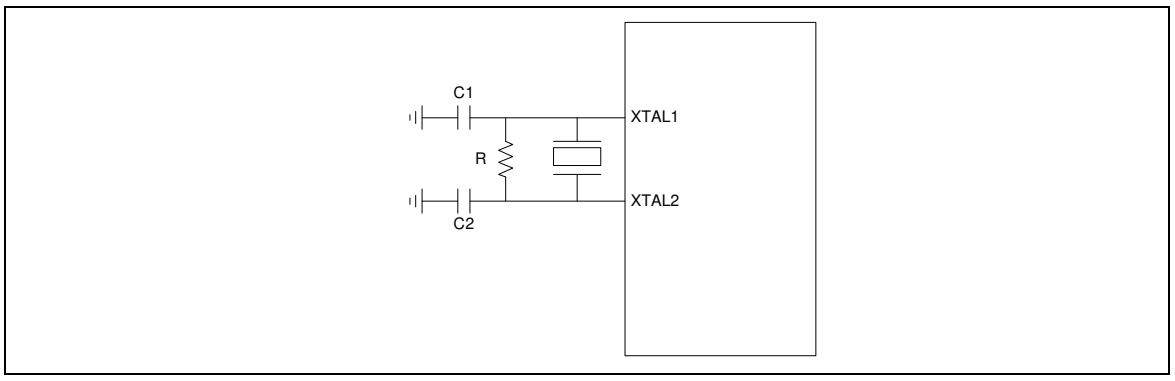


Figure 7–1 Typical Crystal Application Circuit

7.3.2 Internal 22.1184 MHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	2.5	-	5.5	V
Frequency (After calibration)	-	-	22.1184	-	MHz
	+25°C; V_{DD} = 5V	-1	-	+1	%
	-40 to +105°C; V_{DD} = 2.5V~5.5V	-2	-	+2	%
Operation Current	V_{DD} =5V	-	500	-	uA

7.3.3 Internal 10 kHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-30	-	+30	%
	-40℃~+85℃; V_{DD}=2.5 V~5.5 V	-50	-	+50	%

7.4 Analog Characteristics

7.4.1 12-bit SARADC

PARAMETER	SYMBOL	CONDITON	MIN.	TYP.	MAX.	UNIT
Resolution	-		-	-	12	Bit
Differential nonlinearity error	DNL		-	-1~2	-1~4	LSB
Integral nonlinearity error	INL		-	±2	±4	LSB
Offset error	EO		-	±1	10	LSB
Full scale error	EG		-	1	1.005	LSB
Monotonic	-		Guaranteed			
ADC clock frequency	F_{ADC}	AVDD = 5V	-	-	16	MHz
		AVDD = 3V	-	-	8	
Sample rate	F_S	AVDD = 5V	-	-	800	ksps
		AVDD = 3V	-	-	400	
Sample time	T_S		-	8	-	Clock
Conversion time	T_{ADC}		-	12	-	Clock
Supply voltage	AV_{DD}		2.5	-	5.5	V
V_{REF} voltage	V_{REF}		2.0		AV_{DD}	
Supply current	I_{DDA}		-	1.5	-	mA
Reference current	I_{REF}		-	1	-	mA
Input voltage	VIN		0	-	V_{REF}	V
Capacitance	CIN		-	5	-	pF

7.4.2 LDO

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage V_{DD}	2.5		5.5	V	V_{DD} input voltage
Output Voltage	1.62	1.8	1.98	V	V_{DD} > 2.5 V
Operating Temperature	-40	25	105	℃	
Cbp	-	1	-	μF	R_{ESR} = 1 Ω

Note:

1. It is recommended that a 10 uF or higher capacitor and a 100 nF bypass capacitor are connected between V_{DD} and the closest V_{SS} pin of the device.

2. To ensure power stability, a 1 μF or higher capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

7.4.3 Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Quiescent Current	AV_{DD}=5.5 V	-	1	5	μA
Operation Temperature	-	-40	25	105	℃
Threshold Voltage	-	1.6	2.0	2.4	V
Hysteresis	-	0	0	0	V

7.4.4 Brown-out Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Temperature	-	-40	25	105	℃
Quiescent Current	AV_{DD}=5.5 V	-	-	125	μA
Brown-out Voltage	BOD_VL[1:0]=11	4.2	4.4	4.6	V
	BOD_VL [1:0]=10	3.5	3.7	3.9	V
	BOD_VL [1:0]=01	2.6	2.7	2.8	V
	BOD_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

7.4.5 Power-On Reset (5V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Temperature	-	-40	25	105	℃
Reset Voltage	V+	-	2	-	V
Quiescent Current	Vin > reset voltage	-	1	-	nA

7.4.6 Temperature Sensor

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operation Voltage[1]		2.5	-	5.5	V
Operation Temperature		-40	-	105	℃
Current Consumption		6.4	-	10.5	μA
Gain			-1.76		mV/℃
Offset Voltage	Temp=0 ℃		720		mV

7.4.7 Comparator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage AV_{DD}	-	2.5		5.5	V
Operation Temperature	-	-40	25	85	℃
Operation Current	V_{DD}=3.0 V	-	20	40	μA
Input Offset Voltage	-	-	5	15	mV
Output Swing	-	0.1	-	V_{DD}-0.1	V
Input Common Mode Range	-	0.1	-	V_{DD}-1.2	V
DC Gain	-	-	70	-	dB
Propagation Delay	VCM=1.2 V and VDIFF=0.1 V	-	200	-	ns
Comparison Voltage	20 mV at VCM=1 V 50 mV at VCM=0.1 V 50 mV at VCM=V_{DD}-1.2 10 mV for non-hysteresis	10	20	-	mV
Hysteresis	VCM=0.4 V ~ V_{DD}-1.2 V	-	±10	-	mV
Wake-up Time	CINP=1.3 V CINN=1.2 V	-	-	2	μs

7.4.8 OP Amplifier

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AVDD	-	3.0	3.3	5.5	V
Input offset voltage	-	-	2	5	mV
Input offset average drift		-	-	1	uV/℃
Output swing	-	0.1	-	VDD-0.1	V
Input common mode range	-	0.1	-	VDD-1.2	V
DC gain	-	-	80	-	dB
Unity gain freq.	AVDD=5V	-	-	5	MHz
Phase margin		-	50°	-	°
PSRR+	AVDD=5V	-	90	-	dB
CMRR	AVDD=5V	-	90	-	dB
Slew rate	AVDD=5V, RLOAD=33K, CLOAD=50p	6.0	-	-	V/us
Wake up time		-	-	1	us
Quiescent current		-	-	2	mA

7.5 Flash DC Electrical Characteristics

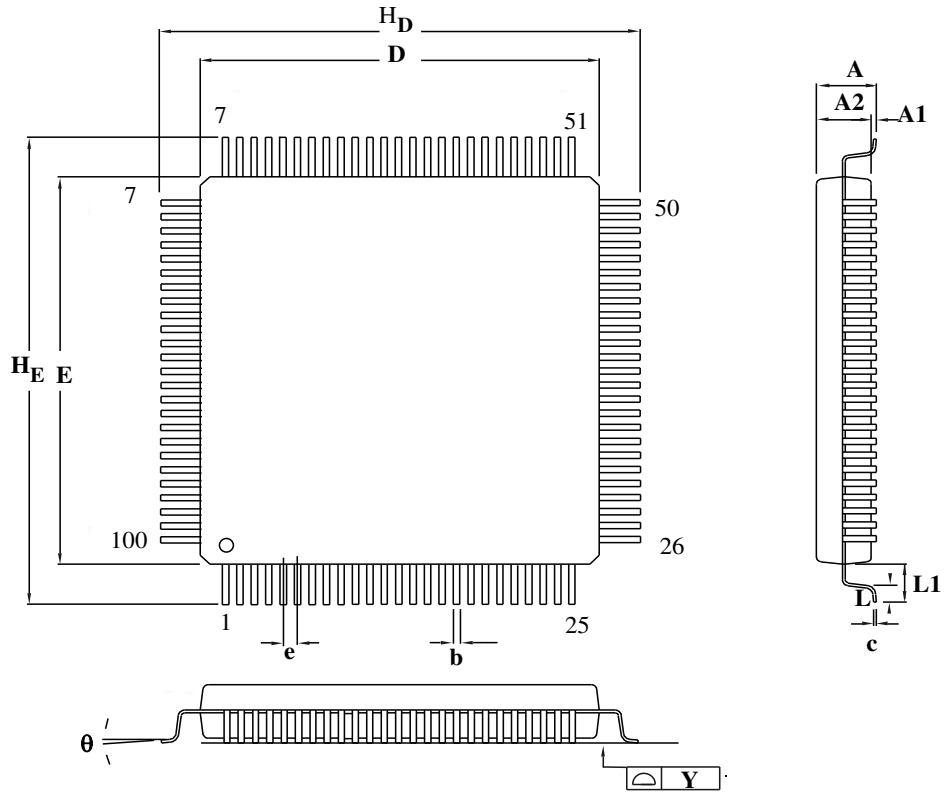
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage		1.62	1.8	1.98	V[2]
N_{ENDUR}	Endurance		10000			cycles[1]
T_{RET}	Data Retention	At 25℃	100			year
T_{ERASE}	Page Erase Time			20		ms
T_{MER}	Mass Erase Time			40		ms
T_{PROG}	Program Time			40		μs
I_{DD1}	Read Current		-	0.15	0.5	mA/MHz
I_{DD2}	Program/Erase Current				7	mA

Note : This table is guaranteed by design, not test in production.

[1] Number of program/erase cycles.
[2] V_{DD} is source from chip LDO output voltage.

8 PACKAGE DIMENSIONS

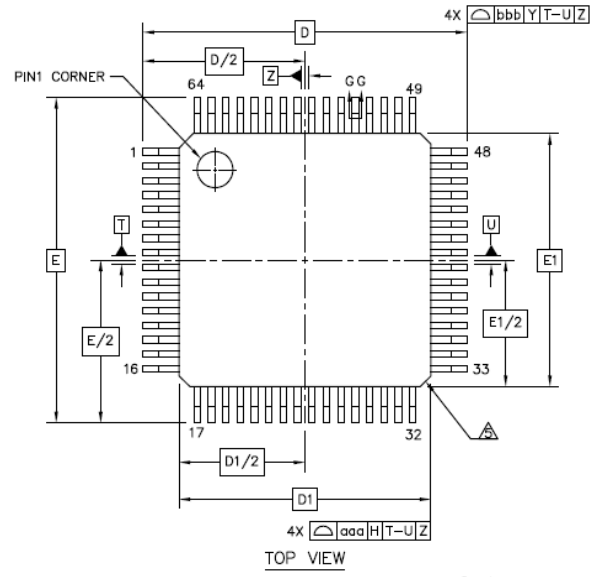
8.1 LQFP 100V (14x14x1.4 mm footprint 2.0mm)



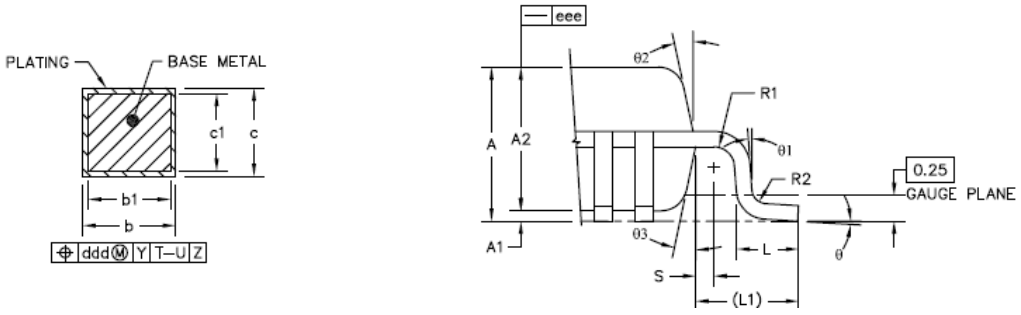
Controlling Dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

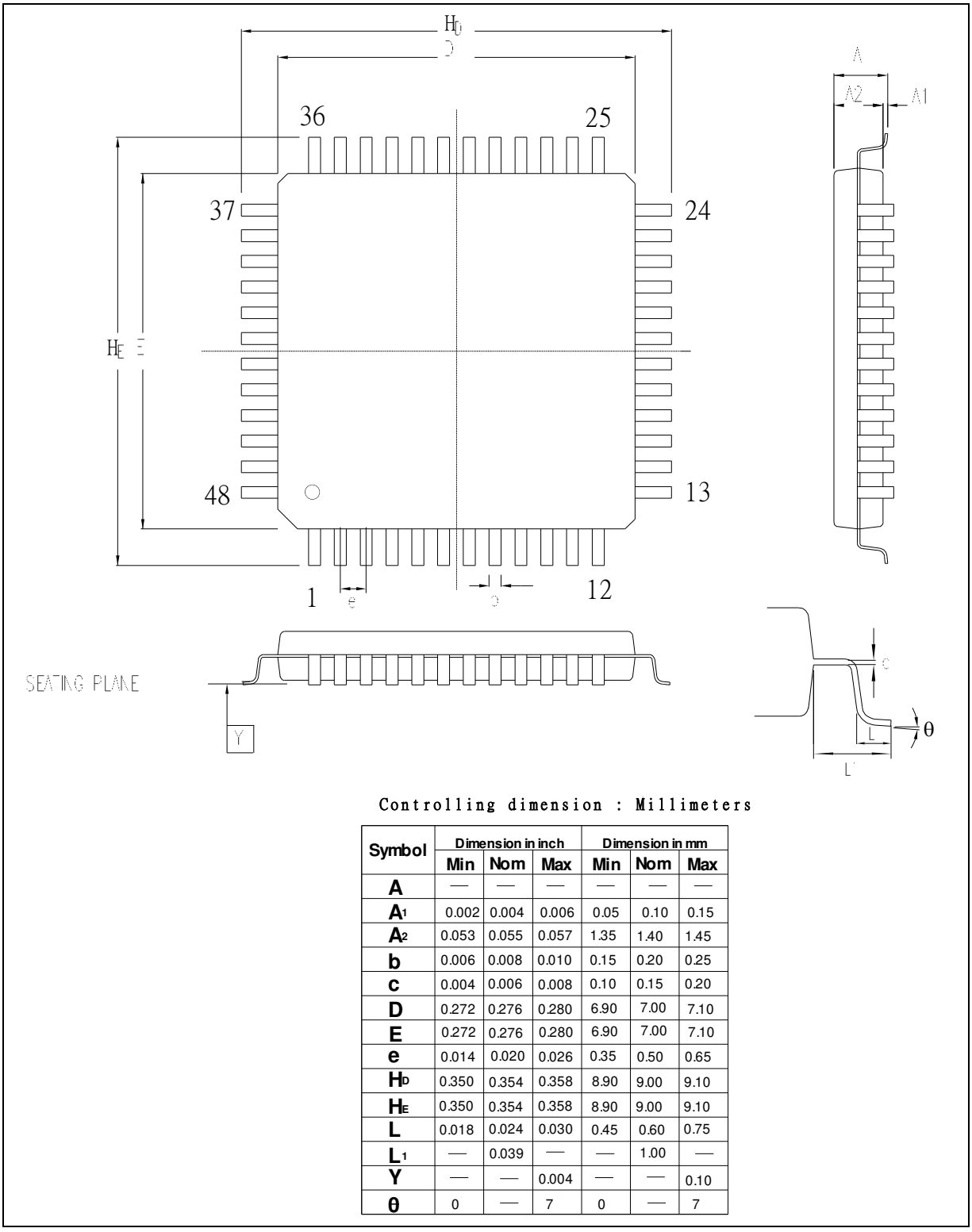
8.2 LQFP 64S (7x7x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



8.3 LQFP 48L (7x7x1.4mm footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

9 REVISION HISTORY

Date	Revision	Description
2015.06.11	1.00	1. Preliminary version.
2016.07.31	1.01	1. Added “Flash DC Electrical Characteristics” in section 7.5.
2016.11.02	1.02	1. Updated OPA and ADC item in 4.1.1 selection guide.

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