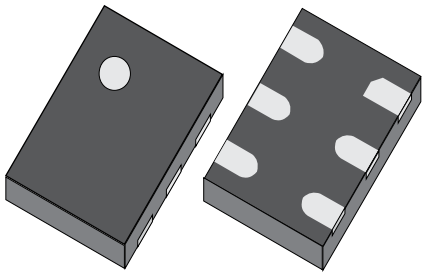
ECMF02-2AMX6

Common mode filter with ESD protection for USB 2.0 and MIPI D-PHY/MDDI interface

Datasheet - production data



QFN-6L

Features

- High common mode attenuation:
  - -34 dB at 900 MHz
  - -20 dB between 800 MHz and 2.2 GHz
- Large bandwidth: 1.7 GHz
- Very low PCB space consumption
- Thin package: 0.55 mm max.
- RoHS package
- High reduction of parasitic elements through integration

Complies with the following standards

- IEC 61000-4-2 (exceeds level 4)
  - ±15 kV (air discharge)
  - ±8 kV (contact discharge)

Applications

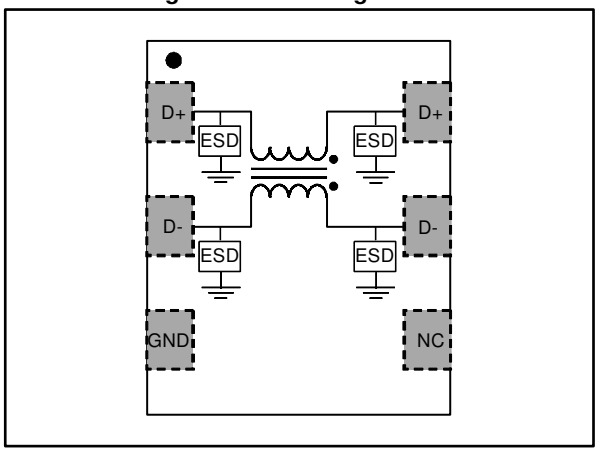
- Mobile phones
- Notebook, laptop
- Portable devices
- PND

Description

The device is a highly integrated common mode filter designed to suppress EMI/RFI common mode noise on high speed differential serial buses like MIPI D-PHY, MDDI or USB 2.0.

Also it can protect and filter one differential lane.

Figure 1: Pin configuration



1 Characteristics

Table 1: Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2: Contact discharge Air discharge	 8 20	kV
I_{DC}	Maximum DC current		200	mA
T_j	Maximum junction temperature range		-55 to +125	°C
T_{stg}	Storage temperature range		-55 to +150	
T_L	Maximum temperature for soldering during 10 s		260	

Figure 2: Electrical characteristics (definitions)

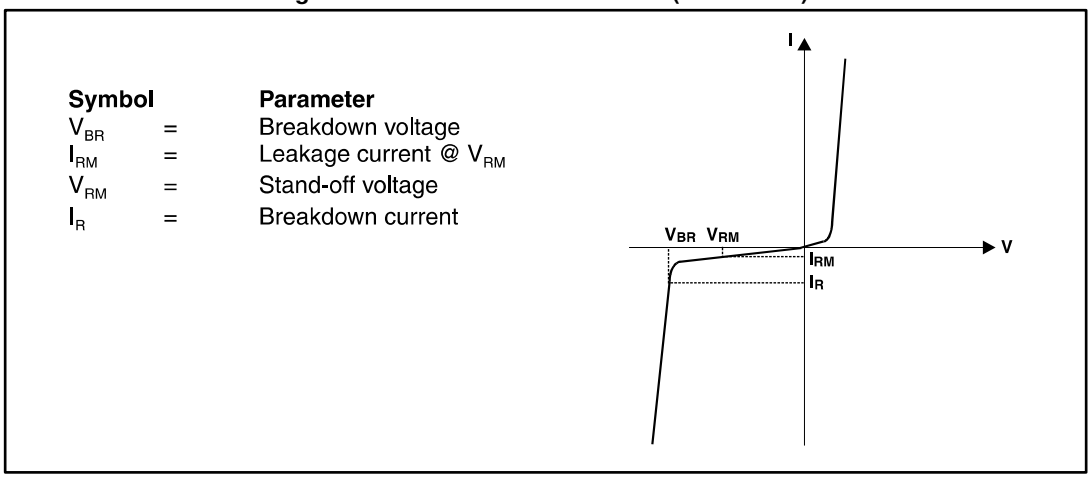


Table 2: Electrical characteristics (T_{amb} = 25 °C)

Symbol	Test condition	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6			V
I_{RM}	V_{RM} = 1.5 V per line			100	nA
R_{DC}	DC serial resistance		1.8	2.5	Ω

Compliant with USB 2.0 high speed sync field test (150 mV diff).

1.1 Characteristics (curves)

Figure 3: Differential insertion losses ($Z_{0\ diff}$ = 100 Ω)

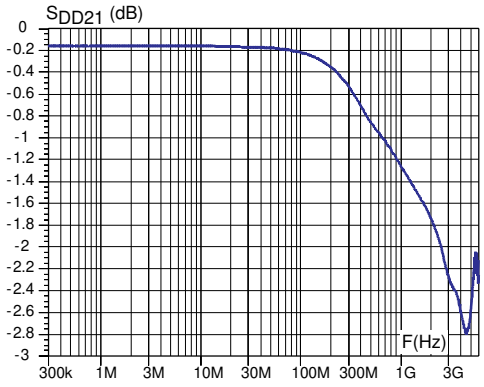


Figure 4: Differential insertion losses ($Z_{0\ diff}$ = 90 Ω)

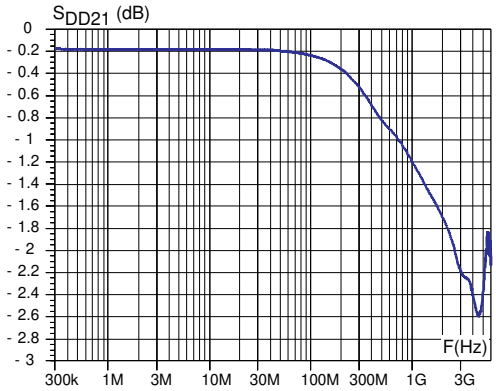


Figure 5: Common mode attenuation ($Z_{0\ com}$ = 50 Ω)

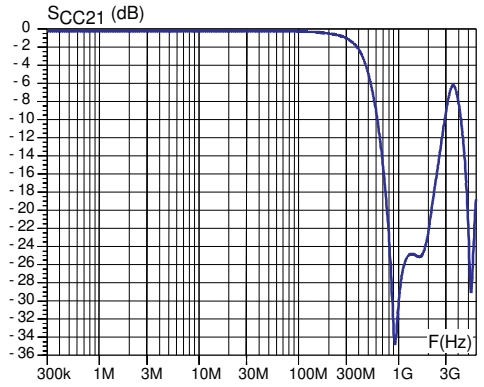


Figure 6: Common mode attenuation ($Z_{0\ com}$ = 45 Ω)

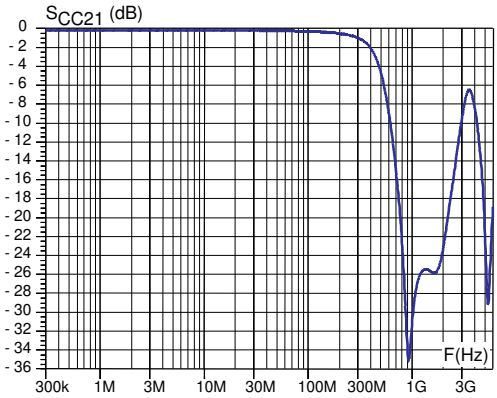


Figure 7: Differential return loss ($Z_{0\ diff}$ = 100 Ω)

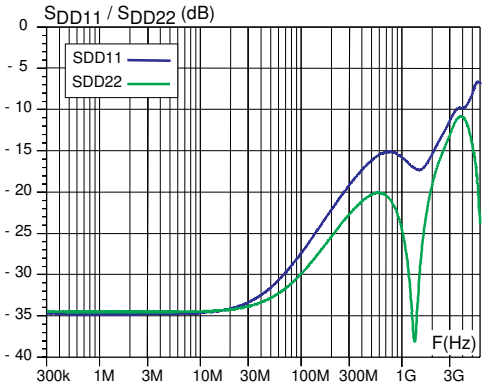


Figure 8: Differential (Z_{DD21}) and common mode (Z_{CC21}) impedance versus frequency

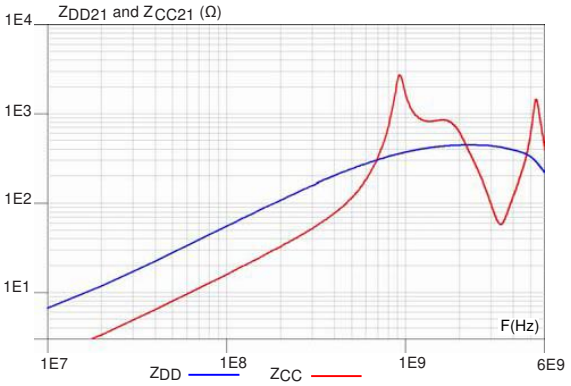


Figure 9: ESD response to IEC 61000-4-2 (+8 kV contact discharge)

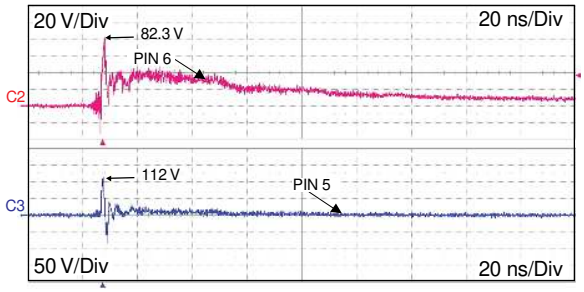


Figure 10: ESD response to IEC 61000-4-2 (-8 kV contact discharge)

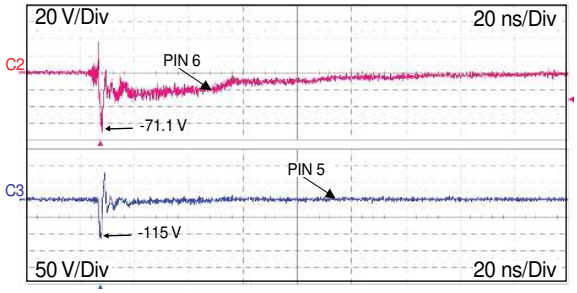


Figure 11: Low power pulse response

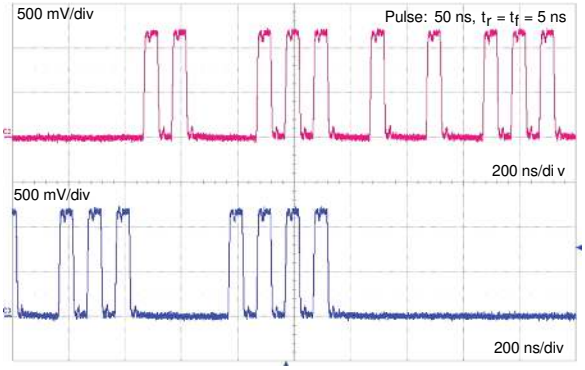


Figure 12: USB 2.0 HSync measurement result

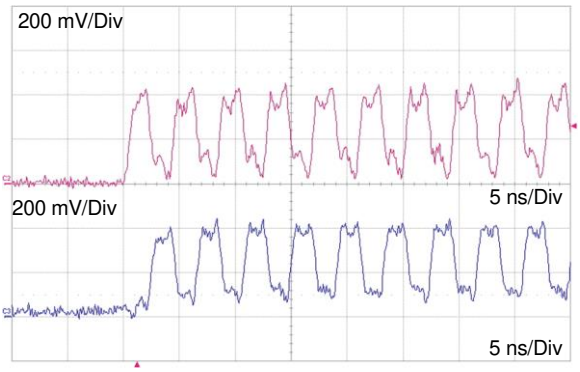
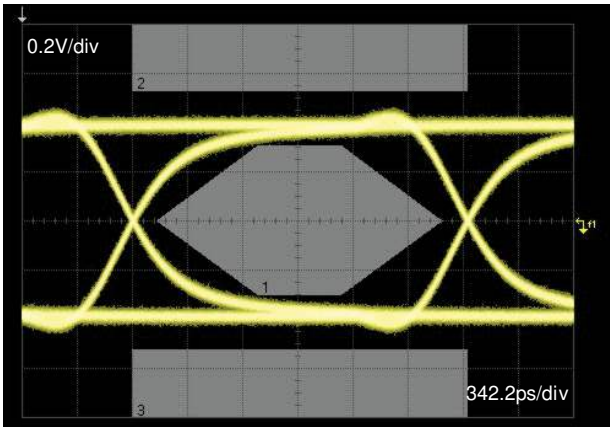


Figure 13: USB 2.0 eye diagram, mask T1



2 Application schematics

Figure 14: MIPI D-PHY

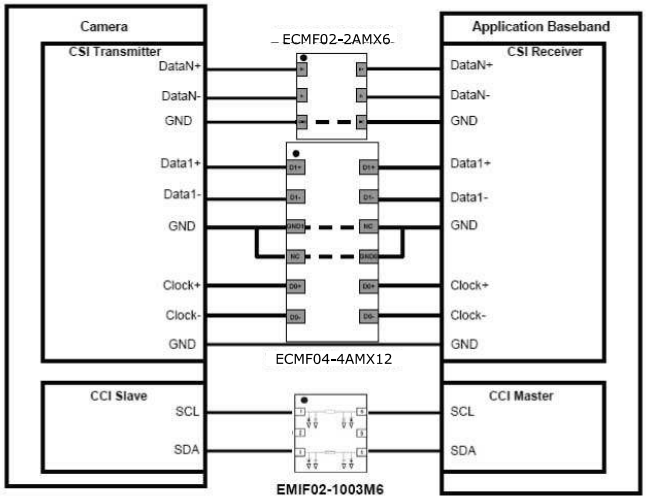
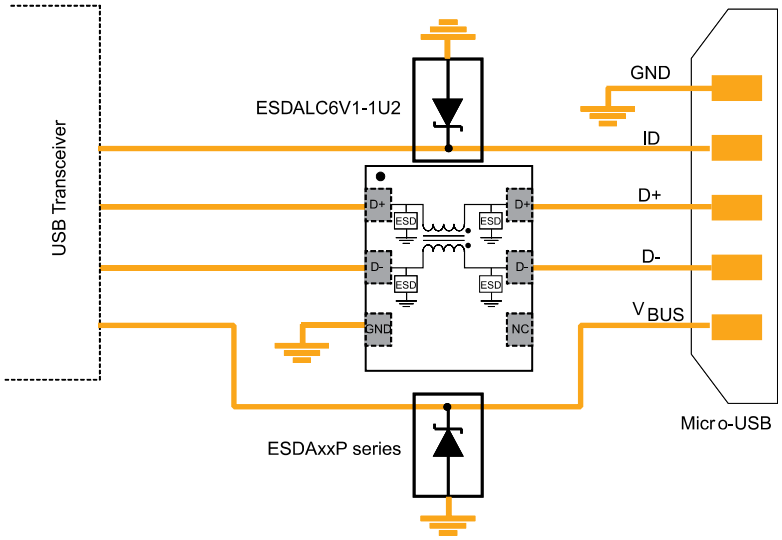


Figure 15: USB 2.0



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

3.1 QFN-6L package information

Figure 16: QFN-6L package outline

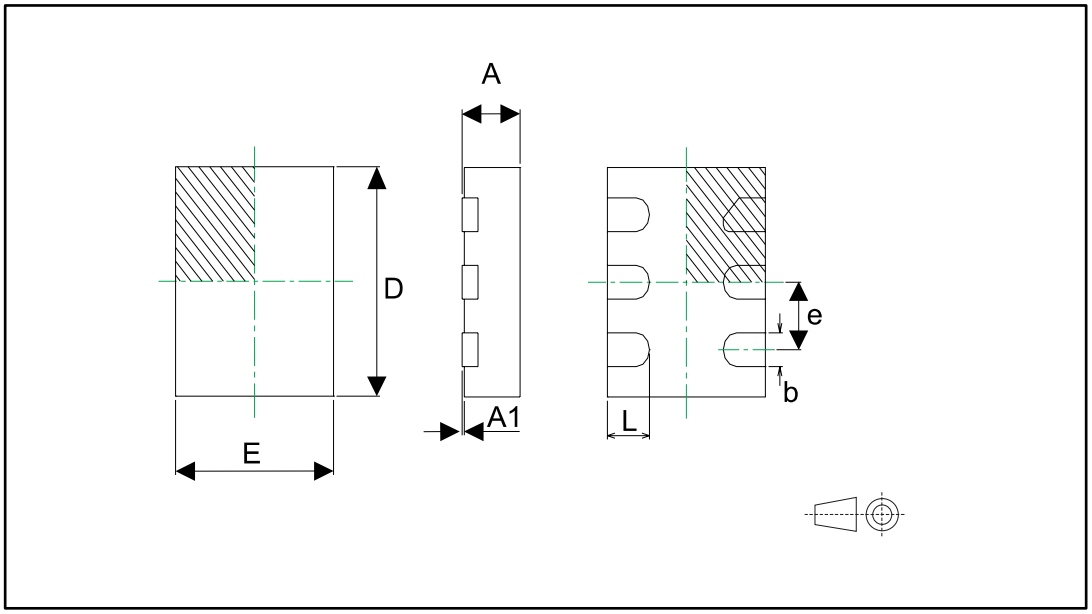


Table 3: QFN-6L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.00	0.0008	0.0009
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.65	1.70	1.75	0.065	0.067	0.069
E	1.45	1.50	1.55	0.057	0.059	0.061
e	0.45	0.50	0.55	0.018	0.020	0.022
L	0.30	0.40	0.50	0.012	0.016	0.020

Figure 17: Footprint recommendations, dimensions in mm (inches)

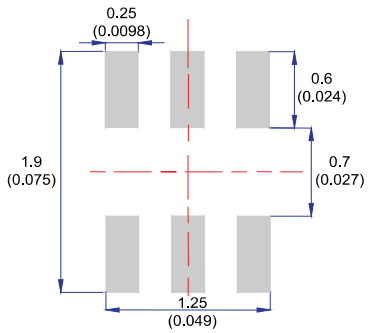
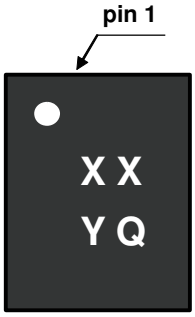
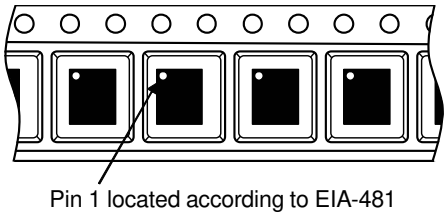


Figure 18: Marking layout



XX : Marking
Y : Year
Q : Quarter

Figure 19: Package orientation in reel



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Figure 20: Tape and reel orientation

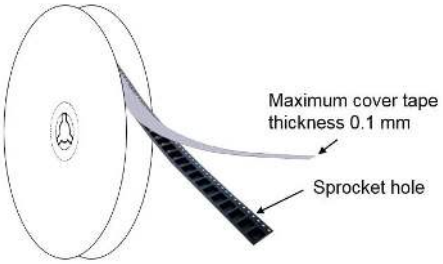


Figure 21: Reel dimensions in mm

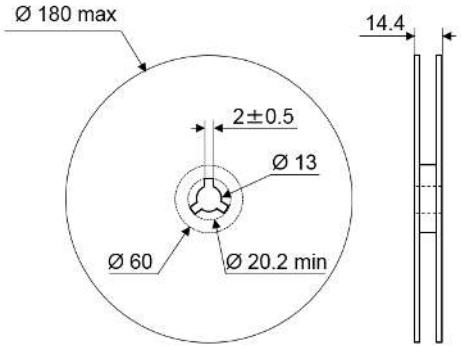


Figure 22: Inner box dimension definition in mm

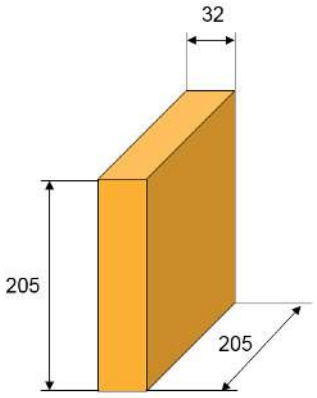
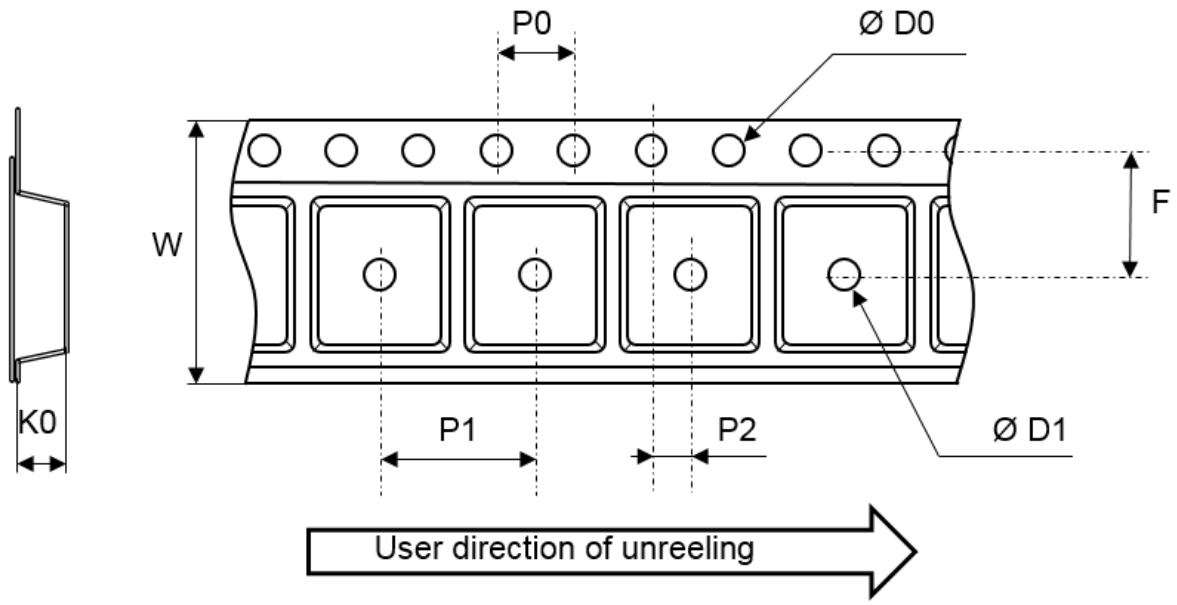


Figure 23: Tape dimension definitions



Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 4: Tape mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
P0	3.9	4.0	4.1
P1	3.9	4.0	4.1
P2	1.95	2	2.05
Ø D0	1.5	1.55	1.6
Ø D1	1		
F	3.4	3.5	3.6
K0	0.65	0.7	0.75
W	7.7	8	8.3

4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).
2. General design rule
   a. Stencil thickness (T) = 75 ~ 125 µm
   b. Aspect ratio = $\frac{W}{T} \geq 1.5$
   c. Aspect area = $\frac{L \times W}{2T(L+W)} \geq 0.66$
3. Reference design
   a. Stencil opening thickness: 100 µm
   b. Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 24: Recommended stencil window position

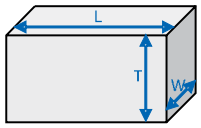
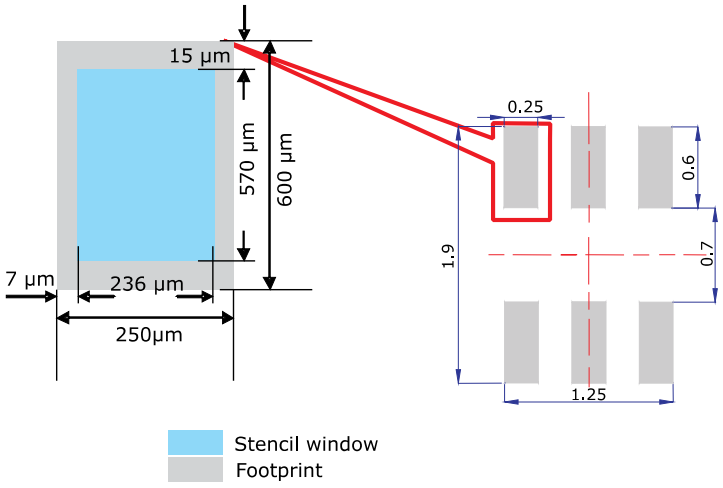


Figure 25: Recommended stencil window position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

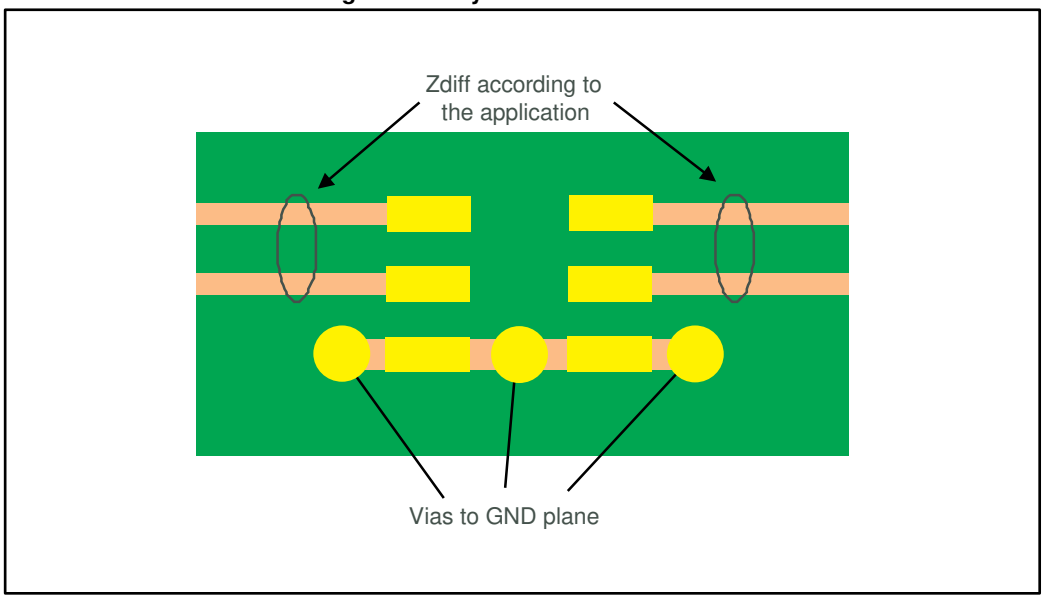
4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

4.5 Layout recommendation

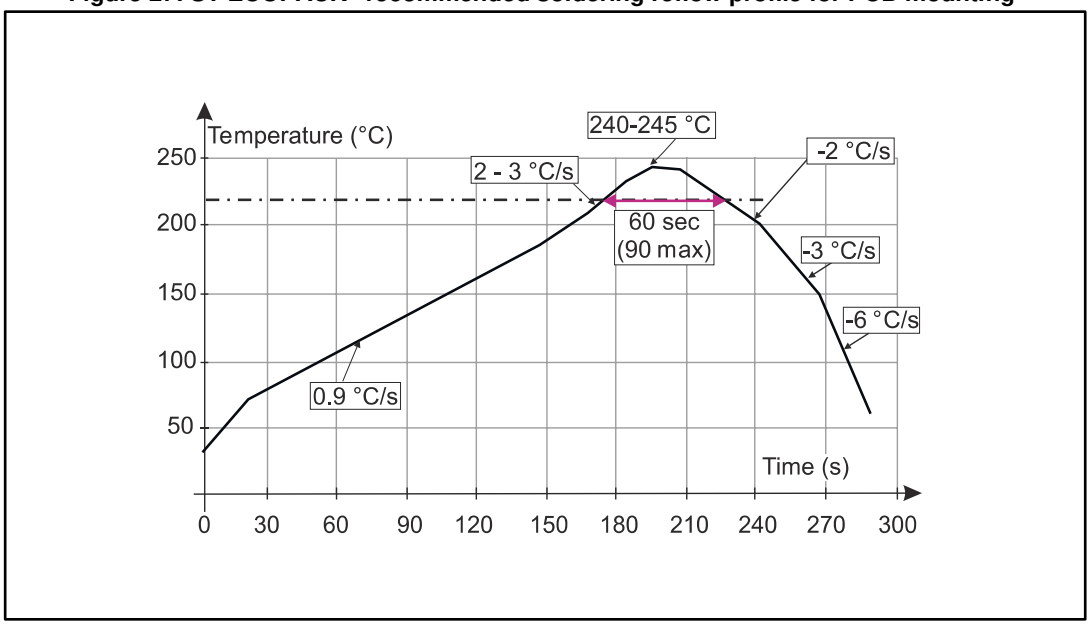
Connection to PCB GND must be as short as possible to ensure ESD remaining voltage and S_{CC21} performance.

Figure 26: Layout recommendation



4.6 Reflow profile

Figure 27: ST ECOPACK® recommended soldering reflow profile for PCB mounting



Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

5 Ordering information

Figure 28: Ordering information scheme

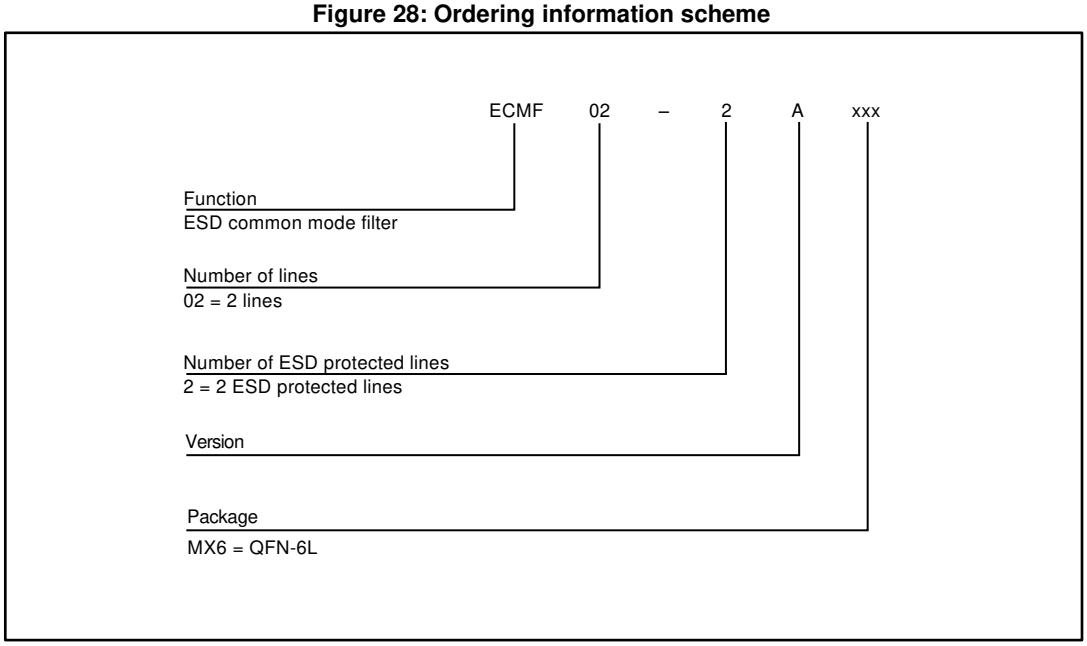


Table 5: Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ECMF02-2AMX6	KD(1)	QFN-6L	3.35 mg	3000	Tape and reel 7"

Notes:

(1)The marking can be rotated by 90° to differentiate assembly location

6 Revision history

Table 6: Document revision history

Date	Revision	Changes
10-Aug-2010	1	Initial release.
28-Jun-2011	2	Added *Complies with the following standards:*, and Air discharge parameter in *Table 1*. Removed Figure 6. Sdd41 / Sdd23 inter-lane differential cross-coupling measurements.
01-Mar-2017	3	Updated marking in *Figure 17* and *Figure 18* and inserted *Figure 9*. Removed Figure 11 and Figure 14. Updated cover page, *Section 3.1: "QFN-6L package information"*, *Section 1: "Characteristics"* and *Table 5: "Ordering information"*.

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