19-3570; Rev 1; 6/05

Low-Cost, 144MHz, Dual/Triple Op Amps with ±15kV ESD Protection

General Description

The MAX4030E/MAX4031E unity-gain stable op amps combine high-speed performance, rail-to-rail outputs, and ±15kV ESD protection. Targeted for applications where an input or an output is exposed to the outside world, such as video and communications, these devices are compliant with International ESD Standards: ±15kV IEC 1000-4-2 Air-Gap Discharge, ±8kV IEC 1000-4-2 Contact Discharge, and the ±15kV Human Body Model.

The MAX4030E/MAX4031E operate from a single 5V supply and consume only 12mA of quiescent supply current per amplifier while achieving a 144MHz -3dB bandwidth, 20MHz 0.1dB gain flatness, and a 115V/µs slew rate. The MAX4031E provides individual shutdown control for each of the amplifiers.

The dual MAX4030E is available in 8-pin µMAX® and SO packages, and the triple MAX4031E is available in 14-pin TSSOP and SO packages. All devices are specified over the -40°C to +85°C extended temperature range.

Applications

Set-Top Boxes

Standard Definition Television (SDTV)

Enhanced Television (ETV)

High-Definition Television (HDTV)

Notebooks

Projectors

Security Video Systems

Camcorders

Digital Still Cameras

Portable DVD Players

µMAX is a registered trademark of Maxim Integrated Products, Inc.

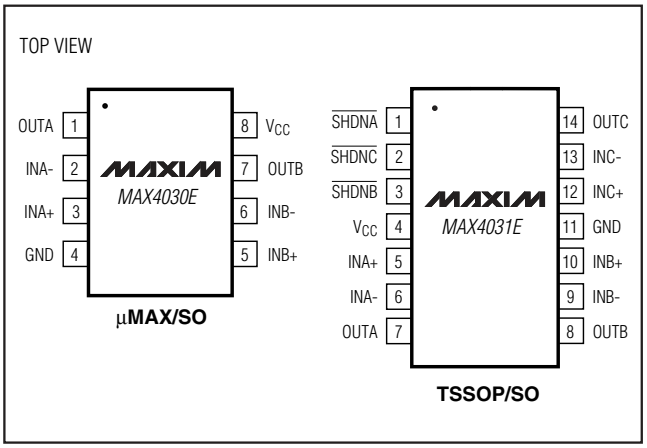
Features

- **ESD-Protected Video Inputs and Outputs**
  - **±15kV – Human Body Model**
  - **±8kV – IEC 1000-4-2 Contact Discharge**
  - **±15kV – IEC 1000-4-2 Air-Gap Discharge**
- **5V Single-Supply Operation**
- **0.1µA Low-Power Shutdown Mode (MAX4031E)**
- **Input Common-Mode Range Extends to Ground**
- **2VP-P Large-Signal -3dB BW > 50MHz**
- **Directly Drives 150Ω Loads**
- **Low Differential Gain/Phase: 0.2%/0.2°**
- **-40°C to +85°C Extended Temperature Range**
- **Compact 8-Pin µMAX and 14-Pin TSSOP Packages**

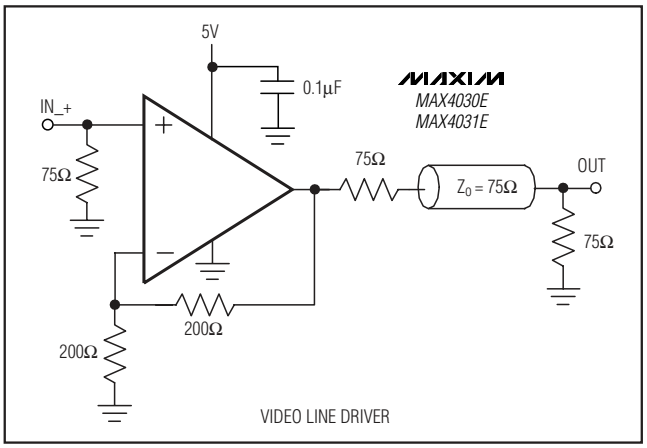
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4030EEUA	-40°C to +85°C	8 µMAX
MAX4030EESA	-40°C to +85°C	8 SO
MAX4031EEUD	-40°C to +85°C	14 TSSOP
MAX4031EESD	-40°C to +85°C	14 SO

Pin Configurations



Typical Operating Circuit



Low-Cost, 144MHz, Dual/Triple Op Amps with ±15kV ESD Protection

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
V_{CC} .....-0.3V to +6V
IN_-, IN_+, OUT_, $\overline{SHDN\_}$ .....-0.3V to (V_{CC} + 0.3V)
Current into IN_-, IN_+, $\overline{SHDN}$.....±20mA
Output Short-Circuit Duration to V_{CC} or GND.....Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.5mW/°C above +70°C) 362mW
8-Pin SO (derate 5.9mW/°C above +70°C).....471mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
14-Pin SO (derate 8.3mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{CM} = 0V, $V_{OUT\_}$ = V_{CC}/2, $\overline{SHDN\_}$ = V_{CC}, R_L = ∞ to V_{CC}/2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{CC}	Guaranteed by PSRR		4.5		5.5	V
Quiescent Current (per Amplifier)	I_{CC}				12	22	mA
Shutdown Current (per Amplifier)	I_{SHDN}	$\overline{SHDN\_}$ = GND (MAX4031E)			0.1	10	µA
Input Common-Mode Voltage	V_{CM}	Guaranteed by CMRR		0		V_{CC} - 2.25	V
Input Offset Voltage	V_{OS}	T_A = +25°C			5	13	mV
		T_A = -40°C to +85°C				26	
Input Offset Voltage Matching	ΔV_{OS}				2.6		mV
Input Offset Voltage Tempco	TC_{VOS}				31		µV/°C
Input Bias Current	I_B				0.01	1	µA
Input Offset Current	I_{OS}				0.01		µA
Input Resistance	R_{IN}				1		GΩ
Common-Mode Rejection Ratio	CMRR	GND ≤ V_{CM} ≤ V_{CC} - 2.25V		50	70		dB
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{CC} ≤ 5.5V		40	60		dB
Open-Loop Gain	A_{VOL}	0.5V ≤ $V_{OUT\_}$ ≤ 4.5V, R_L = 2kΩ to V_{CC}/2			80		dB
		0.6V ≤ $V_{OUT\_}$ ≤ 4.4V, R_L = 150Ω to V_{CC}/2		50	70		
		0.4V ≤ $V_{OUT\_}$ ≤ 3.5V, R_L = 150Ω to GND		50	70		
Output Voltage Swing	$V_{OUT\_}$	R_L = 2kΩ to V_{CC}/2	V_{CC} - V_{OH}		0.05		V
			V_{OL} - GND		0.05		
		R_L = 150Ω to V_{CC}/2	V_{CC} - V_{OH}		0.15	0.4	
			V_{OL} - GND		0.15	0.4	
		R_L = 150Ω to GND	V_{CC} - V_{OH}		0.3	0.8	
			V_{OL} - GND		0.01	0.05	
Output Short-Circuit Current	I_{SC}	Sinking or sourcing			±100		mA
$\overline{SHDN\_}$ Logic Threshold	V_{IL}	MAX4031E				0.8	V
	V_{IH}	MAX4031E		2.0			
$\overline{SHDN\_}$ Logic Input Current	I_{IL}	$\overline{SHDN\_}$ = GND (MAX4031E)			0.10	10	µA
	I_{IH}	$\overline{SHDN\_}$ = V_{CC} (MAX4031E)			0.10	10	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, V_{CM} = 0V, $V_{OUT\_}$ = V_{CC}/2, $\overline{SHDN\_}$ = V_{CC}, R_L = ∞ to V_{CC}/2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Disabled Output Leakage Current	I_{OUT_SH}	$\overline{SHDN\_}$ = GND (MAX4031E)		0.1	10	µA
ESD Protection Voltage (Note 2)		Human Body Model		±15		kV
		IEC 1000-4-2 Contact Discharge		±8		
		IEC 1000-4-2 Air-Gap Discharge		±15		

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{CM} = 1.5V, R_L = 150Ω to GND, $\overline{SHDN\_}$ = V_{CC}, $A_{VCL\_}$ = +2V/V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{SS}	$V_{OUT\_}$ = 100mV_{P-P}, A_{VCL}= +1V/V		144		MHz
		$V_{OUT\_}$ = 100mV_{P-P}, A_{VCL}= +2V/V		53		
Large-Signal -3dB Bandwidth	BW_{LS}	$V_{OUT\_}$ = 2V_{P-P}, A_{VCL}= +1V/V		52		MHz
		$V_{OUT\_}$ = 2V_{P-P}, A_{VCL}= +2V/V		40		
Small-Signal 0.1dB Gain Flatness	$BW_{0.1dBSS}$	$V_{OUT\_}$ = 100mV_{P-P}, A_{VCL}= +1V/V		20		MHz
		$V_{OUT\_}$ = 100mV_{P-P}, A_{VCL}= +2V/V		10		
Large-Signal 0.1dB Gain Flatness	$BW_{0.1dBLS}$	$V_{OUT\_}$ = 2V_{P-P}, A_{VCL}= +1V/V		20		MHz
		$V_{OUT\_}$ = 2V_{P-P}, A_{VCL}= +2V/V		9		
Slew Rate	SR	$V_{OUT\_}$ = 2V step		115		V/µs
Settling Time to 0.1%	t_S	$V_{OUT\_}$ = 2V step		40		ns
Channel-to-Channel Isolation	CH_{ISO}	f = 4.43MHz		65		dB
Differential Phase Error	DP	NTSC, R_L = 150Ω to GND, A_{VCL} = +2V/V		0.2		Degrees
Differential Gain Error	DG	NTSC, R_L = 150Ω to GND, A_{VCL} = +2V/V		0.2		%
Input Capacitance	C_{IN}			8		pF
Capacitive-Load Stability		No sustained oscillations		200		pF
Output Impedance	Z_{OUT}	f = 4.43MHz		2		Ω
Enable Time	t_{ON}	$V_{IN\_}$ = 1V (MAX4031E)		2		µs
Disable Time	t_{OFF}	$V_{IN\_}$ = 1V (MAX4031E)		0.15		µs

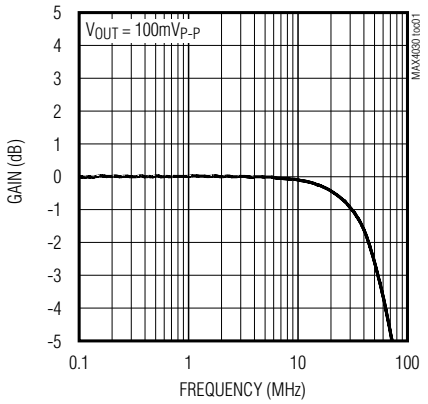
Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: ESD protection is specified for test point A and test point B only (Figure 7).

Low-Cost, 144MHz, Dual/Triple Op Amps with ±15kV ESD Protection

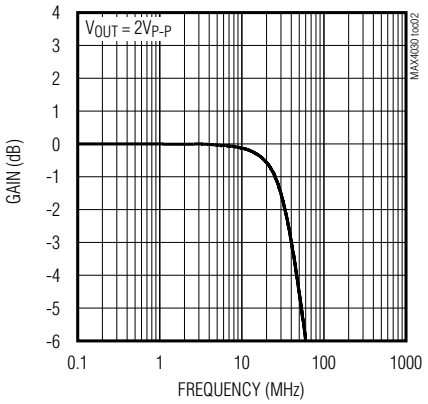
Typical Operating Characteristics

(V_{CC} = 5V, V_{CM} = 1.5V, A_{VCL}= +2V/V, R_L= 150Ω to V_{CC}/2, T_A = +25°C, unless otherwise noted.)

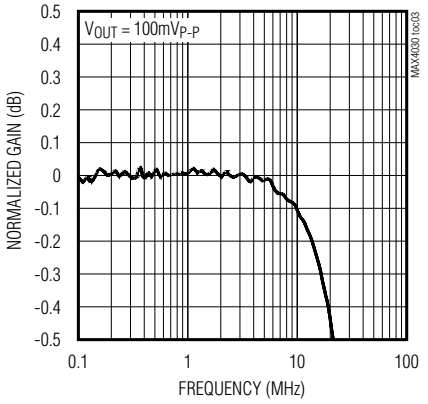
SMALL-SIGNAL GAIN vs. FREQUENCY



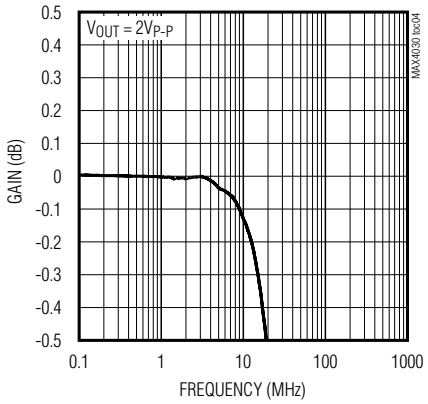
LARGE-SIGNAL GAIN vs. FREQUENCY



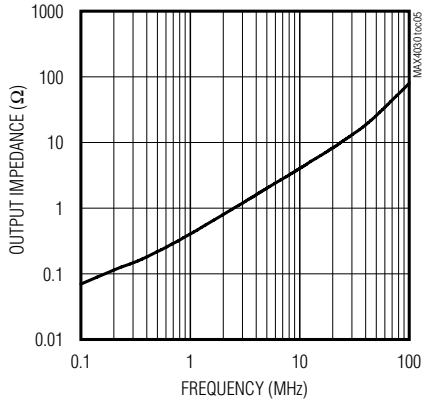
SMALL-SIGNAL GAIN FLATNESS vs. FREQUENCY



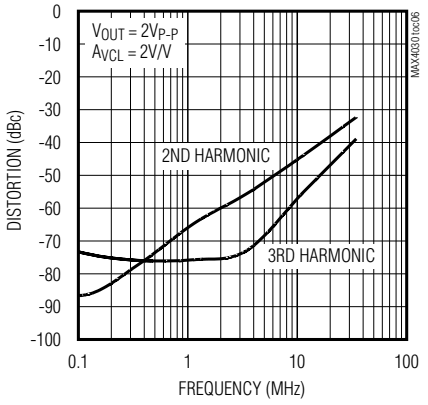
LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



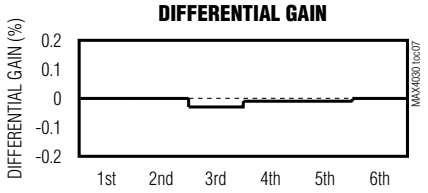
OUTPUT IMPEDANCE vs. FREQUENCY



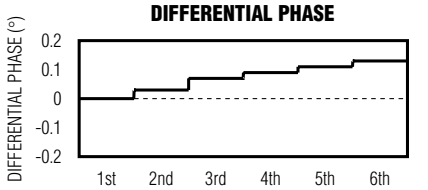
DISTORTION vs. FREQUENCY



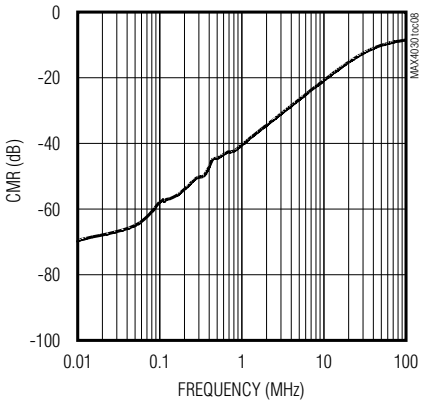
DIFFERENTIAL GAIN



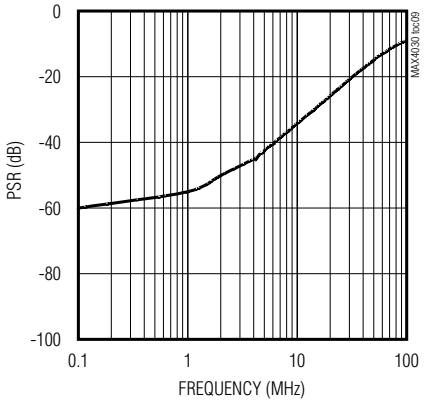
DIFFERENTIAL PHASE



COMMON-MODE REJECTION vs. FREQUENCY



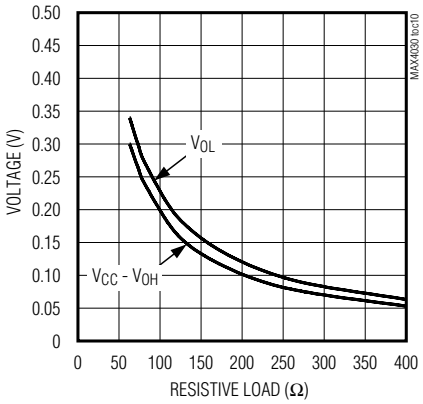
POWER-SUPPLY REJECTION vs. FREQUENCY



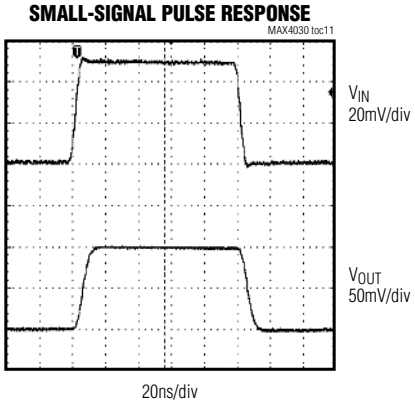
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{CM} = 1.5V, A_{VCL}= +2V/V, R_L= 150Ω to V_{CC}/2, T_A = +25°C, unless otherwise noted.)

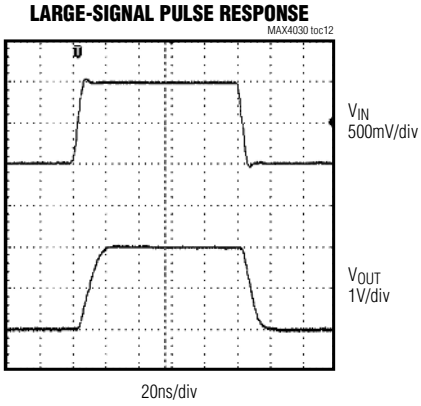
OUTPUT VOLTAGE SWING vs. RESISTIVE LOAD



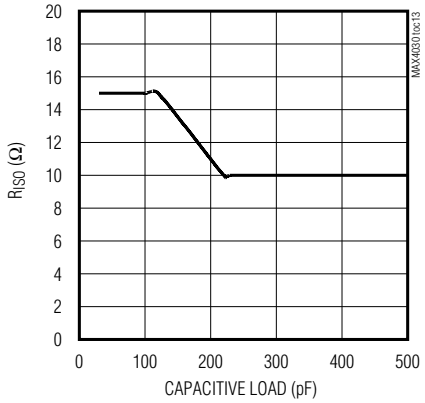
SMALL-SIGNAL PULSE RESPONSE



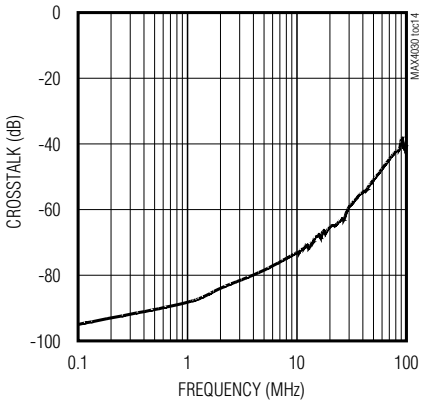
LARGE-SIGNAL PULSE RESPONSE



ISOLATION RESISTANCE vs. CAPACITIVE LOAD



CROSSTALK vs. FREQUENCY



Low-Cost, 144MHz, Dual/Triple Op Amps with ±15kV ESD Protection

Pin Description

PIN		NAME	FUNCTION
MAX4030E	MAX4031E		
1	7	OUTA	Amplifier A Output
2	6	INA-	Amplifier A Inverting Input
3	5	INA+	Amplifier A Noninverting Input
4	11	GND	Ground
5	10	INB+	Amplifier B Noninverting Input
6	9	INB-	Amplifier B Inverting Input
7	8	OUTB	Amplifier B Output
8	4	V_{CC}	Positive Power Supply. Bypass V_{CC} to GND with a 0.1µF capacitor.
—	1	$\overline{SHDNA}$	Amplifier A Shutdown Input. Connect $\overline{SHDNA}$ high to enable amplifier A.
—	2	$\overline{SHDNC}$	Amplifier C Shutdown Input. Connect $\overline{SHDNC}$ high to enable amplifier C.
—	3	$\overline{SHDNB}$	Amplifier B Shutdown Input. Connect $\overline{SHDNB}$ high to enable amplifier B.
—	12	INC+	Amplifier C Noninverting Input
—	13	INC-	Amplifier C Inverting Input
—	14	OUTC	Amplifier C Output

Detailed Description

The MAX4030E/MAX4031E dual/triple, 5V operational amplifiers achieve 115V/µs slew rates and 144MHz bandwidths. High ±15kV ESD protection at video inputs and outputs guards against unexpected discharge. Excellent harmonic distortion and differential gain/phase performance make these amplifiers an ideal choice for a wide variety of video and RF signal-processing applications.

Ground-Sensing Inputs

The MAX4030E/MAX4031E input stage can sense common-mode voltages from ground to within 2.25V of the positive supply.

Rail-to-Rail Outputs

The MAX4030E/MAX4031E rail-to-rail outputs can swing to within 100mV of each supply because local feedback around the output stage ensures low open-loop output impedance, reducing gain sensitivity to load variations.

Shutdown (MAX4031E Only)

The MAX4031E offers individual shutdown control for each amplifier. Drive $\overline{SHDN}$_ low to shut down the amplifier. In shutdown, the amplifier output impedance is high impedance.

Applications Information

Choosing Resistor Values

Unity-Gain Configuration

The MAX4030E/MAX4031E are internally compensated for unity gain. When configured for unity gain, a 24Ω resistor (R_F) in series with the feedback path optimizes AC performance. This resistor improves AC response by reducing the Q of the parallel LC circuit formed by the parasitic feedback capacitance and lead inductance.

Video Line Driver

The MAX4030E/MAX4031E are low-power, voltage-feedback amplifiers featuring bandwidths up to 40MHz and 0.1dB gain flatness to 9MHz. They are designed to minimize differential-gain error and differential-phase error to 0.2% and 0.2°, respectively. They have a 40ns settling time to 0.1%, 110V/µs slew rates, and output-current-drive capability of up to 50mA, making them ideal for driving video loads.

Inverting and Noninverting Configurations

Select the feedback (R_F) and input (R_G) resistor values to fit the gain requirements of the application. Large resistor values increase voltage noise and interact with the amplifier's input and PC board capacitance. This can generate undesirable poles and zeros and

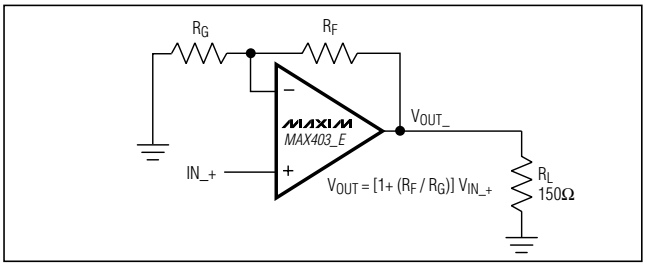


Figure 1. Noninverting Gain Configuration

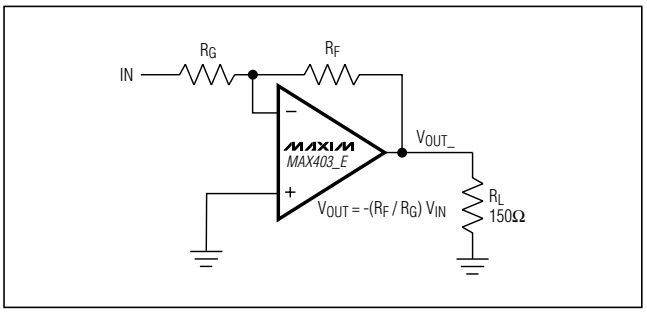


Figure 2. Inverting Gain Configuration

decrease bandwidth or cause oscillations. For example, a noninverting gain-of-two configuration ($R_F = R_G$) using 2kΩ resistors, combined with 4pF of amplifier input capacitance and 1pF of PC board capacitance, cause a pole at 79.6MHz. Since this pole is within the amplifier bandwidth, it jeopardizes stability. Reducing the 2kΩ resistors to 100Ω extends the pole frequency to 1.59GHz, but could limit output swing by adding 200Ω in parallel with the amplifier's load resistor (Figures 1 and 2).

Layout and Power-Supply Bypassing

These amplifiers operate from a single 5V power supply. Bypass V_{CC} to ground with a 0.1µF capacitor as close to V_{CC} as possible. Maxim recommends using microstrip and stripline techniques to obtain full bandwidth. To ensure that the PC board does not degrade the amplifier's performance, design it for a frequency greater than 1GHz. Pay careful attention to inputs and outputs to avoid large parasitic capacitance. Under all conditions observe the following design guidelines:

- Do not use wire-wrap boards. Wire-wrap boards are too inductive.
- Do not use IC sockets. Sockets increase parasitic capacitance and inductance.
- Use surface mount instead of through-hole components for better high-frequency performance.
- Use a PC board with at least two layers. The PC board should be as free from voids as possible.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.

Output Capacitive Loading and Stability

The MAX4030E/MAX4031E are optimized for AC performance and do not drive highly reactive loads, which decreases phase margin and can produce excessive ringing and oscillation. Figure 3 shows a circuit modification that uses an isolation resistor (R_{ISO}) to eliminate this problem. Figure 4 shows a graph of the Optimal Isolation Resistor (R_{ISO}) vs. Capacitive Load. Figure 5 shows how a capacitive load causes excessive peaking of the amplifier's frequency response if the capacitor is not isolated from the amplifier by a resistor. A small isolation resistor (usually 10Ω to 15Ω) placed before the reactive load prevents ringing and oscillation. At higher capacitive loads, the interaction of the load capacitance and the isolation resistor controls the AC performance. Figure 6 shows the effect of a 10Ω isolation resistor on closed-loop response.

ESD Protection

As with all Maxim devices, ESD protection structures are incorporated on all pins to protect against ESD encountered during handling and assembly. Input and output pins of the MAX4030E/MAX4031E have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures enabling these pins to withstand ESD up to ±15kV without damage when placed in the test circuit (Figure 7). The MAX4030E/MAX4031E are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge method specified in IEC 1000-4-2
- ±15kV using the Air-Gap Discharge method specified in IEC 1000-4-2

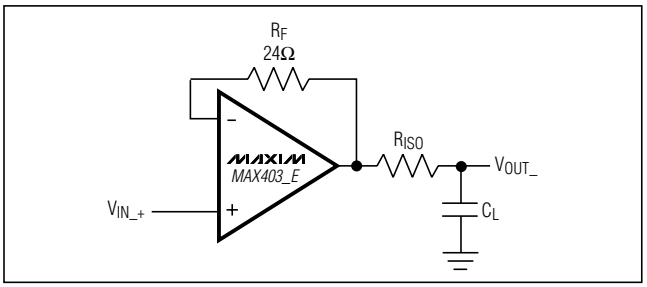


Figure 3. Driving a Capacitive Load Through an Isolation Resistor

Low-Cost, 144MHz, Dual/Triple Op Amps with ±15kV ESD Protection

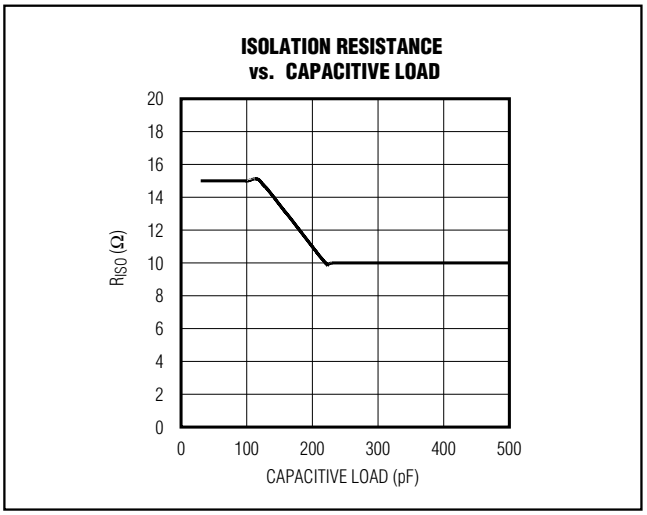


Figure 4. Isolation Resistance vs. Capacitive Load

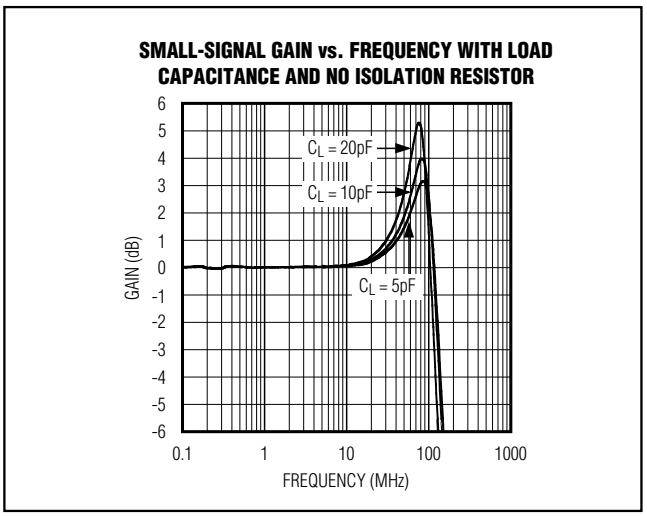


Figure 5. Small-Signal Gain vs. Frequency with Load Capacitance and No Isolation Resistor

Human Body Model

Figure 8 shows the Human Body Model and Figure 9 shows the current waveform it generates when discharged into low impedance. This model consists of a 150pF capacitor charged to the ESD voltage of interest, and then discharged into the test device through a 1.5kΩ resistor.

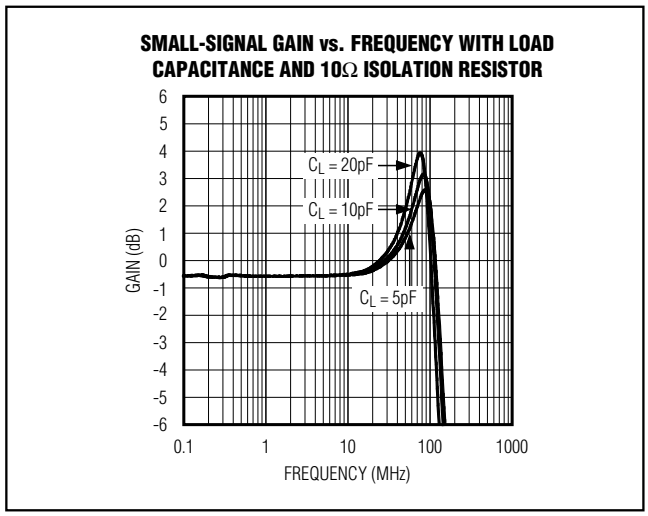


Figure 6. Small-Signal Gain vs. Frequency with Load Capacitance and 10Ω Isolation Resistor

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to ICs. The MAX4030E/MAX4031E enable the design of equipment that meets the highest level (level 4) of IEC 1000-4-2 without the need for additional ESD protection components. The major difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2. Because series resistance is lower in the IEC 1000-4-2 model, the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body. Figure 10 shows the IEC 1000-4-2 model and Figure 11 shows the current waveform for the ±8kV IEC 1000-4-2 level 4 ESD Contact Discharge test. The Air-Gap test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Chip Information

MAX4030E TRANSISTOR COUNT: 271

MAX4031E TRANSISTOR COUNT: 387

PROCESS: BiCMOS

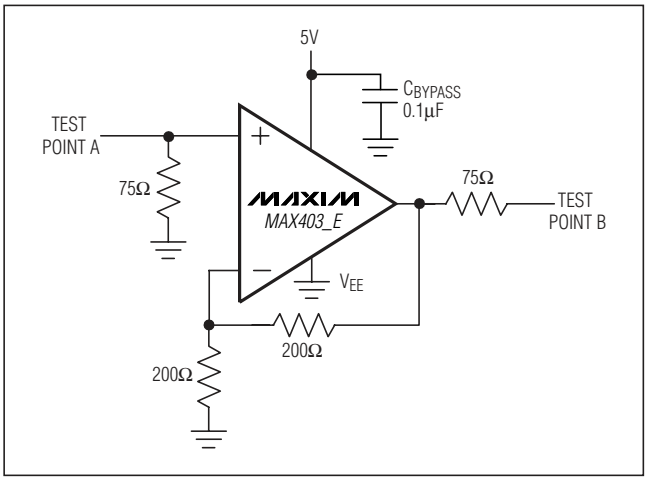


Figure 7. ESD Test Circuit

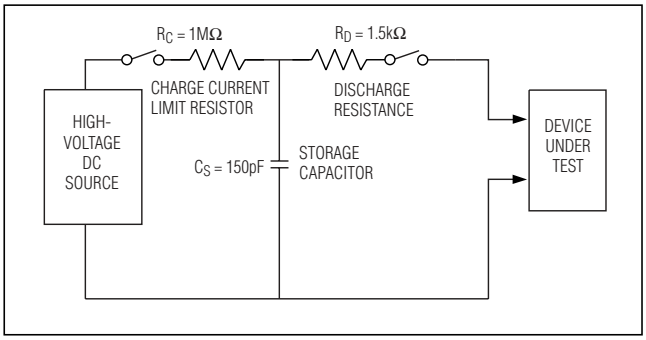


Figure 8. Human Body ESD Model

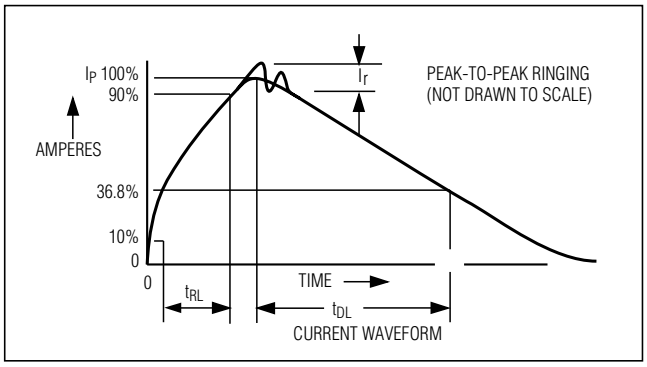


Figure 9. Human Body Current Waveform

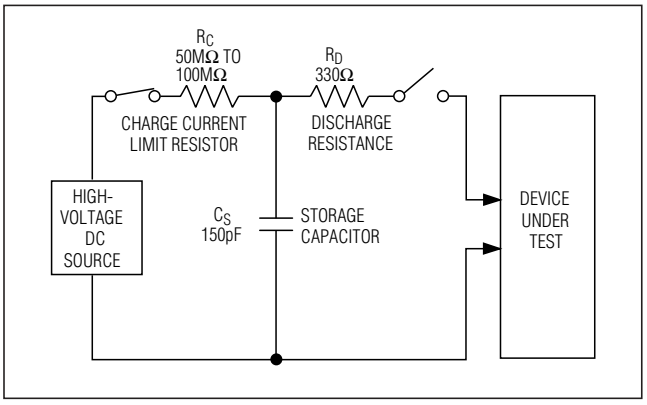


Figure 10. IEC 1000-4-2 ESD Test Model

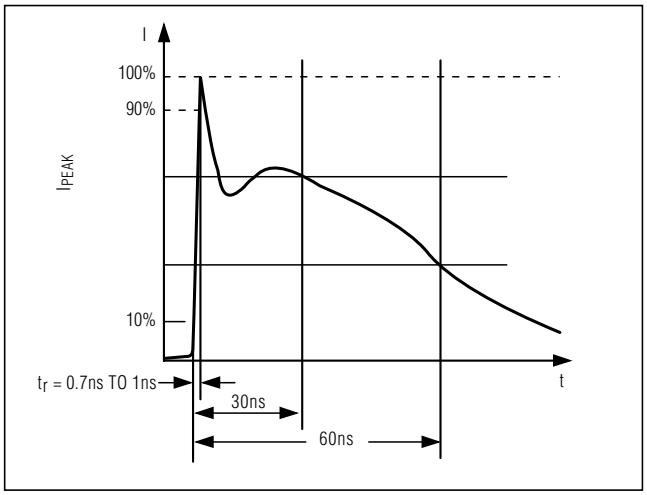


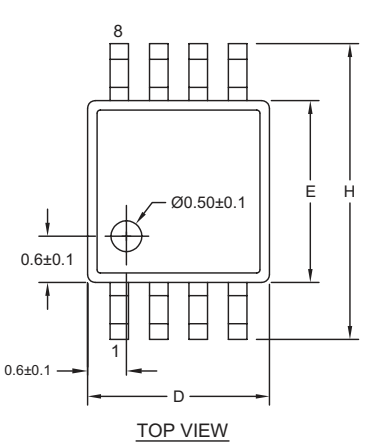
Figure 11. IEC 1000-4-2 ESD Generator Current Waveform

Low-Cost, 144MHz, Dual/Triple Op Amps with ±15kV ESD Protection

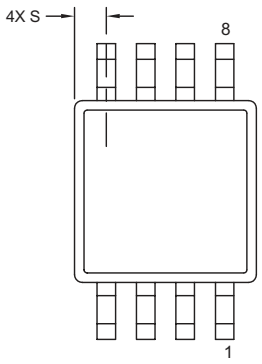
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

8LUMAXD.EPS

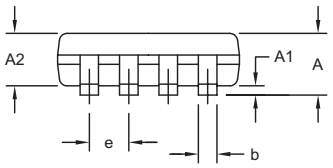


TOP VIEW

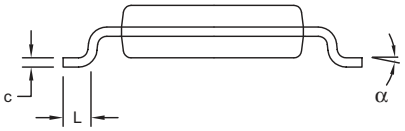


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0∞	6∞	0∞	6∞
S	0.0207 BSC		0.5250 BSC	



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

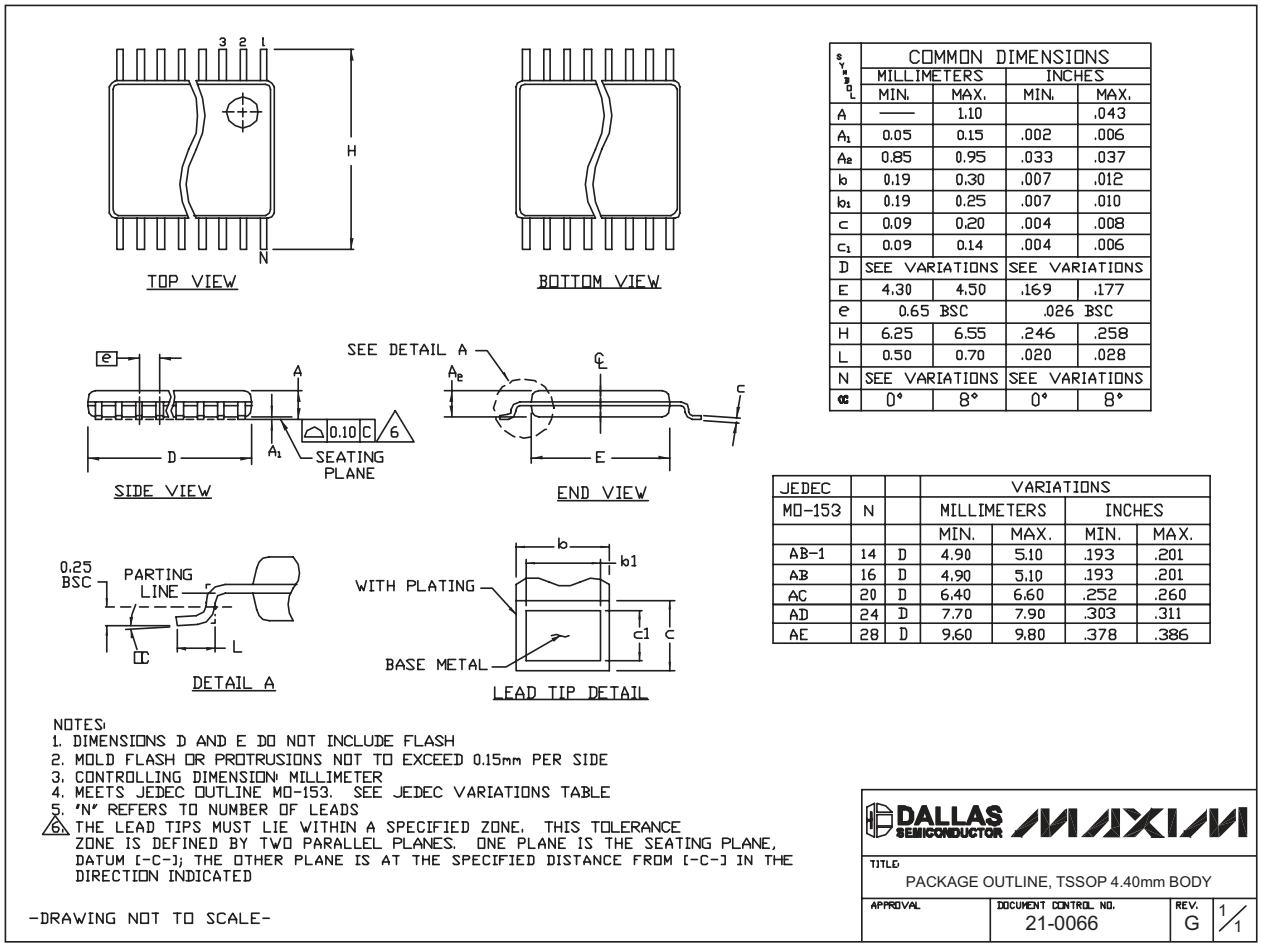
TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0036	J	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	G	1/1

Low-Cost, 144MHz, Dual/Triple Op Amps with ±15kV ESD Protection

Package Information (continued)

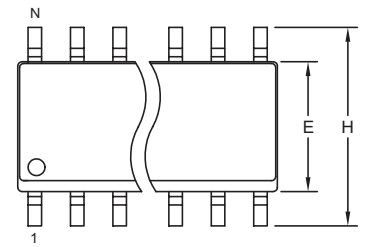
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

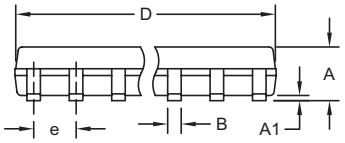
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

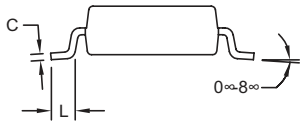
	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



TOP VIEW



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

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