MOSFET

OptiMOS™3 Power-Transistor, 80 V

Features

- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC[1] for target applications
- Halogen-free according to IEC61249-2-21

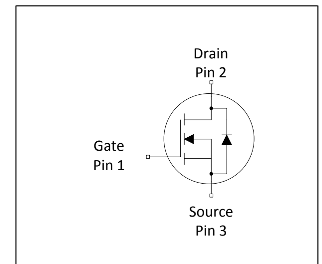


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$	2.8	mΩ
I_D	89	A

Type / Ordering Code	Package	Marking	Related Links
IPA028N08N3 G	PG-TO220-FP	028N08N	-

[1] J-STD20 and JESD22

Table of Contents

Description 1
Maximum ratings 3
Thermal characteristics 3
Electrical characteristics 3
Electrical characteristics diagrams 5
Package Outlines 9
Revision History 10
Trademarks 10
Disclaimer 10

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- -	- -	89 62	A	T_C=25 °C[1] T_C=100 °C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	352	A	T_C=25 °C
Avalanche energy, single pulse[3]	E_{AS}	-	-	1430	mJ	I_D=89 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	42	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.6	K/W	-

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2	2.8	3.5	V	V_{DS}=V_{GS}, I_D=270 μA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	μA	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	1	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	2.4 2.8	2.8 4.2	mΩ	V_{GS}=10 V, I_D=89 A V_{GS}=6 V, I_D=44 A
Gate resistance	R_G	-	2.7	-	Ω	-
Transconductance	g_{fs}	89	178	-	S	$\lvert V_{DS}\rvert>2\lvert I_D\rvert R_{DS(on)max}$, I_D=89 A

[1] Current is limited by package; with an R_{thJC}=0.5K/W in a standard TO-220 package the chip is able
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	10700	14200	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Output capacitance	C_{oss}	-	2890	3840	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	100	-	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	30	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=89 A, R_G=1.6 Ω
Rise time	t_r	-	59	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=89 A, R_G=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	77	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=89 A, R_G=1.6 Ω
Fall time	t_f	-	26	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=89 A, R_G=1.6 Ω

Table 6 Gate charge characteristics[1)]

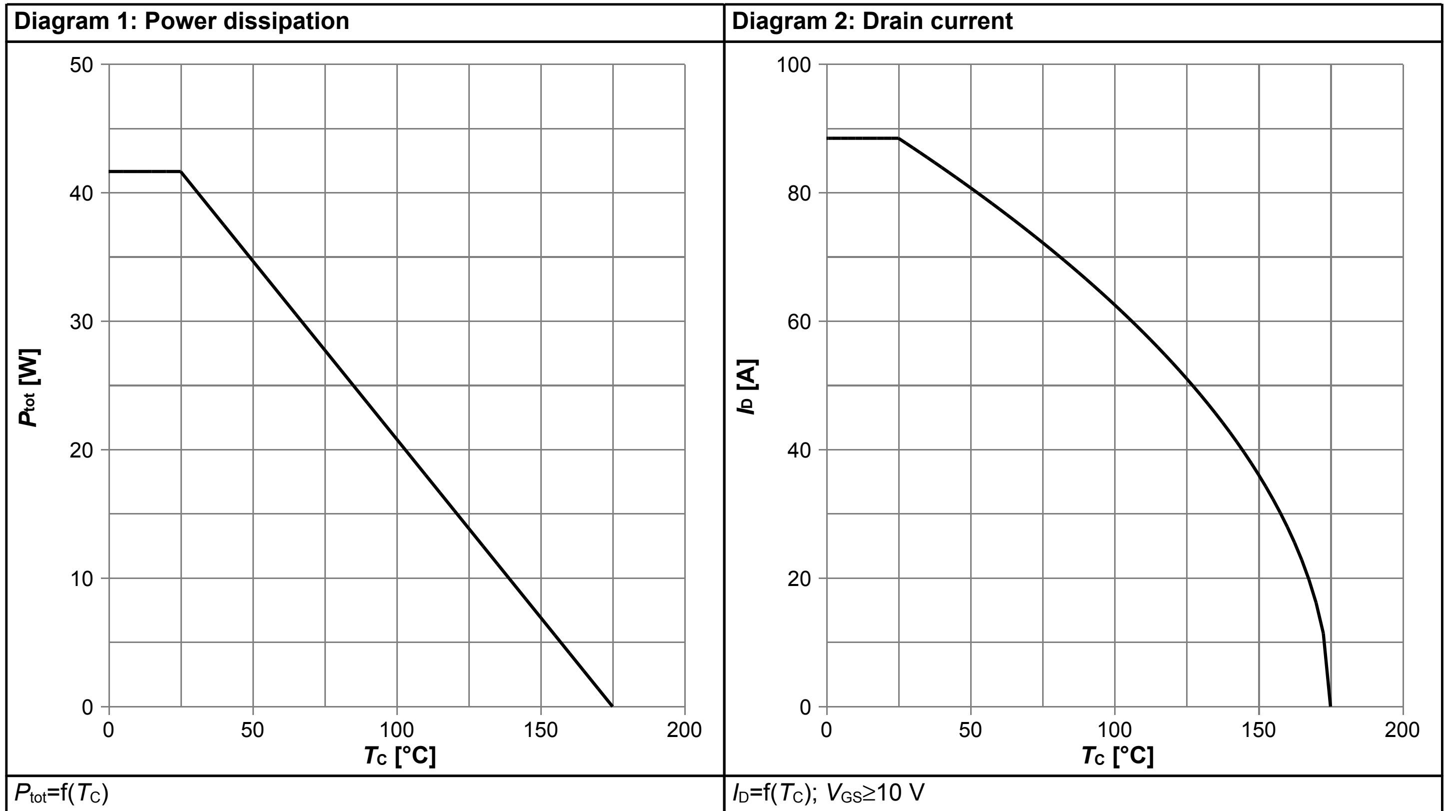
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	50	-	nC	V_{DD}=40 V, I_D=89 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	30	-	nC	V_{DD}=40 V, I_D=89 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	50	-	nC	V_{DD}=40 V, I_D=89 A, V_{GS}=0 to 10 V
Gate charge total	Q_g	-	155	206	nC	V_{DD}=40 V, I_D=89 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.6	-	V	V_{DD}=40 V, I_D=89 A, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	210	279	nC	V_{DD}=40 V, V_{GS}=0 V

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continous forward current	I_S	-	-	89	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	356	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.9	1.2	V	V_{GS}=0 V, I_F=89 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	78	-	ns	V_R=40 V, I_F=I_S, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	181	-	nC	V_R=40 V, I_F=I_S, di_F/dt=100 A/µs

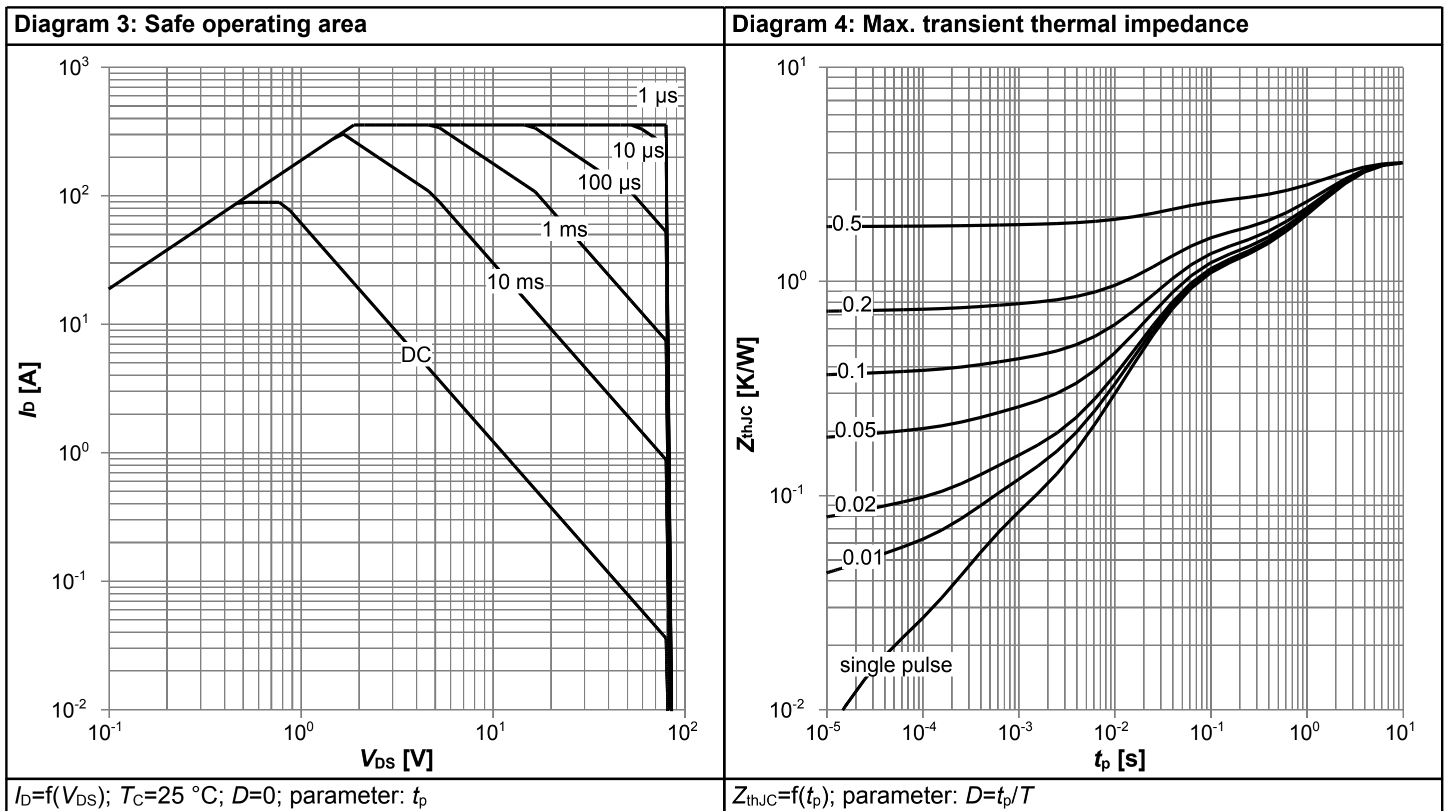
[1)] See "Gate charge waveforms" for parameter definition

4 Electrical characteristics diagrams



P_{tot}=f(T_C)

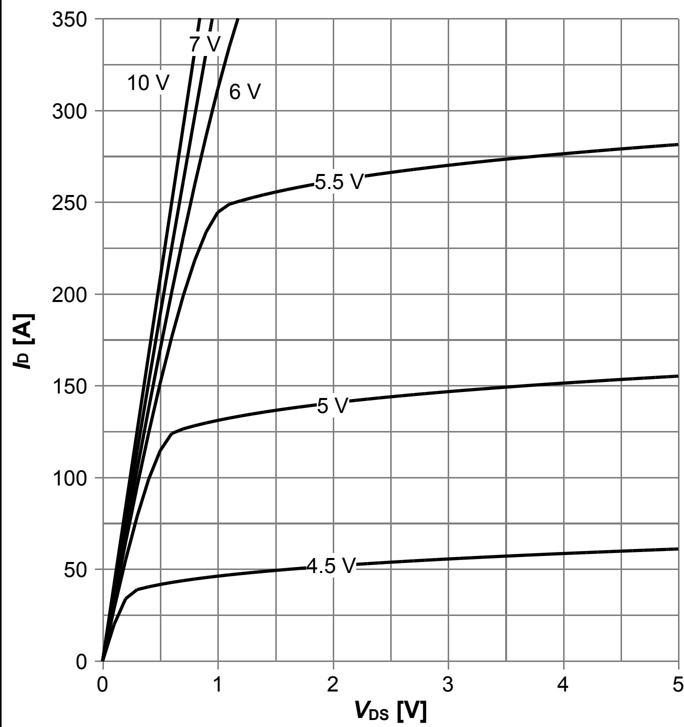
I_D=f(T_C); V_{GS}≥10 V



I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

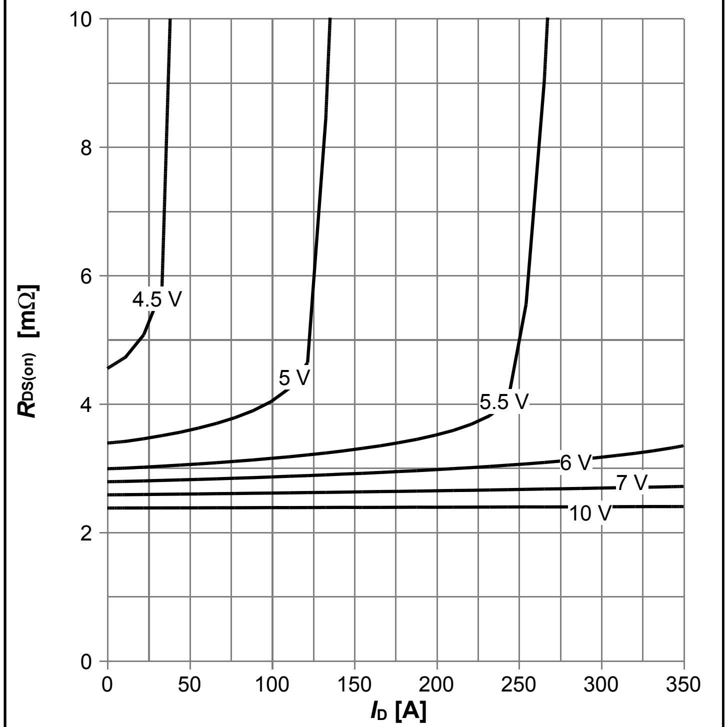
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



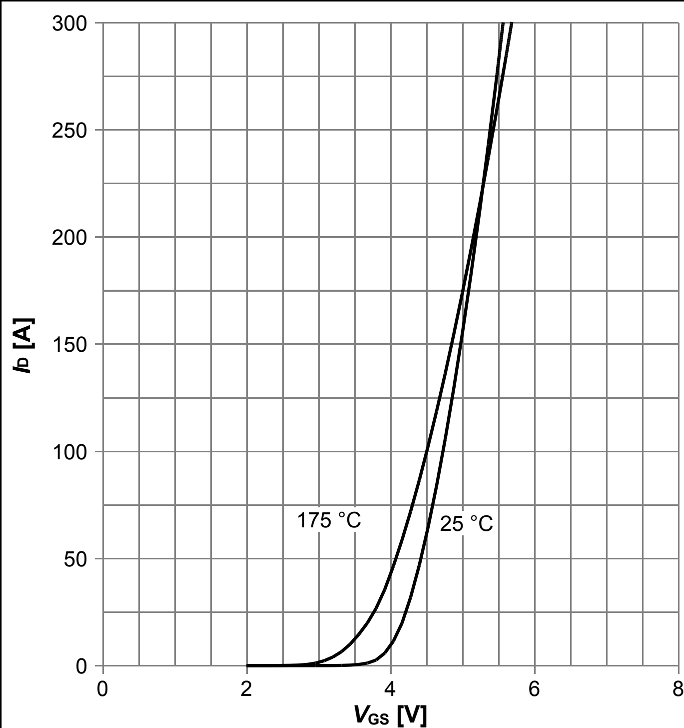
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



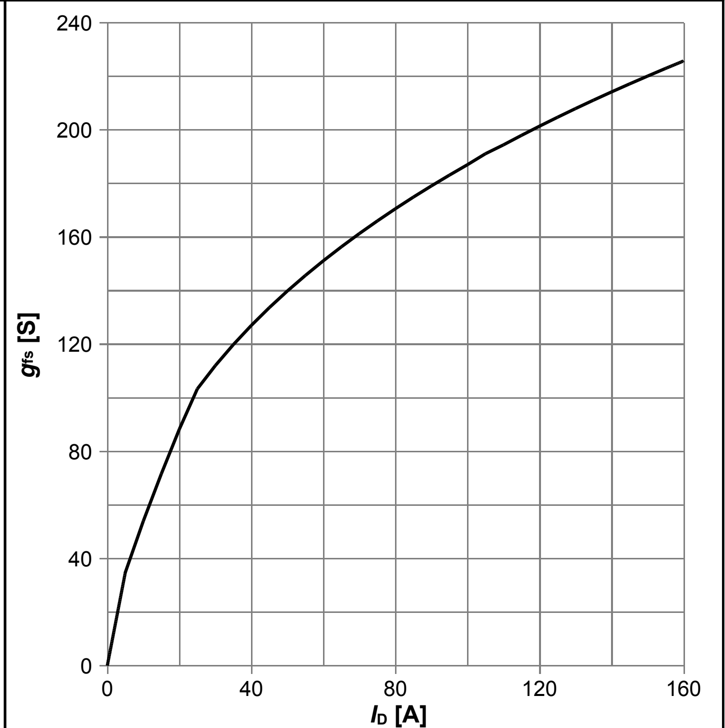
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



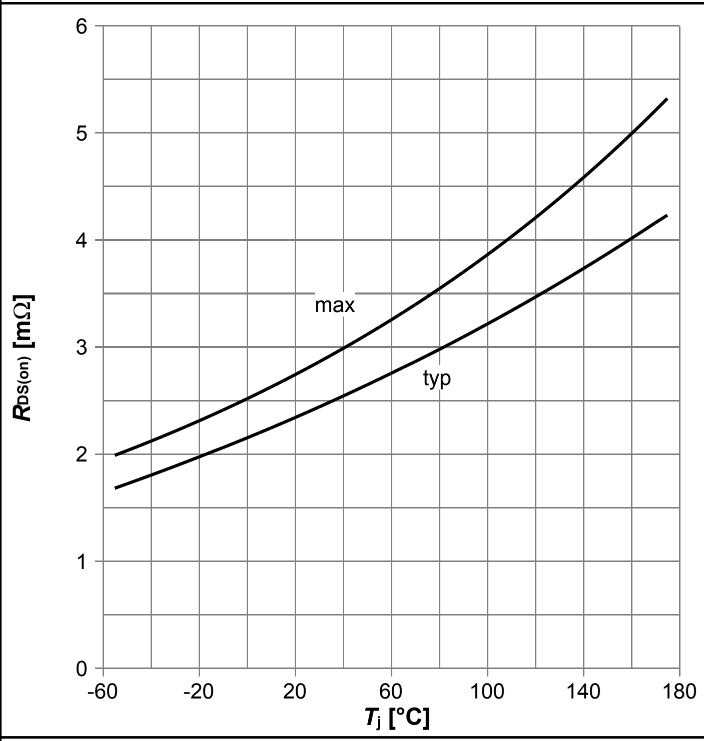
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



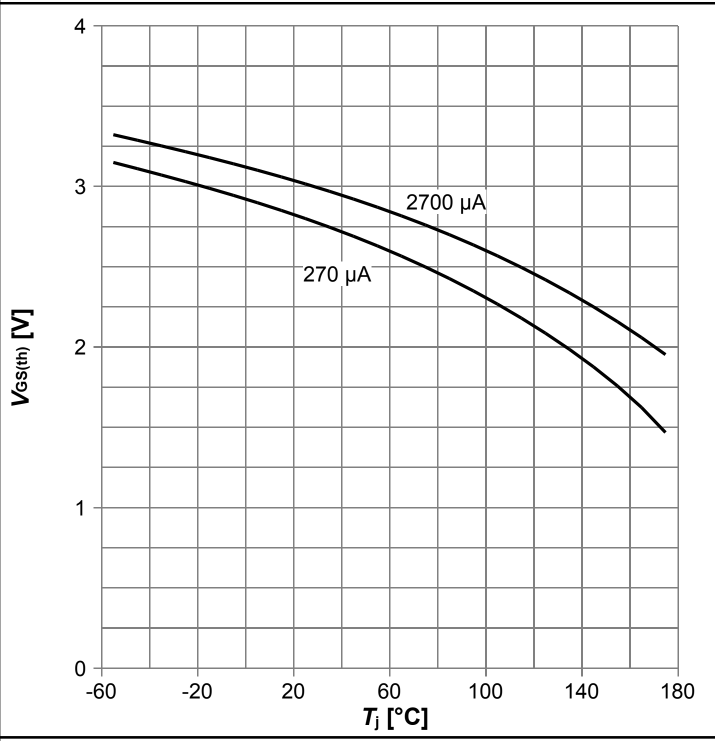
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance



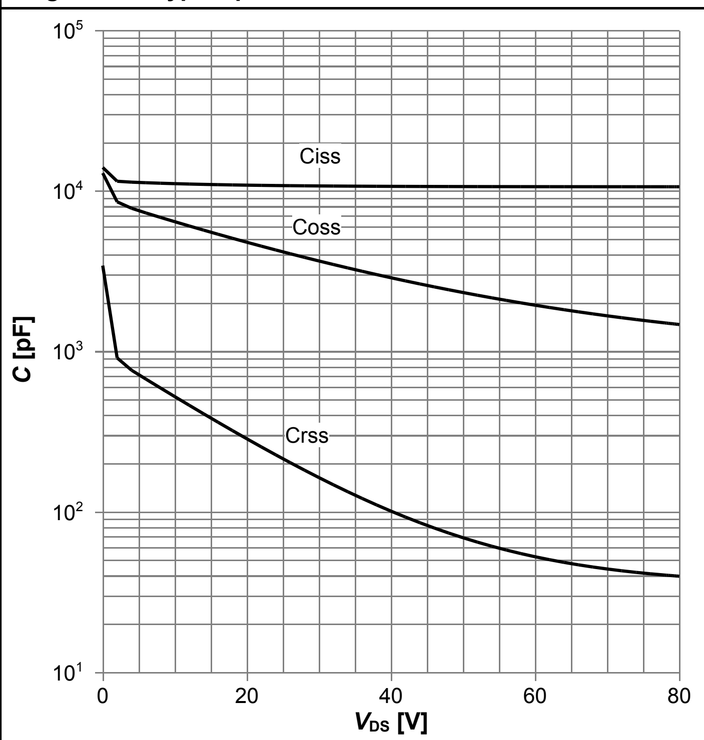
$R_{DS(on)}$=f(T_j); I_D=89 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



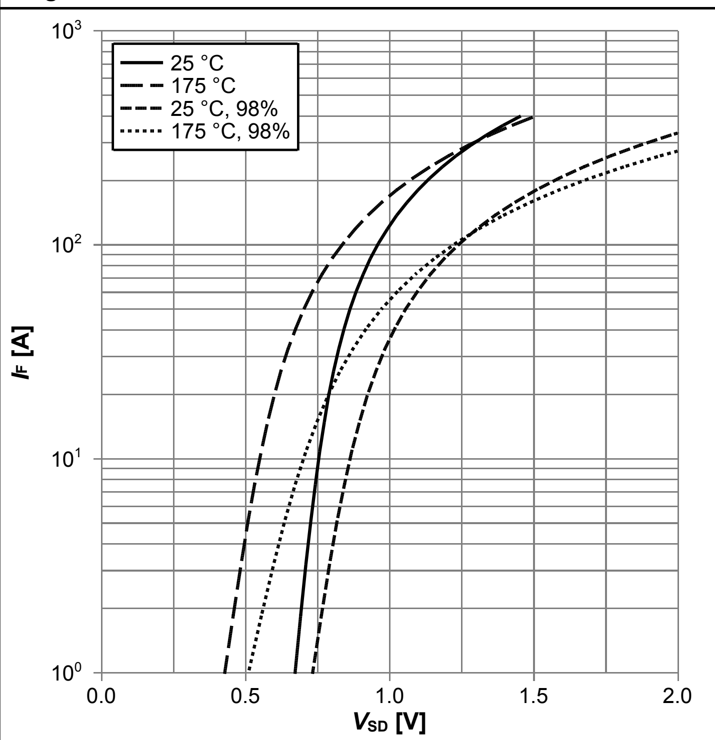
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



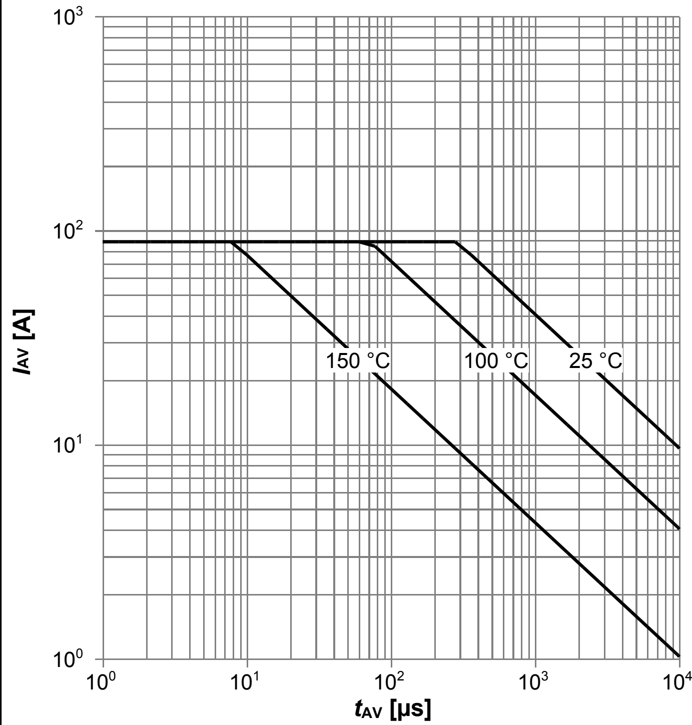
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



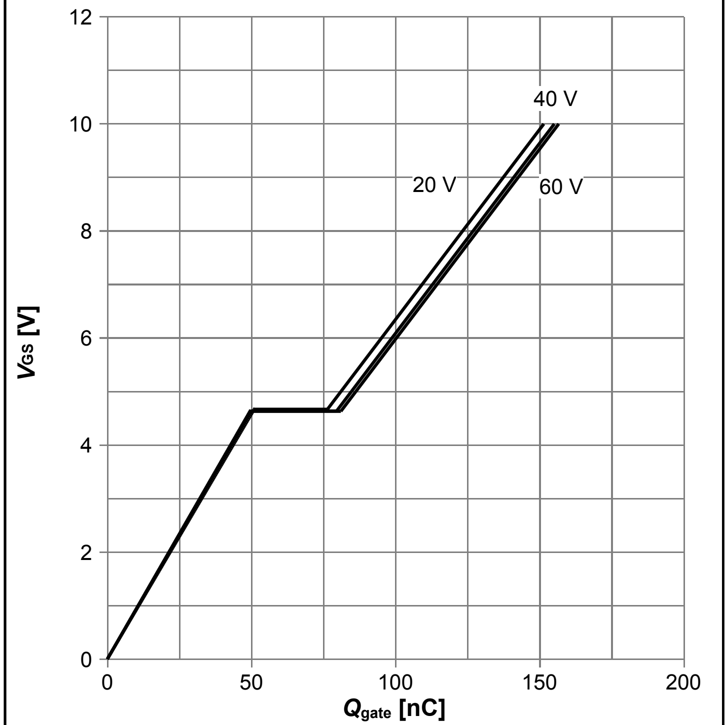
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



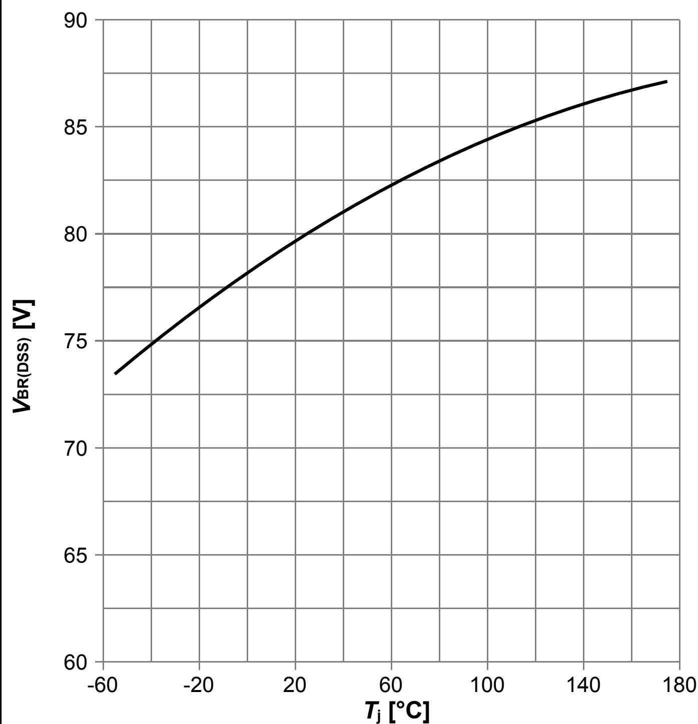
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



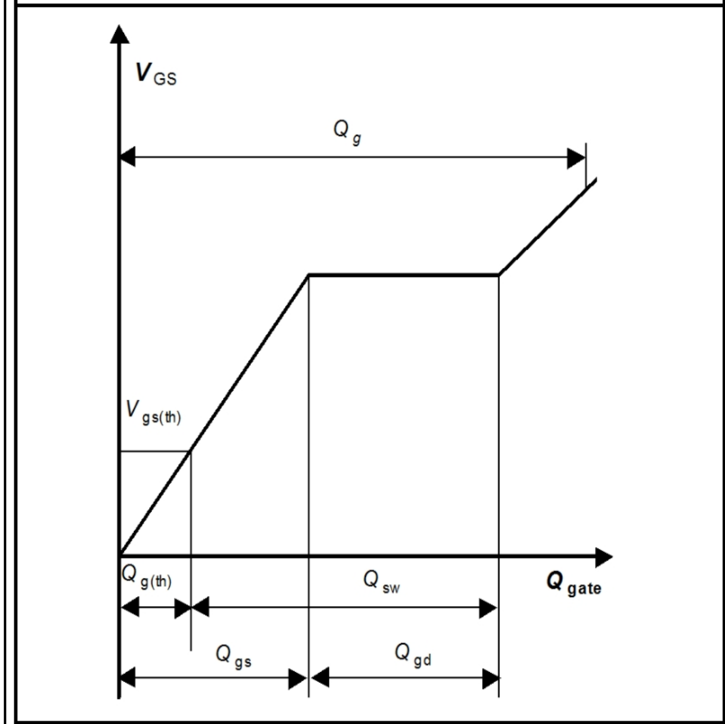
V_{GS}=f(Q_{gate}); I_D=89A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

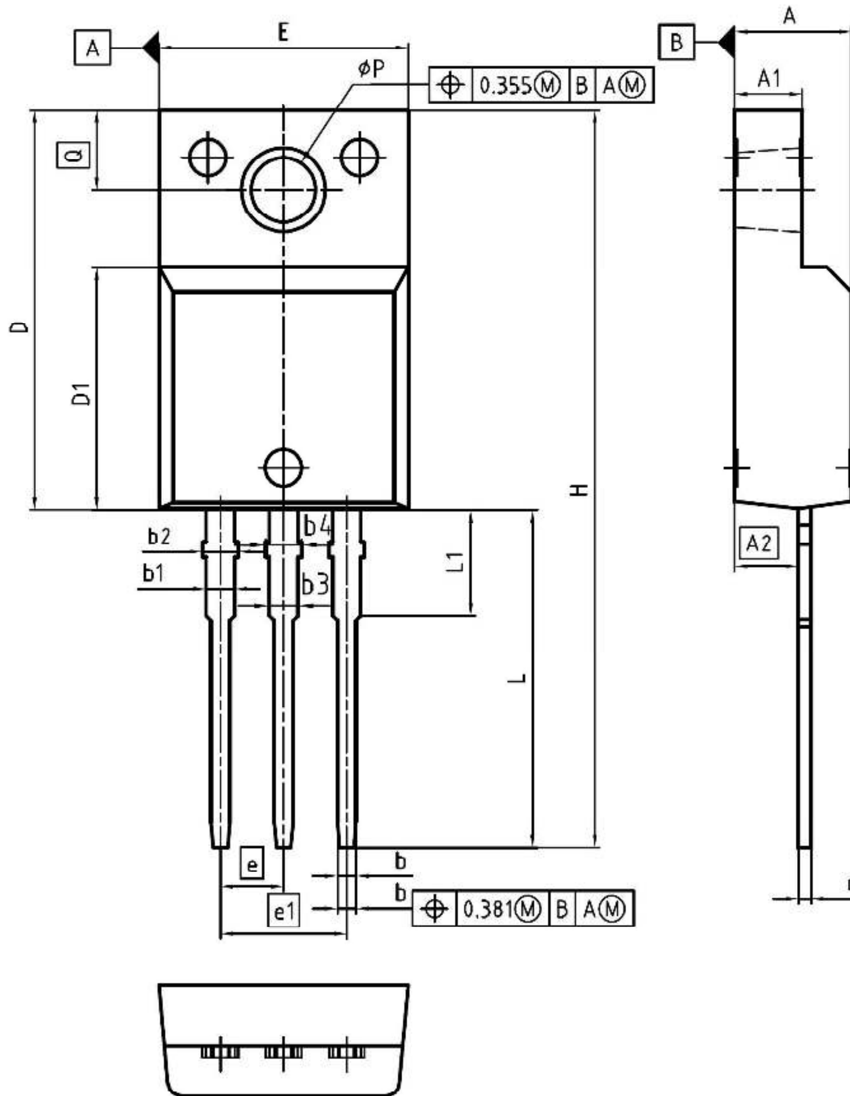


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Gate charge waveforms



5 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.55	4.85	0.179	0.191
A1	2.55	2.85	0.100	0.112
A2	2.42	2.72	0.095	0.107
b	0.65	0.85	0.026	0.033
b1	0.95	1.33	0.037	0.052
b2	0.95	1.51	0.037	0.059
b3	0.65	1.33	0.026	0.052
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.85	16.15	0.624	0.636
D1	9.53	9.83	0.375	0.387
E	10.35	10.65	0.407	0.419
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H	29.45	29.75	1.159	1.171
L	13.45	13.75	0.530	0.541
L1	3.15	3.45	0.124	0.136
øP	2.95	3.20	0.116	0.126
Q	3.15	3.50	0.124	0.138

DOCUMENT NO.
Z8B00003319

SCALE
0
2.5
0 2.5
5mm

EUROPEAN PROJECTION

ISSUE DATE
08-03-2007

REVISION
03

Figure 1 Outline PG-TO220-FP, dimensions in mm/inches

Revision History

IPA028N08N3 G

Revision: 2016-06-30, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-06-30	Release of final version

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