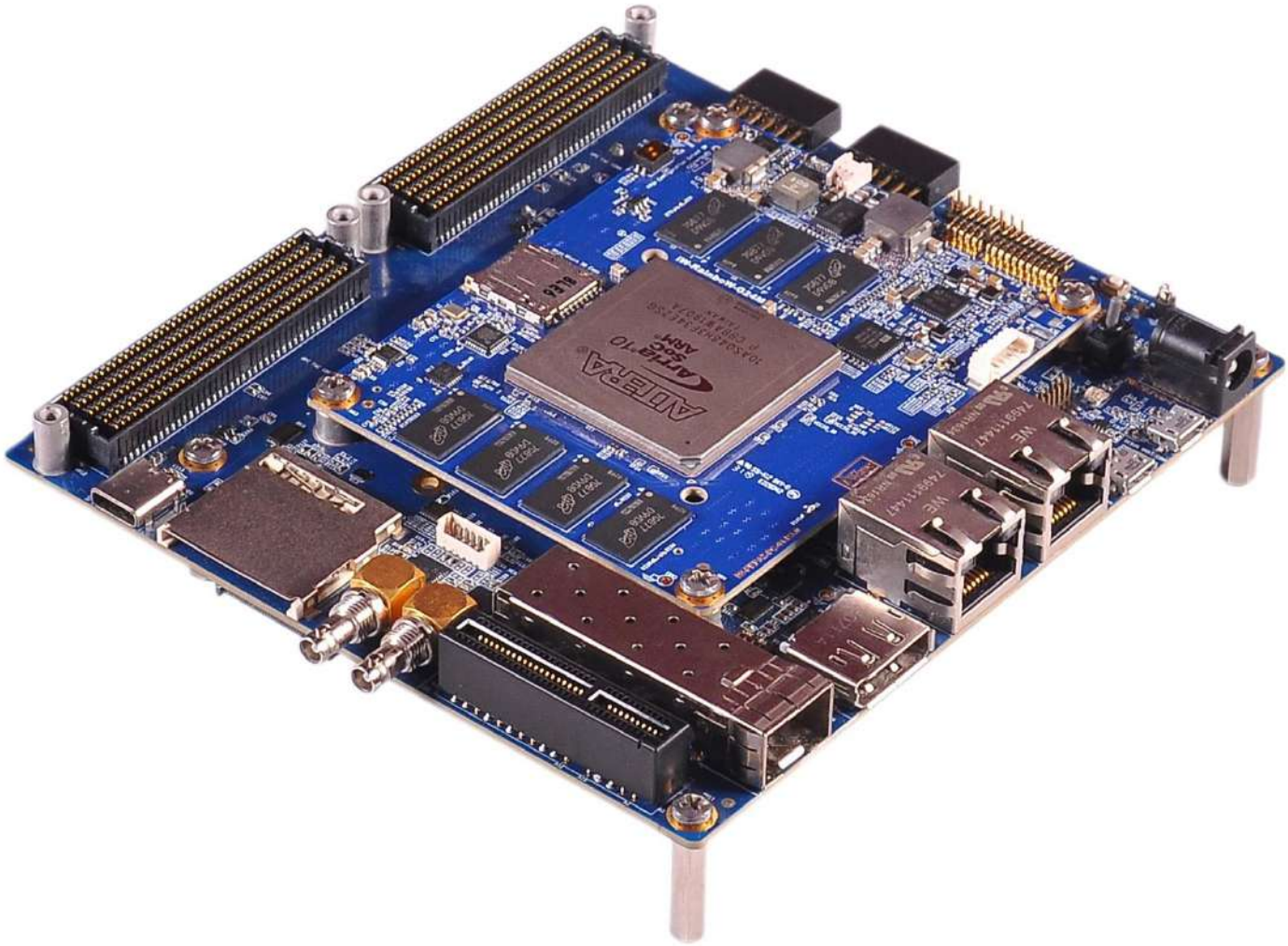
iW-RainboW-G24D
Arria10 SoC/FPGA SOM Development Platform Hardware User Guide



Embedding Intelligence

Document Revision History

Document Number		iW-PRFUD-UM-01-R3.0-REL0.2-Hardware-Arria10-DevKit
Revision	**Date**	**Change Description**
0.1	08th Nov 2019	Initial Draft Release
0.2	02nd Jan 2020	Updated Release

Disclaimer

iWave Systems reserves the right to change details in this publication including but not limited to any Product specification without notice.

No warranty of accuracy is given concerning the contents of the information contained in this publication. To the extent permitted by law no liability (including liability to any person by reason of negligence) will be accepted by iWave Systems, its subsidiaries or employees for any direct or indirect loss or damage caused by omissions from or inaccuracies in this document.

CPU and other major components used in this product may have several silicon errata associated with it. Under no circumstances, iWave Systems shall be liable for the silicon errata and associated issues.

Trademarks

All registered trademarks, product names mentioned in this publication are the property of their respective owners and used for identification purposes only.

Certification

iWave Systems Technologies Pvt. Ltd. is an ISO 9001:2015 Certified Company.

Warranty & RMA

Warranty support for Hardware: 1 Year from iWave or iWave's EMS partner.
For warranty terms, go through the below web link,
http://www.iwavesystems.com/support/warranty.html

For Return Merchandise Authorization (RMA), go through the below web link,
http://www.iwavesystems.com/support/rma.html

Technical Support

iWave Systems technical support team is committed to provide the best possible support for our customers so that our Hardware and Software can be easily migrated and used.

For assistance, contact our Technical Support team at,

Email : support.ip@iwavesystems.com
Website : www.iwavesystems.com
Address : iWave Systems Technologies Pvt. Ltd.
7/B, 29th Main, BTM Layout 2nd Stage,
Bangalore, Karnataka,
India – 560076

Table of Contents

List of Figures

List of Tables

1. INTRODUCTION

1.1 Purpose

The Arria10 SoC/FPGA SOM Development platform incorporates Arria10 SoC/FPGA based SOM and High-Performance Carrier board for complete validation of Arria10 SoC/FPGA functionality. This document is the Hardware User Guide for the Arria10 SoC Carrier Board and provides detailed information on the overall design & usage of the Carrier Board from a Hardware Systems perspective. The details about the Arria10 SoC/FPGA SOM hardware is explained in another document “iW-RainboW-G24M-Arria10_SoC_FPGA_SOM-HardwareUserGuide”.

1.2 Overview

iWave's Arria10 SoC/FPGA Development platform incorporates Arria10 SoC/FPGA SOM which is based on Altera’s high performance Arria10 SoC and the High-Performance Carrier Board. The development board can be used for quick prototyping of various applications targeted by the Arria10 SoC/FPGA. With the 130mmx140mm size, carrier board is packed with all the necessary on-board connectors to validate the features of Arria10 SoC/FPGA SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
B2B	Board to Board
CAN	Controller Area Network
CH	Channel
CMOS	Complementary Metal Oxide Semiconductor Signal
DP	Display Port
FPGA	Field Programmable Gate Array
FMC	FPGA Mezzanine Card
Gbps	Gigabits per sec
GEM	Gigabit Ethernet Controller
GPIO	General Purpose Input Output
HPC	High Pin Count
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
Mbps	Megabits per sec
MHz	Mega Hertz

Acronyms	Abbreviations
NC	No Connect
NPTH	Non Plated Through Hole
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PMOD	Peripheral Module
PTH	Plated Through Hole
RGMII	Reduced Gigabit Media Independent Interface
RX	Receiver
SATA	Serial Advanced Technology Attachment
SDI	Serial Digital Interface
SDIO	Secure Digital Input Output
SDHI	SD Card Host Interface
SFP	Small Form-factor Pluggable
SOM	System On Module
TXVR	Transceiver
TX	Transmitter
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go

Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
OD	Open Drain Signal
OC	Open Collector Signal
Analog	Analog Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on board.

1.4 References

- Arria10 SoC/FPGA Datasheet & Reference Manual
- Arria10 SoC/FPGA SOM Hardware User Guide

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Arria10 SoC/FPGA Development platform carrier board features with high level block diagram and detailed information about each block.

2.1 Arria10 SoC/FPGA SOM Carrier Board Block Diagram

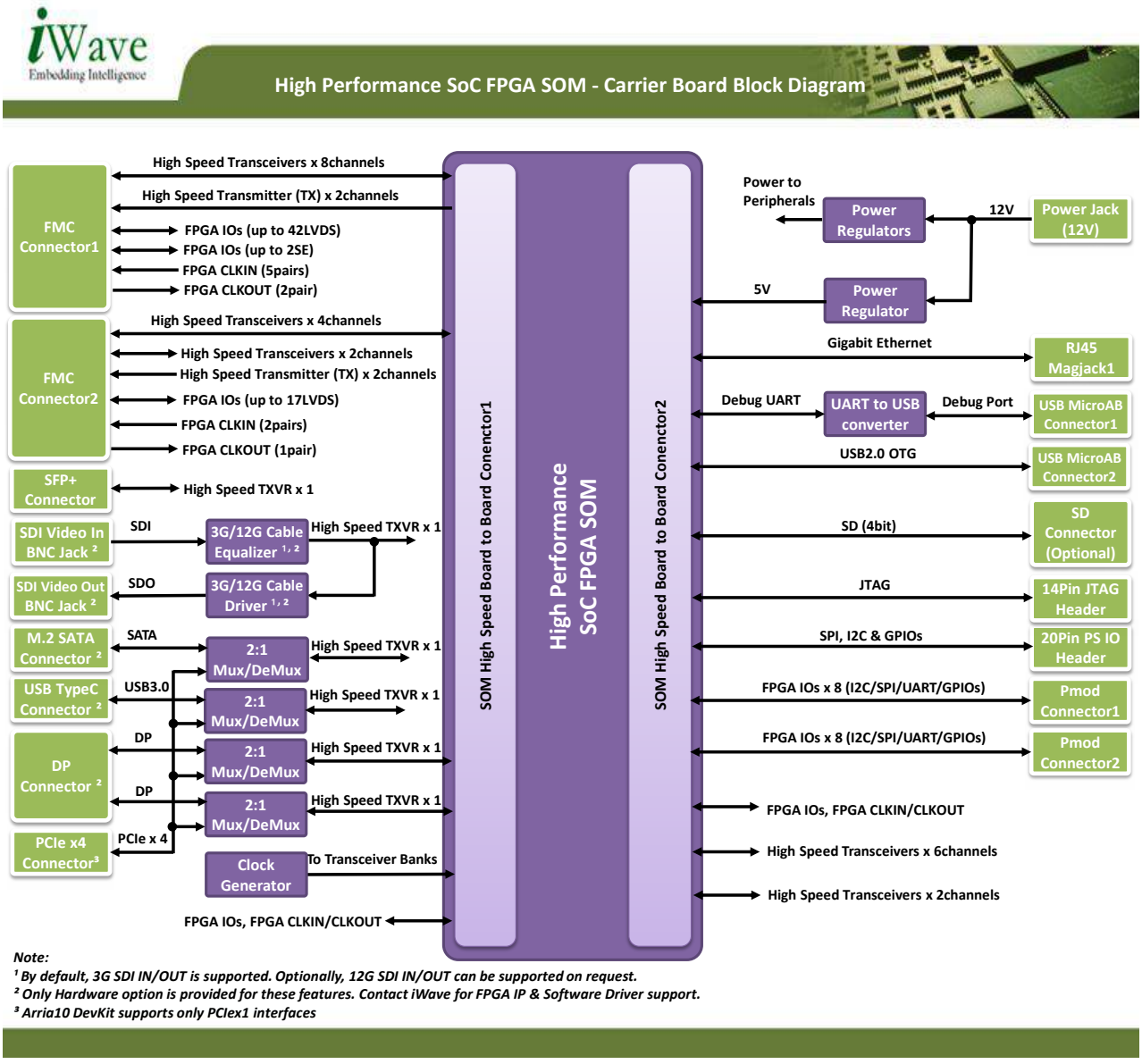


Figure 1: Arria10 SoC/FPGA SOM Carrier Board Block Diagram

2.2 Arria10 SoC/FPGA SOM Carrier Board Features

The Arria10 SoC/FPGA Carrier board supports the following features to validate the Arria10 SoC/FPGA SOM supported interfaces.

HPS Interface Features

- Gigabit Ethernet through RJ45MagJack x 1
- USB2.0 OTG through Micro AB connector x 1
- Debug UART through USB Micro AB connector x 1

FPGA Interface Features

- SFP+ Connectors x 1
- PCIex4 Connector x 1[1]
- FMC High Pin Count (HPC) Connector 1
    - 8 High Speed Transceivers
    - 2 High Speed Transmitter (TX)
    - Up to 42 LVDS IOs
    - Up to 2 Single Ended (SE) IOs
    - 5 Clock Input Capable LVDS/SE pins
    - 2 Clock Output Capable LVDS/SE pins
- FMC High Pin Count (HPC) Connector 2
    - 6 High Speed Transceivers
    - 2 High Speed Transmitter (TX)
    - Up to 17 LVDS IOs
    - 2 Clock Input Capable LVDS/SE pins
    - 1 Clock Output Capable LVDS/SE pins
- PMOD Connectors x 2
- Optional Features[2]
    - SDI Video IN through HD BNC Connector x 1
    - SDI Video OUT through HD BNC Connector x 1
    - M.2 SATA Connector x 1
    - USB3.0 TypeC connector x 1
    - Display Port Connector x 1

Additional Features

- Clock Synthesizer/Generator
- 16-Bit IO Expander
- JTAG Connector x 1
- 20 Pin GPIO Header x 1
- Power ON/OFF DIP Switch x 1
- Reset Pushbutton Switch x 1

General Specification

- Power Supply : DC 12V, 5A Power Input Jack
- Form Factor : 130mm X 140mm

[1] In iWave Arria10 SoC/FPGA DevKit Supports only One PCIex1.

[2] Only hardware circuit is mounted in carrier board. But for FPGA IP & Software driver support, contact iWave.

2.3 Board to Board Connectors

The Arria10 SoC/FPGA Carrier board supports two 240 Pin Board to Board mating connectors for Arria10 SoC/FPGA SOM attachment. This 240 pin Board to Board connector is capable of handling high-speed serialized signals and can be used for size constrained embedded applications.

2.3.1 Board to Board Connector1

Board to Board Connector1 (J10) is physically located at the top of the board as shown below.

Note: For the Board to Board Connector1 pinout, refer the Arria10 SoC/FPGA SOM Hardware User Guide.

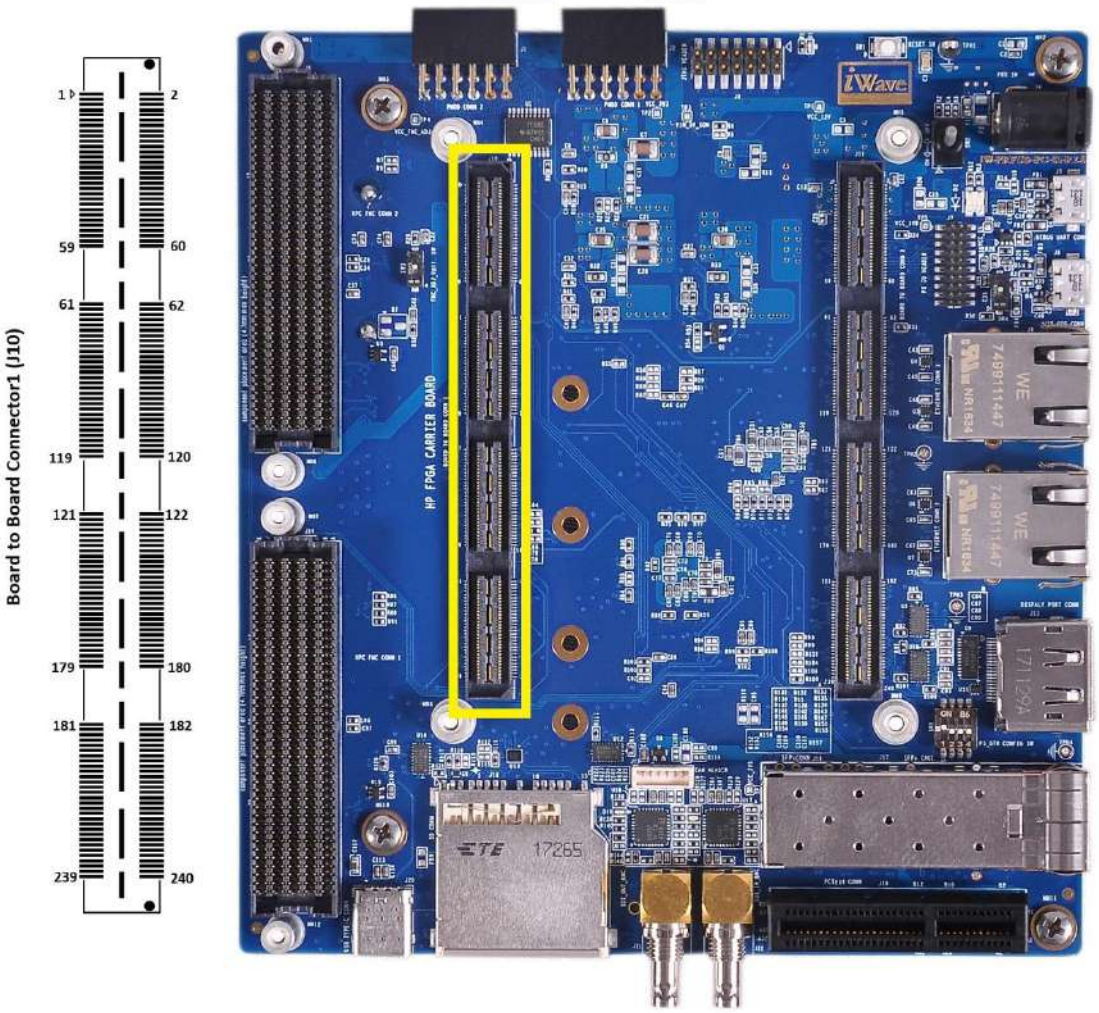


Figure 2: Board to Board Connector1

2.3.2 Board to Board Connector2

Board to Board Connector2 (J11) is physically located at the top of the board as shown below.

Note: For the Board to Board Connector2 pinout, refer the Arria10 SoC/FPGA SOM Hardware User Guide.

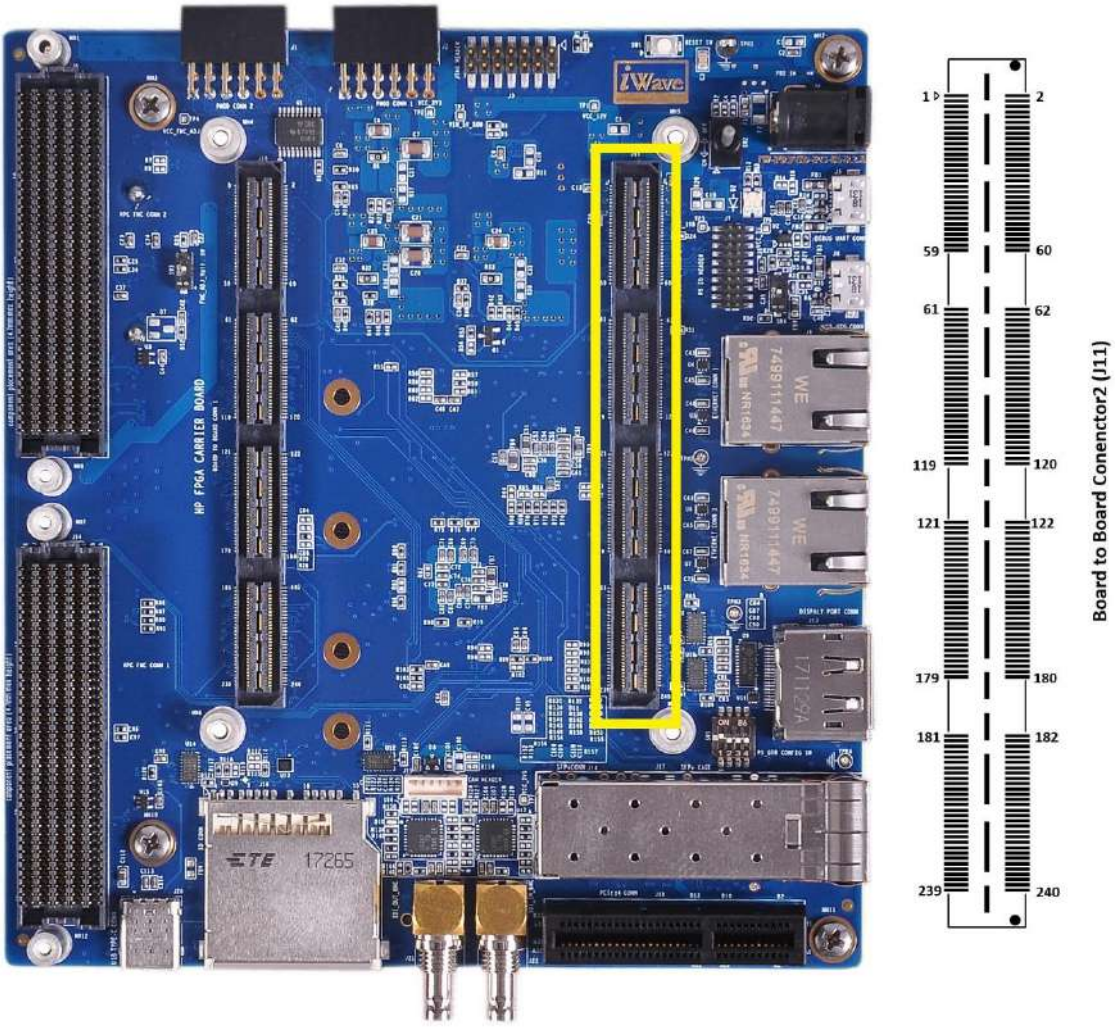


Figure 3: Board to Board Connector2

2.4 HPS Interface Features

The features which are supported from Arria10 SoC/FPGA's HPS is explained in the following section.

2.4.1 Gigabit Ethernet Port

The Arria10 SoC/FPGA SOM Carrier board supports one 10/100/1000Mbps Ethernet port. Ethernet port is supported through EMAC1 interface of Arria10 SoC/FPGA HPS. Ethernet PHY output signals from Board to Board connector2 is directly connected to RJ45 Magjack (J9). The Ethernet supports Link/Activity (Orange) LED indication on RJ45 Magjack connector. This RJ45 Magjack connector(J9) is physically located at the top of the board as shown below.

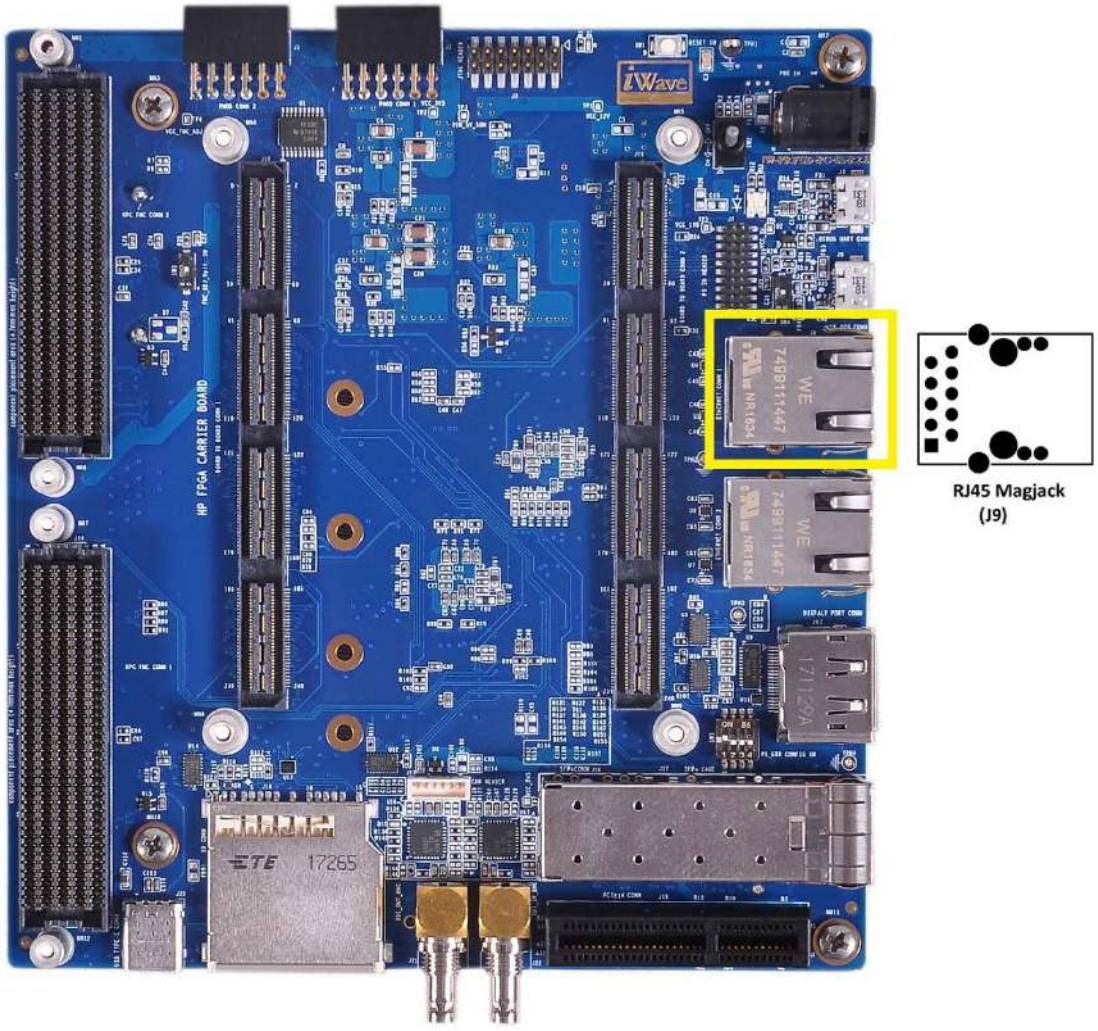


Figure 4: Gigabit Ethernet Connector

2.4.2 USB2.0 OTG Port

The Arria10 SoC/FPGA carrier Board supports USB2.0 High Speed OTG interface through USB0 OTG Controller of Arria10 SoC/FPGA HPS. This USB2.0 OTG interface is supported through USB2.0 MicroAB connector (J8). The USB PHY Transceiver output signals from Board to Board connector2 is connected to "FUSB340" USB Switch for selecting the USB2.0 OTG connection of USB2.0 MicroAB connector (J8). If the DIP switch (SW4) is set to ON, USB2.0 OTG is connected to MicroAB connector (J8) and if the DIP switch (SW4) is set to OFF, USB2.0 OTG is connected to USB TypeC connector (J20).

The USB2.0 OTG port can be used as full functional OTG functionality which supports USB2.0 host and USB2.0 device based on USB ID pin status. The VBUS power of this USB2.0 MicroAB connector is connected through current limit power switch which can be used to switch On/Off the power based on the device or Host and also limits the current above 900mA in host mode. The USB PHY transceiver in SOM detects the USB functionality through USB ID pin (34th pin of B2B-2) and controls the power using the USB_PWR_EN pin (32nd pin of B2B-2). This USB2.0 OTG connector (J13) is physically located at the top of the board as shown below.

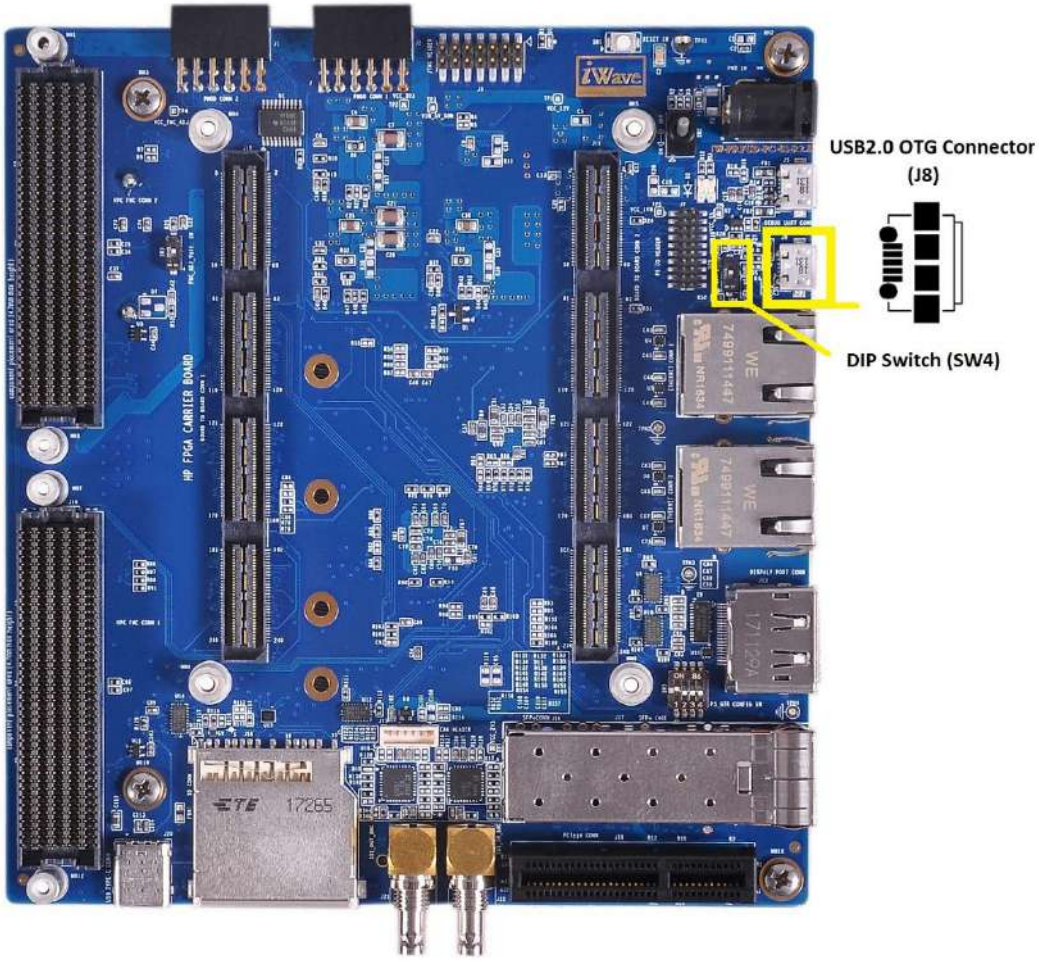


Figure 5: USB OTG Connector

2.4.3 Debug UART

The Arria10 SoC/FPGA Carrier Board supports debug interface through UART1 interface of Arria10 SoC/FPGA HPS. This UART1 signals from Board to Board Connector2 is connected to UART to USB Convertor “FT232RQ”. The output of the USB convetor is conencted to USB MicroAB Connector (J5). This USB MicroAB Connector can be used for Debug purpose which is is physically located at the top of the board as shown below.

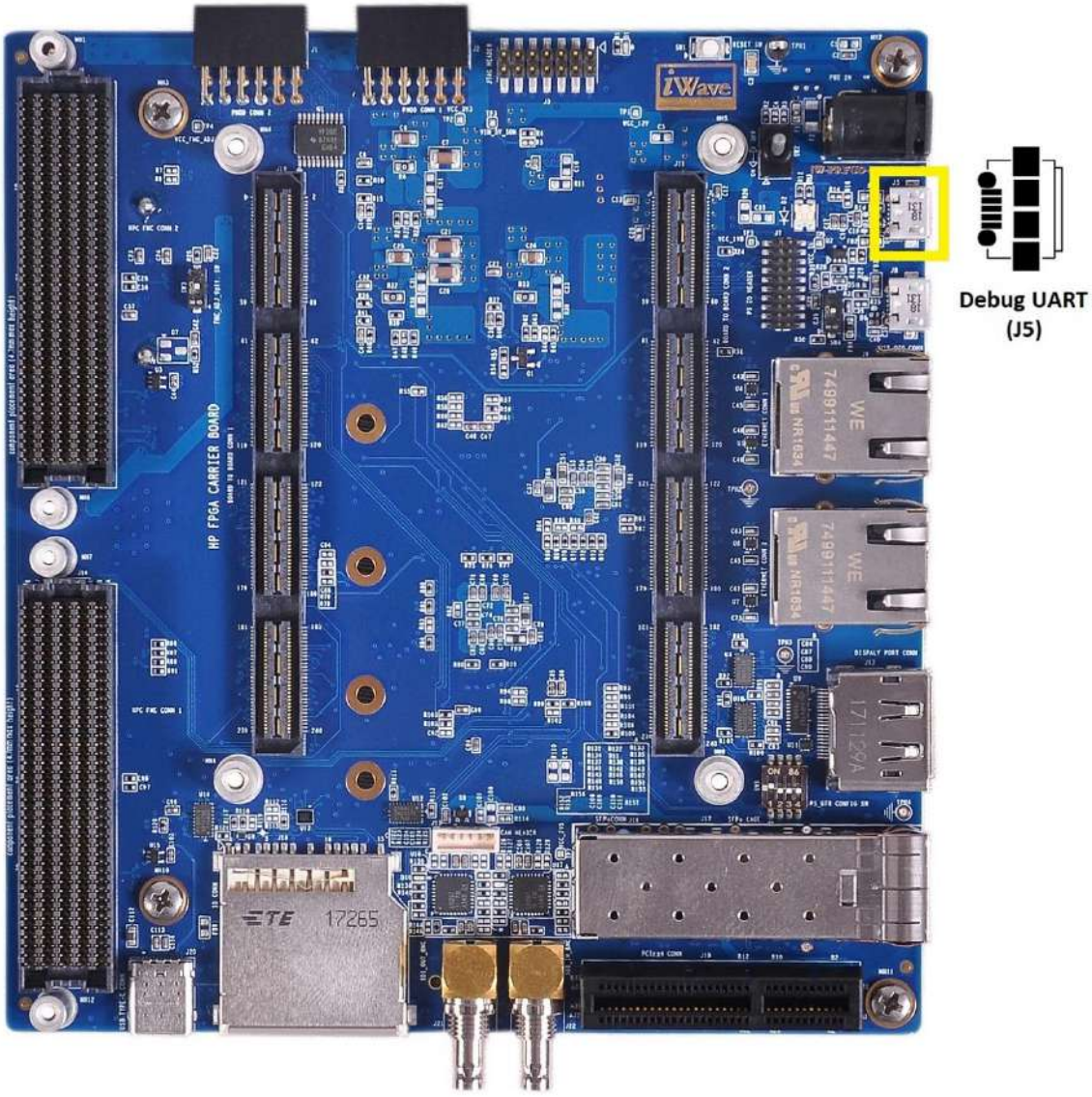


Figure 6: Debug UART Connector

2.5 FPGA Interface Features

The features which are supported from Arria10 SoC/FPGA's FPGA is explained in the following section.

2.5.1 High Speed Transceivers

The Arria10 SoC/FPGA Carrier board supports different high speed interfaces through 24 Transceivers (16 from B2B-1 and 8 from B2B-2) as mentioned below.

- SFP+ Connector (1 HS Transceiver)
- PCIe x4 Connector[1]
- Dual FMC HPC Connectors (14 HS Transceiver & 4 HS Transmitter)

Optional: [2]

- 3G/12G SDI Video IN (1 HS Transmitter)
- 3G/12G SDI Video OUT (1 HS Receiver)
- M.2 SATA Connector x 1
- USB3.0 TypeC connector x 1
- Display Port Connector x 1

[1] In iWave Arria10 SoC/FPGA DevKit Supports only One PCIex1.

[2] Only hardware circuit is mounted in carrier board. But for FPGA IP & Software driver support, contact iWave.

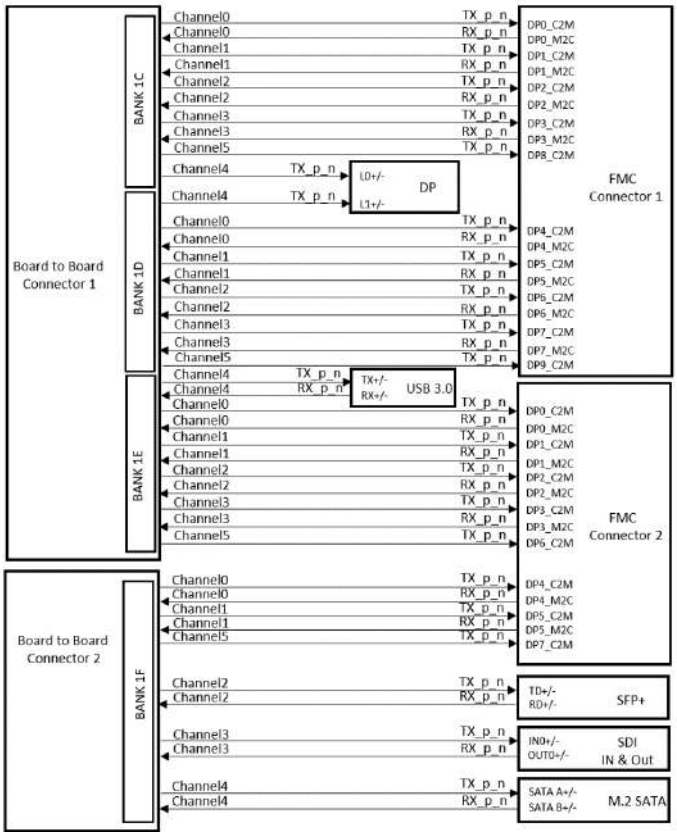


Figure 7: High Speed Transceiver Connections

In Arria10 SoC/FPGA Carrier board, some of the High speed transcivers are multiplexed to multiple high speed interfaces which is mentioned below through MUX/DEMUX IC.

- x1, x2, or x4 lane PCIe
- 1 SATA port
- 1 USB3.0 port
- 1 or 2 lanes of DisplayPort (TX only)

The MUX/DEMUX connection and interface selection option is shown below for easy understanding. The selection control of each MUX IC is connected to Channel selection 4bit DIP switch (SW5).

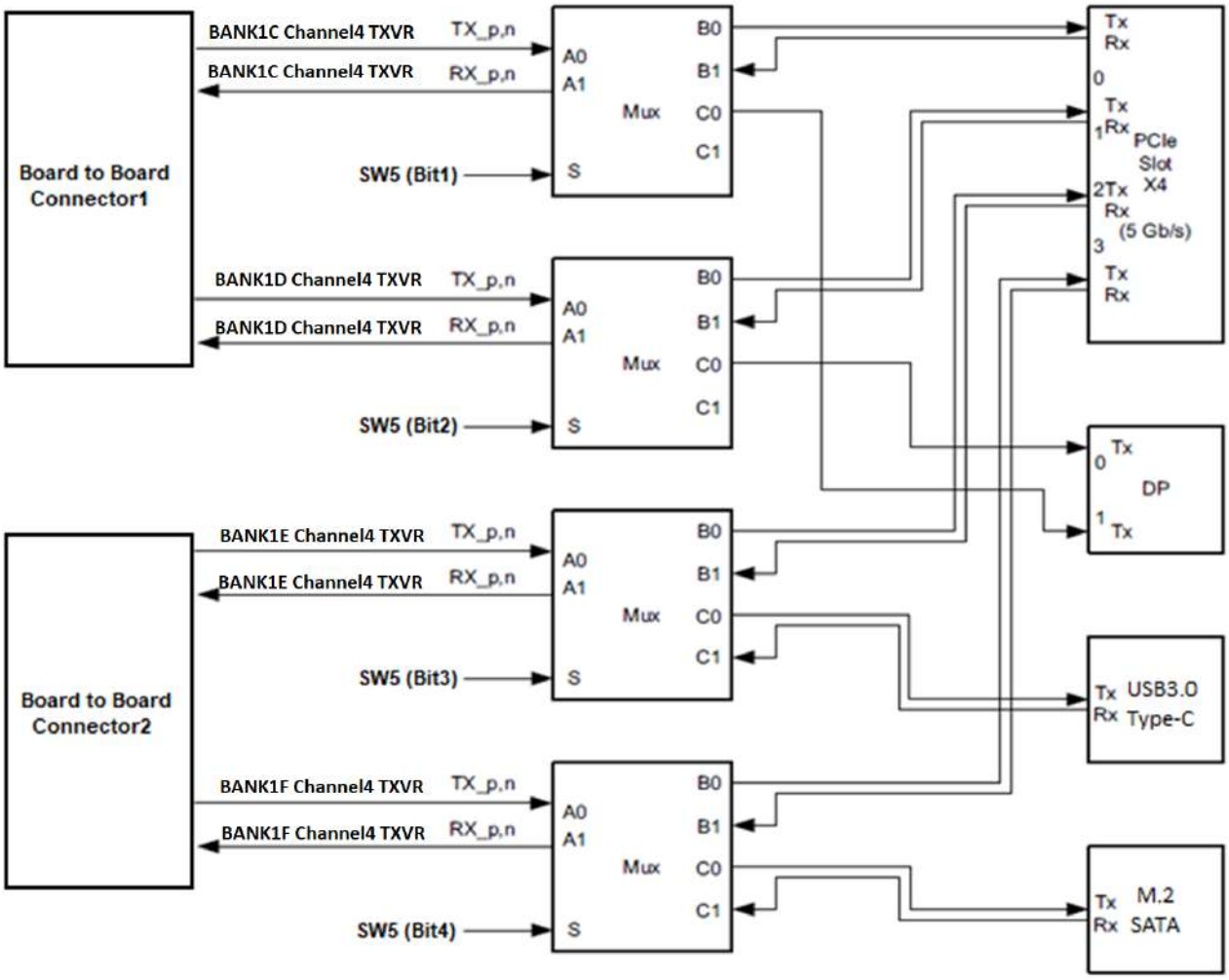


Figure 8:MUX/DEMUX Switch Connectivity.

Note: In iWave Arria10 DevKit, Channels from different Banks are not supported for PCIex4 interface.

The Channel selection switch (SW5) setting and corresponding interface selection option is explained below.

Table 3: High Speed Transceiver Channel Selection Switch Setting

High Speed Transceiver Channel	Channel Selection Switch (SW5)		
	Switch Bit Number	Switch Bit Position	
		ON	OFF
Bank 1C Channel4	**Bit1**	Bank 1C channel4 is connected to Lane0 of PCIe x4 connector (default)	Bank 1C channel4 is connected to Lane1 of DP connector
Bank 1D Channel4	**Bit2**	Bank 1D channel4 is connected to Lane1 of PCIe x4 connector (default)	Bank 1D channel4 is connected to Lane0 of DP connector
Bank 1E Channel4	**Bit3**	Bank 1E channel4 is connected to Lane2 of PCIe x4 connector (default)	Bank 1E channel4 is connected to Lane1 of USB3.0 TypeC connector
Bank 1F Channel4	**Bit4**	Bank 1F channel4 is connected to Lane3 of PCIe x4 connector (default)	Bank 1F channel4 is connected to M.2 SATA connector

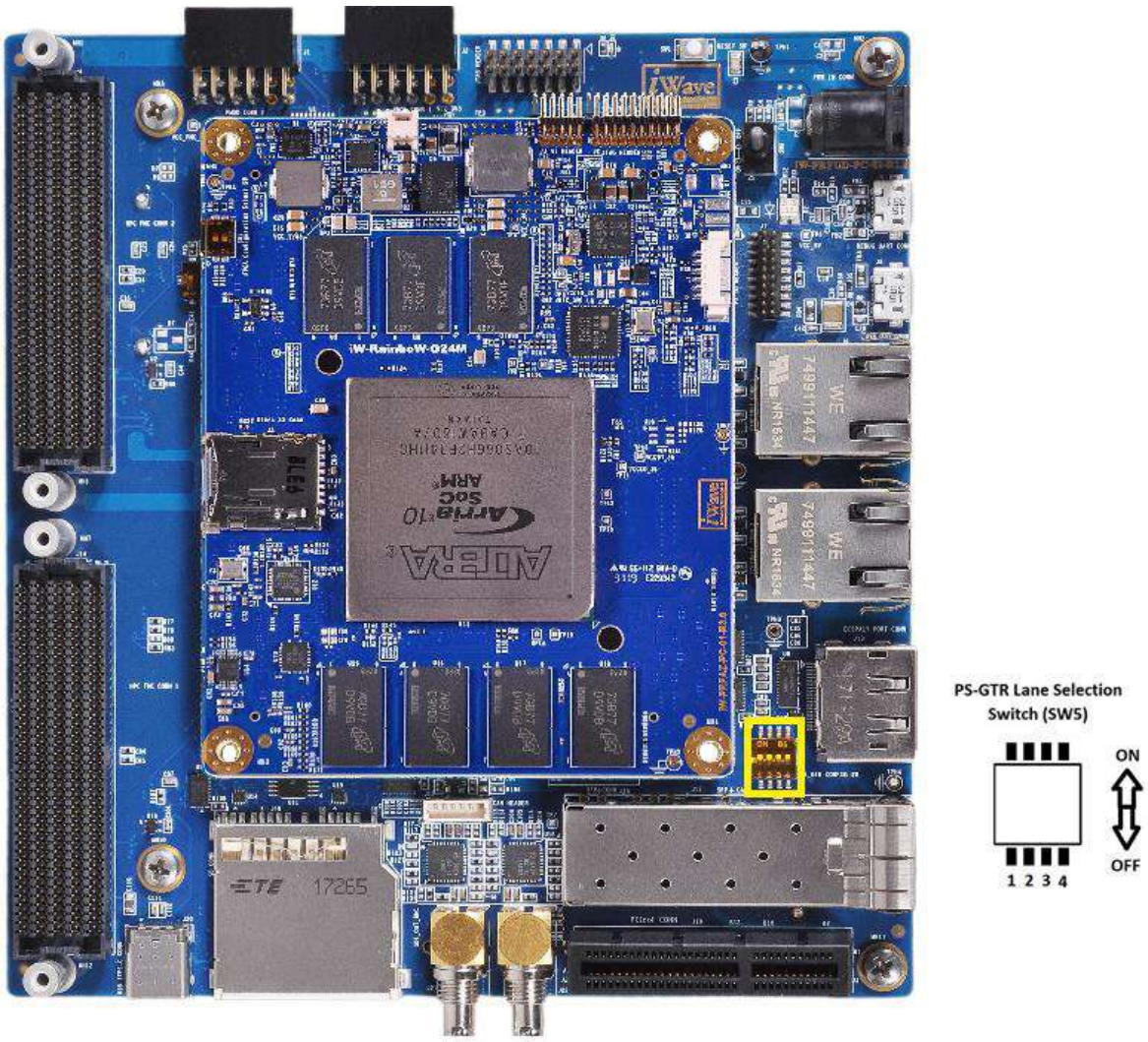


Figure 9: Channel Selection Switch

2.5.1.1 SFP+ Connector

The Arria10 SoC/FPGA Carrier board supports one SFP+ Connector through Bank 1F transceiver of Arria10 SoC/FPGA. Bank 1F Channel2 from Board to Board Connector2 is connected to SFP+ connector. Also HPS I2C0 is connected to this connector for control and configuration. All other contorl signals of SFP+ connnector is connected from IO Expander. This SFP+ connector (J16) is physically located at the top of the board as shown below.

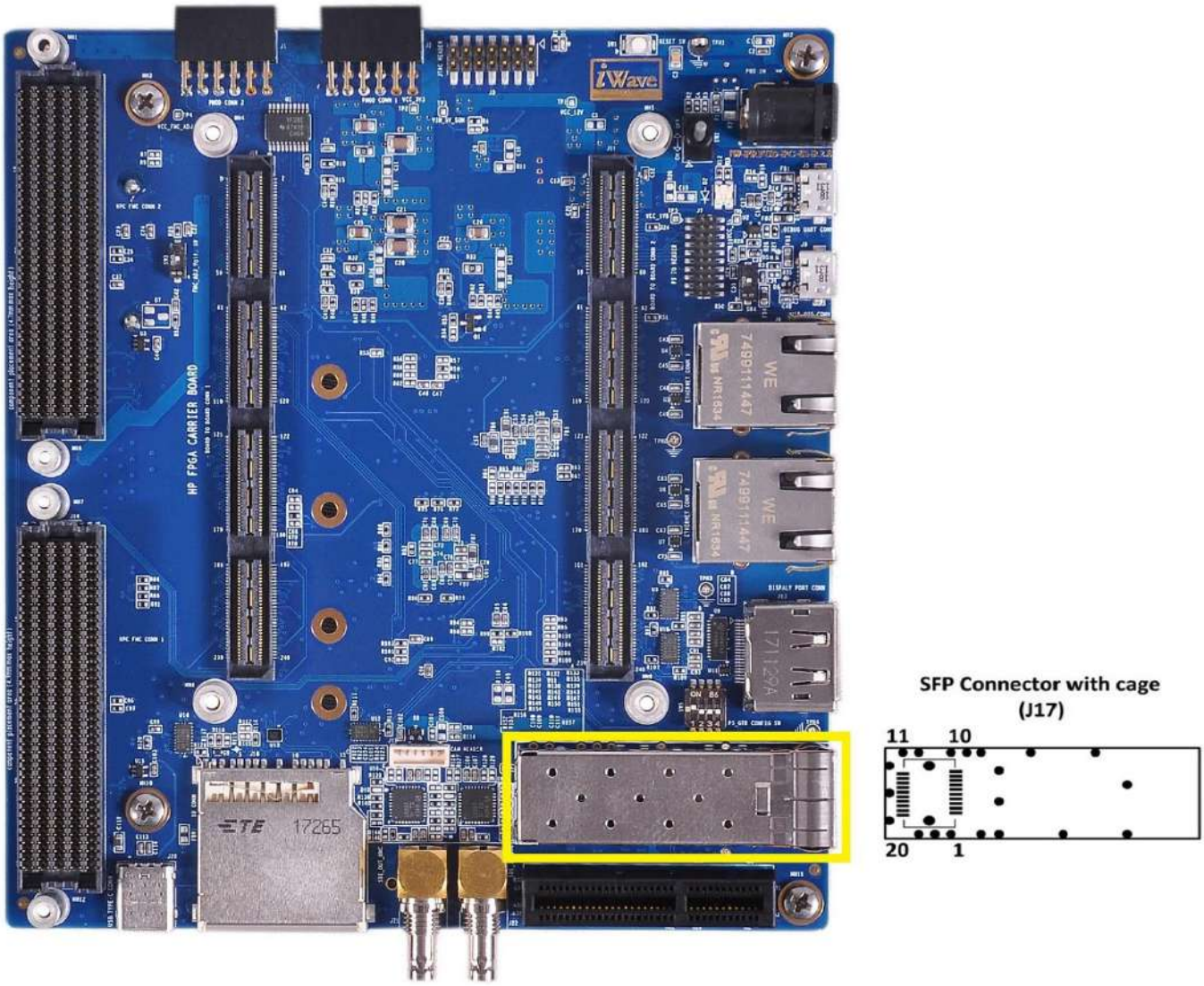


Figure 10: SFP+ Connector with Cage

Table 4: SFP+ Connector Pin Assignment

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VEET1	GND	Power	Ground.
2	TFAULT	IOEXP_P00_SFP_TFAULT	I, LVTTL/ 4.7K PU	Module Transmitter Fault. This Pin is connected to IO Expander Port 0 for software access if required.
3	TDIS	IOEXP_P05_SFP_TDIS	O, LVTTL/ 4.7K PD	Transmitter Disable. This Pin is connected to IO Expander Port 5 for software control if required.
4	SDA	HPS_GPIO0_IO4/I2C0_SDA	IO, 3.3V CMOS	I2C Data.
5	SCL	HPS_GPIO0_IO5/I2C0_SCL	O, 3.3V CMOS	I2C Clock.
6	MOD_ABS	IOEXP_P02_SFP_MOD_ABS	I, 3.3V CMOS/ 4.7K PU	Module Definition. This Pin is connected to IO Expander Port 2 for software access if required.
7	RS0	IOEXP_P04_SFP_RS0	O, 3.3V CMOS/ 4.7K PU	Rate select 0. This Pin is connected to IO Expander Port 4 for software control if required.
8	RX_LOS	IOEXP_P01_SFP_RX_LOS	I, 3.3V CMOS/ 4.7K PU	Receiver loss of signal indication. This Pin is connected to IO Expander Port 1 for software access if required.
9	RS1	IOEXP_P03_SFP_RS1	O, 3.3V CMOS/ 4.7K PU	Rate select 1. This Pin is connected to IO Expander Port 3 for software control if required.
10	VEER1	GND	Power	Ground.
11	VEER2	GND	Power	Ground.
12	RD-	GXBL1F_RX_CH2n	I, DIFF	SFP+ Receiver Data Negative
13	RD+	GXBL1F_RX_CH2p	I, DIFF	SFP+ Receiver Data Positive
14	VEER3	GND	Power	Ground.
15	VCCR	VCC_3V3	O, 3.3V Power	3.3V Receiver Supply Voltage
16	VCCT	VCC_3V3	O, 3.3V Power	3.3V Transmitter Supply Voltage
17	VEET2	GND	Power	Ground.
18	TD+	GXBL1F_TX_CH2p	O, DIFF	SFP+ Transmit Data Positive
19	TD-	GXBL1F_TX_CH2n	O, DIFF	SFP+ Transmit Data Negative
20	VEET3	GND	Power	Ground.

2.5.1.2 PCIe x4 Connector

The Arria10 SoC/FPGA Carrier board supports one PCIe x4 connector through Bank1C CH4, Bank1D CH4, Bank1E CH4 & Bank1F CH4 of Arria10 SoC/FPGA. All the four channels from Board to Board Connectors are connected to PCIe x4 connector to support x1, x2 & x4 PCIe devices. The Channel selection to PCIe x4 connector is done through Channel Selection Switch (SW5). The Carrier board provides 100MHz reference clock to PCIe x4 connector from on board Clock Synthesizer. This PCIe x4 connector (J19) is physically located at the top of the board as shown below.

*Note: For more details on Channel selection options, refer **Table 3**.*

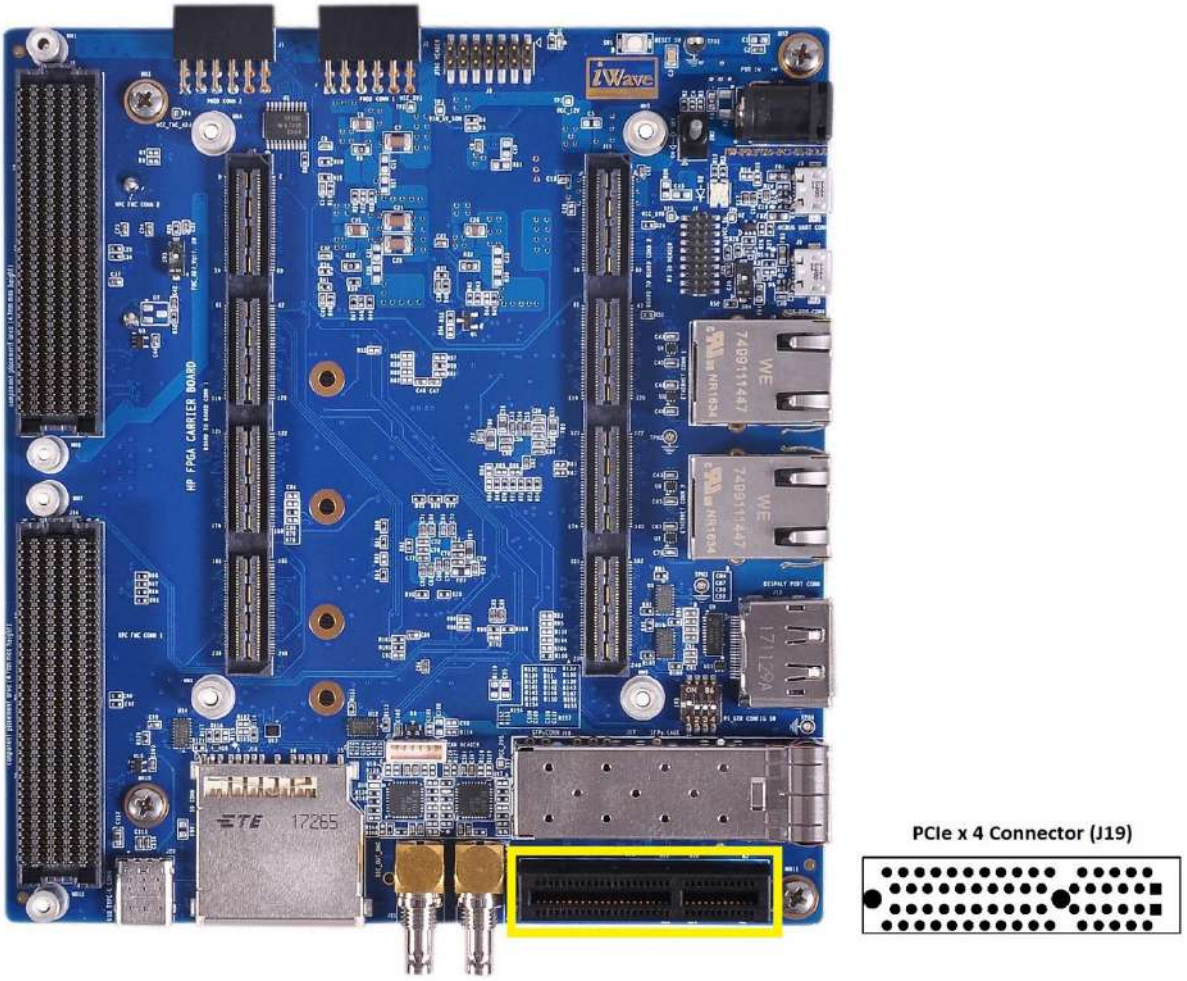


Figure 11: PCIe x4 Connector

Note: In iWave Arria10 SoC/FPGA DevKit Supports only One PCIex1.

Table 5: PCIe x4 Connector Pin Assignment

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	PRSNT1#	NA	NA	Default Grounded.
2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
3	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
4	GND	GND	Power	Ground.
5	TCK	NA	NA	NC.
6	TDI	NA	NA	NC.
7	TDO	NA	NA	NC.
8	TMS	NA	NA	NC.
9	+3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
10	+3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
11	PERST#	FPGA_AP9_LVDS3A_22p	O, 3.3V CMOS	PCIe Reset through FPGA IO.
12	GND	GND	Power	Ground.
13	REFCLK+	PCIe_REFCLKP	O, DIFF	100MHz PCIe Reference Clock positive.
14	REFCLK-	PCIe_REFCLKn	O, DIFF	100MHz PCIe Reference Clock negative.
15	GND	GND	Power	Ground.
16	PERp0	GXBL1C_RX_CH4p	I, DIFF	PCIe Lane0 Receive pair positive.
17	PERn0	GXBL1C_RX_CH4n	I, DIFF	PCIe Lane0 Receive pair negative.
18	GND	GND	Power	Ground.
19	RSVD	NA	NA	NC.
20	GND	GND	Power	Ground.
21	PERp1	GXBL1D_RX_CH4p	NA	PCIe Lane1 Receive pair positive.
22	PERn1	GXBL1D_RX_CH4n	NA	PCIe Lane1 Receive pair negative
23	GND	GND	Power	Ground.
24	GND	GND	Power	Ground.
25	PERp2	GXBL1E_RX_CH4p	NA	PCIe Lane2 Receive pair positive.
26	PERn2	GXBL1E_RX_CH4n	NA	PCIe Lane2 Receive pair negative.
27	GND	GND	Power	Ground.
28	GND	GND	Power	Ground.
29	PERp3	GXBL1F_RX_CH4p	NA	PCIe Lane3 Receive pair positive.
30	PERn3	GXBL1F_RX_CH4n	NA	PCIe Lane3 Receive pair negative.
31	GND	GND	Power	Ground.
32	RSVD	NA	NA	NC.
33	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
34	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
35	RSVD	NA	NA	NC.
36	GND	GND	Power	Ground.
37	SMCLK	HPS_GPIO0_IO5/I2C0_SCL	O, 3.3V CMOS	SMB Clock.
38	SMDAT	HPS_GPIO0_IO4/I2C0_SDA	IO, 3.3V CMOS	SMB DATA.
39	GND	GND	Power	Ground.
40	+3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
41	TRST#	NA	NA	NC.
42	3V3AUX	VCC_3V3_AUX	O, 3.3V Power	3.3V Supply Voltage
43	WAKE#	FPGA_AN9_LVDS3A_22n	O, 3.3V CMOS	PCIe Wake through FPGA IO.
44	RSVD	NA	NA	NC.
45	GND	GND	Power	Ground.
46	PETp0	GXBL1C_TX_CH4p	O, DIFF	PCIe Lane0 Transmit pair positive.
47	PETn0	GXBL1C_TX_CH4n	O, DIFF	PCIe Lane0 Transmit pair negative.
48	GND	GND	Power	Ground.
49	PRSNT2	NA	NA	NC.
50	GND	GND	Power	Ground.
51	PETp1	GXBL1D_TX_CH4p	NA	PCIe Lane1 Transmit pair positive.
52	PETn1	GXBL1D_TX_CH4n	NA	PCIe Lane1 Transmit pair negative
53	GND	GND	Power	Ground.
54	GND	GND	Power	Ground.
55	PETp2	GXBL1E_TX_CH4p	NA	PCIe Lane2 Transmit pair positive.
56	PETn2	GXBL1E_TX_CH4n	NA	PCIe Lane2 Transmit pair negative
57	GND	GND	Power	Ground.
58	GND	GND	Power	Ground.
59	PETp3	GXBL1F_TX_CH4p	NA	PCIe Lane3 Transmit pair positive.
60	PETn3	GXBL1F_TX_CH4n	NA	PCIe Lane3 Transmit pair negative
61	GND	GND	Power	Ground.
62	RSVD	NA	NA	NC.
63	PRSNT#2	NA	NA	NC.
64	GND	GND	Power	Ground.

2.5.1.3 FMC HPC Connector1

The Arria10 SoC/FPGA Carrier board supports two 400Pin Standard FMC HPC connectors to support standard ANSI/VITA 57.1 FMC modules. These FMC HPC connectors can accept two Single width FMC modules or one double width FMC module.

Number of Pins - 400
Connector Part Number - ASP-134486-01
Mating Connector - ASP-134488-01 from Samtec

The FMC HPC Connector1 (J14) supports the below mentioned interface from Arria10 SoC/FPGA.

- 8 High Speed Transceivers
- 2 High Speed Transmitter (TX)
- 21 LVDS IOs
- 22 Single ended (SE) IOs
- 3 Clock Input Capable LVDS/SE pins
- 2 Clock Output Capable LVDS/SE pins

This 400Pin FMC HPC connector1 (J14) is physically located at the top of the board as shown below.

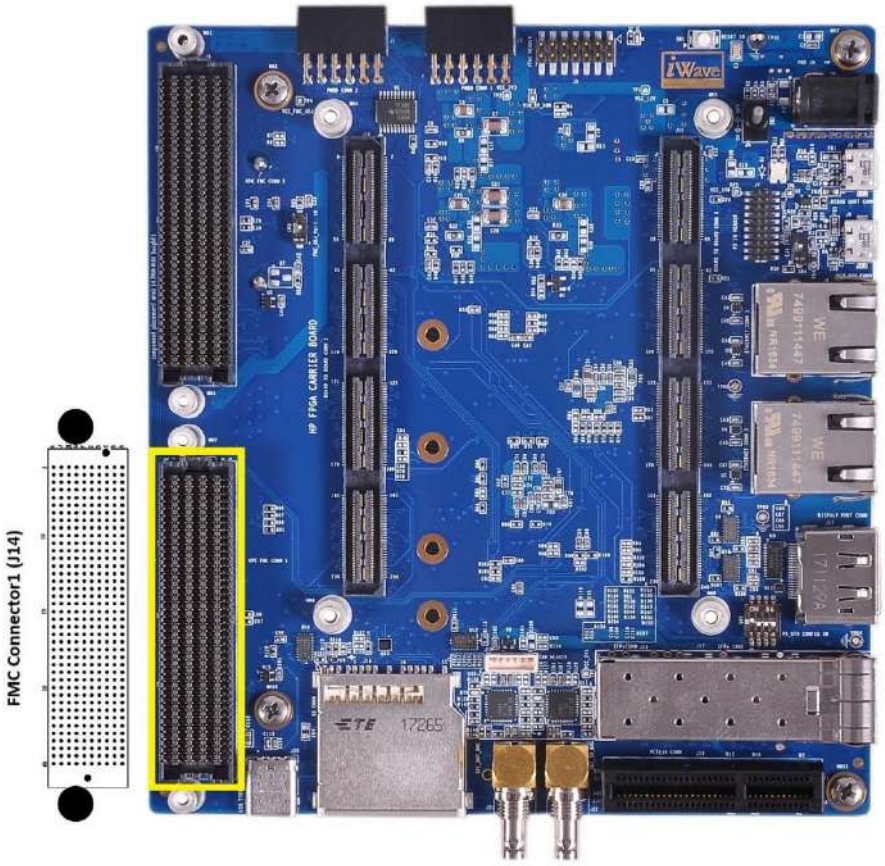


Figure 12: FMC Connector1

This 400Pin FMC HPC connector1 (J14) pin mapping is shown below.

	K	J	H	G	F	E	D	C	B	A
1	NC	GND	NC	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	CLK1_C2M_P	PRSNT_M2C_L	CLK0_C2M_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK1_C2M_N	GND	CLK0_C2M_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	NC	GND	NC	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	NC	GND
5	NC	GND	NC	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	NC	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	NC	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	NC	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	NC	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	NC	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	NC	GND	LA12_P	GND	NC	LA09_N	LA10_N	GND	DP4_M2C_N
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	DP6_M2C_P	GND
17	NC	GND	LA11_N	GND	NC	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	NC	LA13_N	LA14_P	GND	DP5_M2C_P
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	GND	DP5_M2C_N
20	NC	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	NC	GND	LA20_P	GND	NC	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	GND	DP1_C2M_P
23	NC	GND	LA19_N	GND	NC	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	NC	GND	LA22_P	GND	NC	LA23_N	GND	DP9_C2M_P	GND
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	DP9_C2M_N	GND
26	NC	GND	LA21_N	GND	NC	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	NC	GND	LA25_P	GND	NC	LA26_N	LA27_N	GND	DP2_C2M_N
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	DP8_C2M_P	GND
29	NC	GND	LA24_N	GND	NC	GND	TCK	GND	DP8_C2M_N	GND
30	GND	NC	GND	LA29_P	GND	NC	TDI	SCL	GND	DP3_C2M_P
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	GND	DP3_C2M_N
32	NC	GND	LA28_N	GND	NC	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	NC	GND	LA31_P	GND	NC	TMS	GND	DP7_C2M_N	GND
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	GND	DP4_C2M_P
35	NC	GND	LA30_N	GND	NC	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	NC	GND	LA33_P	GND	NC	3P3V	GND	DP6_C2M_P	GND
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	DP6_C2M_N	GND
38	NC	GND	LA32_N	GND	NC	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	NC	GND	VADJ	GND15	VADJ	GND	3P3V	GND	NC	GND

Figure 13: FMC HPC Connector1 Pin Out

Table 6: FMC HPC Connector1 Pin Assignment

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
A1	GND	GND	Power	Ground.
A2	DP1_M2C_P	GXBL1C_RX_CH1p	I, DIFF	Bank 1C channel1 High speed differential receiver positive. This Pin is connected to 17th pin of Board to Board Connector1 (J10).
A3	DP1_M2C_N	GXBL1C_RX_CH1n	I, DIFF	Bank 1C channel1 High speed differential receiver negative. This Pin is connected to 15th pin of Board to Board Connector1 (J10).
A4	GND	GND	Power	Ground.
A5	GND	GND	Power	Ground.
A6	DP2_M2C_P	GXBL1C_RX_CH2p	I, DIFF	Bank 1C channel2 High speed differential receiver positive. This Pin is connected to 57th pin of Board to Board Connector1 (J10).
A7	DP2_M2C_N	GXBL1C_RX_CH2n	I, DIFF	Bank 1C channel2 High speed differential receiver negative. This Pin is connected to 55th pin of Board to Board Connector1 (J10).
A8	GND	GND	Power	Ground.

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
A9	GND	GND	Power	Ground.
A10	DP3_M2C_P	GXBL1C_RX_CH3p	I, DIFF	Bank 1C channel3 High speed differential receiver positive. This Pin is connected to 51st pin of Board to Board Connector1 (J10).
A11	DP3_M2C_N	GXBL1C_RX_CH3n	I, DIFF	Bank 1C channel3 High speed differential receiver negative. This Pin is connected to 49th pin of Board to Board Connector1 (J10).
A12	GND	GND	Power	Ground.
A13	GND	GND	Power	Ground.
A14	DP4_M2C_P	GXBL1D_RX_CH0p	I, DIFF	Bank 1D channel0 High speed differential receiver positive. This Pin is connected to 117th pin of Board to Board Connector1 (J10).
A15	DP4_M2C_N	GXBL1D_RX_CH0n	I, DIFF	Bank 1D channel0 High speed differential receiver negative. This Pin is connected to 115th pin of Board to Board Connector1 (J10).
A16	GND	GND	Power	Ground.
A17	GND	GND	Power	Ground.
A18	DP5_M2C_P	GXBL1D_RX_CH1p	I, DIFF	Bank 1D channel1 High speed differential receiver positive. This Pin is connected to 111st pin of Board to Board Connector1 (J10).
A19	DP5_M2C_N	GXBL1D_RX_CH1n	I, DIFF	Bank 1D channel1 High speed differential receiver negative. This Pin is connected to 109th pin of Board to Board Connector1 (J10).
A20	GND	GND	Power	Ground.
A21	GND	GND	Power	Ground.
A22	DP1_C2M_P	GXBL1C_TX_CH1p	O, DIFF	Bank 1C channel1 High speed differential transmitter positive. This Pin is connected to 9th pin of Board to Board Connector1 (J10).
A23	DP1_C2M_N	GXBL1C_TX_CH1n	O, DIFF	Bank 1C channel1 High speed differential transmitter negative. This Pin is connected to 11th pin of Board to Board Connector1 (J10).
A24	GND	GND	Power	Ground.
A25	GND	GND	Power	Ground.
A26	DP2_C2M_P	GXBL1C_TX_CH2p	O, DIFF	Bank 1C channel2 High speed differential transmitter positive. This Pin is connected to 37th pin of Board to Board Connector1 (J10).

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
A27	DP2_C2M_N	GXBL1C_TX_CH2n	O, DIFF	Bank 1C channel2 High speed differential transmitter negative. This Pin is connected to 39th pin of Board to Board Connector1 (J10).
A28	GND	GND	Power	Ground.
A29	GND	GND	Power	Ground.
A30	DP3_C2M_P	GXBL1C_TX_CH3p	O, DIFF	Bank 1C channel3 High speed differential transmitter positive. This Pin is connected to 43rd pin of Board to Board Connector1 (J10).
A31	DP3_C2M_N	GXBL1C_TX_CH3n	O, DIFF	Bank 1C channel3 High speed differential transmitter negative. This Pin is connected to 45th pin of Board to Board Connector1 (J10).
A32	GND	GND	Power	Ground.
A33	GND	GND	Power	Ground.
A34	DP4_C2M_P	GXBL1D_TX_CH0p	O, DIFF	Bank 1D channel0 High speed differential transmitter positive. This Pin is connected to 97th pin of Board to Board Connector1 (J10).
A35	DP4_C2M_N	GXBL1D_TX_CH0n	O, DIFF	Bank 1D channel0 High speed differential transmitter negative. This Pin is connected to 99th pin of Board to Board Connector1 (J10).
A36	GND	GND	Power	Ground.
A37	GND	GND	Power	Ground.
A38	DP5_C2M_P	GXBL1D_TX_CH1p	O, DIFF	Bank 1D channel1 High speed differential transmitter positive. This Pin is connected to 103rd pin of Board to Board Connector1 (J10).
A39	DP5_C2M_N	GXBL1D_TX_CH1n	O, DIFF	Bank 1D channel1 High speed differential transmitter negative. This Pin is connected to 105th pin of Board to Board Connector1 (J10).
A40	GND	GND	Power	Ground.
B1	CLK_DIR	FPGA_AE17_LVDS2A_19n	IO, 3.3V CMOS	Bank 2A IO19 Single Ended pin. This Pin is connected to 168th pin of Board to Board Connector1 (J10) through level translator.
B2	GND	GND	Power	Ground.
B3	GND	GND	Power	Ground.
B4	DP9_M2C_P	NA	NA	NC.
B5	DP9_M2C_N	NA	NA	NC.
B6	GND	GND	Power	Ground.

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
B7	GND	GND	Power	Ground.
B8	DP8_M2C_P	NA	NA	NC.
B9	DP8_M2C_N	NA	NA	NC.
B10	GND	GND	Power	Ground.
B11	GND	GND	Power	Ground.
B12	DP7_M2C_P	GXBL1D_RX_CH3p	I, DIFF	Bank 1D channel3 High speed differential receiver positive. This Pin is connected to 137th pin of Board to Board Connector1 (J10).
B13	DP7_M2C_N	GXBL1D_RX_CH3n	I, DIFF	Bank 1D channel3 High speed differential receiver negative. This Pin is connected to 135th pin of Board to Board Connector1 (J10).
B14	GND	GND	Power	Ground.
B15	GND	GND	Power	Ground.
B16	DP6_M2C_P	GXBL1D_RX_CH2p	I, DIFF	Bank 1D channel2 High speed differential receiver positive. This Pin is connected to 143rd pin of Board to Board Connector1 (J10).
B17	DP6_M2C_N	GXBL1D_RX_CH2n	I, DIFF	Bank 1D channel2 High speed differential receiver negative. This Pin is connected to 141st pin of Board to Board Connector1 (J10).
B18	GND	GND	Power	Ground.
B19	GND	GND	Power	Ground.
B20	GBTCLK1_M2C_P	REFCLK_GXBL1D_CHTp	I, DIFF	Bank 1D differential reference clock top positive. This Pin is connected to 98th pin of Board to Board Connector1 (J10)
B21	GBTCLK1_M2C_N	REFCLK_GXBL1D_CHTn	I, DIFF	Bank 1D differential reference clock top negative. This Pin is connected to 100th pin of Board to Board Connector1 (J10).
B22	GND	GND	Power	Ground.
B23	GND	GND	Power	Ground.
B24	DP9_C2M_P	GXBL1D_TX_CH5p	O, DIFF	Bank 1D channel5 High speed differential transmitter positive. This Pin is connected to 163rd pin of Board to Board Connector1 (J10).
B25	DP9_C2M_N	GXBL1D_TX_CH5n	O, DIFF	Bank 1D channel5 High speed differential transmitter negative. This Pin is connected to 165th pin of Board to Board Connector1 (J10).
B26	GND	GND	Power	Ground.
B27	GND	GND	Power	Ground.

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
B28	DP8_C2M_P	GXBL1C_TX_CH5p	O, DIFF	Bank 1C channel5 High speed differential transmitter positive. This Pin is connected to 69th pin of Board to Board Connector1 (J10).
B29	DP8_C2M_N	GXBL1C_TX_CH5n	O, DIFF	Bank 1C channel5 High speed differential transmitter negative. This Pin is connected to 71st pin of Board to Board Connector1 (J10).
B30	GND	GND	Power	Ground.
B31	GND	GND	Power	Ground.
B32	DP7_C2M_P	GXBL1D_TX_CH3p	O, DIFF	Bank 1D channel3 High speed differential transmitter positive. This Pin is connected to 129th pin of Board to Board Connector1 (J10).
B33	DP7_C2M_N	GXBL1D_TX_CH3n	O, DIFF	Bank 1D channel3 High speed differential transmitter negative. This Pin is connected to 131st pin of Board to Board Connector1 (J10).
B34	GND	GND	Power	Ground.
B35	GND	GND	Power	Ground.
B36	DP6_C2M_P	GXBL1D_TX_CH2p	O, DIFF	Bank 1D channel2 High speed differential transmitter positive. This Pin is connected to 123rd pin of Board to Board Connector1 (J10).
B37	DP6_C2M_N	GXBL1D_TX_CH2n	O, DIFF	Bank 1D channel2 High speed differential transmitter negative. This Pin is connected to 125th pin of Board to Board Connector1 (J10).
B38	GND	GND	Power	Ground.
B39	GND	GND	Power	Ground.
B40	RES0	NA	NA	NC.
C1	GND	GND	Power	Ground.
C2	DP0_C2M_P	GXBL1C_TX_CH0p	O, DIFF	Bank 1C channel0 High speed differential transmitter positive. This Pin is connected to 3rd pin of Board to Board Connector1 (J10).
C3	DP0_C2M_N	GXBL1C_TX_CH0n	O, DIFF	Bank 1C channel0 High speed differential transmitter negative. This Pin is connected to 5th pin of Board to Board Connector1 (J10).
C4	GND	GND	Power	Ground.
C5	GND	GND	Power	Ground.

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
C6	DP0_M2C_P	GXBL1C_RX_CH0p	I, DIFF	Bank 1C channel0 High speed differential receiver positive. This Pin is connected to 23rd pin of Board to Board Connector1 (J10).
C7	DP0_M2C_N	GXBL1C_RX_CH0n	I, DIFF	Bank 1C channel0 High speed differential receiver negative. This Pin is connected to 21st pin of Board to Board Connector1 (J10).
C8	GND	GND	Power	Ground.
C9	GND	GND	Power	Ground.
C10	LA06_P	FPGA_Y1_LVDS3C_23p	IO, 1.8V LVDS	Bank 3C IO23 differential positive. This Pin is connected to 139th pin of Board to Board Connector2 (J11).
C11	LA06_N	FPGA_Y2_LVDS3C_23n	IO, 1.8V LVDS	Bank 3C IO23 differential negative. This Pin is connected to 141st pin of Board to Board Connector2 (J11).
C12	GND	GND	Power	Ground.
C13	GND	GND	Power	Ground.
C14	LA10_P	FPGA_V2_LVDS3C_11p	IO, 1.8V LVDS	Bank 3C IO11 differential positive. This Pin is connected to 147th pin of Board to Board Connector2 (J11).
C15	LA10_N	FPGA_U2_LVDS3C_11n	IO, 1.8V LVDS	Bank 3C IO11 differential negative. This Pin is connected to 149th pin of Board to Board Connector2 (J11).
C16	GND	GND	Power	Ground.
C17	GND	GND	Power	Ground.
C18	LA14_P	FPGA_Y8_LVDS3C_14p	IO, 1.8V LVDS	Bank 3C IO14 differential positive. This Pin is connected to 156th pin of Board to Board Connector2 (J11).
C19	LA14_N	FPGA_Y9_LVDS3C_14n	IO, 1.8V LVDS	Bank 3C IO14 differential negative. This Pin is connected to 158th pin of Board to Board Connector2 (J11).
C20	GND	GND	Power	Ground.
C21	GND	GND	Power	Ground.
C22	LA18_P_CC	FPGA_AJ9_LVDS3A_12 p/CLKIN_1p	IO, 1.8V LVDS	Bank 3A IO12 differential positive. This pin can be configured as clock input1 positive. This Pin is connected to 84th pin of Board to Board Connector1 (J10).
C23	LA18_N_CC	FPGA_AK9_LVDS3A_12 n/CLKIN_1n	IO, 1.8V LVDS	Bank 3A IO12 differential negative. This pin can be configured as clock input1 negative. This Pin is connected to 82nd pin of Board to Board Connector1 (J10).

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
C24	GND	GND	Power	Ground.
C25	GND	GND	Power	Ground.
C26	LA27_P	FPGA_AC8_LVDS3B_10p/CLKOUT_1p	IO, 1.8V LVDS	Bank 3B IO10 differential positive. This pin can be configured as clock output1 positive. This Pin is connected to 110th pin of Board to Board Connector2 (J11).
C27	LA27_N	FPGA_AD9_LVDS3B_10n/CLKOUT_1n	IO, 1.8V LVDS	Bank 3B IO10 differential negative. This pin can be configured as clock output1 negative. This Pin is connected to 112nd pin of Board to Board Connector2 (J11).
C28	GND	GND	Power	Ground.
C29	GND	GND	Power	Ground.
C30	SCL	HPS_GPIO0_IO5/I2C0_SCL	IO, 3.3V LVCMOS	I2C0 Clock Signal through Voltage Level Translator.
C31	SDA	HPS_GPIO0_IO4/I2C0_SDA	IO, 3.3V LVCMOS	I2C0 Data Signal through Voltage Level Translator.
C32	GND	GND	Power	Ground.
C33	GND	GND	Power	Ground.
C34	GA0	GA0	1K, PU	Geographical address 0
C35	12P0V	VCC_12V	O, 12V Power	Supply Voltage.
C36	GND	GND	Power	Ground.
C37	12P0V	VCC_12V	O, 12V Power	Supply Voltage.
C38	GND	GND	Power	Ground.
C39	3P3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
C40	GND	GND	Power	Ground.
D1	PG_C2M	PG_C2M	O, 3.3V	Power Good Signal from Carrier to FMC Module. This Pin is connected from the Power good signal of VCC_FMC_ADJ voltage regulator(U27).
D2	GND	GND	Power	Ground.
D3	GND	GND	Power	Ground.
D4	GBTCLK0_M2C_P	REFCLK_GXBL1C_CHTp	I, DIFF	Bank 1C differential reference clock top positive. This Pin is connected to 4th pin of Board to Board Connector1 (J10).
D5	GBTCLK0_M2C_N	REFCLK_GXBL1C_CHTn	I, DIFF	Bank 1C differential reference clock top negative. This Pin is connected to 6th pin of Board to Board Connector1 (J10).
D6	GND	GND	Power	Ground.
D7	GND	GND	Power	Ground.

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
D8	LA01_P_CC	FPGA_AE2_LVDS3B_13p	IO, 1.8V LVDS	Bank 3B IO13 differential positive. This pin can be configured as clock input0 positive. This Pin is connected to 116th pin of Board to Board Connector2 (J11).
D9	LA01_N_CC	FPGA_AE3_LVDS3B_13n	IO, 1.8V LVDS	Bank 3B IO13 differential negative. This pin can be configured as clock input0 negative. This Pin is connected to 178th pin of Board to Board Connector2 (J11).
D10	GND	GND	Power	Ground.
D11	LA05_P	FPGA_U3_LVDS3C_9p	IO, 1.8V LVDS	Bank 3C IO9 differential positive. This Pin is connected to 145th pin of Board to Board Connector2 (J11).
D12	LA05_N	FPGA_V3_LVDS3C_9n	IO, 1.8V LVDS	Bank 3C IO9 differential negative. This Pin is connected to 143rd pin of Board to Board Connector2 (J11).
D13	GND	GND	Power	Ground.
D14	LA09_P	FPGA_R1_LVDS3C_8p	IO,1.8V LVDS	Bank 3C IO8 differential positive. This Pin is connected to 159th pin of Board to Board Connector2 (J11).
D15	LA09_N	FPGA_P1_LVDS3C_8n	IO, 1.8V LVDS	Bank 3C IO8 differential negative. This Pin is connected to 161st pin of Board to Board Connector2 (J11).
D16	GND	GND	Power	Ground.
D17	LA13_P	FPGA_T4_LVDS3C_1p	IO, 1.8V LVDS	Bank 3C IO1 differential positive. This Pin is connected to 155th pin of Board to Board Connector2 (J11).
D18	LA13_N	FPGA_R4_LVDS3C_1n	IO, 1.8V LVDS	Bank 3C IO1 differential negative. This Pin is connected to 157th pin of Board to Board Connector2 (J11).
D19	GND	GND	Power	Ground.
D20	LA17_P_CC	FPGA_AL5_LVDS3A_13p/CLKIN_0p	IO, 1.8V LVDS	Bank 3A IO13 differential positive. This pin can be configured as clock input0 positive. This Pin is connected to 58th pin of Board to Board Connector1 (J10).
D21	LA17_N_CC	FPGA_AL4_LVDS3A_13n/CLKIN_0n	IO, 1.8V LVDS	Bank 3A IO13 differential negative. This pin can be configured as clock input0 negative. This Pin is connected to 56th pin of Board to Board Connector1 (J10).
D22	GND	GND	Power	Ground.

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
D23	LA23_P	FPGA_T3_LVDS3C_3p	IO, 1.8V LVDS	Bank 3C IO3 differential positive. This Pin is connected to 162nd pin of Board to Board Connector2 (J11).
D24	LA23_N	FPGA_R3_LVDS3C_3n	IO, 1.8V LVDS	Bank 3C IO3 differential negative. This Pin is connected to 160th pin of Board to Board Connector2 (J11).
D25	GND	GND	Power	Ground.
D26	LA26_P	FPGA_AF8_LVDS3A_2p	IO, 1.8V LVDS	Bank 3A IO2 differential positive. This Pin is connected to 91th pin of Board to Board Connector1 (J10).
D27	LA26_N	FPGA_AE8_LVDS3A_2n	IO, 1.8V LVDS	Bank 3A IO2 differential negative. This Pin is connected to 93rd pin of Board to Board Connector1 (J10).
D28	GND	GND	Power	Ground.
D29	TCK	CSS_TCK	I, 3.3V CMOS/ 49.9K PU	JTAG Test Clock This Pin is connected to 31st pin of Board to Board Connector2 (J11) through Voltage level translator.
D30	TDI	JTAG_TDO	O, 3.3V CMOS	JTAG Test Data Output
D31	TDO	JTAG_TDI	I, 3.3V CMOS	JTAG Test Data Input.
D32	3P3VAUX	3V3_AUX1	O, 3.3V Power	Supply Voltage.
D33	TMS	CSS_TMS	I, 3.3V CMOS/ 49.9K PU	JTAG Test Mode Select This Pin is connected to 29th pin of Board to Board Connector2 (J11) through Voltage level translator.
D34	TRST_L	CSS_TRST	I, 3.3V CMOS	JTAG Test Reset This Pin is connected to 25th pin of Board to Board Connector2 (J11) through Voltage level translator.
D35	GA1	GA1	1K, PD	Geographical address 1
D36	3P3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
D37	GND	GND	Power	Ground.
D38	3P3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
D39	GND	GND	Power	Ground.
D40	3P3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
E1	GND	GND	Power	Ground.
E2	HA01_P_CC	FPGA_AM17_LVDS2A_8p	IO, 1.8V LVDS	Bank 2A IO8 differential positive. This Pin is connected to 204th pin of Board to Board Connector1 (J10).
E3	HA01_N_CC	FPGA_AN17_LVDS2A_8n	IO, 1.8V LVDS	Bank 2A IO8 differential negative. This Pin is connected to 202th pin of Board to Board Connector1 (J10).
E4	GND	GND	Power	Ground.

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
E5	GND	GND	Power	Ground.
E6	HA05_P	FPGA_AJ15_LVDS2A_17p	IO, 1.8V LVDS	Bank 2A IO17 differential positive. This Pin is connected to 154th pin of Board to Board Connector1 (J10).
E7	HA05_N	FPGA_AH15_LVDS2A_17n	IO, 1.8V LVDS	Bank 2A IO17 differential negative. This Pin is connected to 152nd pin of Board to Board Connector1 (J10).
E8	GND	GND	Power	Ground.
E9	HA09_P	FPGA_AD19_LVDS2A_21p	IO, 1.8V LVDS	Bank 2A IO21 differential positive. This Pin is connected to 128th pin of Board to Board Connector1 (J10).
E10	HA09_N	FPGA_AE18_LVDS2A_21n	IO, 1.8V LVDS	Bank 2A IO21 differential negative. This Pin is connected to 134th pin of Board to Board Connector1 (J10).
E11	GND	GND	Power	Ground.
E12	HA13_P	NA	NA	NC.
E13	HA13_N	NA	NA	NC.
E14	GND	GND	Power	Ground.
E15	HA16_P	NA	NA	NC.
E16	HA16_N	NA	NA	NC.
E17	GND	GND	Power	Ground.
E18	HA20_P	NA	NA	NC.
E19	HA20_N	NA	NA	NC.
E20	GND	GND	Power	Ground.
E21	HB03_P	NA	NA	NC.
E22	HB03_N	NA	NA	NC.
E23	GND	GND	Power	Ground.
E24	HB05_P	NA	NA	NC.
E25	HB05_N	NA	NA	NC.
E26	GND	GND	Power	Ground.
E27	HB09_P	NA	NA	NC.
E28	HB09_N	NA	NA	NC.
E29	GND	GND	Power	Ground.
E30	HB13_P	NA	NA	NC.
E31	HB13_N	NA	NA	NC.
E32	GND	GND	Power	Ground.
E33	HB19_P	NA	NA	NC.
E34	HB19_N	NA	NA	NC.
E35	GND	GND	Power	Ground.
E36	HB21_P	NA	NA	NC.
E37	HB21_N	NA	NA	NC.
E38	GND	GND	Power	Ground.

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
E39	VADJ	VCC_FMC_ADJ	O, 1.8V Power	Supply Voltage.
E40	GND	GND	Power	Ground.
F1	PG_M2C	IOEXP_P17_PG_M2C1	O,3.3V/ 10K PU	Power Good Signal from FMC Module to Carrier. This Pin is connected to 20th pin of IO Expander (U40).
F2	GND	GND	Power	Ground.
F3	GND	GND	Power	Ground.
F4	HA00_P_CC	FPGA_AH18_LVDS2A_ 13p/CLKIN_0p	IO, 1.8V LVDS	Bank 2A IO13 differential positive. This pin can be configured as clock input0 positive. This Pin is connected to 130th pin of Board to Board Connector1 (J10).
F5	HA00_N_CC	FPGA_AH19_LVDS2A_ 13n/CLKIN_0n	IO, 1.8V LVDS	Bank 2A IO13 differential negative. This pin can be configured as clock input0 negative. This Pin is connected to 132nd pin of Board to Board Connector1 (J10).
F6	GND	GND	Power	Ground.
F7	HA04_P	FPGA_AF11_LVDS3A_5 p	IO, 1.8V LVDS	Bank 3A IO5 differential positive. This Pin is connected to 108th pin of Board to Board Connector1 (J10).
F8	HA04_N	FPGA_AG11_LVDS3A_ 5n	IO, 1.8V LVDS	Bank 3A IO5 differential negative. This Pin is connected to 106th pin of Board to Board Connector1 (J10).
F9	GND	GND	Power	Ground.
F10	HA08_P	FPGA_AK18_LVDS2A_1 1p	IO, 1.8V LVDS	Bank 2A IO11 differential positive. This Pin is connected to 153rd pin of Board to Board Connector1 (J10).
F11	HA08_N	FPGA_AL18_LVDS2A_1 1n	IO, 1.8V LVDS	Bank 2A IO11 differential negative. This Pin is connected to 151st pin of Board to Board Connector1 (J10).
F12	GND	GND	Power	Ground.
F13	HA12_P	FPGA_AG16_LVDS2A_ 20p	IO, 1.8V LVDS	Bank 2A IO20 differential positive. This Pin is connected to 164th pin of Board to Board Connector1 (J10).
F14	HA12_N	FPGA_AF16_LVDS2A_2 0n	IO, 1.8V LVDS	Bank 2A IO20 differential negative. This Pin is connected to 166th pin of Board to Board Connector1 (J10).
F15	GND	GND	Power	Ground.
F16	HA15_P	NA	NA	NC.
F17	HA15_N	NA	NA	NC.
F18	GND	GND	Power	Ground.
F19	HA19_P	NA	NA	NC.

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
F20	HA19_N	FPGA_AM7_LVDS3A_24n	IO, 1.8V LVCMOS	Bank 3A IO24 Single Ended pin. This Pin is connected to 10th pin of Board to Board Connector1 (J10).
F21	GND	GND	Power	Ground.
F22	HB02_P	NA	NA	NC.
F23	HB02_N	NA	NA	NC.
F24	GND	GND	Power	Ground.
F25	HB04_P	NA	NA	NC.
F26	HB04_N	NA	NA	NC.
F27	GND	GND	Power	Ground.
F28	HB08_P	NA	NA	NC.
F29	HB08_N	NA	NA	NC.
F30	GND	GND	Power	Ground.
F31	HB12_P	NA	NA	NC.
F32	HB12_N	NA	NA	NC.
F33	GND	GND	Power	Ground.
F34	HB16_P	NA	NA	NC.
F35	HB16_N	NA	NA	NC.
F36	GND	GND	Power	Ground.
F37	HB20_P	NA	NA	NC.
F38	HB20_N	NA	NA	NC.
F39	GND	GND	Power	Ground.
F40	VADJ	VCC_FMC_ADJ	O, 1.8V Power	Supply Voltage.
G1	GND	GND	Power	Ground.
G2	CLK1_M2C_P	FPGA_U1_LVDS3C_10p/CLKOUT_1p	IO, 1.8V LVDS	Bank 3C IO10 differential positive. This pin can be configured as clock output1 positive. This Pin is connected to 169th pin of Board to Board Connector2 (J11).
G3	CLK1_M2C_N	FPGA_T1_LVDS3C_10n/CLKOUT_1n	IO, 1.8V LVDS	Bank 3C IO10 differential negative. This pin can be configured as clock output1 negative. This Pin is connected to 171st pin of Board to Board Connector2 (J11).
G4	GND	GND	Power	Ground.
G5	GND	GND	Power	Ground.
G6	LA00_P_CC	FPGA_W1_LVDS3C_12p/CLKIN_1p	IO, 1.8V LVDS	Bank 3C IO12 differential positive. This pin can be configured as clock input1 positive. This Pin is connected to 175th pin of Board to Board Connector2 (J11).

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
G7	LA00_N_CC	FPGA_W2_LVDS3C_12n/CLKIN_1n	IO, 1.8V LVDS	Bank 3C IO12 differential negative. This pin can be configured as clock input1 negative. This Pin is connected to 177th pin of Board to Board Connector2 (J11).
G8	GND	GND	Power	Ground.
G9	LA03_P	FPGA_AA3_LVDS3C_20p	IO, 1.8V LVDS	Bank 3C IO20 differential positive. This Pin is connected to 135th pin of Board to Board Connector2 (J11).
G10	LA03_N	FPGA_AA4_LVDS3C_20n	IO, 1.8V LVDS	Bank 3C IO20 differential negative. This Pin is connected to 137th pin of Board to Board Connector2 (J11).
G11	GND	GND	Power	Ground.
G12	LA08_P	FPGA_AA8_LVDS3C_17p	IO, 1.8V LVDS	Bank 3C IO17 differential positive. This Pin is connected to 140th pin of Board to Board Connector2 (J11).
G13	LA08_N	FPGA_AA9_LVDS3C_17n	IO, 1.8V LVDS	Bank 3C IO17 differential negative. This Pin is connected to 142nd pin of Board to Board Connector2 (J11).
G14	GND	GND	Power	Ground.
G15	LA12_P	FPGA_V5_LVDS3C_6p	IO, 1.8V LVDS	Bank 3C IO6 differential positive. This Pin is connected to 148th pin of Board to Board Connector2 (J11).
G16	LA12_N	FPGA_V4_LVDS3C_6n	IO, 1.8V LVDS	Bank 3C IO6 differential negative. This Pin is connected to 150th pin of Board to Board Connector2 (J11).
G17	GND	GND	Power	Ground.
G18	LA16_P	FPGA_P4_LVDS3C_2p	IO, 1.8V LVDS	Bank 3C IO2 differential positive. This Pin is connected to 164th pin of Board to Board Connector2 (J11).
G19	LA16_N	FPGA_P5_LVDS3C_2n	IO, 1.8V LVDS	Bank 3C IO2 differential negative. This Pin is connected to 166th pin of Board to Board Connector2 (J11).
G20	GND	GND	Power	Ground.
G21	LA20_P	FPGA_Y3_LVDS3C_19p	IO, 1.8V LVDS	Bank 3C IO19 differential positive. This Pin is connected to 144th pin of Board to Board Connector2 (J11).
G22	LA20_N	FPGA_Y4_LVDS3C_19n	IO, 1.8V LVDS	Bank 3C IO19 differential negative. This Pin is connected to 146th pin of Board to Board Connector2 (J11).
G23	GND	GND	Power	Ground.
G24	LA22_P	FPGA_T5_LVDS3C_4p	IO, 1.8V LVDS	Bank 3C IO4 differential positive. This Pin is connected to 183rd pin of Board to Board Connector2 (J11).

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
G25	LA22_N	FPGA_T6_LVDS3C_4n	IO, 1.8V LVDS	Bank 3C IO4 differential negative. This Pin is connected to 181st pin of Board to Board Connector2 (J11).
G26	GND	GND	Power	Ground.
G27	LA25_P	FPGA_AJ7_LVDS3A_11p	IO, 1.8V LVDS	Bank 3A IO11 differential positive. This Pin is connected to 44th pin of Board to Board Connector1 (J10).
G28	LA25_N	FPGA_AJ6_LVDS3A_11n	IO, 1.8V LVDS	Bank 3A IO11 differential negative. This Pin is connected to 42nd pin of Board to Board Connector1 (J10).
G29	GND	GND	Power	Ground.
G30	LA29_P	FPGA_AL6_LVDS3A_14p	IO, 1.8V LVDS	Bank 3A IO14 differential positive. This Pin is connected to 32nd pin of Board to Board Connector1 (J10).
G31	LA29_N	FPGA_AK6_LVDS3A_14n	IO, 1.8V LVDS	Bank 3A IO14 differential negative. This Pin is connected to 34th pin of Board to Board Connector1 (J10).
G32	GND	GND	Power	Ground.
G33	LA31_P	FPGA_AP7_LVDS3A_20p	IO, 1.8V LVDS	Bank 3A IO20 differential positive. This Pin is connected to 30th pin of Board to Board Connector1 (J10).
G34	LA31_N	FPGA_AP6_LVDS3A_20n	IO, 1.8V LVDS	Bank 3A IO20 differential negative. This Pin is connected to 28th pin of Board to Board Connector1 (J10).
G35	GND	GND	Power	Ground.
G36	LA33_P	FPGA_AM1_LVDS3A_16p	IO, 1.8V LVDS	Bank 3A IO16 differential positive. This Pin is connected to 12th pin of Board to Board Connector1 (J10).
G37	LA33_N	FPGA_AM2_LVDS3A_16n	IO, 1.8V LVDS	Bank 3A IO16 differential negative. This Pin is connected to 14th pin of Board to Board Connector1 (J10).
G38	GND	GND	Power	Ground.
G39	VADJ	VCC_FMC_ADJ	O, 1.8V Power	Supply Voltage.
G40	GND	GND	Power	Ground.
H1	VREF_A_M2C	NA	NA	NC
H2	PRSNT_M2C_L	IOEXP_P15_PR_M2C_L1	I,3.3V/10K PU	Module Present Signal. This Pin is connected to 18th pin of IO Expander (U40).
H3	GND	GND	Power	Ground.
H4	CLK0_M2C_P	NA	NA	NC.
H5	CLK0_M2C_N	NA	NA	NC.
H6	GND	GND	Power	Ground.

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
H7	LA02_P	FPGA_AC3_LVDS3C_22p	IO, 1.8V LVDS	Bank 3C IO22 differential positive. This Pin is connected to 132nd pin of Board to Board Connector2 (J11).
H8	LA02_N	FPGA_AC2_LVDS3C_22n	IO, 1.8V LVDS	Bank 3C IO22 differential negative. This Pin is connected to 134th pin of Board to Board Connector2 (J11).
H9	GND	GND	Power	Ground.
H10	LA04_P	FPGA_AB1_LVDS3C_24p	IO, 1.8V LVDS	Bank 3C IO24 differential positive. This Pin is connected to 131st pin of Board to Board Connector2 (J11).
H11	LA04_N	FPGA_AA1_LVDS3C_24n	IO, 1.8V LVDS	Bank 3C IO24 differential negative. This Pin is connected to 133rd pin of Board to Board Connector2 (J11).
H12	GND	GND	Power	Ground.
H13	LA07_P	FPGA_U6_LVDS3C_5p	IO, 1.8V LVDS	Bank 3C IO5 differential positive. This Pin is connected to 151st pin of Board to Board Connector2 (J11).
H14	LA07_N	FPGA_U5_LVDS3C_5n	IO, 1.8V LVDS	Bank 3C IO5 differential negative. This Pin is connected to 153rd pin of Board to Board Connector2 (J11).
H15	GND	GND	Power	Ground.
H16	LA11_P	FPGA_P2_LVDS3C_7p	IO, 1.8V LVDS	Bank 3C IO7 differential positive. This Pin is connected to 163rd pin of Board to Board Connector2 (J11).
H17	LA11_N	FPGA_R2_LVDS3C_7n	IO, 1.8V LVDS	Bank 3C IO7 differential negative. This Pin is connected to 165th pin of Board to Board Connector2 (J11).
H18	GND	GND	Power	Ground.
H19	LA15_P	FPGA_AB2_LVDS3C_21p	IO, 1.8V LVDS	Bank 3C IO21 differential positive. This Pin is connected to 136th pin of Board to Board Connector2 (J11).
H20	LA15_N	FPGA_AB3_LVDS3C_21n	IO, 1.8V LVDS	Bank 3C IO21 differential negative. This Pin is connected to 138th pin of Board to Board Connector2 (J11).
H21	GND	GND	Power	Ground.
H22	LA19_P	FPGA_W6_LVDS3C_16p	IO, 1.8V LVDS	Bank 3C IO16 differential positive. This Pin is connected to 152nd pin of Board to Board Connector2 (J11).
H23	LA19_N	FPGA_W7_LVDS3C_16n	IO, 1.8V LVDS	Bank 3C IO16 differential negative. This Pin is connected to 154th pin of Board to Board Connector2 (J11).
H24	GND	GND	Power	Ground.

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
H25	LA21_P	FPGA_AA5_LVDS3C_18p	IO, 1.8V LVDS	Bank 3C IO18 differential positive. This Pin is connected to 182nd pin of Board to Board Connector2 (J11).
H26	LA21_N	FPGA_AA6_LVDS3C_18n	IO, 1.8V LVDS	Bank 3C IO18 differential negative. This Pin is connected to 184th pin of Board to Board Connector2 (J11).
H27	GND	GND	Power	Ground.
H28	LA24_P	FPGA_AK7_LVDS3A_9p	IO, 1.8V LVDS	Bank 3A IO9 differential positive. This Pin is connected to 38th pin of Board to Board Connector1 (J10).
H29	LA24_N	FPGA_AK8_LVDS3A_9n	IO, 1.8V LVDS	Bank 3A IO9 differential negative. This Pin is connected to 40th pin of Board to Board Connector1 (J10).
H30	GND	GND	Power	Ground.
H31	LA28_P	FPGA_AP5_LVDS3A_19p	IO, 1.8V LVDS	Bank 3A IO19 differential positive. This Pin is connected to 31st pin of Board to Board Connector1 (J10).
H32	LA28_N	FPGA_AN5_LVDS3A_19n	IO, 1.8V LVDS	Bank 3A IO19 differential negative. This Pin is connected to 33rd pin of Board to Board Connector1 (J10).
H33	GND	GND	Power	Ground.
H34	LA30_P	FPGA_AM6_LVDS3A_17p	IO, 1.8V LVDS	Bank 3A IO17 differential positive. This Pin is connected to 27th pin of Board to Board Connector1 (J10).
H35	LA30_N	FPGA_AM5_LVDS3A_17n	IO, 1.8V LVDS	Bank 3A IO17 differential negative. This Pin is connected to 29th pin of Board to Board Connector1 (J10).
H36	GND	GND	Power	Ground.
H37	LA32_P	FPGA_AP4_LVDS3A_18p	IO, 1.8V LVDS	Bank 3A IO18 differential positive. This Pin is connected to 16th pin of Board to Board Connector1 (J10).
H38	LA32_N	FPGA_AN4_LVDS3A_18n	IO, 1.8V LVDS	Bank 3A IO18 differential negative. This Pin is connected to 18th pin of Board to Board Connector1 (J10).
H39	GND	GND	Power	Ground.
H40	VADJ	VCC_FMC_ADJ	O, 1.8V Power	Supply Voltage.
J1	GND	GND	Power	Ground.
J2	CLK3_BIDIR_P	FPGA_W4_LVDS3C_15p/CLKOUT_0p	IO, 1.8V LVDS	Bank 3C IO15 differential positive. This pin can be configured as clock input0 positive. This Pin is connected to 170th pin of Board to Board Connector2 (J11).

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
J3	CLK3_BIDIR_N	FPGA_W5_LVDS3C_15n/CLKOUT_0n	IO, 1.8V LVDS	Bank 3C IO15 differential negative. This pin can be configured as clock input0 negative. This Pin is connected to 172nd pin of Board to Board Connector2 (J11).
J4	GND	GND	Power	Ground.
J5	GND	GND	Power	Ground.
J6	HA03_P	FPGA_AN13_LVDS2A_4p	IO, 1.8V LVDS	Bank 2A IO4 differential positive. This Pin is connected to 238th pin of Board to Board Connector1 (J10).
J7	HA03_N	FPGA_AM13_LVDS2A_4n	IO, 1.8V LVDS	Bank 2A IO4 differential negative. This Pin is connected to 236th pin of Board to Board Connector1 (J10).
J8	GND	GND	Power	Ground.
J9	HA07_P	FPGA_AP16_LVDS2A_2p	IO, 1.8V LVDS	Bank 2A IO2 differential positive. This Pin is connected to 147th pin of Board to Board Connector1 (J10).
J10	HA07_N	FPGA_AP17_LVDS2A_2n	IO, 1.8V LVDS	Bank 2A IO2 differential negative. This Pin is connected to 149th pin of Board to Board Connector1 (J10).
J11	GND	GND	Power	Ground.
J12	HA11_P	FPGA_AN12_LVDS2A_5p	IO, 1.8V LVDS	Bank 2A IO5 differential positive. This Pin is connected to 150th pin of Board to Board Connector1 (J10).
J13	HA11_N	FPGA_AP12_LVDS2A_5n	IO, 1.8V LVDS	Bank 2A IO5 differential negative. This Pin is connected to 148th pin of Board to Board Connector1 (J10).
J14	GND	GND	Power	Ground.
J15	HA14_P	NA	NA	NC.
J16	HA14_N	NA	NA	NC.
J17	GND	GND	Power	Ground.
J18	HA18_P	FPGA_AC17_LVDS2A_24p	IO, 1.8V LVDS	Bank 2A IO24 differential positive. This Pin is connected to 172nd pin of Board to Board Connector1 (J10).
J19	HA18_N	NA	NA	NC.
J20	GND	GND	Power	Ground.
J21	HA22_P	NA	NA	NC.
J22	HA22_N	NA	NA	NC.
J23	GND	GND	Power	Ground.
J24	HB01_P	NA	NA	NC.
J25	HB01_N	NA	NA	NC.
J26	GND	GND	Power	Ground.

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
J27	HB07_P	NA	NA	NC.
J28	HB07_N	NA	NA	NC.
J29	GND	GND	Power	Ground.
J30	HB11_P	NA	NA	NC.
J31	HB11_N	NA	NA	NC.
J32	GND	GND	Power	Ground.
J33	HB15_P	NA	NA	NC.
J34	HB15_N	NA	NA	NC.
J35	GND	GND	Power	Ground.
J36	HB18_P	NA	NA	NC.
J37	HB18_N	NA	NA	NC.
J38	GND	GND	Power	Ground.
J39	VIO_B_M2C	NA	NA	NC.
J40	GND	GND	Power	Ground.
K1	VREF_B_M2C	NA	NA	NC.
K2	GND	GND	Power	Ground.
K3	GND	GND	Power	Ground.
K4	CLK2_BIDIR_P	NA	NA	NC
K5	CLK2_BIDIR_N	NA	NA	NC
K6	GND	GND	Power	Ground.
K7	HA02_P	FPGA_AE12_LVDS3A_6p	IO, 1.8V LVDS	Bank 3A IO6 differential positive. This Pin is connected to 112nd pin of Board to Board Connector1 (J10).
K8	HA02_N	FPGA_AE11_LVDS3A_6n	IO, 1.8V LVDS	Bank 3A IO6 differential negative. This Pin is connected to 110th pin of Board to Board Connector1 (J10).
K9	GND	GND	Power	Ground.
K10	HA06_P	FPGA_AL9_LVDS3A_23p	IO, 1.8V LVCMOS	Bank 3A IO23 Single Ended pin. This Pin is connected to 78th pin of Board to Board Connector1 (J10).
K11	HA06_N	FPGA_AL8_LVDS3A_23n	IO, 1.8V LVCMOS	Bank 3A IO23 Single Ended pin. This Pin is connected to 104th pin of Board to Board Connector1 (J10).
K12	GND	GND	Power	Ground.
K13	HA10_P	FPGA_AJ17_LVDS2A_16p	IO, 1.8V LVDS	Bank 2A IO16 differential positive. This Pin is connected to 136th pin of Board to Board Connector1 (J10).
K14	HA10_N	FPGA_AK17_LVDS2A_16n	IO, 1.8V LVDS	Bank 2A IO16 differential negative. This Pin is connected to 138th pin of Board to Board Connector1 (J10).
K15	GND	GND	Power	Ground.
K16	HA17_P_CC	NA	NA	NC.

Pin No	FMC Connector1 Pin Name	Signal Name	Signal Type/ Termination	Description
K17	HA17_N_CC	NA	NA	NC.
K18	GND	GND	Power	Ground.
K19	HA21_P	NA	NA	NC.
K20	HA21_N	NA	NA	NC.
K21	GND	GND	Power	Ground.
K22	HA23_P	NA	NA	NC.
K23	HA23_N	NA	NA	NC.
K24	GND	GND	Power	Ground.
K25	HB00_P_CC	NA	NA	NC.
K26	HB00_N_CC	NA	NA	NC.
K27	GND	GND	Power	Ground.
K28	HB06_P_CC	NA	NA	NC.
K29	HB06_N_CC	NA	NA	NC.
K30	GND	GND	Power	Ground.
K31	HB10_P	NA	NA	NC.
K32	HB10_N	NA	NA	NC.
K33	GND	GND	Power	Ground.
K34	HB14_P	NA	NA	NC.
K35	HB14_N	NA	NA	NC.
K36	GND	GND	Power	Ground.
K37	HB17_P_CC	NA	NA	NC.
K38	HB17_N_CC	NA	NA	NC.
K39	GND	GND	Power	Ground.
K40	VIO_B_M2C	NA	NA	NC.

2.5.1.4 FMC HPC Connector2

The Arria10 SoC/FPGA Carrier board supports two 400Pin Standard FMC HPC connectors to support standard ANSI/VITA 57.1 FMC modules. These FMC HPC connectors can accept two Single width FMC modules or one double width FMC module.

Number of Pins - 400
Connector Part Number - ASP-134486-01
Mating Connector - ASP-134488-01 from Samtech

The FMC HPC Connector2 (J6) supports the below mentioned interface from Arria10 SoC/FPGA.

- 6 High Speed Transceivers
- 2 High Speed Transmitter (TX)
- 14 LVDS IOs
- 3 Single ended (SE) IOs
- 2 Clock Input Capable LVDS/SE pins
- 1 Clock Output Capable LVDS/SE pins

This 400Pin FMC HPC connector2 (J6) is physically located at the top of the board as shown below.

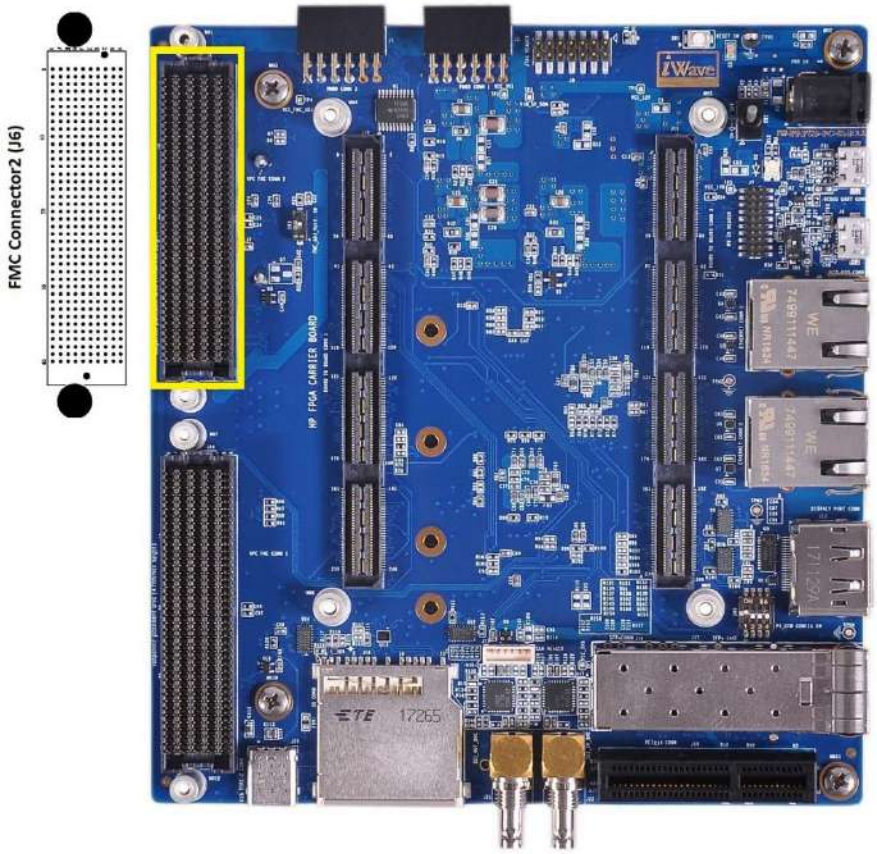


Figure 14: FMC Connector2

This 400Pin FMC HPC connector2 (J6) pin mapping is shown below.

	K	J	H	G	F	E	D	C	B	A
1	NC	GND	NC	GND	PG_M2C	GND	PG_C2M	GND	NC	GND
2	GND	NC	PRSNT_M2C_L	CLK0_C2M_P	GND	NC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	NC	GND	CLK0_C2M_N	GND	NC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	NC	GND	NC	GND	NC	GND	GBTCLK0_M2C_P	GND	NC	GND
5	NC	GND	NC	GND	NC	GND	GBTCLK0_M2C_N	GND	NC	GND
6	GND	NC	GND	LA00_P_CC	GND	NC	GND	DP0_M2C_P	GND	DP2_M2C_P
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	GND	DP2_M2C_N
8	NC	GND	LA02_N	GND	NC	GND	LA01_P_CC	GND	NC	GND
9	GND	NC	GND	LA03_P	GND	NC	LA01_N_CC	GND	NC	GND
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	GND	DP3_M2C_P
11	NC	GND	LA04_N	GND	NC	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	NC	GND	LA08_P	GND	NC	LA05_N	GND	NC	GND
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	GND
14	NC	GND	LA07_N	GND	NC	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	NC	GND	LA12_P	GND	NC	LA09_N	LA10_N	GND	DP4_M2C_N
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	GND
17	NC	GND	LA11_N	GND	NC	GND	LA13_P	GND	NC	GND
18	GND	NC	GND	LA16_P	GND	NC	LA13_N	LA14_P	GND	DP5_M2C_P
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	GND	DP5_M2C_N
20	NC	GND	LA15_N	GND	NC	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	NC	GND	NC	GND	NC	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	NC	NC	NC	NC	NC	NC	GND	NC	GND	DP1_C2M_P
23	NC	GND	NC	GND	NC	GND	NC	NC	GND	DP1_C2M_N
24	GND	NC	GND	NC	GND	NC	NC	GND	NC	GND
25	NC	NC	NC	NC	NC	NC	GND	GND	NC	GND
26	NC	GND	NC	GND	NC	GND	NC	LA27_P	GND	DP2_C2M_P
27	GND	NC	GND	NC	GND	NC	NC	LA27_N	GND	DP2_C2M_N
28	NC	NC	NC	NC	NC	NC	GND	GND	NC	GND
29	NC	GND	NC	GND	NC	GND	TCK	GND	NC	GND
30	GND	NC	GND	NC	GND	NC	TDI	SCL	GND	DP3_C2M_P
31	NC	NC	NC	NC	NC	NC	TDO	SDA	GND	DP3_C2M_N
32	NC	GND	NC	GND	NC	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	NC	GND	NC	GND	NC	TMS	GND	DP7_C2M_N	GND
34	NC	NC	NC	NC	NC	NC	TRST_L	GA0	GND	DP4_C2M_P
35	NC	GND	NC	GND	NC	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	NC	GND	NC	GND	NC	3P3V	GND	DP6_C2M_P	GND
37	NC	NC	NC	NC	NC	NC	GND	12P0V	DP6_C2M_N	GND
38	NC	GND	NC	GND	NC	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	NC	GND

Figure 15: FMC HPC Connector2 Pin Out

Table 7: FMC HPC Connector2 Pin Assignment

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
A1	GND	GND	Power	Ground.
A2	DP1_M2C_P	GXBL1E_RX_CH1p	I, DIFF	Bank 1E channel1 High speed differential receiver positive. This Pin is connected to 197th pin of Board to Board Connector1 (J10).
A3	DP1_M2C_N	GXBL1E_RX_CH1n	I, DIFF	Bank 1E channel1 High speed differential receiver negative. This Pin is connected to 195th pin of Board to Board Connector1 (J10).
A4	GND	GND	Power	Ground.
A5	GND	GND	Power	Ground.
A6	DP2_M2C_P	GXBL1E_RX_CH2p	I, DIFF	Bank 1E channel2 High speed differential receiver positive This Pin is connected to 237th pin of Board to Board Connector1 (J10).

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
A7	DP2_M2C_N	GXBL1E_RX_CH2n	I, DIFF	Bank 1E channel2 High speed differential receiver negative. This Pin is connected to 235th pin of Board to Board Connector1 (J10).
A8	GND	GND	Power	Ground.
A9	GND	GND	Power	Ground.
A10	DP3_M2C_P	GXBL1E_RX_CH3p	I, DIFF	Bank 1E channel3 High speed differential receiver positive. This Pin is connected to 231st pin of Board to Board Connector1 (J10).
A11	DP3_M2C_N	GXBL1E_RX_CH3n	I, DIFF	Bank 1E channel3 High speed differential receiver negative. This Pin is connected to 229th pin of Board to Board Connector1 (J10).
A12	GND	GND	Power	Ground.
A13	GND	GND	Power	Ground.
A14	DP4_M2C_P	GXBL1F_RX_CH0p	I, DIFF	Bank 1F channel0 High speed differential receiver positive. This Pin is connected to 187th pin of Board to Board Connector2(J11).
A15	DP4_M2C_N	GXBL1F_RX_CH0n	I, DIFF	Bank 1F channel0 High speed differential receiver negative. This Pin is connected to 189th pin of Board to Board Connector2(J11).
A16	GND	GND	Power	Ground.
A17	GND	GND	Power	Ground.
A18	DP5_M2C_P	GXBL1F_RX_CH1p	I, DIFF	Bank 1F channel1 High speed differential receiver positive. This Pin is connected to 199th pin of Board to Board Connector2(J11).
A19	DP5_M2C_N	GXBL1F_RX_CH1n	I, DIFF	Bank 1F channel1 High speed differential receiver negative. This Pin is connected to 201st pin of Board to Board Connector2(J11).
A20	GND	GND	Power	Ground.
A21	GND	GND	Power	Ground.
A22	DP1_C2M_P	GXBL1E_TX_CH1p	O, DIFF	Bank 1E channel1 High speed differential transmitter positive. This Pin is connected to 189th pin of Board to Board Connector1 (J10).
A23	DP1_C2M_N	GXBL1E_TX_CH1n	O, DIFF	Bank 1E channel1 High speed differential transmitter negative. This Pin is connected to 191st pin of Board to Board Connector1 (J10).

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
A24	GND	GND	Power	Ground.
A25	GND	GND	Power	Ground.
A26	DP2_C2M_P	GXBL1E_TX_CH2p	O, DIFF	Bank 1E channel2 High speed differential transmitter positive. This Pin is connected to 217th pin of Board to Board Connector1 (J10).
A27	DP2_C2M_N	GXBL1E_TX_CH2n	O, DIFF	Bank 1E channel2 High speed differential transmitter negative. This Pin is connected to 219th pin of Board to Board Connector1 (J10).
A28	GND	GND	Power	Ground.
A29	GND	GND	Power	Ground.
A30	DP3_C2M_P	GXBL1E_TX_CH3p	O, DIFF	Bank 1E channel3 High speed differential transmitter positive. This Pin is connected to 223rd pin of Board to Board Connector1 (J10).
A31	DP3_C2M_N	GXBL1E_TX_CH3n	O, DIFF	Bank 1E channel3 High speed differential transmitter negative. This Pin is connected to 225th pin of Board to Board Connector1 (J10).
A32	GND	GND	Power	Ground.
A33	GND	GND	Power	Ground.
A34	DP4_C2M_P	GXBL1F_TX_CH0p	O, DIFF	Bank 1F channel0 High speed differential transmitter positive. This Pin is connected to 193rd pin of Board to Board Connector2 (J11).
A35	DP4_C2M_N	GXBL1F_TX_CH0n	O, DIFF	Bank 1F channel0 High speed differential transmitter negative. This Pin is connected to 195th pin of Board to Board Connector2 (J11).
A36	GND	GND	Power	Ground.
A37	GND	GND	Power	Ground.
A38	DP5_C2M_P	GXBL1F_TX_CH1p	O, DIFF	Bank 1F channel1 High speed differential transmitter positive. This Pin is connected to 205th pin of Board to Board Connector2 (J11).
A39	DP5_C2M_N	GXBL1F_TX_CH1n	O, DIFF	Bank 1F channel1 High speed differential transmitter negative. This Pin is connected to 207th pin of Board to Board Connector2 (J11).
A40	GND	GND	Power	Ground.
B1	CLK_DIR	NA	NA	NC.
B2	GND	GND	Power	Ground.
B3	GND	GND	Power	Ground.

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
B4	DP9_M2C_P	NA	NA	NC.
B5	DP9_M2C_N	NA	NA	NC.
B6	GND	GND	Power	Ground.
B7	GND	GND	Power	Ground.
B8	DP8_M2C_P	NA	NA	NC.
B9	DP8_M2C_N	NA	NA	NC.
B10	GND	GND	Power	Ground.
B11	GND	GND	Power	Ground.
B12	DP7_M2C_P	NA	NA	NC.
B13	DP7_M2C_N	NA	NA	NC.
B14	GND	GND	Power	Ground.
B15	GND	GND	Power	Ground.
B16	DP6_M2C_P	NA	NA	NC.
B17	DP6_M2C_N	NA	NA	NC.
B18	GND	GND	Power	Ground.
B19	GND	GND	Power	Ground.
B20	GBTCLK1_M2C_P	REFCLK_GXBL1F_CHTp	I, DIFF	Bank 1F differential reference clock top positive. This Pin is connected to 188th pin of Board to Board Connector2 (J11).
B21	GBTCLK1_M2C_N	REFCLK_GXBL1F_CHTn	I, DIFF	Bank 1F differential reference clock top negative. This Pin is connected to 190th pin of Board to Board Connector2 (J11).
B22	GND	GND	Power	Ground.
B23	GND	GND	Power	Ground.
B24	DP9_C2M_P	NA	NA	NC.
B25	DP9_C2M_N	NA	NA	NC.
B26	GND	GND	Power	Ground.
B27	GND	GND	Power	Ground.
B28	DP8_C2M_P	NA	NA	NC.
B29	DP8_C2M_N	NA	NA	NC.
B30	GND	GND	Power	Ground.
B31	GND	GND	Power	Ground.
B32	DP7_C2M_P	GXBL1F_TX_CH5p	O, DIFF	Bank 1F channel5 High speed differential transmitter positive. This Pin is connected to 224th pin of Board to Board Connector1 (J11).
B33	DP7_C2M_N	GXBL1F_TX_CH5n	O, DIFF	Bank 1F channel5 High speed differential transmitter negative. This Pin is connected to 226th pin of Board to Board Connector1 (J11).
B34	GND	GND	Power	Ground.

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
B35	GND	GND	Power	Ground.
B36	DP6_C2M_P	GXBL1E_TX_CH5p	O, DIFF	Bank 1E channel5 High speed differential transmitter positive. This Pin is connected to 236th pin of Board to Board Connector1 (J11).
B37	DP6_C2M_N	GXBL1E_TX_CH5n	O, DIFF	Bank 1E channel5 High speed differential transmitter negative. This Pin is connected to 238th pin of Board to Board Connector1 (J11).
B38	GND	GND	Power	Ground.
B39	GND	GND	Power	Ground.
B40	RES0	NA	NA	NC.
C1	GND	GND	Power	Ground.
C2	DP0_C2M_P	GXBL1E_TX_CH0p	O, DIFF	Bank 1E channel0 High speed differential transmitter positive. This Pin is connected to 183rd pin of Board to Board Connector1 (J10).
C3	DP0_C2M_N	GXBL1E_TX_CH0n	O, DIFF	Bank 1E channel0 High speed differential transmitter negative. This Pin is connected to 185th pin of Board to Board Connector1 (J10).
C4	GND	GND	Power	Ground.
C5	GND	GND	Power	Ground.
C6	DP0_M2C_P	GXBL1E_RX_CH0p	I, DIFF	Bank 1E channel0 High speed differential receiver positive. This Pin is connected to 203rd pin of Board to Board Connector1 (J10).
C7	DP0_M2C_N	GXBL1E_RX_CH0n	I, DIFF	Bank 1E channel0 High speed differential receiver negative. This Pin is connected to 201st pin of Board to Board Connector1 (J10).
C8	GND	GND	Power	Ground.
C9	GND	GND	Power	Ground.
C10	LA06_P	FPGA_AL1_LVDS3B_24p	IO, 1.8V LVDS	Bank 3B IO24 differential positive. This Pin is connected to 95th pin of Board to Board Connector2 (J11).
C11	LA06_N	FPGA_AK1_LVDS3B_24n	IO, 1.8V LVDS	Bank 3B IO24 differential negative. This Pin is connected to 97th pin of Board to Board Connector2 (J11).
C12	GND	GND	Power	Ground.
C13	GND	GND	Power	Ground.
C14	LA10_P	FPGA_AK2_LVDS3B_23p	IO, 1.8V LVDS	Bank 3A IO23 differential positive. This Pin is connected to 99th pin of Board to Board Connector2 (J11).

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
C15	LA10_N	FPGA_AJ2_LVDS3B_23n	IO, 1.8V LVDS	Bank 3A IO23 differential negative. This Pin is connected to 101st pin of Board to Board Connector2 (J11).
C16	GND	GND	Power	Ground.
C17	GND	GND	Power	Ground.
C18	LA14_P	FPGA_AF9_LVDS3A_1p	IO, 1.8V LVDS	Bank 3A IO1 differential positive. This Pin is connected to 87th pin of Board to Board Connector1 (J10).
C19	LA14_N	FPGA_AE9_LVDS3A_1n	IO, 1.8V LVDS	Bank 3A IO1 differential negative. This Pin is connected to 89th pin of Board to Board Connector1 (J10).
C20	GND	GND	Power	Ground.
C21	GND	GND	Power	Ground.
C22	LA18_P_CC	NA	NA	NC.
C23	LA18_N_CC	NA	NA	NC.
C24	GND	GND	Power	Ground.
C25	GND	GND	Power	Ground.
C26	LA27_P	FPGA_AM3_LVDS3A_15p/CLKOUT_0p	IO, 1.8V LVDS	Bank 3A IO15 differential positive. This Pin is connected to 24th pin of Board to Board Connector1 (J10).
C27	LA27_N	FPGA_AL3_LVDS3A_15n/CLKOUT_0n	IO, 1.8V LVDS	Bank 3A IO15 differential negative. This Pin is connected to 22nd pin of Board to Board Connector1 (J10).
C28	GND	GND	Power	Ground.
C29	GND	GND	Power	Ground.
C30	SCL	HPS_GPIO0_IO5/I2C0_SCL	IO, 3.3V LVCMOS	HPC FMC I2C Clock Signal. This Pin is connected to 48th pin of Board to Board Connector2 (J11).
C31	SDA	HPS_GPIO0_IO4/I2C0_SDA	IO, 3.3V LVCMOS	HPC FMC I2C Data Signal. This Pin is connected to 46th pin of Board to Board Connector2 (J11).
C32	GND	GND	Power	Ground.
C33	GND	GND	Power	Ground.
C34	GA0	GA0_2	1K, PD	Geographical address 0
C35	12P0V	VCC_12V	O, 12V Power	Supply Voltage.
C36	GND	GND	Power	Ground.
C37	12P0V	VCC_12V	O, 12V Power	Supply Voltage.
C38	GND	GND	Power	Ground.
C39	3P3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
C40	GND	GND	Power	Ground.

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
D1	PG_C2M	PG_C2M	O, 3.3V	Power Good Signal from Carrier to FMC Module. This Pin is connected from the Power good signal of VCC_FMC_ADJ voltage regulator (U27).
D2	GND	GND	Power	Ground.
D3	GND	GND	Power	Ground.
D4	GBTCLK0_M2C_P	REFCLK_GXBL1E_CHTp	I, DIFF	Bank 1E differential reference clock top positive. This Pin is connected to 184th pin of Board to Board Connector1 (J10).
D5	GBTCLK0_M2C_N	REFCLK_GXBL1E_CHTn	I, DIFF	Bank 1E differential reference clock top negative. This Pin is connected to 186th pin of Board to Board Connector1 (J10).
D6	GND	GND	Power	Ground.
D7	GND	GND	Power	Ground.
D8	LA01_P_CC	FPGA_AE2_LVDS3B_13p/CLKIN_0p	IO, 1.8V LVDS	Bank 3B IO13 differential positive. This Pin can be configured as clock input0 positive. This Pin is connected to 116th pin of Board to Board Connector2 (J11).
D9	LA01_N_CC	FPGA_AE3_LVDS3B_13n/CLKIN_0n	IO, 1.8V LVDS	Bank 3B IO13 differential negative. This Pin can be configured as clock input0 negative. This Pin is connected to 118th pin of Board to Board Connector2 (J11).
D10	GND	GND	Power	Ground.
D11	LA05_P	FPGA_AG1_LVDS3B_19p	IO, 1.8V LVDS	Bank 3B IO19 differential positive. This Pin is connected to 98th pin of Board to Board Connector2 (J11).
D12	LA05_N	FPGA_AG2_LVDS3B_19n	IO, 1.8V LVDS	Bank 3B IO19 differential negative. This Pin is connected to 96th pin of Board to Board Connector2 (J11).
D13	GND	GND	Power	Ground.
D14	LA09_P	FPGA_AJ1_LVDS3B_20p	IO, 1.8V LVDS	Bank 3B IO20 differential positive. This Pin is connected to 103rd pin of Board to Board Connector2 (J11).
D15	LA09_N	FPGA_AH2_LVDS3B_20n	IO, 1.8V LVDS	Bank 3B IO20 differential negative This Pin is connected to 105th pin of Board to Board Connector2 (J11).
D16	GND	GND	Power	Ground.

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
D17	LA13_P	FPGA_AL16_LVDS2A_10p/CLKOUT_0p	IO, 1.8V LVDS	Bank 2A IO10 differential positive. This Pin is connected to 144th pin of Board to Board Connector1 (J10).
D18	LA13_N	FPGA_AM16_LVDS2A_10n/CLKOUT_0n	IO, 1.8V LVDS	Bank 2A IO10 differential negative. This Pin is connected to 142nd pin of Board to Board Connector1 (J10).
D19	GND	GND	Power	Ground.
D20	LA17_P_CC	FPGA_AJ5_LVDS3A_10p/CLKOUT_1p	IO, 1.8V LVDS	Bank 3A IO10 differential positive. This Pin is connected to 118th pin of Board to Board Connector1 (J10).
D21	LA17_N_CC	FPGA_AH5_LVDS3A_10n/CLKOUT_1n	IO, 1.8V LVDS	Bank 3A IO10 differential negative. This Pin is connected to 116th pin of Board to Board Connector1 (J10).
D22	GND	GND	Power	Ground.
D23	LA23_P	NA	NA	NC.
D24	LA23_N	NA	NA	NC.
D25	GND	GND	Power	Ground.
D26	LA26_P	NA	NA	NC.
D27	LA26_N	NA	NA	NC.
D28	GND	GND	Power	Ground.
D29	TCK	CSS_TCK	I, 3.3V CMOS/ 49.9K PU	JTAG Test Clock This Pin is connected to 31st pin of Board to Board Connector2 (J11) through Voltage level translator.
D30	TDI	JTAG_TDO	O, 3.3V CMOS	JTAG Test Data Output
D31	TDO	JTAG_TDI	I, 3.3V CMOS	JTAG Test Data Input.
D32	3P3VAUX	3V3_AUX1	O, 3.3V Power	Supply Voltage.
D33	TMS	CSS_TMS	I, 3.3V CMOS/ 49.9K PU	JTAG Test Mode Select This Pin is connected to 29th pin of Board to Board Connector2 (J11) through Voltage level translator.
D34	TRST_L	CSS_TRST	I, 3.3V CMOS	JTAG Test Reset This Pin is connected to 25th pin of Board to Board Connector2 (J11) through Voltage level translator.
D35	GA1	GA1_2	1K, PU	Geographical address 1
D36	3P3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
D37	GND	GND	Power	Ground.
D38	3P3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
D39	GND	GND	Power	Ground.
D40	3P3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
E1	GND	GND	Power	Ground.
E2	HA01_P_CC	NA	NA	NC.

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
E3	HA01_N_CC	NA	NA	NC.
E4	GND	GND	Power	Ground.
E5	GND	GND	Power	Ground.
E6	HA05_P	NA	NA	NC.
E7	HA05_N	NA	NA	NC.
E8	GND	GND	Power	Ground.
E9	HA09_P	NA	NA	NC.
E10	HA09_N	NA	NA	NC.
E11	GND	GND	Power	Ground.
E12	HA13_P	NA	NA	NC.
E13	HA13_N	NA	NA	NC.
E14	GND	GND	Power	Ground.
E15	HA16_P	NA	NA	NC.
E16	HA16_N	NA	NA	NC.
E17	GND	GND	Power	Ground.
E18	HA20_P	NA	NA	NC.
E19	HA20_N	NA	NA	NC.
E20	GND	GND	Power	Ground.
E21	HB03_P	NA	NA	NC.
E22	HB03_N	NA	NA	NC.
E23	GND	GND	Power	Ground.
E24	HB05_P	NA	NA	NC.
E25	HB05_N	NA	NA	NC.
E26	GND	GND	Power	Ground.
E27	HB09_P	NA	NA	NC.
E28	HB09_N	NA	NA	NC.
E29	GND	GND	Power	Ground.
E30	HB13_P	NA	NA	NC.
E31	HB13_N	NA	NA	NC.
E32	GND	GND	Power	Ground.
E33	HB19_P	NA	NA	NC.
E34	HB19_N	NA	NA	NC.
E35	GND	GND	Power	Ground.
E36	HB21_P	NA	NA	NC.
E37	HB21_N	NA	NA	NC.
E38	GND	GND	Power	Ground.
E39	VADJ	VCC_FMC_ADJ	O, 1.8V Power	Supply Voltage.
E40	GND	GND	Power	Ground.
F1	PG_M2C	IOEXP_P06_PG_M2C2	I, 3.3V CMOS/ 10K PU	Power Good Signal from FMC Module to Carrier. This Pin is connected to 10th pin of IO Expander (U40).

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
F2	GND	GND	Power	Ground.
F3	GND	GND	Power	Ground.
F4	HA00_P_CC	NA	NA	NC.
F5	HA00_N_CC	NA	NA	NC.
F6	GND	GND	Power	Ground.
F7	HA04_P	NA	NA	NC.
F8	HA04_N	NA	NA	NC.
F9	GND	GND	Power	Ground.
F10	HA08_P	NA	NA	NC.
F11	HA08_N	NA	NA	NC.
F12	GND	GND	Power	Ground.
F13	HA12_P	NA	NA	NC.
F14	HA12_N	NA	NA	NC.
F15	GND	GND	Power	Ground.
F16	HA15_P	NA	NA	NC.
F17	HA15_N	NA	NA	NC.
F18	GND	GND	Power	Ground.
F19	HA19_P	NA	NA	NC.
F20	HA19_N	NA	NA	NC.
F21	GND	GND	Power	Ground.
F22	HB02_P	NA	NA	NC.
F23	HB02_N	NA	NA	NC.
F24	GND	GND	Power	Ground.
F25	HB04_P	NA	NA	NC.
F26	HB04_N	NA	NA	NC.
F27	GND	GND	Power	Ground.
F28	HB08_P	NA	NA	NC.
F29	HB08_N	NA	NA	NC.
F30	GND	GND	Power	Ground.
F31	HB12_P	NA	NA	NC.
F32	HB12_N	NA	NA	NC.
F33	GND	GND	Power	Ground.
F34	HB16_P	NA	NA	NC.
F35	HB16_N	NA	NA	NC.
F36	GND	GND	Power	Ground.
F37	HB20_P	NA	NA	NC.
F38	HB20_N	NA	NA	NC.
F39	GND	GND	Power	Ground.
F40	VADJ	VCC_FMC_ADJ	O, 1.8V Power	Supply Voltage.
G1	GND	GND	Power	Ground.

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
G2	CLK1_M2C_P	FPGA_AD10_LVDS3B_12p/CLKIN_1p	IO, 1.8V LVDS	Bank 3B IO12 differential positive. This Pin is connected to 109th pin of Board to Board Connector2 (J11).
G3	CLK1_M2C_N	FPGA_AD11_LVDS3B_12n/CLKIN_1n	IO, 1.8V LVDS	Bank 3B IO12 differential negative. This Pin is connected to 111st pin of Board to Board Connector2 (J11).
G4	GND	GND	Power	Ground.
G5	GND	GND	Power	Ground.
G6	LA00_P_CC	FPGA_AF4_LVDS3B_15p/CLKOUT_0p	IO, 1.8V LVDS	Bank 3B IO15 differential positive. This Pin can be configured as clock output0 positive. This Pin is connected to 115th pin of Board to Board Connector2 (J11).
G7	LA00_N_CC	FPGA_AF3_LVDS3B_15n/CLKOUT_0n	IO, 1.8V LVDS	Bank 3B IO15 differential negative. This Pin can be configured as clock output0 negative. This Pin is connected to 117th pin of Board to Board Connector2 (J11).
G8	GND	GND	Power	Ground.
G9	LA03_P	FPGA_AE4_LVDS3B_3p	IO, 1.8V LVDS	Bank 3B IO3 differential positive. This Pin is connected to 100th pin of Board to Board Connector2 (J11).
G10	LA03_N	FPGA_AD4_LVDS3B_3n	IO, 1.8V LVDS	Bank 3B IO3 differential negative. This Pin is connected to 102nd pin of Board to Board Connector2 (J11).
G11	GND	GND	Power	Ground.
G12	LA08_P	FPGA_AF1_LVDS3B_16p	IO, 1.8V LVDS	Bank 3B IO16 differential positive. This Pin is connected to 104th pin of Board to Board Connector2 (J11).
G13	LA08_N	FPGA_AE1_LVDS3B_16n	IO, 1.8V LVDS	Bank 3B IO16 differential negative. This Pin is connected to 106th pin of Board to Board Connector2 (J11).
G14	GND	GND	Power	Ground.
G15	LA12_P	FPGA_AC4_LVDS3B_6p	IO, 1.8V LVDS	Bank 3B IO6 differential positive. This Pin is connected to 126th pin of Board to Board Connector2 (J11).
G16	LA12_N	FPGA_AC5_LVDS3B_6n	IO, 1.8V LVDS	Bank 3B IO6 differential negative. This Pin is connected to 128th pin of Board to Board Connector2 (J11).
G17	GND	GND	Power	Ground.
G18	LA16_P	FPGA_AH8_LVDS3A_7p	IO, 1.8V LVDS	Bank 3A IO7 differential positive. This Pin is connected to 50th pin of Board to Board Connector1 (J10).

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
G19	LA16_N	FPGA_AG8_LVDS3A_7n	IO, 1.8V LVDS	Bank 3A IO7 differential negative. This Pin is connected to 52nd pin of Board to Board Connector1 (J10).
G20	GND	GND	Power	Ground.
G21	LA20_P	NA	NA	NC.
G22	LA20_N	NA	NA	NC.
G23	GND	GND	Power	Ground.
G24	LA22_P	NA	NA	NC.
G25	LA22_N	NA	NA	NC.
G26	GND	GND	Power	Ground.
G27	LA25_P	NA	NA	NC.
G28	LA25_N	NA	NA	NC.
G29	GND	GND	Power	Ground.
G30	LA29_P	NA	NA	NC.
G31	LA29_N	NA	NA	NC.
G32	GND	GND	Power	Ground.
G33	LA31_P	NA	NA	NC.
G34	LA31_N	NA	NA	NC.
G35	GND	GND	Power	Ground.
G36	LA33_P	NA	NA	NC.
G37	LA33_N	NA	NA	NC.
G38	GND	GND	Power	Ground.
G39	VADJ	VCC_FMC_ADJ	O, 1.8V Power	Supply Voltage.
G40	GND	GND	Power	Ground.
H1	VREF_A_M2C	NA	NA	NC.
H2	PRSNT_M2C_L	IOEXP_P16_PR_M2C_L2	I,3.3V CMOS/ 10K PU	Module Preset Signal. This Pin is connected to 19th pin of IO Expander (U40).
H3	GND	GND	Power	Ground.
H4	CLK0_M2C_P	NA	NA	NC.
H5	CLK0_M2C_N	NA	NA	NC.
H6	GND	GND	Power	Ground.
H7	LA02_P	FPGA_AH3_LVDS3B_18p	IO, 1.8V LVDS	Bank 3B IO18 differential positive. This Pin is connected to 92nd pin of Board to Board Connector2 (J11).
H8	LA02_N	FPGA_AG3_LVDS3B_18n	IO, 1.8V LVDS	Bank 3B IO18 differential negative. This Pin is connected to 94th pin of Board to Board Connector2 (J11).
H9	GND	GND	Power	Ground.
H10	LA04_P	FPGA_AB6_LVDS3B_5p	IO, 1.8V LVDS	Bank 3B IO5 differential positive. This Pin is connected to 127th pin of Board to Board Connector2 (J11).

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
H11	LA04_N	FPGA_AB5_LVDS3B_5n	IO, 1.8V LVDS	Bank 3B IO5 differential negative. This Pin is connected to 125th pin of Board to Board Connector2 (J11).
H12	GND	GND	Power	Ground.
H13	LA07_P	FPGA_AB10_LVDS3B_1p	IO, 1.8V LVDS	Bank 3B IO1 differential positive. This Pin is connected to 123rd pin of Board to Board Connector2 (J11).
H14	LA07_N	FPGA_AB11_LVDS3B_1n	IO, 1.8V LVDS	Bank 3B IO1 differential negative. This Pin is connected to 121st pin of Board to Board Connector2 (J11).
H15	GND	GND	Power	Ground.
H16	LA11_P	FPGA_AD2_LVDS3B_2p	IO, 1.8V LVDS	Bank 3B IO2 differential positive. This Pin is connected to 122nd pin of Board to Board Connector2 (J11).
H17	LA11_N	FPGA_AD1_LVDS3B_2n	IO, 1.8V LVDS	Bank 3B IO2 differential negative. This Pin is connected to 124th pin of Board to Board Connector2 (J11).
H18	GND	GND	Power	Ground.
H19	LA15_P	FPGA_AH7_LVDS3A_8p	IO, 1.8V LVDS	Bank 3A IO8 differential positive. This Pin is connected to 46th pin of Board to Board Connector1 (J10).
H20	LA15_N	FPGA_AG7_LVDS3A_8n	IO, 1.8V LVDS	Bank 3A IO8 differential negative. This Pin is connected to 48th pin of Board to Board Connector1 (J10).
H21	GND	GND	Power	Ground.
H22	LA19_P	NA	NA	NC.
H23	LA19_N	NA	NA	NC.
H24	GND	GND	Power	Ground.
H25	LA21_P	NA	NA	NC.
H26	LA21_N	NA	NA	NC.
H27	GND	GND	Power	Ground.
H28	LA24_P	NA	NA	NC.
H29	LA24_N	NA	NA	NC.
H30	GND	GND	Power	Ground.
H31	LA28_P	NA	NA	NC.
H32	LA28_N	NA	NA	NC.
H33	GND	GND	Power	Ground.
H34	LA30_P	NA	NA	NC.
H35	LA30_N	NA	NA	NC.
H36	GND	GND	Power	Ground.
H37	LA32_P	NA	NA	NC.
H38	LA32_N	NA	NA	NC.
H39	GND	GND	Power	Ground.

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
H40	VADJ	VCC_FMC_ADJ	O, 1.8V Power	Supply Voltage.
J1	GND	GND	Power	Ground.
J2	CLK3_BIDIR_P	NA	NA	NC.
J3	CLK3_BIDIR_N	NA	NA	NC.
J4	GND	GND	Power	Ground.
J5	GND	GND	Power	Ground.
J6	HA03_P	NA	NA	NC.
J7	HA03_N	NA	NA	NC.
J8	GND	GND	Power	Ground.
J9	HA07_P	NA	NA	NC.
J10	HA07_N	NA	NA	NC.
J11	GND	GND	Power	Ground.
J12	HA11_P	NA	NA	NC.
J13	HA11_N	NA	NA	NC.
J14	GND	GND	Power	Ground.
J15	HA14_P	NA	NA	NC.
J16	HA14_N	NA	NA	NC.
J17	GND	GND	Power	Ground.
J18	HA18_P	NA	NA	NC.
J19	HA18_N	NA	NA	NC.
J20	GND	GND	Power	Ground.
J21	HA22_P	NA	NA	NC.
J22	HA22_N	NA	NA	NC.
J23	GND	GND	Power	Ground.
J24	HB01_P	NA	NA	NC.
J25	HB01_N	NA	NA	NC.
J26	GND	GND	Power	Ground.
J27	HB07_P	NA	NA	NC.
J28	HB07_N	NA	NA	NC.
J29	GND	GND	Power	Ground.
J30	HB11_P	NA	NA	NC.
J31	HB11_N	NA	NA	NC.
J32	GND	GND	Power	Ground.
J33	HB15_P	NA	NA	NC.
J34	HB15_N	NA	NA	NC.
J35	GND	GND	Power	Ground.
J36	HB18_P	NA	NA	NC.
J37	HB18_N	NA	NA	NC.
J38	GND	GND	Power	Ground.
J39	VIO_B_M2C	NA	NA	NC.
J40	GND	GND	Power	Ground.
K1	VREF_B_M2C	NA	NA	NC.

Pin No	FMC Connector2 Pin Name	Signal Name	Signal Type/ Termination	Description
K2	GND	GND	Power	Ground.
K3	GND	GND	Power	Ground.
K4	CLK2_BIDIR_P	NA	NA	NC.
K5	CLK2_BIDIR_N	NA	NA	NC.
K6	GND	GND	Power	Ground.
K7	HA02_P	NA	NA	NC.
K8	HA02_N	NA	NA	NC.
K9	GND	GND	Power	Ground.
K10	HA06_P	NA	NA	NC.
K11	HA06_N	NA	NA	NC.
K12	GND	GND	Power	Ground.
K13	HA10_P	NA	NA	NC.
K14	HA10_N	NA	NA	NC.
K15	GND	GND	Power	Ground.
K16	HA17_P_CC	NA	NA	NC.
K17	HA17_N_CC	NA	NA	NC.
K18	GND	GND	Power	Ground.
K19	HA21_P	NA	NA	NC.
K20	HA21_N	NA	NA	NC.
K21	GND	GND	Power	Ground.
K22	HA23_P	NA	NA	NC.
K23	HA23_N	NA	NA	NC.
K24	GND	GND	Power	Ground.
K25	HB00_P_CC	NA	NA	NC.
K26	HB00_N_CC	NA	NA	NC.
K27	GND	GND	Power	Ground.
K28	HB06_P_CC	NA	NA	NC.
K29	HB06_N_CC	NA	NA	NC.
K30	GND	GND	Power	Ground.
K31	HB10_P	NA	NA	NC.
K32	HB10_N	NA	NA	NC.
K33	GND	GND	Power	Ground.
K34	HB14_P	NA	NA	NC.
K35	HB14_N	NA	NA	NC.
K36	GND	GND	Power	Ground.
K37	HB17_P_CC	NA	NA	NC.
K38	HB17_N_CC	NA	NA	NC.
K39	GND	GND	Power	Ground.
K40	VIO_B_M2C	NA	NA	NC.

2.5.2 Optional Features

2.5.2.1 SDI Video IN

The Arria10 SoC/FPGA Carrier board supports one 3G/12G SDI Video IN interface through HD BNC connector (J22). The Video input signals from HD BNC Connector is directly connected to Adaptive Cable Equalizer chip and then connected to Bank1F CH3 high speed receiver of Arria10 SoC/FPGA through Board to Board connector2.

The Arria10 SoC/FPGA Carrier board supports Video Input Lock status LED (D11) for presence and absence of the Video Input signal on HD BNC connector (J22). This LED will glow when the Video Input signal is detected on HD BNC connector (J22). Also PS I2C0 is connected to Adaptive Cable Equalizer chip for control and configuration with I2C address 0x2D. SDI Video IN HD BNC connector (J22) is physically located at the top of the board as shown below.

Note: By default, 3G Adaptive Cable Equalizer chip "LMH0397" is supported on the board. To support 12G Adaptive Cable Equalizer chip "LMH1297", contact iWave.

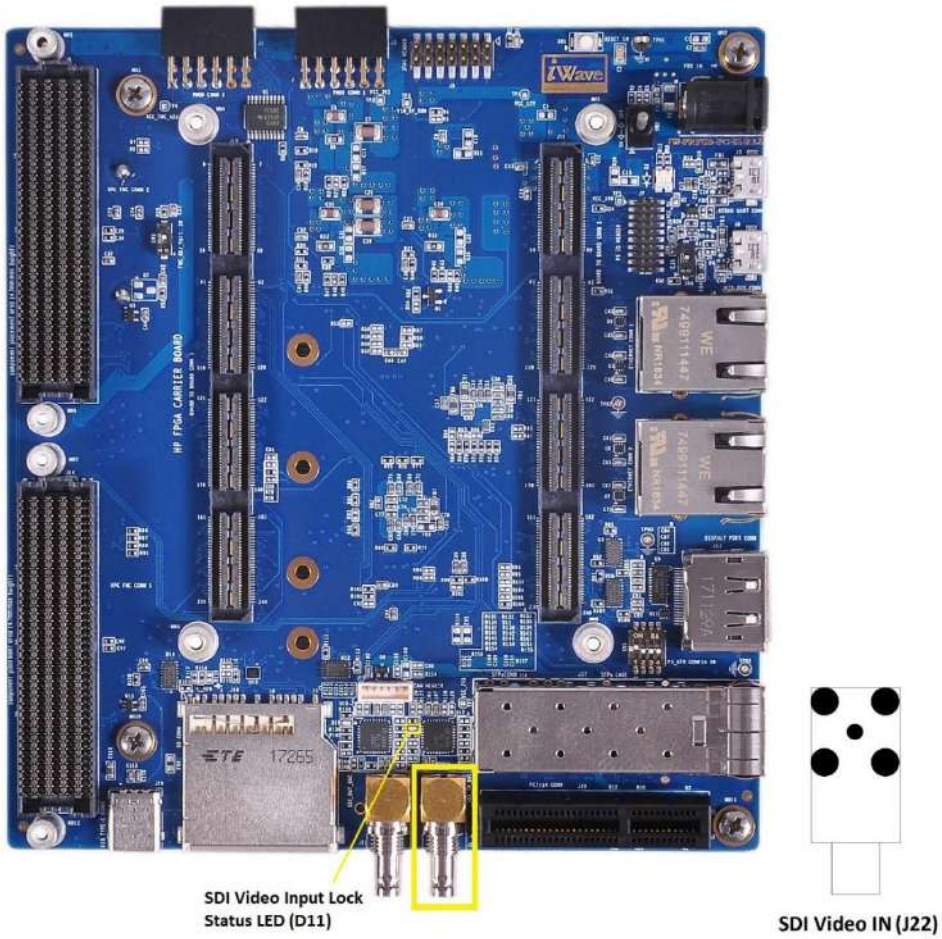


Figure 16: SDI Video IN HD BNC Connector

2.5.2.2 SDI Video Out

The Arria10 SoC/FPGA Carrier board supports one 3G/12G SDI Video OUT interface through HD BNC connector (J21). Arria10 SoC/FPGA's Bank1F CH3 high speed transmitter from Board to Board connector2 is directly connected to Cable Driver chip and then connected to HD BNC Connector (J21) for Video out.

The Arria10 SoC/FPGA Carrier board supports Video Output Lock status LED (D10). This LED will glow when the video signal from GTH transmitter is detected on Cable Driver chip. Also PS I2C0 is connected to Cable Driver chip for control and configuration with I2C address 0x30. SDI Video OUT HD BNC connector (J21) is physically located at the top of the board as shown below.

Note: By default, 3G Cable Driver chip "LMH0397" is supported on the board. To support 12G Cable Driver chip "LMH1297", contact iWave.

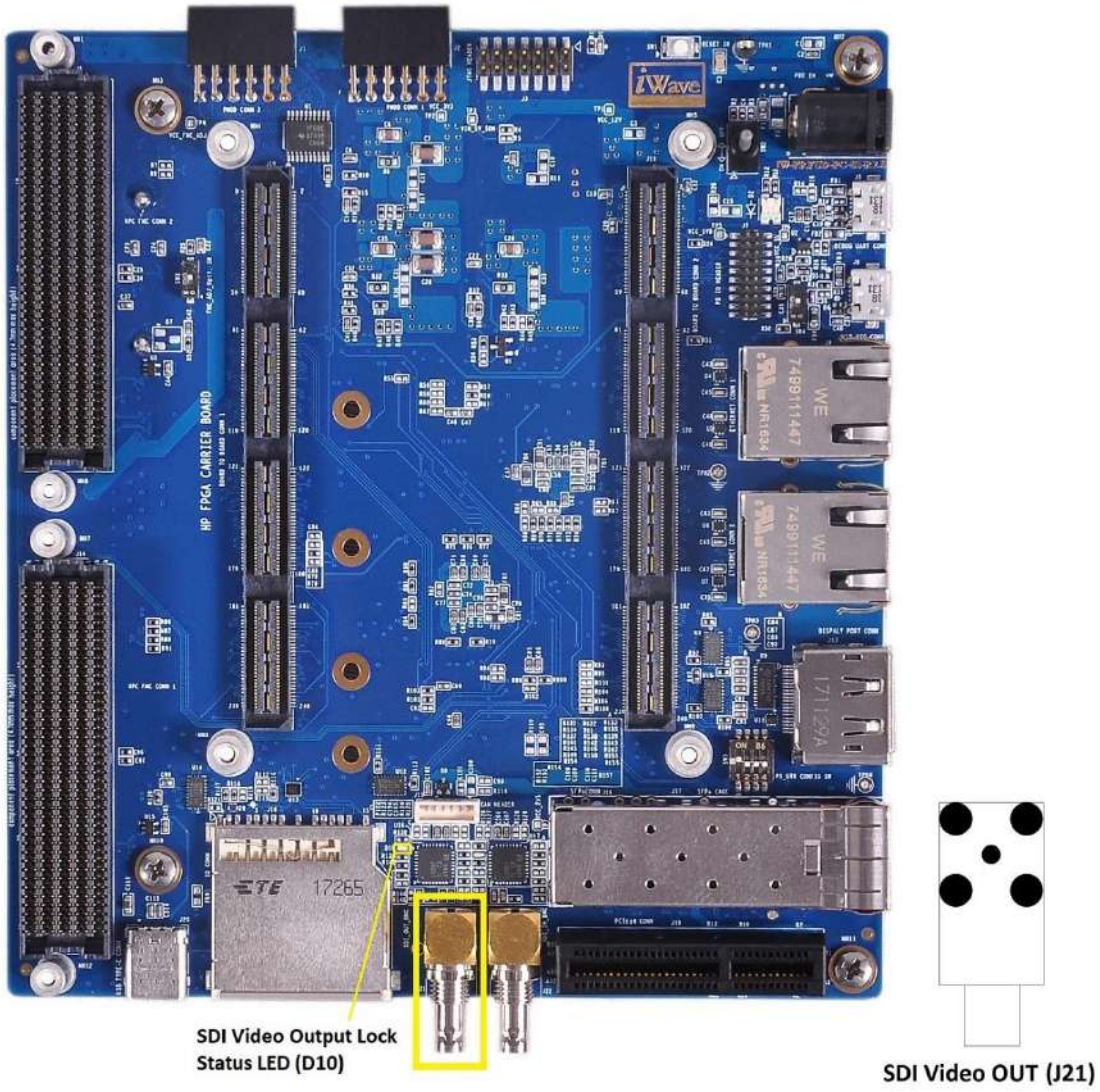


Figure 17: SDI Video OUT HD BNC Connector

2.5.2.3 M.2 SATA Connector

The Arria10 SoC/FPGA Carrier board supports one SATA interface through M.2 (KeyB) SATA connector. Bank1F CH4 of Arria10 SoC/FPGA is connected for SATA interface. The channel selection to M.2 SATA connector is done through Channel Selection Switch (SW5). For more details on Channel selection options, refer **Table 3**.

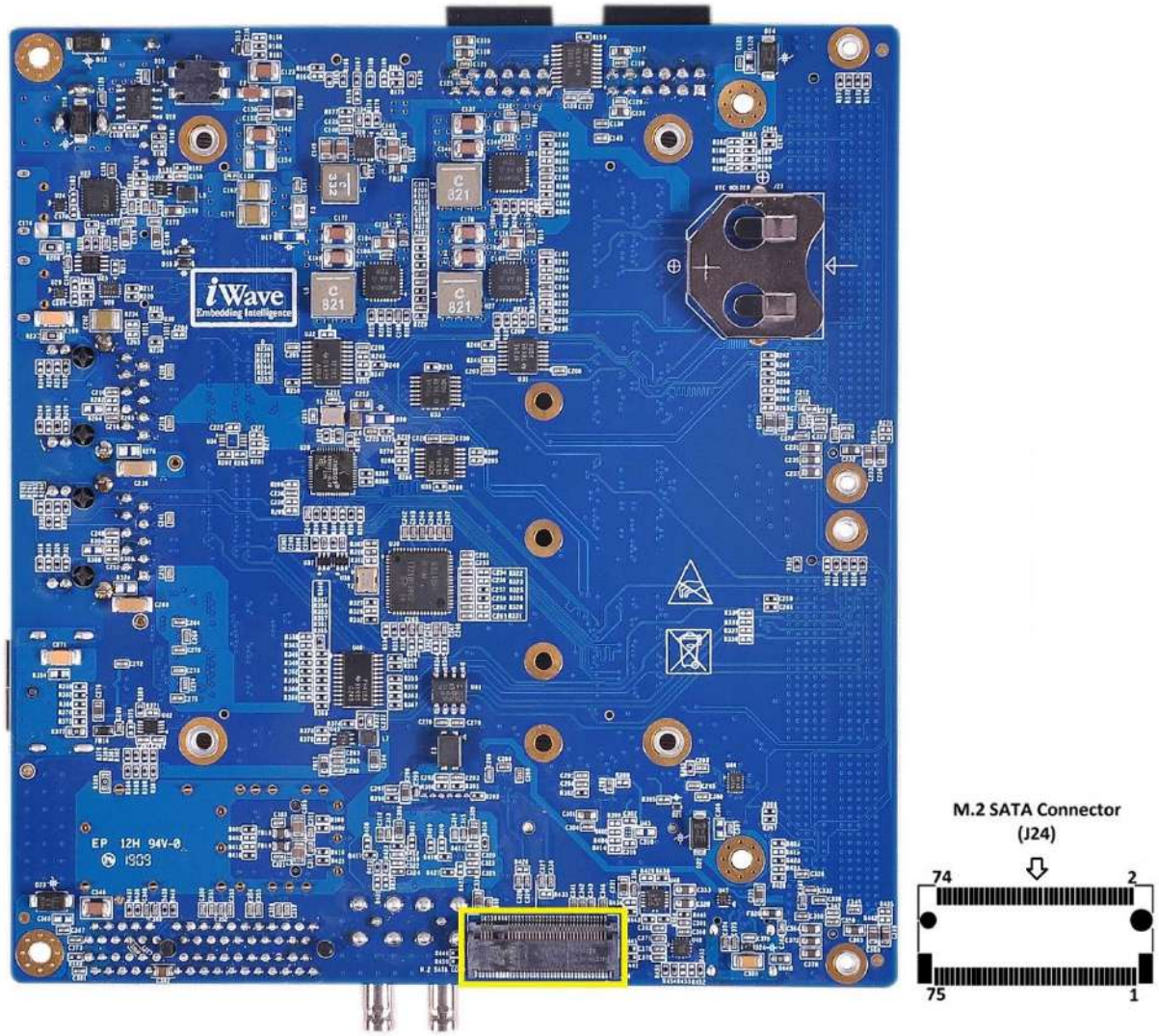


Figure 18: M.2 SATA Connector (Key B)

Table 8: M.2 SATA Connector Pin Assignment

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	NA	NA	This pin is connected to Ground.
2	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
3	GND	GND	Power	Ground.
4	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
5	PERn3	NA	NA	NC.
6	N/A1	NA	NA	NC.
7	PERp3	NA	NA	NC.
8	N/A2	NA	NA	NC.
9	GND	GND	Power	Ground.
10	DAS/DSS	NA	NA	NC.
11	PETn3	NA	NA	NC.
12	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
13	PETp3	NA	NA	NC.
14	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
15	GND	GND	Power	Ground.
16	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
17	PERn2	NA	NA	NC.
18	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
19	PERp2	NA	NA	NC.
20	N/A3	NA	NA	NC.
21	CONFIG_0	NA	NA	This pin is connected to Ground.
22	N/A4	NA	NA	NC.
23	PETn2	NA	NA	NC.
24	N/A5	NA	NA	NC.
25	PETp2	NA	NA	NC.
26	N/A6	NA	NA	NC.
27	GND	GND	Power	Ground.
28	N/A7	NA	NA	NC.
29	PERn1	NA	NA	NC.
30	N/A8	NA	NA	NC.
31	PERp1	NA	NA	NC.
32	N/A9	NA	NA	NC.
33	GND	GND	Power	Ground.
34	N/A10	NA	NA	NC.
35	PETn1	NA	NA	NC.
36	N/A11	NA	NA	NC.
37	PETp1	NA	NA	NC.
38	DEVSLP	NA	NA	NC.
39	GND	GND	Power	Ground.
40	N/A12	NA	NA	NC.
41	SATA-B+/PERn0	GXBL1F_RX_CH4p	I, DIFF	SATA Receive pair positive.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
42	N/A13	NA	NA	NC.
43	SATA-B-/PERp0	GXBL1F_RX_CH4n	I, DIFF	SATA Receive pair negative.
44	N/A14	NA	NA	NC.
45	GND	GND	Power	Ground.
46	N/A15	NA	NA	NC.
47	SATA-A-/PETn0	GXBL1F_TX_CH4n	O, DIFF	SATA Transmit pair negative.
48	N/A16	NA	NA	NC.
49	SATA-A+/PETp0	GXBL1F_TX_CH4p	O, DIFF	SATA Transmit pair positive.
50	PERST#	NA	NA	NC.
51	GND	GND	Power	Ground.
52	CLKREQ#	NA	NA	NC.
53	REFCLKN	NA	NA	NC.
54	PEWAKE#	NA	NA	NC.
55	REFCLKP	NA	NA	NC.
56	MFG1	NA	NA	NC.
57	GND	GND	Power	Ground.
58	MFG2	NA	NA	NC.
59	M1	NA	NA	NC.
60	M2	NA	NA	NC.
61	M3	NA	NA	NC.
62	M4	NA	NA	NC.
63	M5	NA	NA	NC.
64	M6	NA	NA	NC.
65	M7	NA	NA	NC.
66	M8	NA	NA	NC.
67	N/A17	NA	NA	NC.
68	SUSCLK	NA	NA	NC.
69	CONFIG_1	NA	NA	This pin is connected to Ground.
70	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
71	GND	GND	Power	Ground.
72	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
73	GND	GND	Power	Ground.
74	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
75	CONFIG_2	NA	NA	This pin is connected to Ground.

2.5.2.4 USB Type-C Connector

The Arria10 SoC/FPGA Carrier board hardware supports one Super Speed USB3.0 OTG through USB Type-C connector. The Bank1E CH4 High speed transciver of Arria10 SoC/FPGA from Board to Board Connector2 is used for USB3.0 OTG interface. The Bank1E CH4 selection to USB Type-C connector is done through Channel Selection Switch (SW5). For more details on Channel selection options, refer **Table 3**.

The Arria10 SoC/FPGA Carrier board supports "FUSB302" USB Type-C controller for port detection & cable orientation and controlled through I2C0 interface. To support double-way plug in on USB Type-C connector, Bank1E CH4 is connected to "FUSB340" 2:1 data Switch and then connected to USB TypeC connector. The channel selection to Type-C connector (top or bottom port) is controlled through FPGA Bank IO "FPGA_AG10_LVDS3A_4p_IO38" from Board to Board Connector1 pin70.

Also USB2.0 OTG interface of Arria10 SoC/FPGA is connected to USB Type-C connector for backward compatible USB2.0 support. The USB2.0 OTG PHY Transceiver output signals from Board to Board connector2 is connected to "FUSB340" USB Switch for selecting the USB2.0 OTG conenction between USB2.0 MicroAB connector (J8) and USB3.0 Type-C connector (J20). The selection can be done by setting the Single bit DIP switch (SW4). If the DIP switch (SW4) is set to ON, USB2.0 OTG is connected to MicroAB connector (J8) and if the DIP switch (SW4) is set to OFF, USB2.0 OTG is connected to USB3.0 TypeC connector (J20).

The USB3.0 OTG port can be used as full functional OTG functionality which supports USB3.0 host and USB2.0 device based on Type-C . The VBUS power of this USB Type-C connector is connected through current limit power switch which can be used to switch On/Off the power based on the device or Host and also limits the current above 900mA in host mode. Enable pin of the USB Power switch is connected to the HPS GPIO "HPS_GPIO4(GPIO0_IO10)" from Board to Board connector2 pin38. This USB Type-C connector (J20) is physically located at the top of the board as shown below.

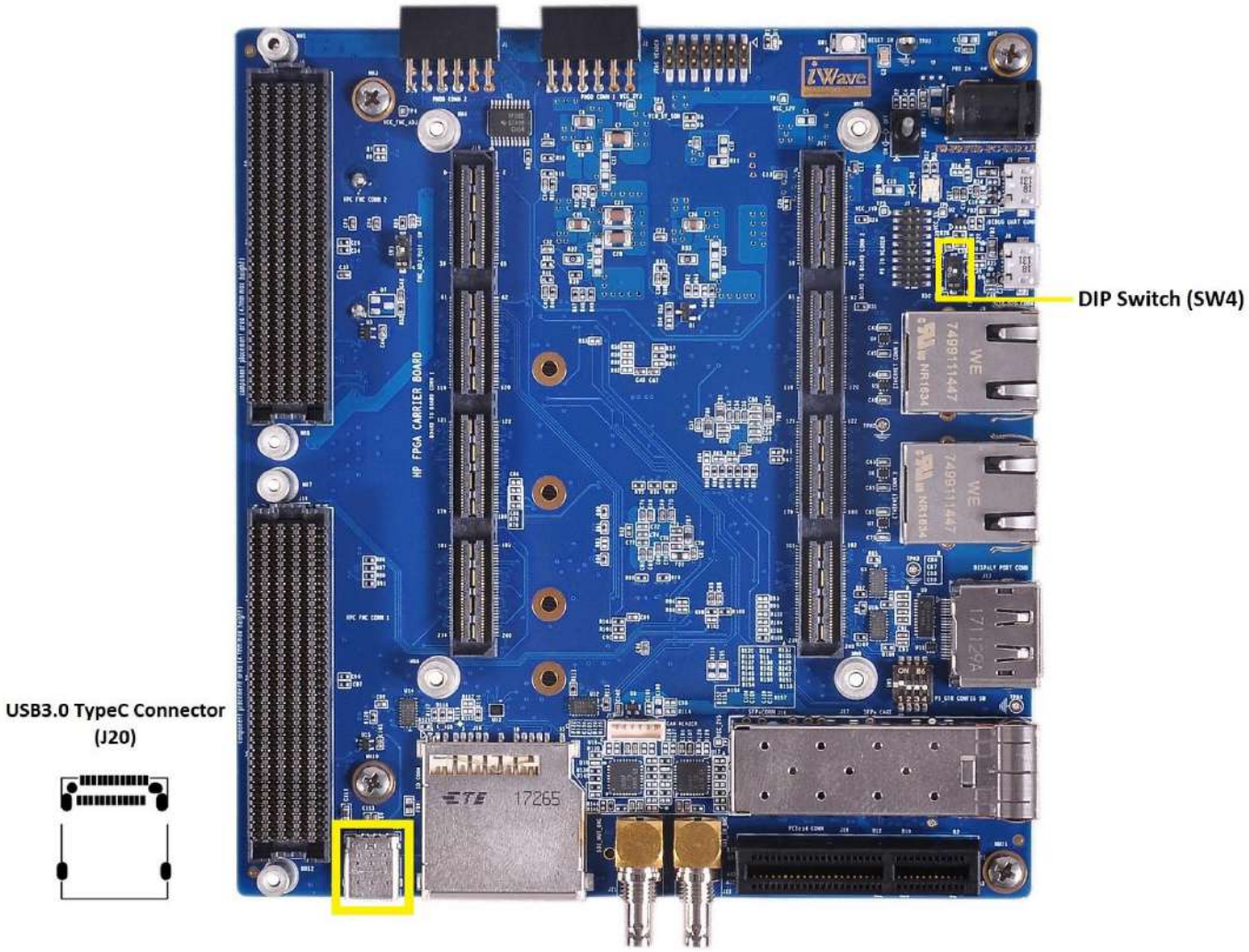


Figure 19: USB Type-C Connector

2.5.2.5 Display Port Connector

The Arria10 SoC/FPGA Carrier board supports one Display port connector through Bank1C CH4 & Bank1D CH4 transceiver. These transceivers from Board to Board Connector1 is connected to Display port connector to support single or dual lane display port. The channel selection to Display port connector is done through Channel Selection Switch (SW5).

The Display port connector supports AUX+ & AUX- signals from the FPGA Bank IOs. Also it supports Hot plug detect signal and connected to FPGA Bank IO. This Display Port connector (J13) is physically located at the top of the board as shown below.

*Note: For more details on Channel selection options, refer **Table 3**.*

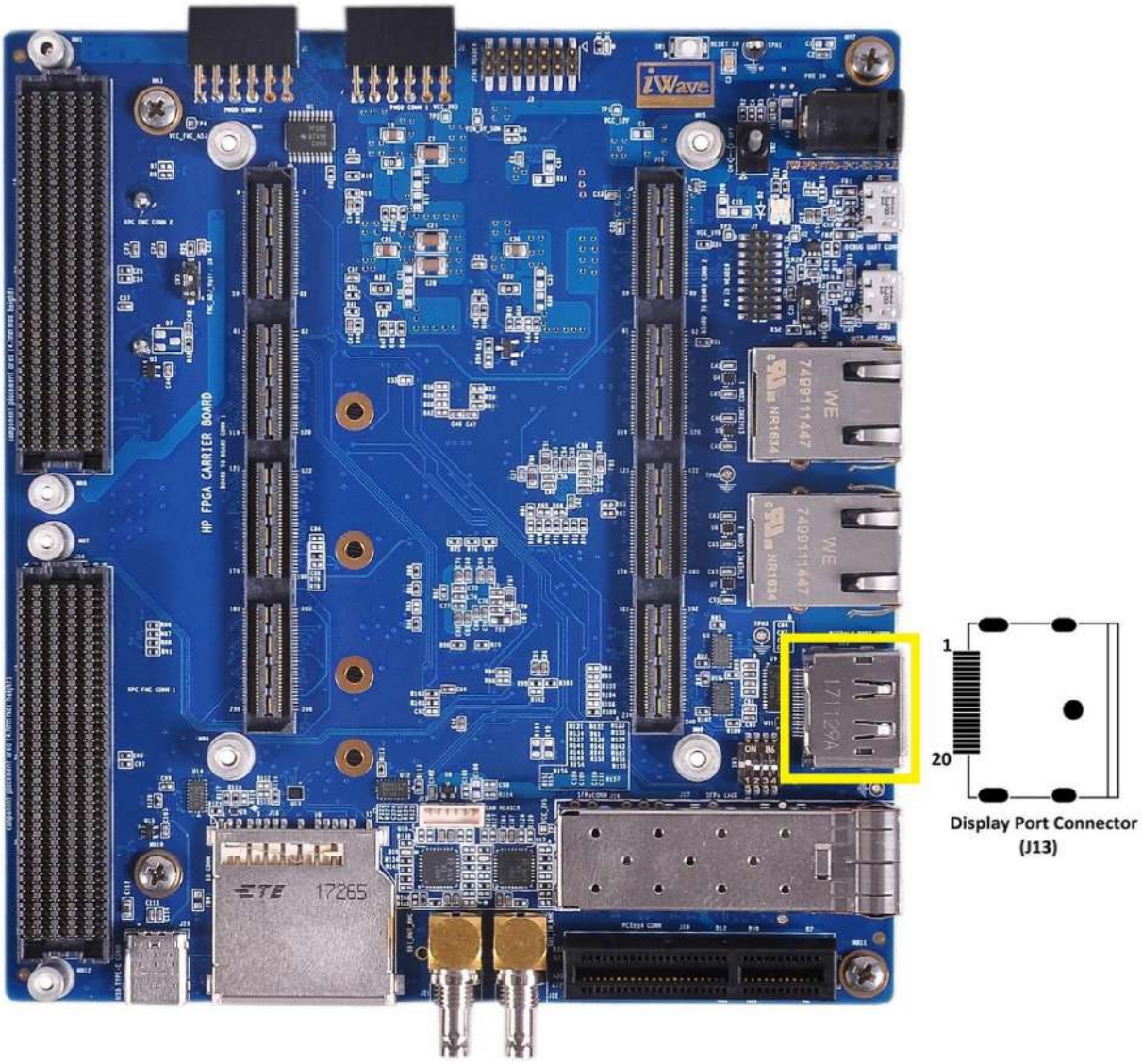


Figure 20: Display Port Connector

Table 9: Display Port Connector Pin Assignment

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	DP_L0+	GXBL1D_TX_CH4p	O, DIFF	Display Port Lane0 Transmit pair positive.
2	GND	GND	Power	Ground.
3	DP_L0-	GXBL1D_TX_CH4n	O, DIFF	Display Port Lane0 Transmit pair negative.
4	DP_L1+	GXBL1C_TX_CH4p	O, DIFF	Display Port Lane1 Transmit pair positive.
5	GND	GND	Power	Ground.
6	DP_L1-	GXBL1C_TX_CH4n	O, DIFF	Display Port Lane1 Transmit pair negative.
7	DP_L2+	NA	NA	NC.
8	GND	GND	Power	Ground.
9	DP_L2-	NA	NA	NC.
10	DP_L3+	NA	NA	NC.
11	GND	GND	Power	Ground.
12	DP_L3-	NA	NA	NC.
13	CONFIG1	NA	1M PD	Configuration Pin.
14	CONFIG2	NA	1M PD	Configuration Pin.
15	AUX_CH+	FPGA_AJ4_LVDS3B_21p	IO, DIFF/ 100K PD	Auxiliary channel positive.
16	GND	GND	Power	Ground.
17	AUX_CH-	FPGA_AH4_LVDS3B_21n	IO, DIFF/ 100K PU	Auxiliary channel negative.
18	HOT_PLUG	FPGA_AM8_LVDS3A_21n	O,3.3V CMOS/ 100K PD	Hot Plug Detect.
19	RETURN	NA	NA	NC.
20	DP_PWR	DP_PWR	O, 3.3V Power	3.3V Supply Voltage.

2.5.3 Pmod Host Port Connectors

Pmod interface or Peripheral Module interface is a standard defined by Digilent Inc The Pmod interface is used to connect low frequency, low I/O pin count peripheral modules to host controller boards. There are twelve-pin of the interface defined, encompassing SPI, I²C, UART, I2S and GPIO protocols.

The Arria10 SoC/FPGA Carrier board supports two 12pin Pmod host port connector for plugging Pmod modules. Since Pmod interface specification requires 3.3V IO level, the signals from Board to Board connector is connected to Pmod Connectors through Voltage level translator. Pmod Host port connector1 (J2) and Connector2 (J1) are physically located at the top of the board as shown below.

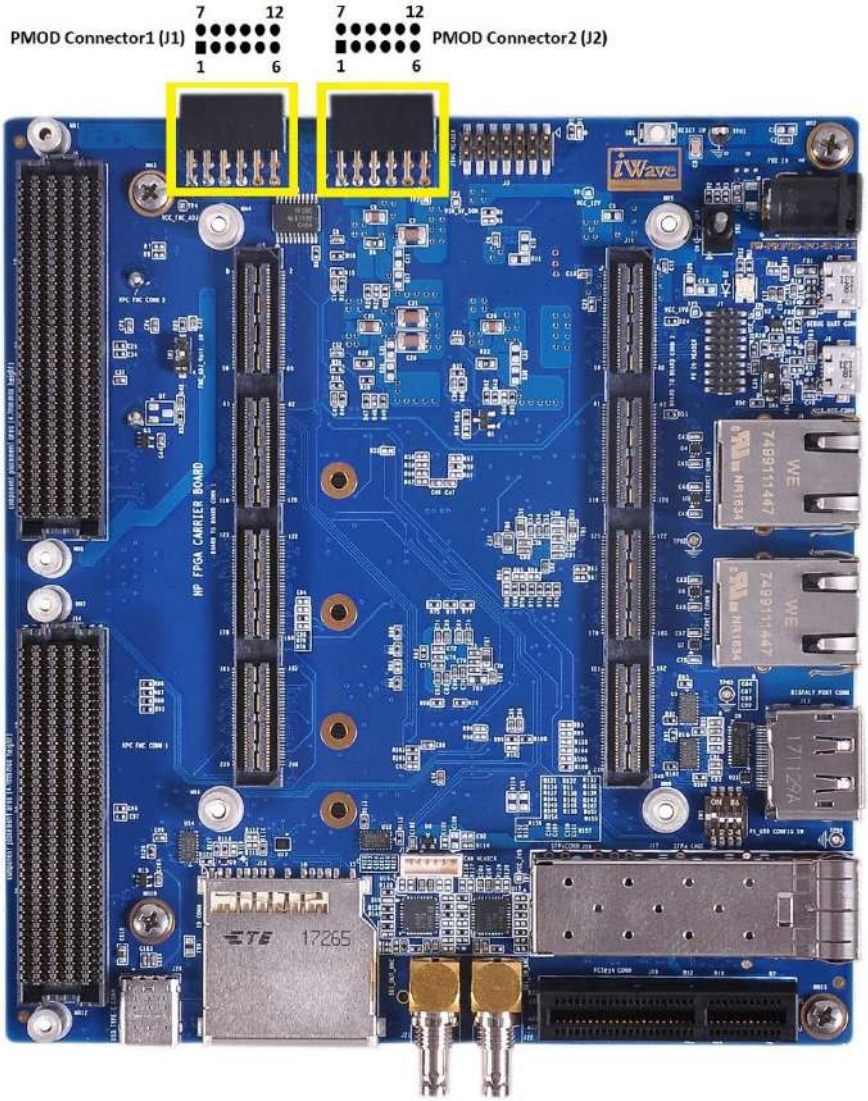


Figure 21: Pmod Host Port Connectors

Table 10: Pmod Connector1 Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	FPGA_AC9_LVDS3B_9p	IO, 3V3 LVDS	General purpose Input Output.
2	FPGA_AC10_LVDS3B_9n	IO, 3V3 LVDS	General purpose Input Output.
3	FPGA_AG6_LVDS3B_17p	IO, 3V3 LVDS	General purpose Input Output.
4	FPGA_AF6_LVDS3B_17n	IO, 3V3 LVDS	General purpose Input Output.
5	GND	Power	Ground.
6	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.
7	FPGA_AB8_LVDS3B_4p	IO, 3V3 LVDS	General purpose Input Output.
8	FPGA_AB7_LVDS3B_4n	IO, 3V3 LVDS	General purpose Input Output.
9	FPGA_AE6_LVDS3B_11p	IO, 3V3 LVCMOS	General purpose Input Output.
10	FPGA_AE7_LVDS3B_11n	IO, 3V3 LVCMOS	General purpose Input Output.
11	GND	Power	Ground.
12	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.

Table 11: Pmod Connector2 Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	FPGA_AF5_LVDS3B_14n	IO, 3V3 LVCMOS	General purpose Input Output.
2	FPGA_AG5_LVDS3B_14p	IO, 3V3 LVCMOS	General purpose Input Output.
3	FPGA_AD5_LVDS3B_8p	IO, 3V3 LVCMOS	General purpose Input Output.
4	FPGA_AD6_LVDS3B_8n	IO, 3V3 LVCMOS	General purpose Input Output.
5	GND	Power	Ground.
6	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.
7	FPGA_AC7_LVDS3B_7n	IO, 3V3 LVCMOS	General purpose Input Output.
8	FPGA_AD7_LVDS3B_7p	IO, 3V3 LVCMOS	General purpose Input Output.
9	FPGA_AK3_LVDS3B_22n	IO, 3V3 LVCMOS	General purpose Input Output.
10	FPGA_AK4_LVDS3B_22p	IO, 3V3 LVCMOS	General purpose Input Output.
11	GND	Power	Ground.
12	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.

2.6 Additional Features

2.6.1 Clock Synthesizer/Generator

The Arria10 SoC/FPGA Carrier board supports one 10-output Clock Synthesizer "SI5341B-D-GM" for on board clock distribution. This Clock Generator outputs are connected to high Speed Transceiver Banks (1C, 1D, 1E & 1F) Reference Clock pins of Board to Board Connectors through 0.01uF AC coupling capacitors. An external 48MHz crystal is connected to this Clock Synthesizer for reference. This Clock Synthesizer supports from 100 Hz to 1028 Mhz clock output and configurable through HPS I2C0. The Clock Synthesizer I2C address is 0X76.

Table 12: Clock Synthesizer Output Clocks

Pin No	Pin Name	Signal Name	Programmed Frequency	Connected To
23	OUT0b	GXBL1F_RX_CH5n_GXB1F_REFCLK5n	125MHZ.	B2B-2 220th pin.
24	OUT0	GXBL1F_RX_CH5p_GXB1F_REFCLK5p		B2B-2 218th pin.
30	OUT2b	GXBL1D_RX_CH5n_GXB1D_REFCLK5n	27MHZ.	B21-2 169th pin.
31	OUT2	GXBL1D_RX_CH5p_GXB1D_REFCLK5p		B2B-1 171th pin.
34	OUT3b	GXBL1E_RX_CH5n_GXB1E_REFCLK5n	52MHZ.	B2B-2 232th pin.
35	OUT3	GXBL1E_RX_CH5p_GXB1E_REFCLK5p		B2B-2 230th pin.
37	OUT4b	PCIe_REFCLKP	100MHZ.	PCIex 4 connector A14th pin.
38	OUT4	PCIe_REFCLKP		PCIex 4 connector A13th pin.
41	OUT5b	GXBL1C_RX_CH5n_GXB1C_REFCLK5n	100MHZ.	B2B-1 75th pin.
42	OUT5	GXBL1C_RX_CH5p_GXB1C_REFCLK5p		B2B-1 77th pin.
44	OUT6b	REFCLK_GXBL1C_CHBn	100MHZ.	B2B-1 66th pin.
45	OUT6	REFCLK_GXBL1C_CHBp		B2B-1 64th pin.
50	OUT7b	REFCLK_GXBL1D_CHBn	125MHZ.	B2B-1 160th pin.
51	OUT7	REFCLK_GXBL1D_CHBp		B2B-1 158th pin.
53	OUT8b	REFCLK_GXBL1E_CHBn	125MHZ.	B2B-1 220th pin.
54	OUT8	REFCLK_GXBL1E_CHBp		B2B-1 218th pin.
58	OUT9b	REFCLK_GXBL1F_CHBn	148.5MHZ.	B2B-2 225th pin.
59	OUT9	REFCLK_GXBL1F_CHBp		B2B-2 223th pin.

Note: In Arria10 SoC/FPGA Development board, High Speed Transceiver clocks are connected from the dedicated clocks on FMC HPC Connectors.

2.6.2 IO Expander

The Arria10 SoC/FPGA Carrier board supports one “TCA6416A” GPIO 16-Bit port Expander. This GPIO 16-Bit port Expander controls the enable pin of SFP+ Control signals and FMC Control Signals. This GPIO 16-Bit port Expander is connected to HPS I2C0 through level translator. The GPIO 16-Bit port Expander I2C address is 0X72.

2.6.3 JTAG Connector

A Standard 14-pin JTAG Header is available in Arria10 SoC/FPGA Carrier board for debug purpose. JTAG signals from Board to Board connector2 is directly connected to JTAG Header (J3) and same JTAG signals are also connected to FMC connector. JTAG-HS2/ JTAG-HS3 programming cable can be plugged to this JTAG Header for programming and debugging purpose. This JTAG Header (J3) is physically located at the top of the board as shown below.

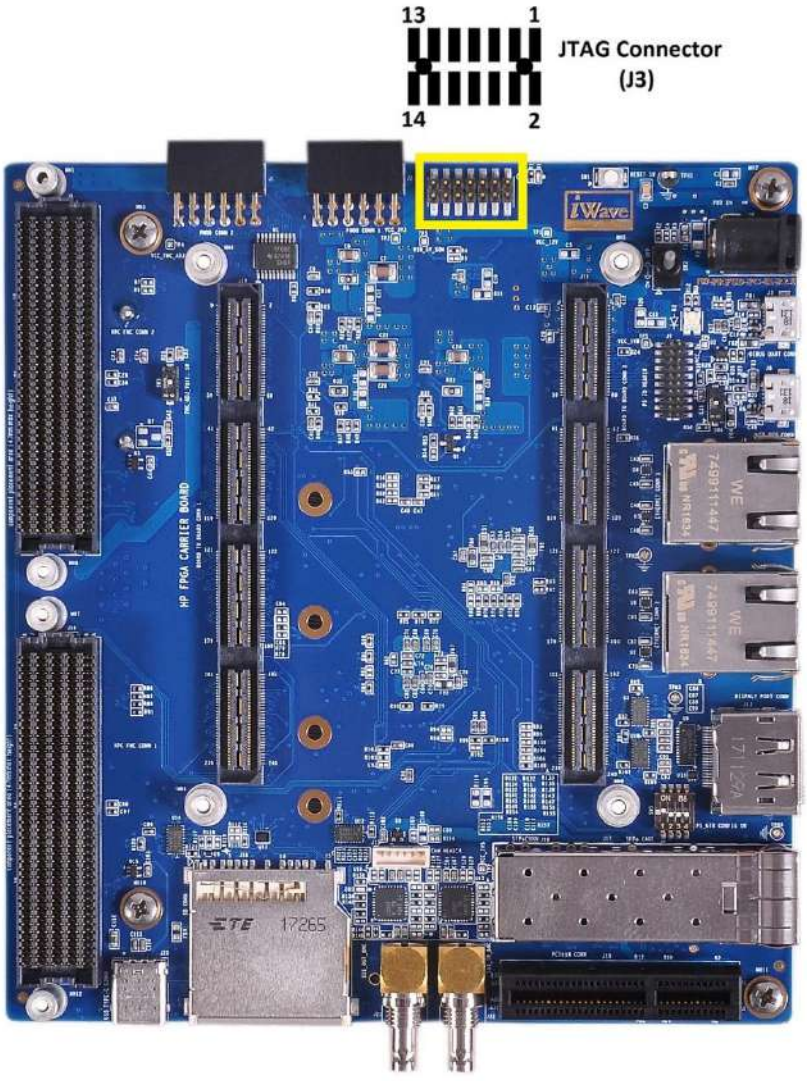


Figure 22: JTAG Connector

Table 13: JTAG Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	NC	-	Not Connected
2	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.
3	GND	Power	Ground
4	CSS_TMS	I, 3V3 LVCMOS/ 49.9K PU	JTAG test mode select.
5	GND	Power	Ground
6	CSS_TCK	I, 3V3 LVCMOS/ 49.9K PU	JTAG test Clock
7	GND	Power	Ground
8	CSS_TDO	O,3V3 LVCMOS/ 49.9K PU	JTAG test data output.
9	GND	Power	Ground
10	CSS_TDI	I, 3V3 LVCMOS	JTAG test data input
11	GND	Power	Ground
12	CSS_TRST	I, 3V3 LVCMOS	JTAG test reset
13	GND	Power	Ground
14	JTAG_RESET	I,3V3 LVCMOS/ 49.9K PU	JTAG reset.

2.6.4 GPIO Header

The Arria10 SoC/FPGA Carrier board supports GPIO Header (J7) for General Purpose. This Header signals are directly connected from Board to Board connectors. This header supports I2C0, SPI and Bank 2A GPIOs. This GPIO Header (J7) is physically located at the top of the board as shown below.

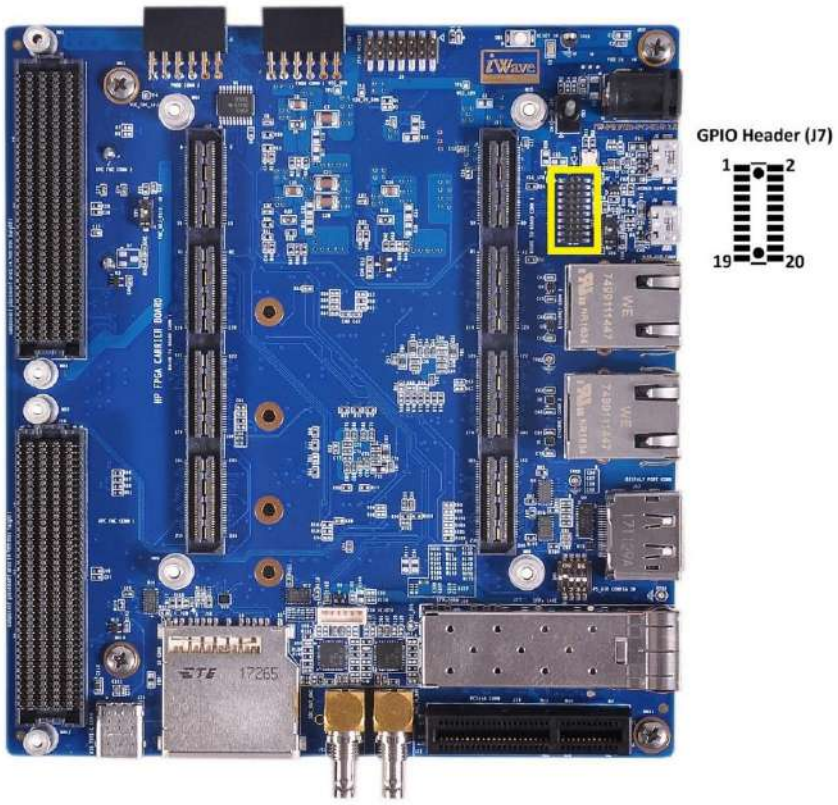


Figure 23: GPIO Header

Table 14: GPIO Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_1V8	O, 1.8V Power	1V8 Supply Voltage.
2	VCC_5V	O, 5V Power	5V Supply Voltage.
3	FPGA_AM18_LVDS2A_7p	IO, 1.8V LVDS	Bank 2A IO7 differential positive. This Pin is connected to 211th pin of Board to Board Connector1 (J10).
4	HPS_GPIO0_IO4/I2C0_SDA	IO, 1.8V OD/ 4.7K PU	I2C0 data. Also, same pin can be configured as General purpose Input Output. This Pin is connected to 46th pin of Board to Board Connector2 (J11).
5	FPGA_AN18_LVDS2A_7n	IO, 1.8V LVDS	Bank 2A IO7 differential negative. This Pin is connected to 213rd pin of Board to Board Connector1 (J10).

Pin No	Signal Name	Signal Type/ Termination	Description
6	HPS_GPIO0_IO5/I2C0_SCL	IO, 1.8V OD/ 4.7K PU	I2C0 Clock. Also, same pin can be configured as General purpose Input Output. This Pin is connected to 48th pin of Board to Board Connector2 (J11).
7	FPGA_AJ14_LVDS2A_14p	IO, 1.8V LVCMOS	General Purpose Input/Output. This Pin is connected to 178rd pin of Board to Board Connector1 (J10).
8	HPS_GPIO0_IO6/EMAC2_ MDIO	O, 1.8V LVCMOS	General Purpose Input/Output. This Pin is connected to 50th pin of Board to Board Connector2 (J11).
9	FPGA_AH14_LVDS2A_14n	IO, 1.8V LVCMOS	General Purpose Input/Output. This Pin is connected to 176th pin of Board to Board Connector1 (J10).
10	HPS_GPIO0_IO7/EMAC2_ MDC	IO, 1.8V LVCMOS	General Purpose Input/Output. This Pin is connected to 52nd pin of Board to Board Connector2 (J11).
11	GND	Power	Ground
12	GND	Power	Ground
13	HPS_SPIM0_CLK/EMAC2_T XD2	IO, 1.8V LVCMOS	SPI Clock output. Also, same pin can be configured as General purpose Input Output. This Pin is connected to 61st pin of Board to Board Connector2 (J11).
14	NC	NA	NC.
15	HPS_SPIM0_SS0_N/EMAC2 _RXD3	O, 1.8V LVCMOS	SPI Chip select 0. Also, same pin can be configured as General purpose Input Output. This Pin is connected to 63rd pin of Board to Board Connector2 (J11).
16	NC	NA	NC.
17	HPS_SPIM0_MOSI/EMAC2 _TXD3	IO, 1.8V LVCMOS	SPI Master output Slave input. Also, same pin can be configured as General purpose Input Output. This Pin is connected to 65th pin of Board to Board Connector2 (J11).
18	HPS_SPIM0_MISO/EMAC2 _RXD2	IO, 1.8V LVCMOS	SPI Master input Slave output. Also, same pin can be configured as General purpose Input Output. This Pin is connected to 67th pin of Board to Board Connector2 (J11).
19	GND	Power	Ground
20	GND	Power	Ground

2.6.5 Power ON/OFF Switch

The Arria10 SoC/FPGA Carrier board has power ON/OFF switch (SW2) to control the Main power Input ON/OFF functionality. This power ON/OFF switch is physically located at the top of the board as shown below.

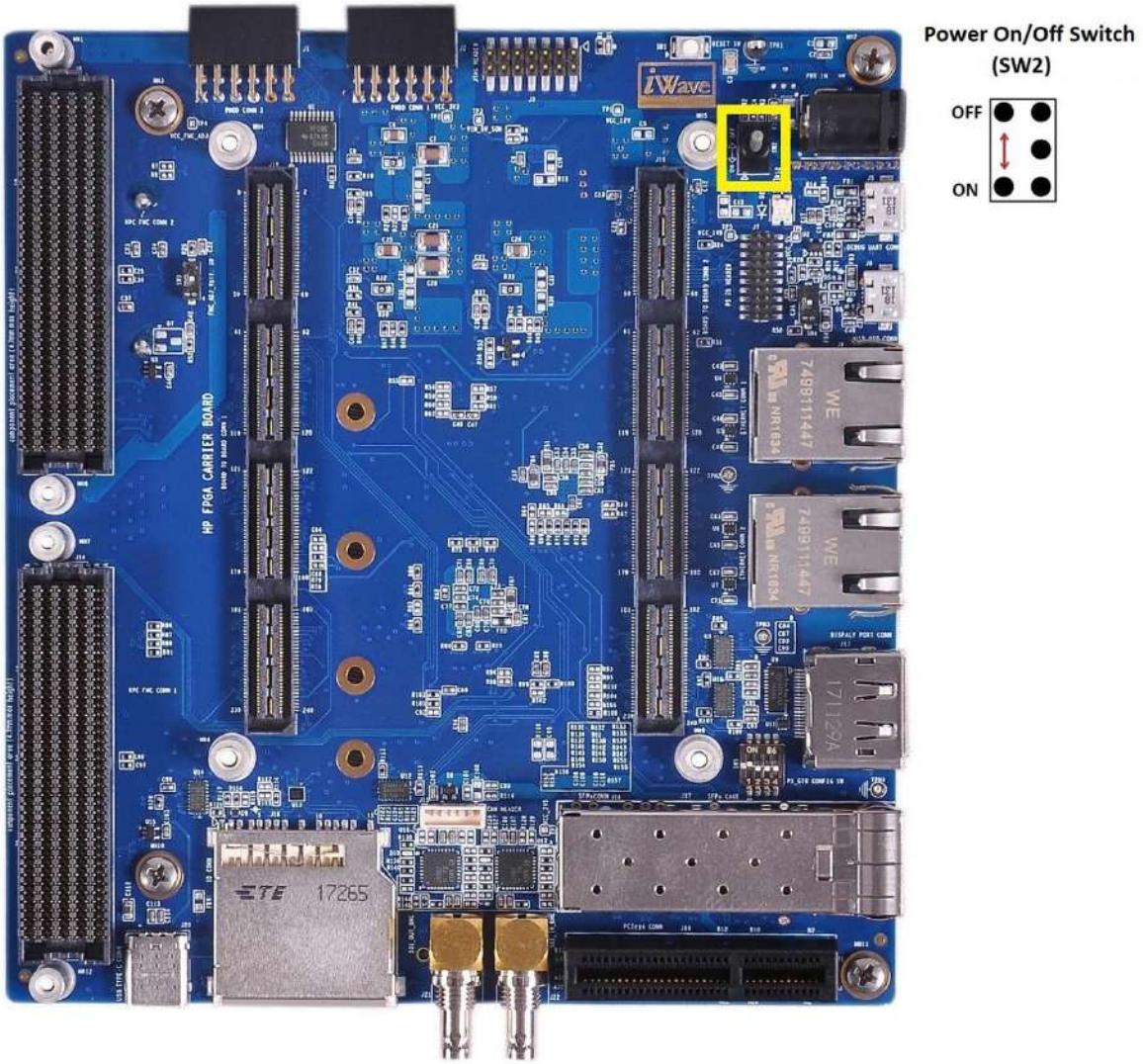


Figure 24: Power On/Off Switch

2.6.6 Reset Switch

The Arria10 SoC/FPGA Carrier board supports Push button switch (SW1) to reset the Arria10 SoC/FPGA CPU. Reset signal of Board to Board connector2 Pin35 is directly connected from Reset Push button switch. This Reset Push button switch (SW1) is physically located at the top of the board as shown below.

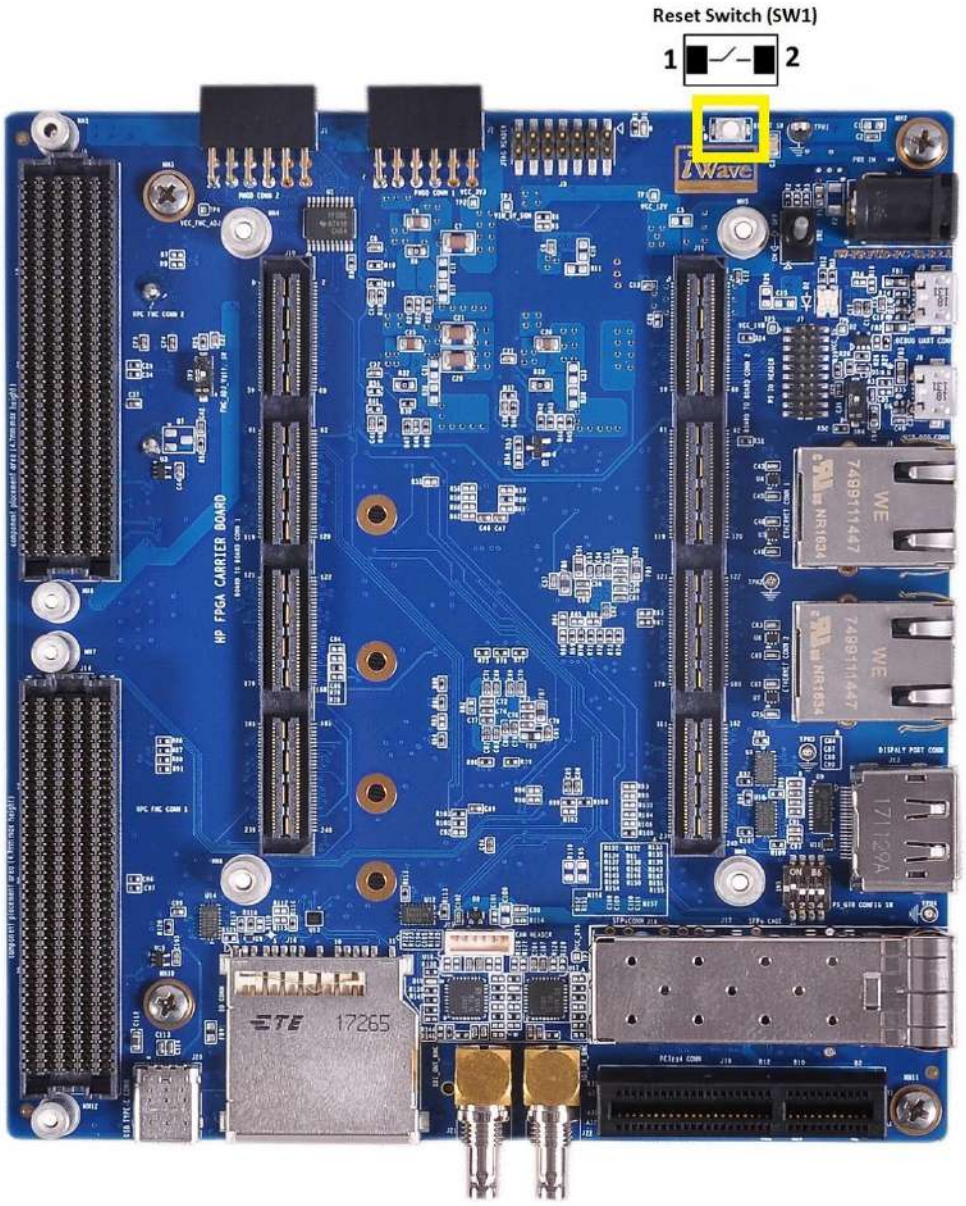


Figure 25: Reset Switch

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Arria10 SoC/FPGA Carrier Board technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Power Input Requirement

The Arria10 SoC/FPGA Carrier Board is designed to work with 12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the Arria10 SoC/FPGA Carrier Board through Power Jack (J4). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. This connector is physically placed at the top of the board as shown below.

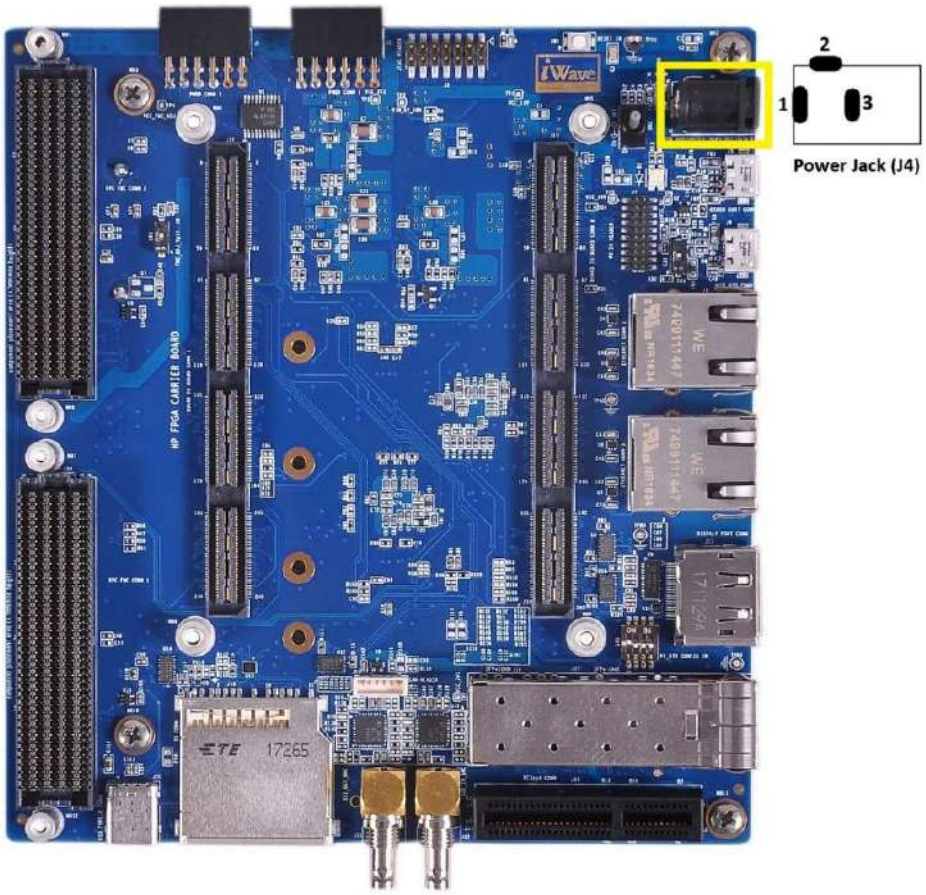


Figure 26: Power Jack

The below table provides the Power Input Requirement Arria10 SoC/FPGA Carrier Board.

Table 15: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V	11.75V	12V	12.25V	±50mV

3.2 Power Output Specification

The Arria10 SoC/FPGA Carrier Board has dedicated power regulator to provide +5V power to SOM for VCC power supply.

The Arria10 SoC/FPGA Carrier Board also shares different on-board power to FMC connectors, Pmod connectors and GPIO Header for its Add-On Module power.

Table 16: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current
To Board to Board Connector2 (for Arria10 SoC/FPGA SOM)					
1	VCC_5V	4.85V	5V	5.15V	15A
To FMC Connector1					
1	VCC_FMC_ADJ	1.75	1.8	1.85	4A
2	VCC_3V3	3.15	3.3	3.45	3A
3	3P3VAUX	3.15	3.3	3.45	100mA
4	VCC_12V	11.75V	12V	12.25V	1A
To FMC Connector2					
1	VCC_FMC_ADJ	1.75	1.8	1.85	4A
2	VCC_3V3	3.15	3.3	3.45	3A
3	3P3VAUX	3.15	3.3	3.45	100mA
4	VCC_12V	11.75V	12V	12.25V	1A
To Pmod Connector1					
1	VCC_3V3	3.15	3.3	3.45	500mA
To Pmod Connector2					
1	VCC_3V3	3.15	3.3	3.45	500mA
To GPIO Header					
1	VCC_5V	3.15	3.3	3.45	500mA
2	VCC_1V8	1.75	1.8	1.85	200mA

3.3 Environmental Characteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of Arria10 SoC/FPGA Development platform.

Table 17: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	0°C	70°C

[1] *iWave only guarantees the component selection for the given operating temperature.*

3.3.2 RoHS Compliance

iWave's Arria10 SoC/FPGA Development platform is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave's Arria10 SoC/FPGA Development platform is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use board except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 Carrier Board Mechanical Dimensions

The High-Performance carrier board PCB form factor is 130mm x 140mm and Board mechanical dimension is shown below.

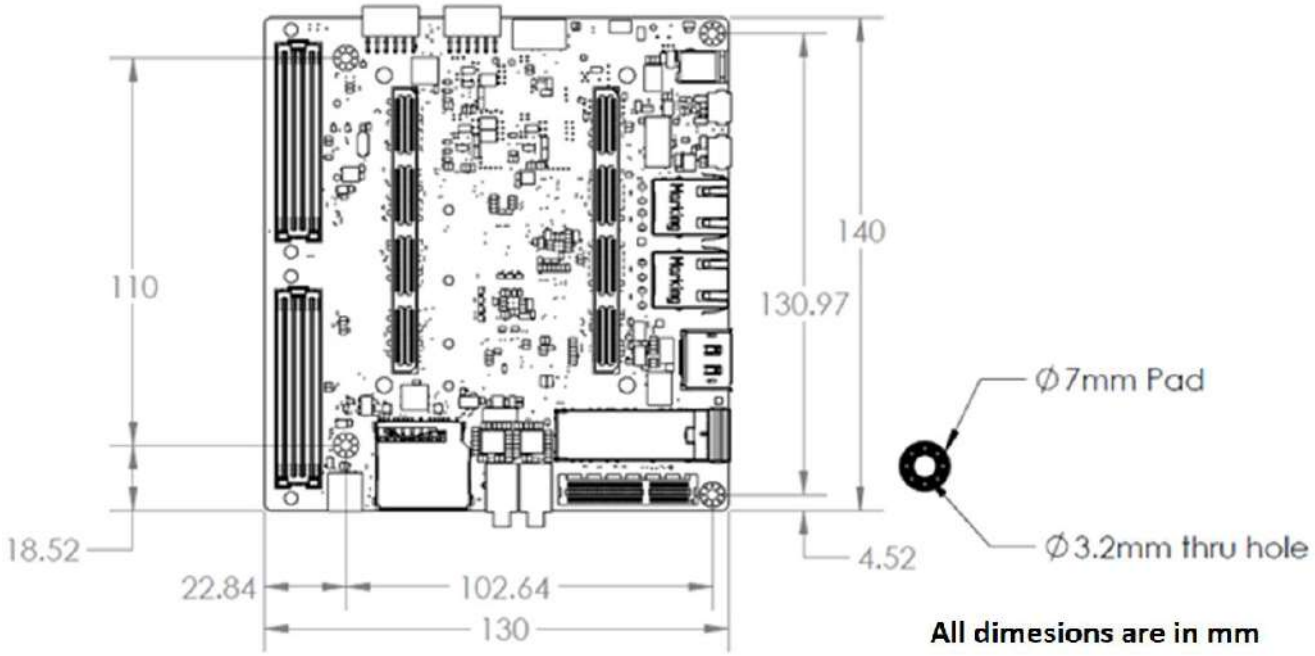


Figure 27: Carrier board Mechanical dimension – Top View

The High-performance carrier board PCB thickness is 1.55mm±0.1mm, top side maximum height component is Ethernet Connector (15.27mm) and bottom side maximum height component is M.2 SATA Connector (4.20mm). Please refer the below figure for height details of the Arria10 SoC/FPGA Carrier board.

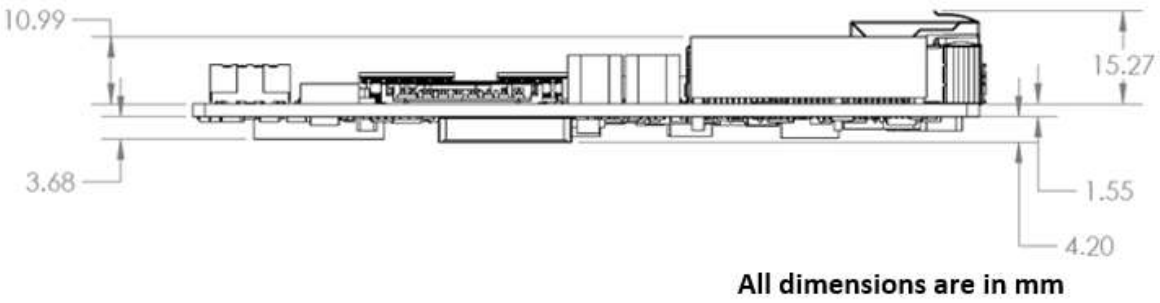


Figure 28: Carrier board Mechanical dimension – Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for Arria10 SoC/FPGA Development platform which includes Arria10 SoC/FPGA SOM and Carrier Board.

Table 18: Orderable Product Part Numbers

Product Part Number	Description	Temperature
Arria10 SoC/FPGA based SOM Development Platform		
TBD	TBD	TBD

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.


iWave
Embedding Intelligence