VN5T016AH-E

Datasheet

Single channel high-side driver with analog current sense for 24 V automotive applications

HPAK

Features

Description	Parameter	Value
Max. transient supply voltage	V_{CC}	58 V
Operating voltage range	V_{CC}	8 to 36 V
Typ. on-state resistance (per channel)	R_{ON}	16 mΩ
Current limitation (typ.)	I_{LIM}	60 A
Off-state supply current	I_S	2 µA (1)

1. *Typical value with all loads connected.*

- AEC-Q100 qualified
- General
  - Very low standby current
  - 3.0 V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - Compliant with European directive 2002/95/EC
  - Fault reset standby pin (FR_Stby)
  - Optimized for LED application
- Diagnostic functions
  - Proportional load current sense
  - Current sense precision for wide range currents
  - Off-state open load detection
  - Output short to V_{CC} detection
  - Overload and short to ground latch-off
  - Thermal shutdown latch-off
  - Very low current sense leakage
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Thermal shutdown
  - Reverse battery protected with self switch of the Power MOSFET
  - Electrostatic discharge protection

Product status link
VN5T016AH-E

Product summary	
Order code	**VN5T016AH-E**
Package	HPAK
Packing	Tube
Order code	**VN5T016AHTR-E**
Package	HPAK
Packing	Tape and reel

Applications

- All types of resistive, inductive and capacitive loads

Description

The VN5T016AH-E is a device made using STMicroelectronics VIPower technology, intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes.

The device integrates an analog current sense, which delivers a current proportional to the load current.

Fault conditions such as overload, overtemperature, or short to V_{CC} are reported via the current sense pin.

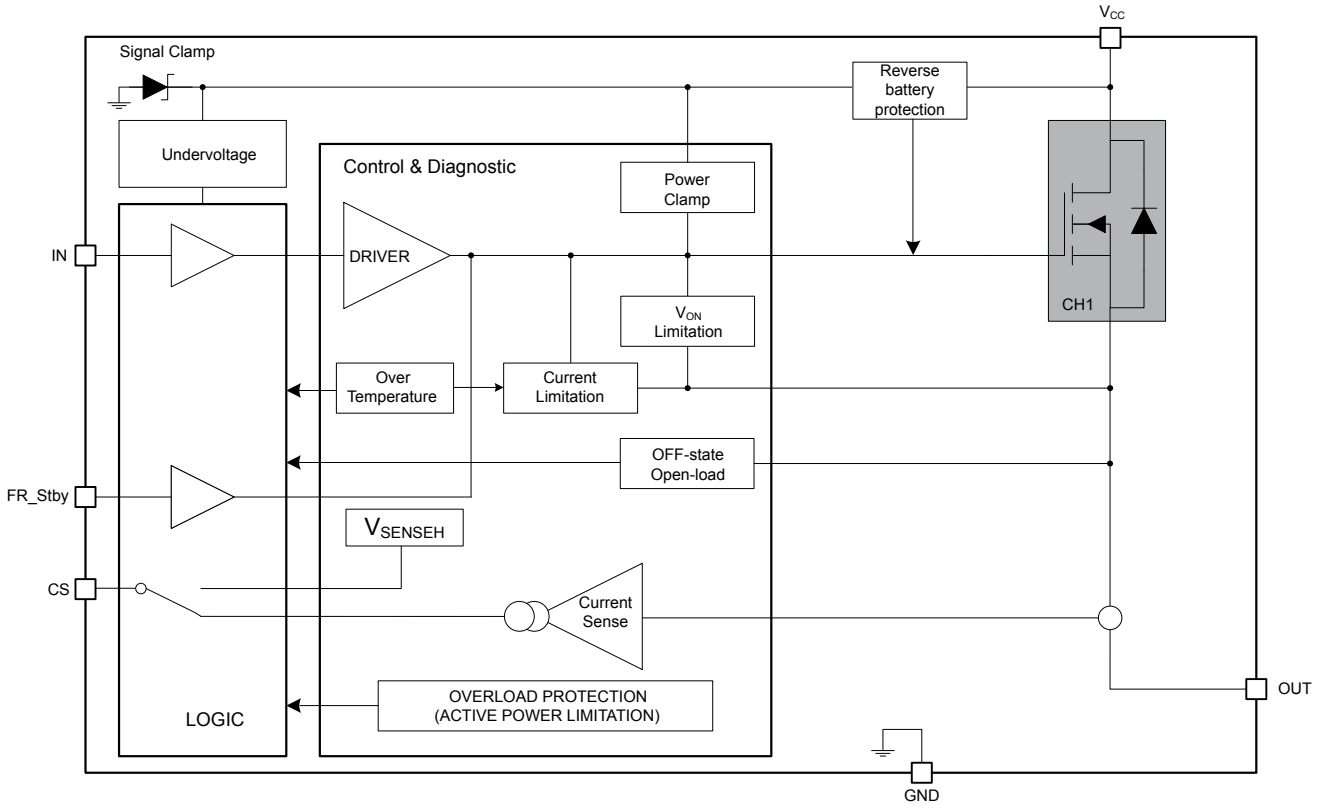
Output current limitation protects the device in overload conditions. The device latches off in case of overload or thermal shutdown.

The device is reset by a low level pass on the fault reset standby pin.

A permanent low level on the inputs and on the fault reset standby pin disables all outputs and sets the device in standby mode.

1 Block diagram and pin description

Figure 1. Block diagram

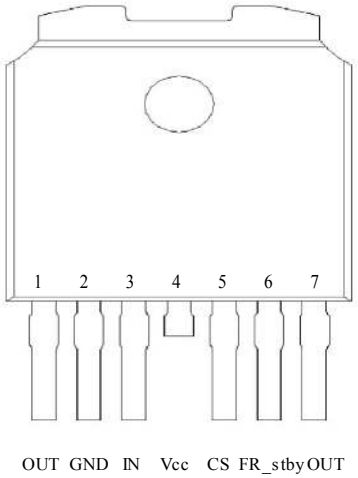


GAPGCFT00198

Table 1. Pin function

Name	Function
V_{CC}	Battery connection
OUT	Power output
GND	Ground connection
IN	Voltage controlled input pin with hysteresis, CMOS compatible. It controls output switch state
CS	Analog current sense pin, it delivers a current proportional to the load current
FR_Stby	In case of latch-off for overtemperature/overcurrent condition, a low pulse on the FR_Stby pin is needed to reset the channel. The device enters in standby mode if all inputs and the FR_Stby pin are low

Figure 2. Configuration diagram (top view)



GAPGCFT00653

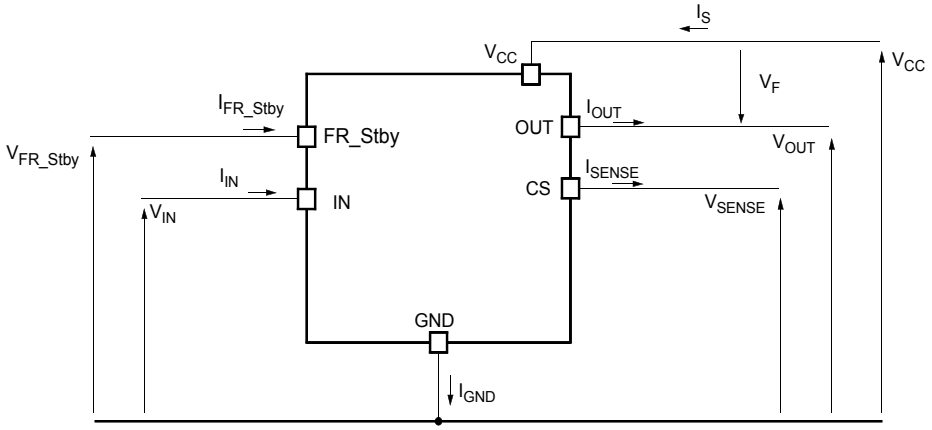
Table 2. Suggested connections for unused and not connected pins

Connection/pin	CurrentSense	NC	Output	Input	FR_Stby
Floating	Not allowed	X(1)	X	X	X
To ground	Through 10 kΩ resistor	X	Not allowed	Through 10 kΩ resistor	Through 10 kΩ resistor

1. *X: do not care.*

2 Electrical specification

Figure 3. **Current and voltage conventions**



GAPGCFT00195

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the Table 3 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 3. **Absolute maximum ratings**

Symbol	Parameter		Value	Unit
V_{CC}	DC supply voltage		58	V
$-V_{CC}$	Reverse DC supply voltage		-32	V
I_{OUT}	DC output current		Internally limited	A
$-I_{OUT}$	Reverse DC output current		30	A
I_{IN}	DC input current		-1 to 10	mA
I_{FR_Stby}	Fault reset standby DC input current		-1 to 1.5	mA
V_{CSENSE}	Current sense maximum voltage		(V_{CC} - 58) to V_{CC}	V
E_{MAX}	Maximum switching energy (L = 10 mH; V_{BAT} = 32 V; T_{Jstart} = 150 °C; I_{OUT} = 5.9 A		390	mJ
L_{smax}	Maximum stray inductance in short circuit condition R_L = 300 mΩ, V_{BAT} = 32 V, T_{Jstart} = 150 °C, I_{OUT} = $I_{limH\ (max.)}$		40	µH
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 kΩ, C = 100 pF)	IN	4000	V
		CS	2000	
		FR_Stby	4000	
		OUT	5000	
		V_{CC}	5000	
V_{ESD}	Charge device model (CDM-AEC-Q100-011)		750	V
T_J	Junction operating temperature		-40 to 150	°C

Symbol	Parameter	Value	Unit
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.5	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	See Figure 27	°C/W

2.3 Electrical characteristics

8 V < V_{CC} < 36 V, -40 °C < T_J < 150 °C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		8	24	36	V
V_{USD}	Undervoltage shutdown			3.5	5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance	I_{OUT} = 5 A, T_J = 25 °C, 8 V < V_{CC} < 36 V		16		mΩ
		I_{OUT} = 5 A, T_J = 150 °C, 8 V < V_{CC} < 36 V			32	
$R_{ON\ REV}$	Reverse battery on-state resistance	V_{CC} = -24 V, I_{OUT} = -5 A, T_J = 25 °C			16	mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA	58	64	70	V
I_S	Supply current	Off-state, V_{CC} = 24 V, T_J = 25 °C, V_{IN} = V_{OUT} = V_{SENSE} = 0 V, V_{FR_Stby} = 0 V		2[1]	5	µA
		On-state, V_{CC} = 24 V, V_{IN} = 5 V, I_{OUT} = 0 A		2.5	5	mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} =0 V, V_{CC} = 24 V, T_J = 25 °C	0	0.01	3	µA
		V_{IN} = V_{OUT} =0 V, V_{CC} = 24 V, T_J = 125 °C	0		5	

1. *Power MOSFET leakage included.*

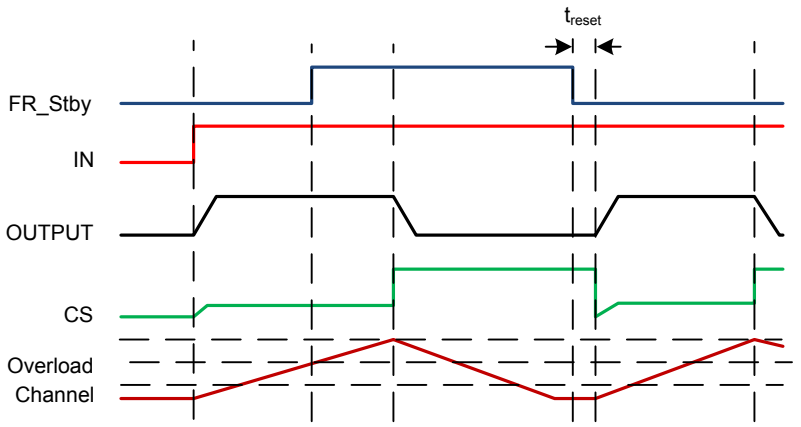
Table 6. Switching (V_{CC} = 24 V, T_J = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 4.8 Ω		55		µs
$t_{d(off)}$	Turn-off delay time	R_L = 4.8 Ω		53		µs
$(dV_{OUT}/dt)_{(on)}$	Turn-on voltage slope	R_L = 4.8 Ω		0.59		V/µs
$(dV_{OUT}/dt)_{(off)}$	Turn-off voltage slope	R_L = 4.8 Ω		0.54		V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 4.8 Ω		2.35		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 4.8 Ω		1.05		mJ

Table 7. Logic inputs

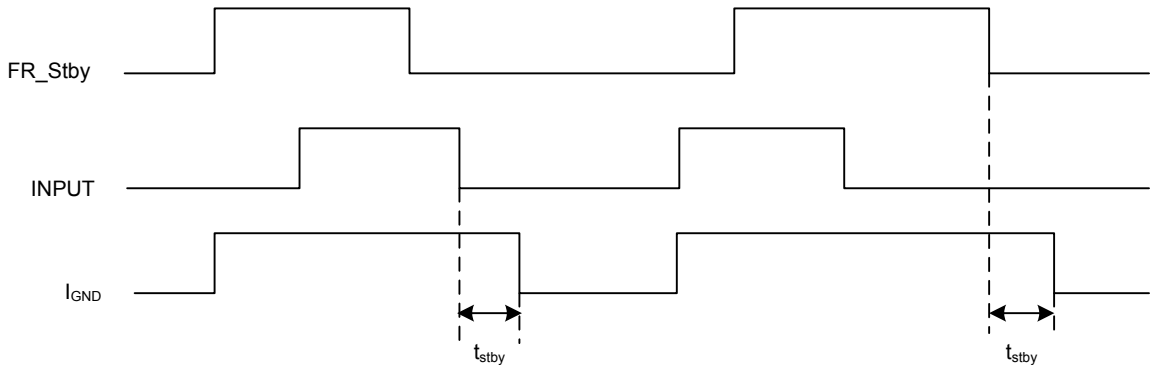
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		
$V_{FR\_Stby\_L}$	Fault_reset_standby low level voltage				0.9	V
$I_{FR\_Stby\_L}$	Low level fault_reset_standby current	V_{FR_Stby} = 0.9 V	1			µA
$V_{FR\_Stby\_H}$	Fault_reset_standby high level voltage		2.1			V
$I_{FR\_Stby\_H}$	High level fault_reset_standby current	V_{FR_Stby} = 2.1 V			10	µA
$V_{FR\_Stby(hyst)}$	Fault_reset_standby hysteresis voltage		0.25			V
$V_{FR\_Stby\_CL}$	Fault_reset_standby clamp voltage	I_{FR_Stby} = 15 mA (10 ms)	11		15	V
		I_{FR_Stby} = -1 mA		-0.7		V
t_{reset}	Overload latch-off reset time	See Figure 4	2		24	µs
t_{stby}	Standby delay	See Figure 5	120		1200	µs

Figure 4. t_{reset} definition



GAPGCFT000112

Figure 5. t_{stby} definition



GAPGCFT000111

Table 8. **Protections and diagnostics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC} = 24 V	43	60	86	A
		5 V < V_{CC} < 36 V			86	
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 24 V, T_R < T_J < T_{TSD}		15		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of status		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 5 A, V_{IN} = 0 V, L = 6 mH	V_{CC} - 58	V_{CC} - 64	V_{CC} - 70	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 500 mA, T_J = -40 °C to 150 °C		25		mV

Table 9. Current sense (8 V < V_{CC} < 36 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dK_{LED}/K_{LEDTOT} (1)	Current sense ratio drift	I_{OUT} = 12 mA to 100 mA, I_{OUTCAL} = 50 mA, V_{SENSE} = 0.5 V, T_J = -40 °C to 150 °C	-50		50	%
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 100 mA, V_{SENSE} = 0.5 V, T_J = -40 °C to 150 °C	1333	5600	11884	
dK_0/K_0 (1)	Current sense ratio drift	I_{OUT} = 100 mA, V_{SENSE} = 0.5 V, T_J = -40 °C to 150 °C	-21		32	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.6 A, V_{SENSE} = 1 V, T_J = -40 °C to 150 °C	2418	5300	9264	
		I_{OUT} = 0.6 A, V_{SENSE} = 1 V, T_J = 25 °C to 150 °C	3139		7981	
dK_1/K_1 (1)	Current sense ratio drift	I_{OUT} = 0.6 A, V_{SENSE} = 1 V, T_J = -40 °C to 150 °C	-21		23	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 1.6 A, V_{SENSE} = 1 V, T_J = -40 °C to 150 °C	2928	4700	7568	
		I_{OUT} = 1.6 A, V_{SENSE} = 1 V, T_J = 25 °C to 150 °C	3072		6693	
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT} = 1.6 A, V_{SENSE} = 1 V, T_J = -40 °C to 150 °C	-26		21	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 2.4 A, V_{SENSE} = 2 V, T_J = -40 °C to 150 °C	2912	4400	7048	
		I_{OUT} = 2.4 A, V_{SENSE} = 2 V, T_J = 25 °C to 150 °C	3007		6039	
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT} = 2.4 A, V_{SENSE} = 2 V, T_J = -40 °C to 150 °C	-19		24	%
K_4	I_{OUT}/I_{SENSE}	I_{OUT} = 3 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	2843	4300	6686	
		I_{OUT} = 3 A, V_{SENSE} = 4 V, T_J = 25 °C to 150 °C	3142		5634	
dK_4/K_4 (1)	Current sense ratio drift	I_{OUT} = 3 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	-16		22	%
K_5	I_{OUT}/I_{SENSE}	I_{OUT} = 4.2 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	3034	4250	5977	
		I_{OUT} = 4.2 A, V_{SENSE} = 4 V, T_J = 25 °C to 150 °C	3402		5276	
dK_5/K_5 (1)	Current sense ratio drift	I_{OUT} = 4.2 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	-13		16	%
K_6	I_{OUT}/I_{SENSE}	I_{OUT} = 20 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	3942	4240	4748	
dK_6/K_6 (1)	Current sense ratio drift	I_{OUT} = 20 A, V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	-5		5	%
$dK/K_{bulb1(TOT)}$ (1)	Current sense ratio drift	I_{OUT} = 1.6 A to 4.2 A, I_{OUTCAL} = 3 A; V_{SENSE} = 4 V, T_J = -40 °C to 150 °C	-17		40	%

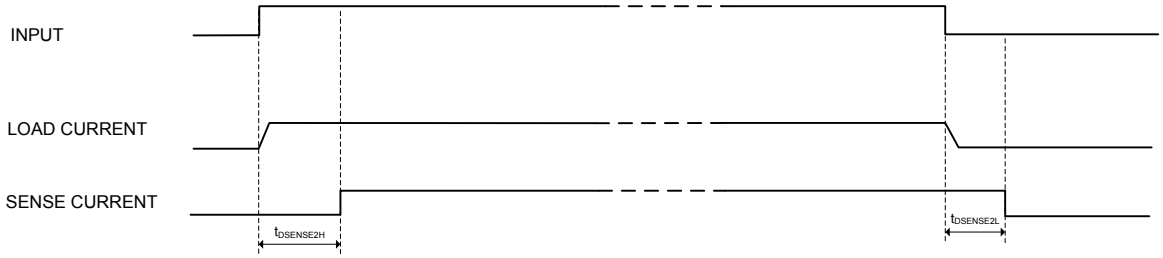
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$dK/K_{bulb2(TOT)}$ (1)	Current sense ratio drift	I_{OUT} = 0.6 A to 2.4 A, I_{OUTCAL} = 1.2 A, V_{SENSE} = 2 V, T_J = -40 °C to 150 °C	-31		33	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A, V_{SENSE} = 0 V, V_{IN} = 0 V, T_J = -40 °C to 150 °C	0		1	µA
		I_{OUT} = 0 A, V_{SENSE} = 0 V, V_{IN} = 5 V, T_J = -40 °C to 150 °C	0		2	
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 20 A, R_{SENSE} = 3.9 kΩ	5			V
V_{SENSEH}	Analog sense output voltage in fault condition(2)	V_{CC} = 24 V, R_{SENSE} = 3.9 kΩ		8		V
I_{SENSEH}	Analog sense output current in fault condition (2)	V_{CC} = 24 V, V_{SENSE} = 5 V		9	12	mA
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE} < 4 V, 0.5 A < I_{OUT} < 20 A, I_{SENSE} = 90% of I_{SENSE} max., (see Figure 6)		300	600	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4 V, I_{SENSE} = 90% of $I_{SENSEMAX}$, I_{OUT} = 90% of I_{OUTMAX}, I_{OUTMAX} = 5 A (see Figure 10)			450	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE} < 4 V, 0.5 A < I_{OUT} < 20 A, I_{SENSE} = 10% of I_{SENSE} max (see Figure 6)		3	20	µs

1. *Specified by design, not tested in production.*
2. *Fault condition includes: power limitation, overtemperature and openload in off-state condition.*

Table 10. Openload detection (V_{FR_Stby} = 5 V)

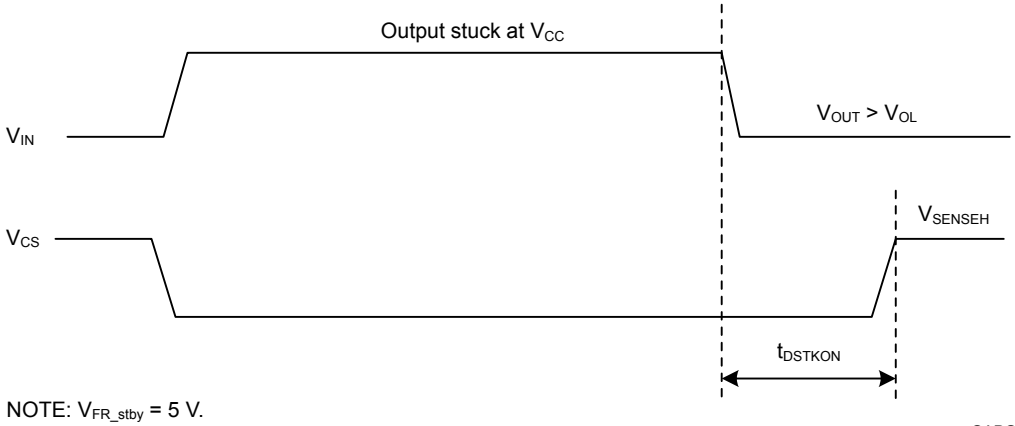
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Openload off-state voltage detection threshold	V_{IN} = 0 V, 8 V < V_{CC} < 36 V	2	-	4	V
t_{DSTKON}	Output short circuit to V_{CC} detection delay at turn off	See Figure 7	180	-	1800	µs
$I_{L(off2)}$	Off-state output current at V_{OUT} = 4 V	V_{IN} = 0 V, V_{SENSE} = 0 V, V_{OUT} rising from 0 V to 4 V	-120	-	0	µA
t_{d_vol}	Delay response from output rising edge to V_{SENSE} rising edge in openload	V_{OUT} = 4 V, V_{IN} = 0 V, V_{SENSE} = 90% of V_{SENSEH}, R_{SENSE} = 3.9 kΩ		-	20	µs
t_{DFRSTK_ON}	Output short circuit to V_{CC} detection delay at FR_Stby activation	See Figure 9, Input = low		-	50	µs

Figure 6. Current sense delay characteristics



GAPGCFT000117

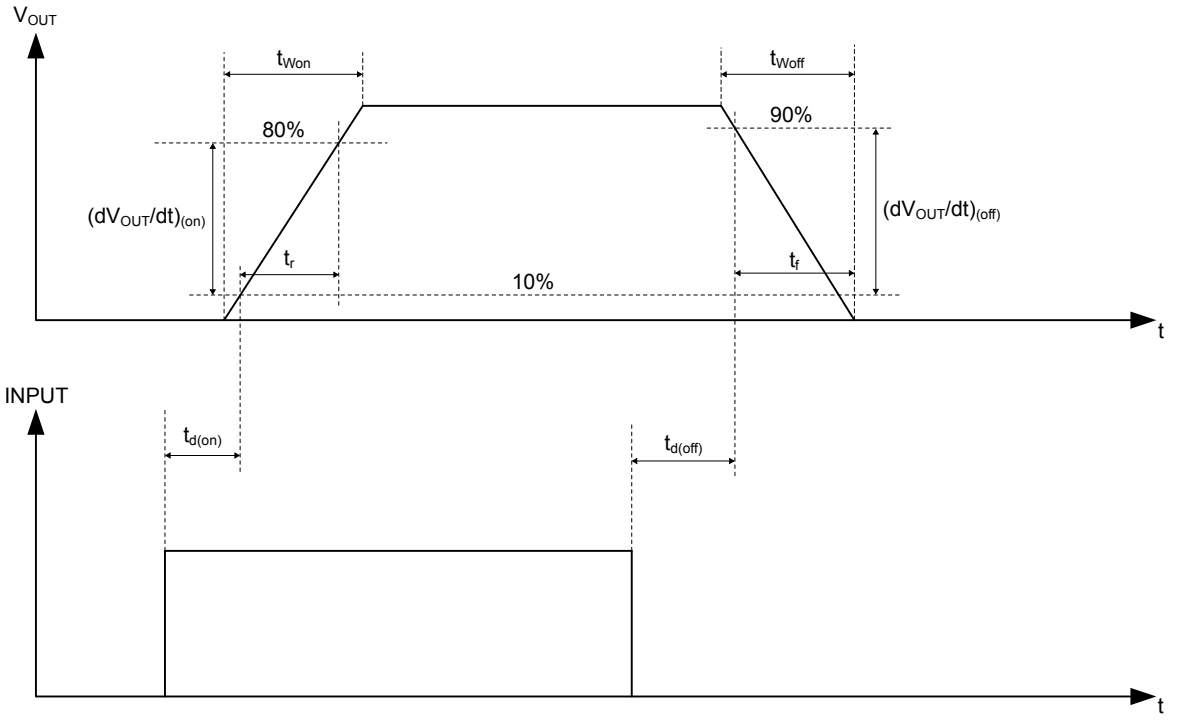
Figure 7. Openload off-state delay timing



NOTE: V_{FR_stby} = 5 V.

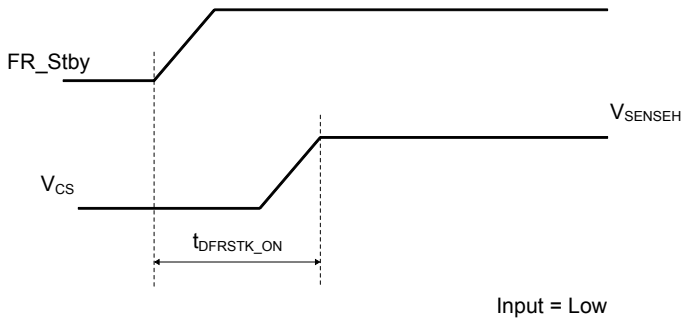
GAPGCFT000113

Figure 8. **Switching characteristics**



GAPGCFT000114

Figure 9. **Output stuck to V_{CC} detection delay time at FR_Stby activation**



GAPGCFT00038

Figure 10. Delay response time between rising edge of ouput current and rising edge of current sense

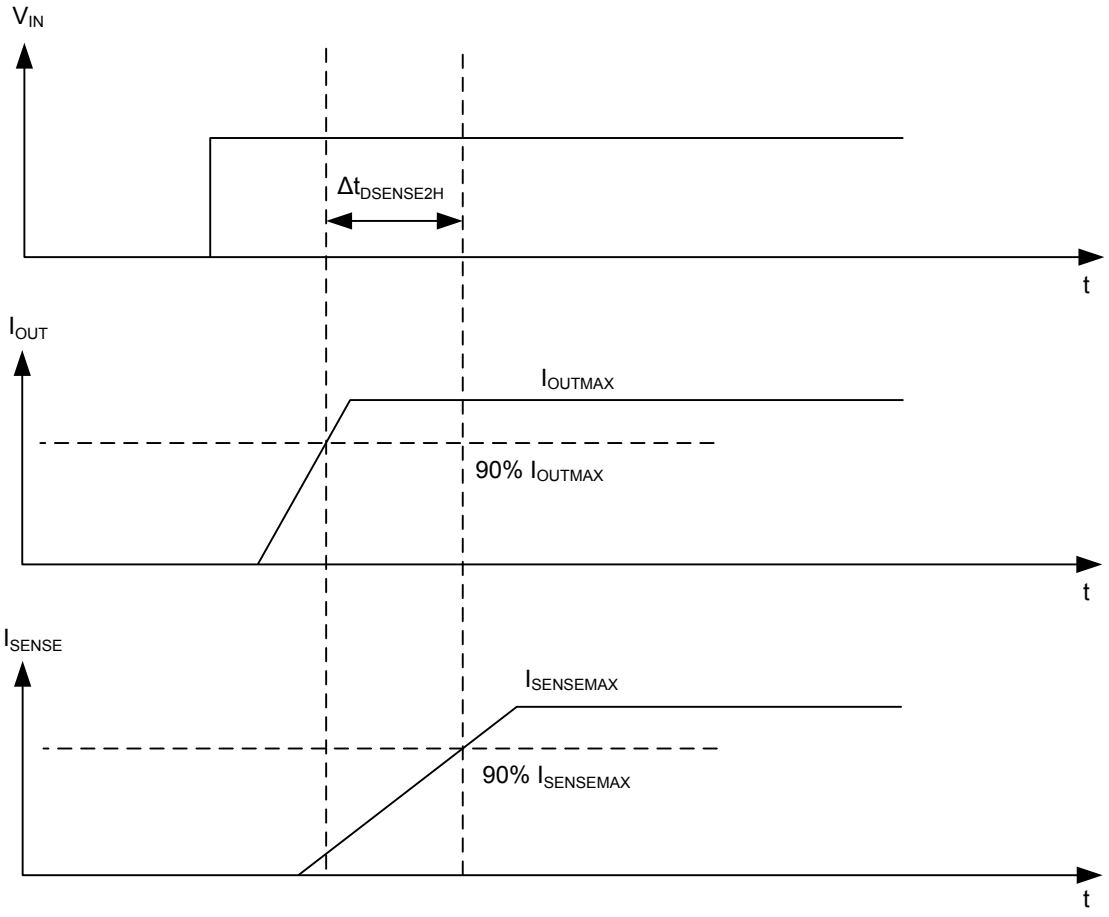


Figure 11. Output voltage drop limitation

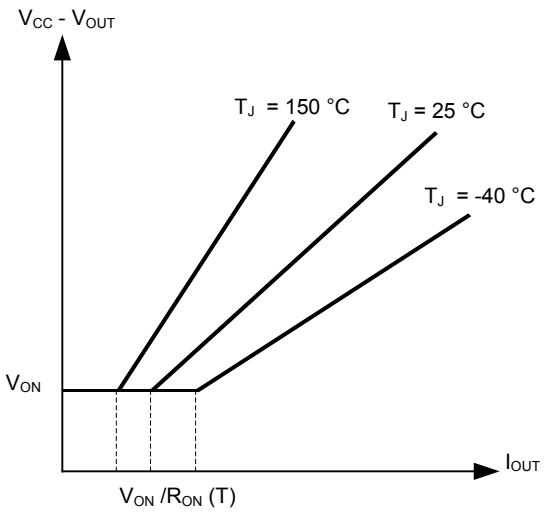
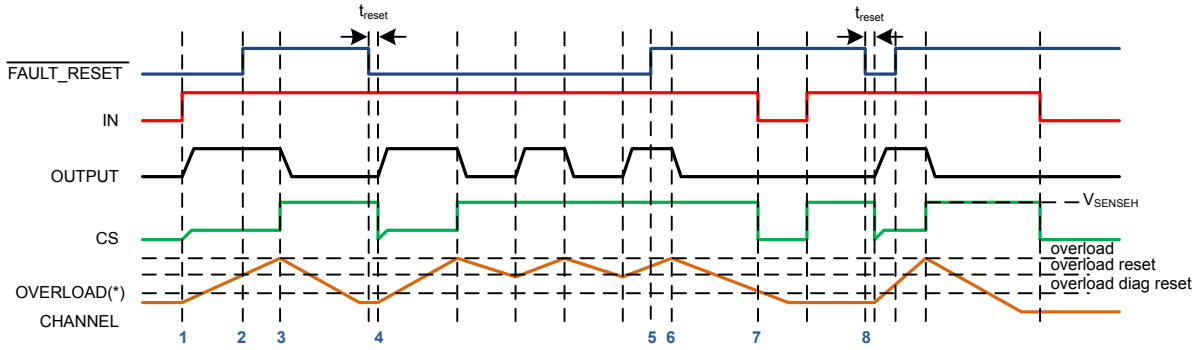


Figure 12. **Device behavior in overload condition**



1: OUTPUT and CS controlled by IN
2: FAULT_RESET from '0' to '1' → no action on CS pin
3: overload latch-off. IN high → CS high
4: FAULT_RESET low AND Temp channel < overload_reset → overload latch reset after t_{reset}
4 to 5: FAULT_RESET low AND IN high → thermal cycling, CS high
5: FAULT_RESET high → latch-off reset disabled
6 to 7: overload event and FAULT_RESET high → latch-off, no thermal cycling
7 to 8: overload diagnostic disabled/enabled by the input
8: overload latch-off reset by FAULT_RESET

(*) OVERLOAD = thermal shutdown OR power limitation

GAPGCFT000116

Table 11. **Truth table**

Conditions	Fault reset standby	Input	Output	Sense
Standby	L	L	X	0
Normal operation	X	L	L	0
	X	H	H	Nominal
Overload	X	L	L	0
	X	H	H	> Nominal
Overtemperature/short to ground	X	L	L	0
	L	H	Cycling	V_{SENSEH}
	H	H	Latched	V_{SENSEH}
Undervoltage	X	X	L	0
Short to V_{BAT}	L	L	H	0
	H	L	H	V_{SENSEH}
	X	H	H	< Nominal
Openload off-state (with pull-up)	L	L	H	0
	H	L	H	V_{SENSEH}
	X	H	H	0
Negative output voltage clamp	X	L	Negative	0

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedence
	III	IV				
1	-450 V	-600 V	5000 pulses	0.5 s	5 s	1 ms, 50 Ω
2a	37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-150 V	- 200 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+150 V	+200 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
4	-12 V	- 16 V	1 pulse			100 ms, 0.01 Ω
5b(2)	+123 V	+174 V	1 pulse			350 ms, 1 Ω

1. *The above test levels must be considered referred to V_{CC} = 24.5 V except for pulse 5b.*
2. *Valid in case of external load dump clamp: 58 V maximum referred to ground.*

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results	
	III	IV
1	C	C (1)
2a	C	C
3a	C	C
3b (2)	E	E
3b (3)	C	C
4	C	C
5b (4)	C	C

1. *With R_{load} < 24 Ω.*
2. *Without capacitor between V_{CC} and GND.*
3. *With 10 nF between V_{CC} and GND.*
4. *External load dump clamp, 58 V maximum, referred to ground.*

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Electrical characteristics (curves)

Figure 13. Off-state output current

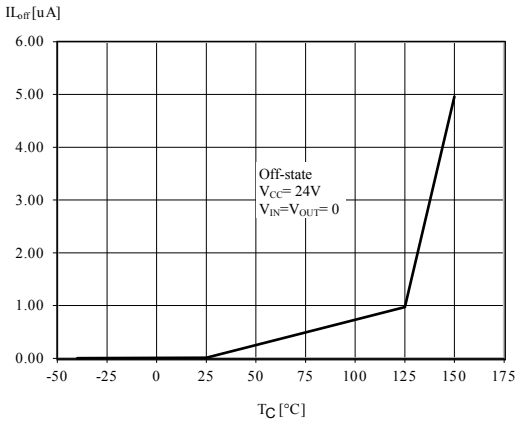


Figure 14. High level input current

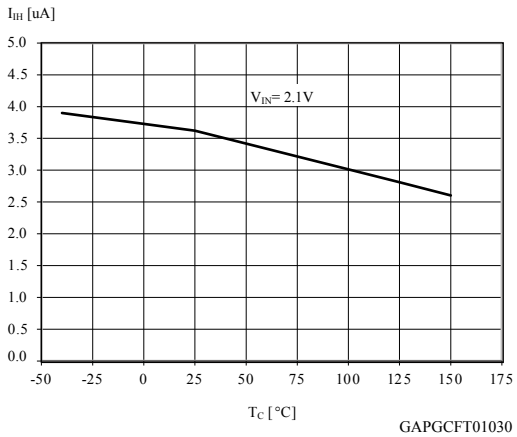


Figure 15. Input clamp voltage

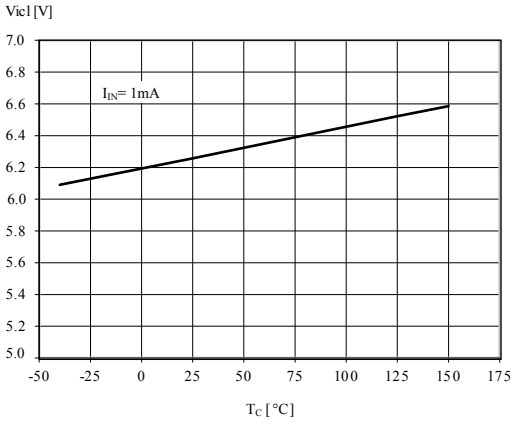


Figure 16. Input low level voltage

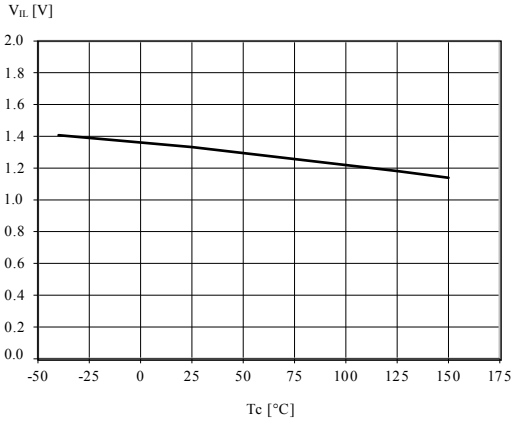


Figure 17. Input high level voltage

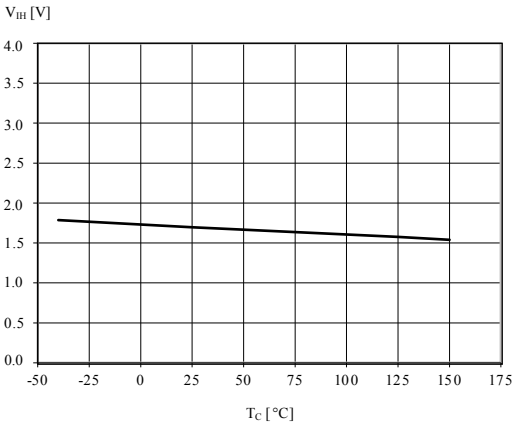


Figure 18. Input hysteresis voltage

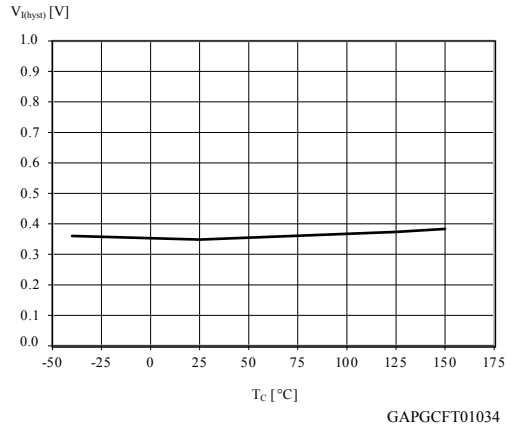
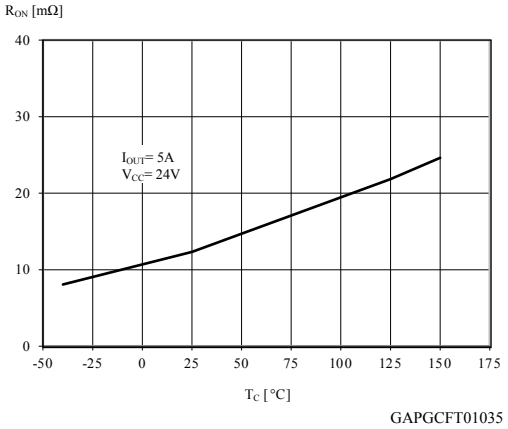
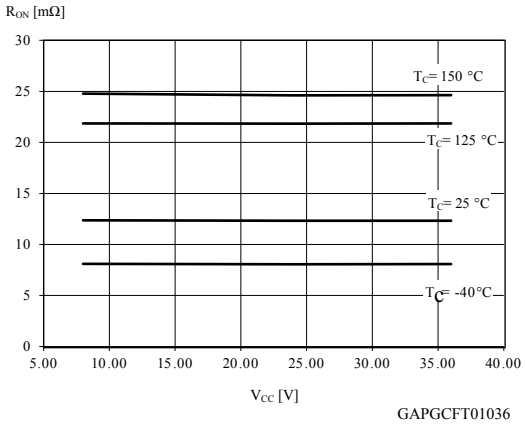


Figure 19. On-state resistance vs T_C



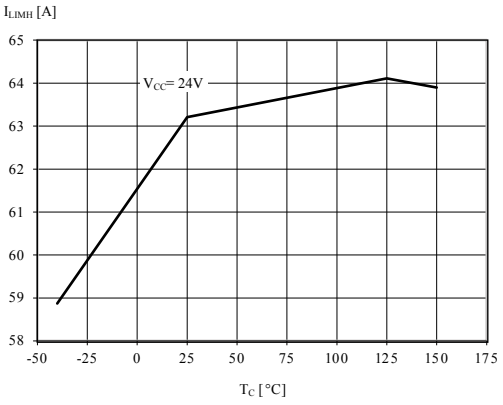
GAPGCFT01035

Figure 20. On-state resistance vs V_{CC}



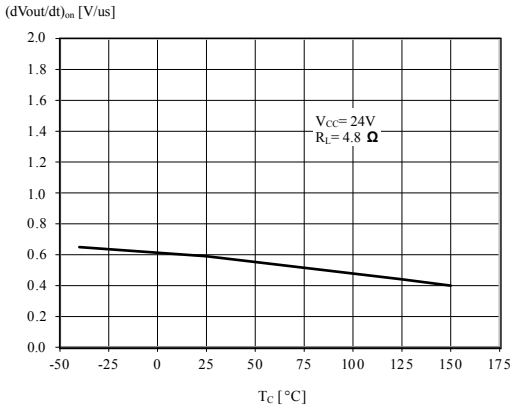
GAPGCFT01036

Figure 21. I_{LIMH} vs T_C



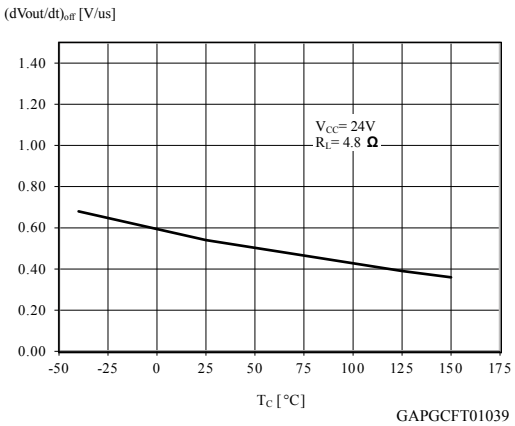
GAPGCFT01037

Figure 22. Turn-on voltage slope



GAPGCFT01038

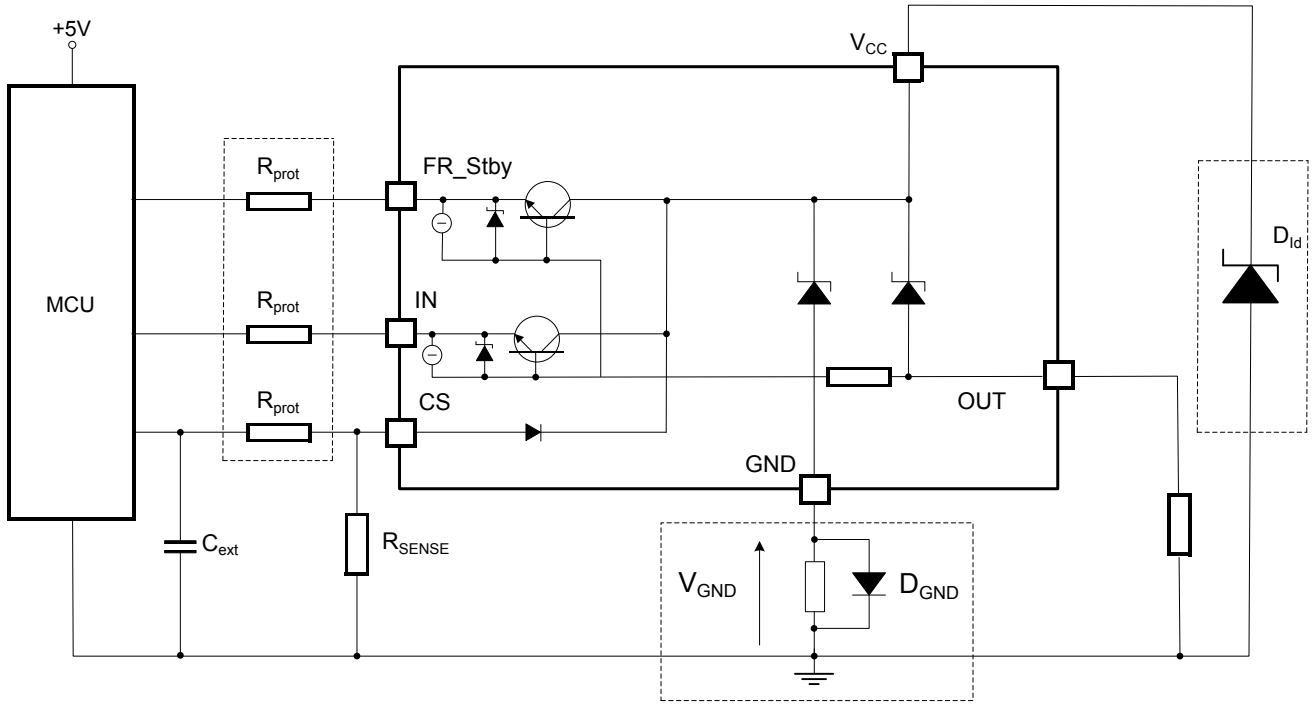
Figure 23. Turn-off voltage slope



GAPGCFT01039

3 Application information

Figure 24. **Application schematic**



GAPGCFT000119

3.1 Load dump protection

D_{Id} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2 2004 (E) in Table 12, Table 13 and Table 14.

3.2 MCU I/Os protection

If a ground protection network is used and negative transient is present on the V_{CC} line, the control pins are pulled negative. ST suggests that a resistor (R_{prot}) has to be inserted in line to prevent the microcontroller I/Os pins from latching-up.

The value of these resistors is a compromise between the leakage current of the microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation: R_{prot} range calculation

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$

Calculation example:

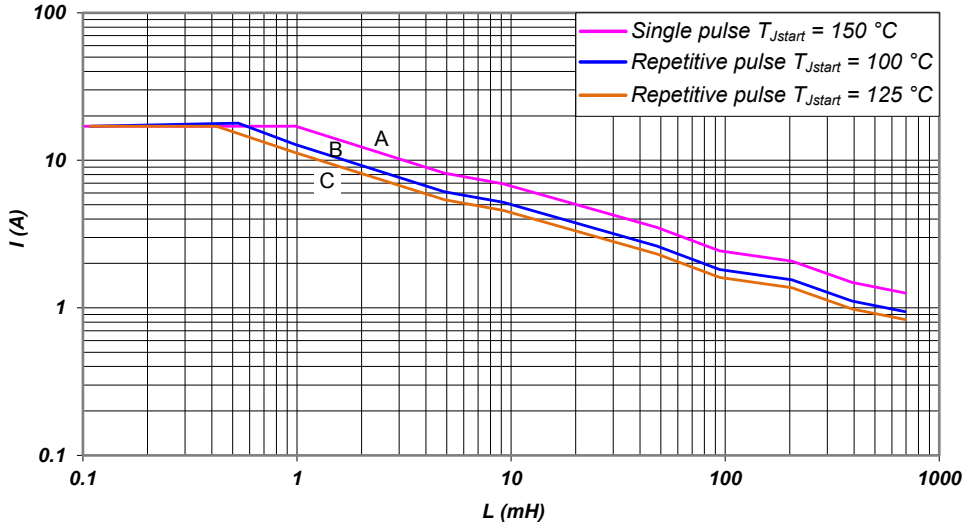
For V_{CCpeak} = -600 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

30 kΩ ≤ R_{prot} ≤ 190 kΩ.

Recommended R_{prot} value is 56 kΩ.

4 Maximum demagnetization energy (V_{CC} = 24 V)

Figure 25. **Maximum turn off current versus inductance**



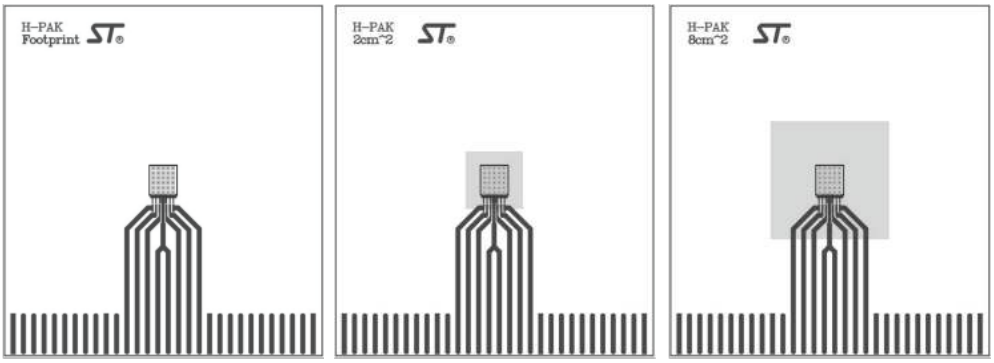
GADG090520221346SA

Note: Values are generated with R_L = 0 Ω. In case of repetitive pulses, T_{Jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

5 Package and PCB thermal data

5.1 HPAK thermal data

Figure 26. **HPAK PCB**



Layout condition of R_{th} and Z_{th} measurements (board finish thickness 1.6 mm +/- 10%, board double layer, board dimension 78x86, board material FR4, Cu thickness 0.070 mm (front and back side), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 6.4 mm x 7 mm).

Figure 27. **R_{thJA} vs PCB copper area in open box free air condition**

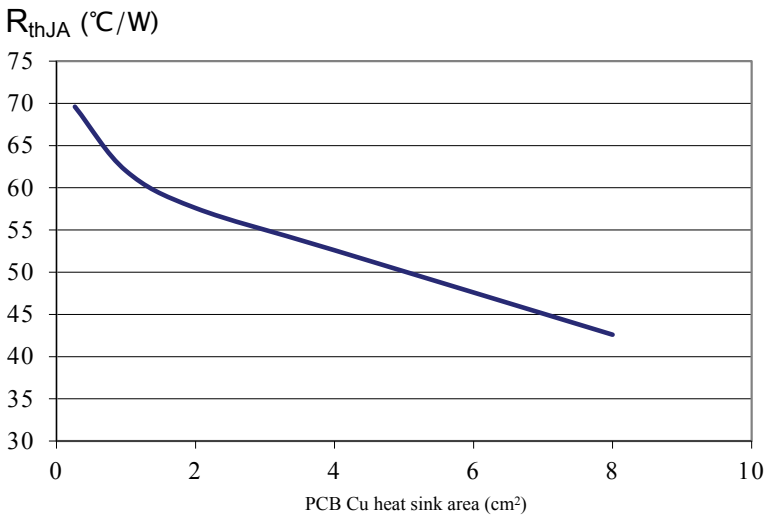


Figure 28. **HPAK thermal impedance junction ambient single pulse**

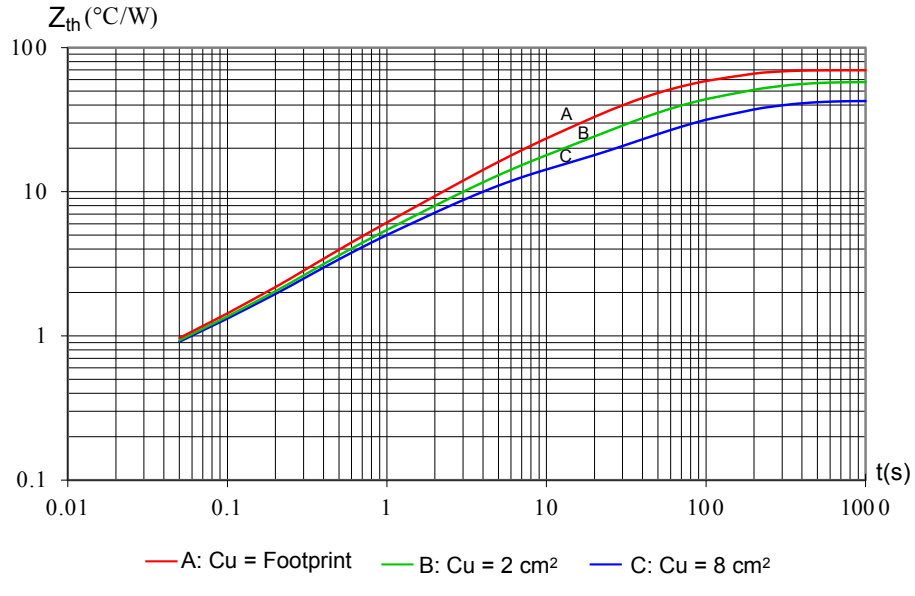
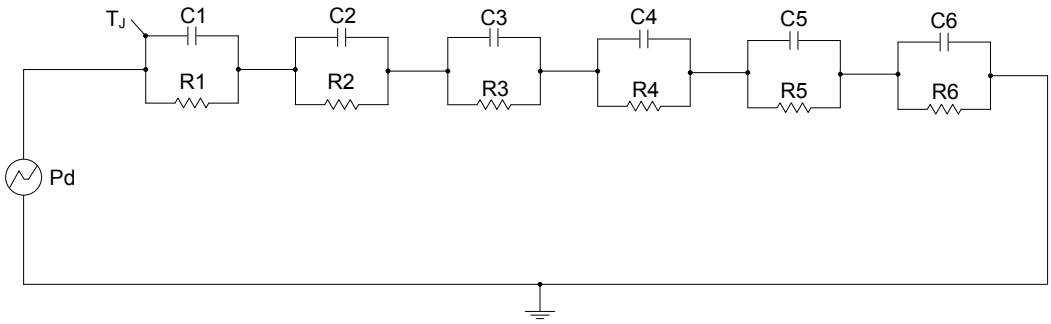


Figure 29. **Thermal fitting model of a single channel HSD in HPAK**



The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation: pulse calculation formula

$Z_{th\delta} = R_{th} \cdot \delta + Z_{thtp} (1 - \delta)$

where $\delta = t_P/T$

Table 15. **Thermal parameters**

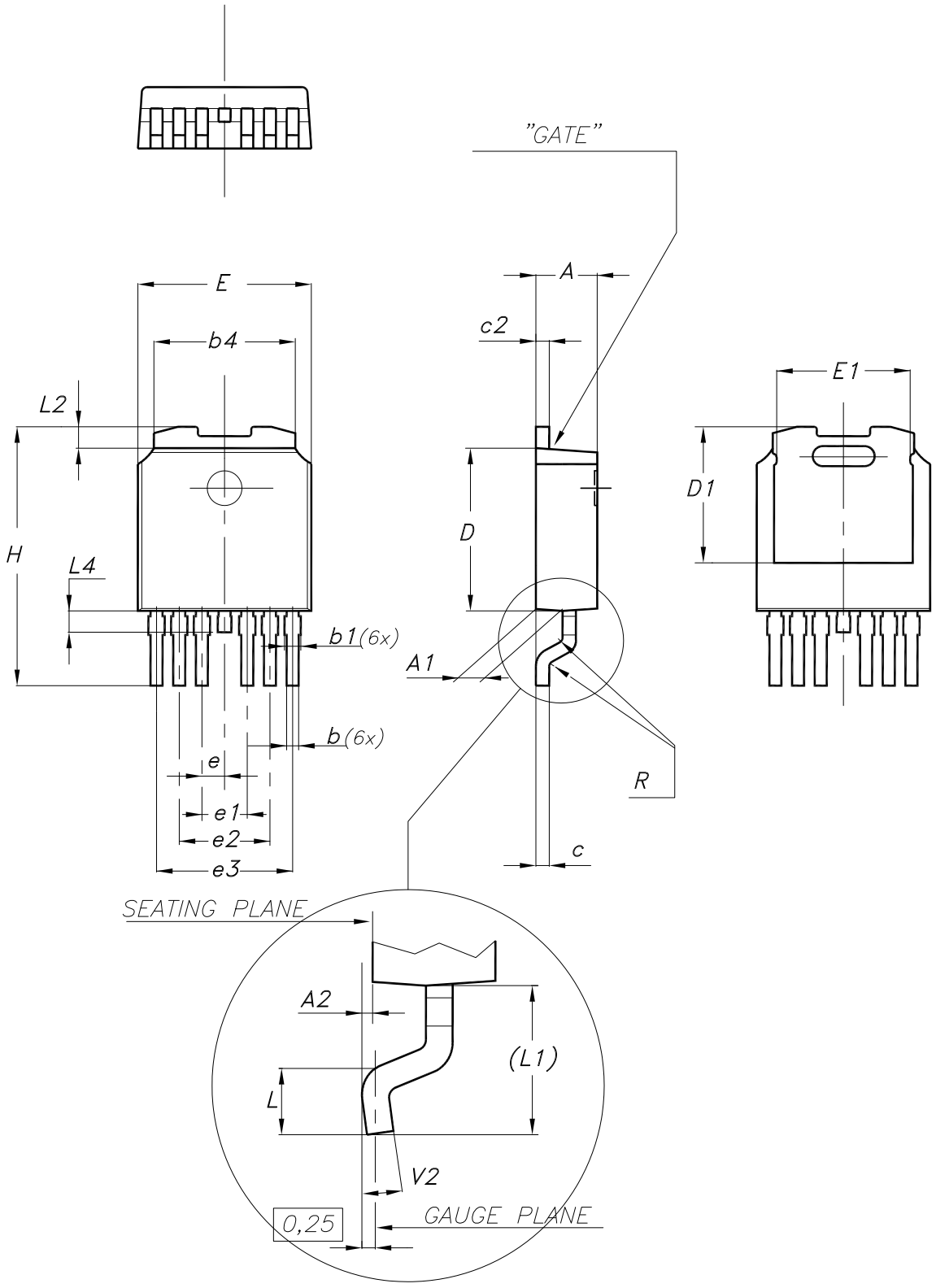
Area/island (cm^2)	Footprint	4	8
R1 (°C/W)	0.1		
R2 (°C/W)	0.5		
R3 (°C/W)	2		
R4 (°C/W)	8		
R5 (°C/W)	28	22	14
R6 (°C/W)	31	25	18
C1 (W.s/°C)	0.01		
C2 (W.s/°C)	0.05		
C3 (W.s/°C)	0.2		
C4 (W.s/°C)	0.4		
C5 (W.s/°C)	0.8	1.4	3
C6 (W.s/°C)	3	6	9

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 HPAK package information

Figure 30. **HPAK package dimensions**



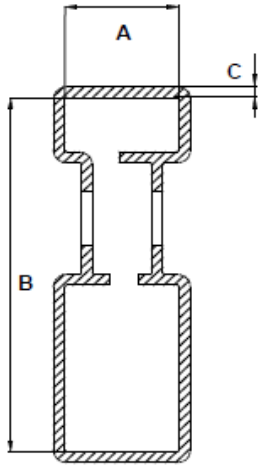
GAPGCFT00134_REV8

Table 16. **HPAK mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.40		0.60
b1	0.45		0.65
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.00	5.20	5.40
e		0.85	
e1	1.60		1.80
e2	3.30		3.50
e3	5.00		5.20
H	9.35		10.10
L	1		1.50
(L1)	2.60	2.80	3.00
L2	0.60	0.80	1.00
L4	0.50		1.00
R		0.20	
V2	0°		8°

6.2 HPAK packing information

Figure 31. **HPAK tube shipment (no suffix)**

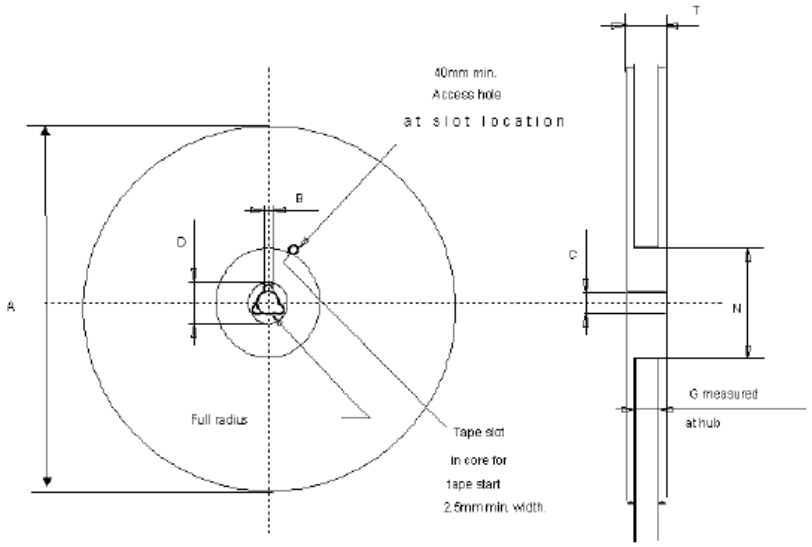


Base q.ty	75
Bulk q.ty	3000
Tube length (± 0.5)	532
A	6
B	21.3
C (± 0.1)	0.6

All dimensions are in mm.

GADG061120191325IG

Figure 32. **HPAK tape and reel (suffix “TR”)**



REEL DIMENSIONS

All dimensions are in mm.

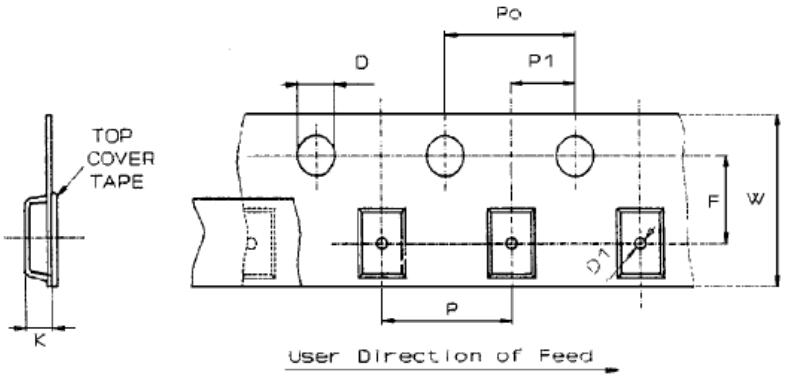
Base q.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

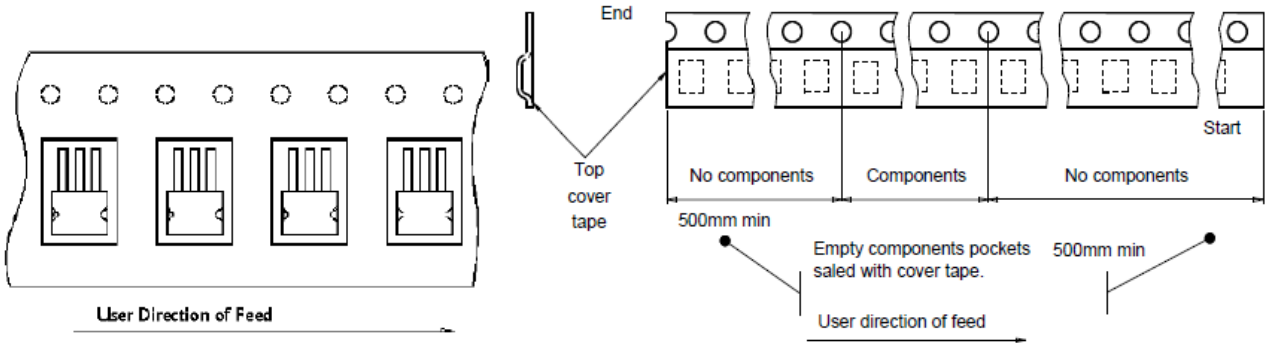
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	16
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	8
Hole diameter	D (± 0.1/-0)	1.5
Hole diameter	D1 (min)	1.5
Hole position	F (± 0.05)	7.5
Compartment depth	K (max)	2.75
Hole spacing	P1 (± 0.1)	2

All dimensions are in mm.





GADG061120191328IG

Revision history

Table 17. **Document revision history**

Date	Revision	Changes
01-Oct-2012	1	First release.
17-Sep-2013	2	Updated disclaimer.
24-Feb-2016	3	Table 4: *Thermal data:* – $R_{thj\text{-}case}$: updated value Updated *Section 5.1: HPAK mechanical data*
16-May-2022	4	Modified Table 5. Power section Updated Figure 24. Application schematic Updated Section 6.1 HPAK package information Minor text changes.

Contents

List of figures

List of tables

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.