HC5509A1R3060

SLIC
Subscriber Line Interface Circuit

June 1997

Features

- **DI Monolithic High Voltage Process**
- **Compatible with Worldwide PBX and CO Performance Requirements**
- **Controlled Supply of Battery Feed Current with Programmable Current Limit**
- **Operates with 5V Positive Supply (V_{B+})**
- **Internal Ring Relay Driver and a Utility Relay Driver**
- **High Impedance Mode for Subscriber Loop**
- **High Temperature Alarm Output**
- **Low Power Consumption During Standby Functions**
- **Switch Hook, Ground Key, and Ring Trip Detection**
- **Selective Power Denial to Subscriber**
- **Voice Path Active During Power Denial**
- **On Chip Op Amp for 2-Wire Impedance Matching**

Applications

- **Solid State Line Interface Circuit for PBX or Central Office Systems, Digital Loop Carrier Systems**
- **Hotel/Motel Switching Systems**
- **Direct Inward Dialing (DID) Trunks**
- **Voice Messaging PBXs**
- **High Voltage 2-Wire/4-Wire, 4-Wire/2-Wire Hybrid**
- **Related Literature**
  - **AN9607, Impedance Matching Design Equations**
  - **AN9628, AC Voltage Gain**
  - **AN9608, Implementing Pulse Metering**
  - **AN549, The HC-5502S/4X Telephone Subscriber Line Interface Circuits (SLIC)**

Description

The HC4P5509A1R3060 telephone Subscriber Line Interface Circuit integrates most of the BORSCHT functions on a monolithic IC. The device is manufactured in a Dielectric Isolation (DI) process and is designed for use as a high voltage interface between the traditional telephone subscriber pair (Tip and Ring) and the low voltage filtering and coding/decoding functions of the line card. Together with a secondary protection diode bridge and “feed” resistors, the device will withstand 1000V lightning induced surges, in plastic packages. The SLIC also maintains specified transmission performance in the presence of externally induced longitudinal currents. The BORSCHT functions that the SLIC provides are:

- Battery Feed with Subscriber Loop Current Limiting
- Overvoltage Protection
- Ring Relay Driver
- Supervisory Signaling Functions
- Hybrid Functions (with External Op Amp)
- Test (or Battery Reversal) Relay Driver

In addition, the SLIC provides selective denial of power to subscriber loops, a programmable subscriber loop current limit from 20mA to 60mA, a thermal shutdown with an alarm output and line fault protection. Switch hook detection, ring trip detection and ground key detection functions are also incorporated in the SLIC device.

The HC4P5509A1R3060 SLIC is ideally suited for line card designs in PBX and CO systems, replacing traditional transformer solutions.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HC4P5509A1R3060	0 to 75	28 Ld PLCC	N28.45

Absolute Maximum Ratings $T_A = 25^oC$

Relay Drivers . . . . . -0.5V to +15V
Maximum Supply Voltages
(V_{B+}) . . . . . -0.5V to +7V
(V_{B+})-(V_{B-}) . . . . . +75V
Junction Temperature Plastic . . . . . 150^oC
Lead Temperature (Soldering 10s) . . . . . 300^oC

Operating Conditions

Operating Temperature Range
HC4P5509A1R3060 . . . . . 0^oC to 75^oC
Storage Temperature Range . . . . . -65^oC to 150^oC
Relay Drivers . . . . . +5V to +12V
Positive Power Supply (V_{B+}) . . . . . +5V ±5%
Negative Power Supply (V_{B-}) . . . . . -42V to -58V
Loop Resistance (R_L) . . . . . 200Ω to 1750Ω (Note 2)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PLCC Package	67

Die Characteristics

Transistor Count 224
Diode Count 28
Die Dimensions . . . . . 174 x 120
Substrate Potential . . . . . Connected
Process . . . . . Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. May be extended to 1900Ω with application circuit.

Electrical Specifications

Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are over Operating Temperature Range, $V_{B-} = -48V$, $V_{B+} = +5V$, AG = BG = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC TRANSMISSION PARAMETERS					
RX Input Impedance	300Hz to 3.4kHz (Note 3)	-	100	-	kΩ
TX Output Impedance	300Hz to 3.4kHz (Note 3)	-	-	20	Ω
4-Wire Input Overload Level	300Hz to 3.4kHz R_L = 1200Ω, 600Ω Reference	+1.5	-	-	V_{PEAK}
2-Wire Return Loss	Matched for 600Ω (Note 3)				
SRL LO		26	35	-	dB
ERL		30	40	-	dB
SRL HI		30	40	-	dB
2-Wire Longitudinal to Metallic Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 3) 300Hz to 3400Hz	58	63	-	dB
4-Wire Longitudinal Balance Off Hook	300Hz to 3400Hz (Note 3)	50	55	-	dB
Low Frequency Longitudinal Balance	R.E.A. Test Circuit	-	-	-67	dBmp
	I_{LINE} = 40mA $T_A = 25^oC$ (Note 3)	-	-	23	dBrnC
Longitudinal Current Capability	I_{LINE} = 40mA $T_A = 25^oC$ (Note 3)	-	-	30	mA_{RMS}
Insertion Loss	0dBm at 1kHz, Referenced 600Ω				
2-Wire/4-Wire		-6.22	-6.02	-5.82	dB
4-Wire/2-Wire		-	±0.05	±0.2	dB
4-Wire/4-Wire		-6.22	-6.02	-5.82	dB

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Response	300Hz to 3400Hz (Note 3) Referenced to Absolute Level at 1kHz, 0dBm Referenced 600Ω	-	±0.02	±0.05	dB
Level Linearity	Referenced to -10dBm (Note 3)				
2-Wire to 4-Wire and 4-Wire to 2-Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
Absolute Delay	(Note 3)				
2-Wire/4-Wire	f_{IN} - 1kHz	-	0.7	1.2	µs
4-Wire/2-Wire	f_{IN} - 1kHz	-	0.3	1.0	µs
4-Wire/4-Wire	f_{IN} - 1kHz	-	1.5	2.0	µs
Transhybrid Loss	$V_{IN} = 1V_{P-P}$ at 1kHz (Note 3)	32	40	-	dB
Total Harmonic Distortion 2-Wire/4-Wire, 4-Wire/2-Wire, 4-Wire/4-Wire	Reference Level 0dBm at 600Ω 300Hz to 3400Hz (Note 3)	-	-	-52	dB
Idle Channel Noise					
2-Wire and 4-Wire	C-Message (Note 3)	-	-	5	dBrnC
	Psophometric	-	-	-85	dBmp
	3kHz Flat	-	-	15	dBrn
Power Supply Rejection Ratio	(Note 3) 30Hz to 200Hz, R_L = 600Ω				
V_{B+} to 2-Wire		25	29	-	dB
V_{B+} to 4-Wire		25	29	-	dB
V_{B-} to 2-Wire		25	29	-	dB
V_{B-} to 4-Wire		25	29	-	dB
V_{B+} to 4-Wire	(Note 3) 200Hz to 16kHz, R_L = 600Ω	25	-	-	dB
V_{B+} to 2-Wire		25	-	-	dB
V_{B-} to 4-Wire		25	25	-	dB
V_{B-} to 2-Wire		25	25	-	dB
Ring Sync Pulse Width		50	-	500	µs
DC PARAMETERS					
Loop Current Programming					
Limit Range	(Note 4)	20 (Note 4)	-	60	mA
Accuracy		10	-	-	%
Loop Current During Power Denial	R_L = 200Ω	-	±3	±5	mA

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Fault Currents					
TIP to Ground		-	38	45	mA
RING to Ground		-	54	60	mA
TIP and RING to Ground		-	85	95	mA
Switch Hook Detection Threshold		-	12	15	mA
Ground Key Detection Threshold		9.5	13.5	17.5	mA
Thermal $\overline{ALARM}$ Output	Safe Operating Die Temperature Exceeded	140	-	160	^oC
Ring Trip Comparator Threshold	See Typical Applications for more information	9.5	13.5	17.5	mA
Dial Pulse Distortion		-	0.1	0.5	ms
Relay Driver Outputs					
On Voltage V_{OL}	I_{OL} ($\overline{PR}$) = 60mA, I_{OL} ($\overline{RD}$) = 60mA	-	0.2	0.5	V
Off Leakage Current	V_{OH} = 13.2V	-	±10	±100	µA
TTL/CMOS Logic Inputs ($\overline{RC}$, $\overline{PD}$, RS, $\overline{TST}$, PRI)					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Input Current ($\overline{RC}$, $\overline{PD}$, RS, $\overline{TST}$, PRI)	$0V \le V_{IN} \le 5V$	-	-	±100	µA
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} = 800µA	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} = 40µA	2.7	-	-	V
Power Dissipation On Hook	Relay Drivers Off	-	200	-	mW
I_{B+}	V_{B+} = +5.25V, V_{B-} = -58V, $R_{LOOP} = \infty$	-	-	6	mA
I_{B-}	V_{B+} = +5.25V, V_{B-} = -58V, $R_{LOOP} = \infty$	-6	-	-	mA
UNCOMMITTED OP AMP PARAMETERS					
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Differential Input Resistance	(Note 2)	-	1	-	MΩ
Output Voltage Swing	R_L = 10kΩ	-	±3	-	V_{P-P}
Small Signal GBW		-	1	-	MHz

NOTES:

3. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
4. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.
5. Application limitation based on maximum switch hook detect limit and metallic currents. Not a part limitation.

Pin Descriptions

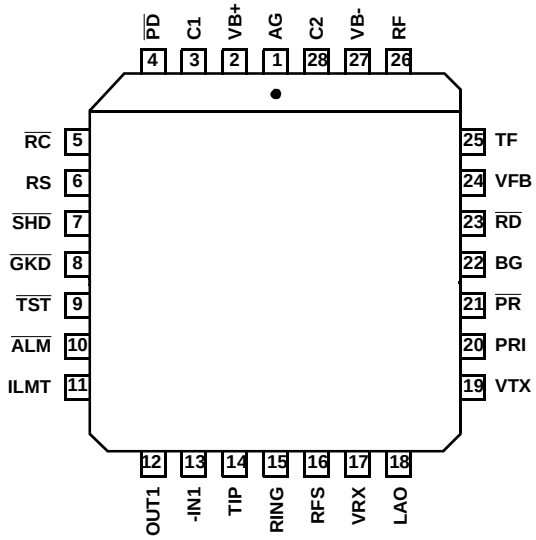
SOIC	SYMBOL	DESCRIPTION
1	AG	Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.
2	VB+	Positive Voltage Source - Most Positive Supply.
3	C1	Capacitor #C1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function.
4	$\overline{PD}$	Power Denial - A low active TTL-compatible logic input. When enabled, the output of the ring amplifier will ramp to close to the output voltage of the tip amplifier.
5	$\overline{RC}$	Ring Command - A low active TTL-compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power down mode ($\overline{TST}$ = 0) or the subscriber is not already off-hook ($\overline{SHD}$ = 0).
6	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50 - 500µs) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5.
7	$\overline{SHD}$	Switch Hook Detection - An active low LS TTL compatible logic output. A line supervisory output.
8	$\overline{GKD}$	Ground Key Detection - An active low LS TTL compatible logic output. A line supervisory output.
9	$\overline{TST}$	A TTL logic input. A low on this pin will keep the SLIC in a power down mode. The TST pin in conjunction with the ALM pin can provide thermal shutdown protection for the SLIC. Thermal shutdown is implemented by a system controller that monitors the ALM pin. When the ALM pin is active (low) the system controller issues a command to the Test pin (low) to power down the SLIC. The timing of the thermal recovery is controlled by the system controller.
10	$\overline{ALM}$	A TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded. Reference the TST pin description for a method to reduce prolonged thermal overstress that may reduce component life.
11	ILMT	Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.
12	OUT1	The analog output of the spare operational amplifier.
13	-IN1	The inverting analog input of the spare operational amplifier.
14	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purpose.
15	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.
16	RFS	Ring Feed Sense - Senses RING side of the loop for Ground Key Detection. During Ring injected ringing the ring signal at this node is isolated from RF via the ring relay. For Tip injected ringing, the RF and RFS pins must be shorted.
17	VRX	Receive Input, 4-Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers differentially.
18	LAO	Longitudinal Amplifier Output - A low impedance output to be connected to C2 through a low pass filter. Output is proportional to the difference in I_{TIP} and I_{RING}.

Pin Descriptions (Continued)

SOIC	SYMBOL	DESCRIPTION
19	VTX	Transmit Output, 4-Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. This output is referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is necessary.
20	PRI	A TTL compatible input used to control $\overline{PR}$. PRI active High = $\overline{PR}$ active low.
21	$\overline{PR}$	An active low open collector output. Can be used to drive a Polarity Reversal Relay.
22	BG	Battery Ground - Tube connected to zero potential. All loop current and some quiescent current flows into this terminal.
23	$\overline{RD}$	Ring Relay Driver - An active low open collector output. Used to drive a relay that switches ringing signals onto the 2-Wire line.
24	VFB	Feedback input to the tip feed amplifier; may be used in conjunction with transmit output signal and the spare op amp to accommodate 2-Wire line impedance matching.
25	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a feed resistor. Functions with the RF terminal to provide loop current, and to feed voice signals to the telephone set and to sink longitudinal currents.
26	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and to sink longitudinal currents.
27	VB-	The battery voltage source. The most negative supply.
28	C2	Capacitor #2 - An external capacitor to be connected between this terminal and ground. It prevents false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from power lines and other noise sources. This capacitor should be nonpolarized.

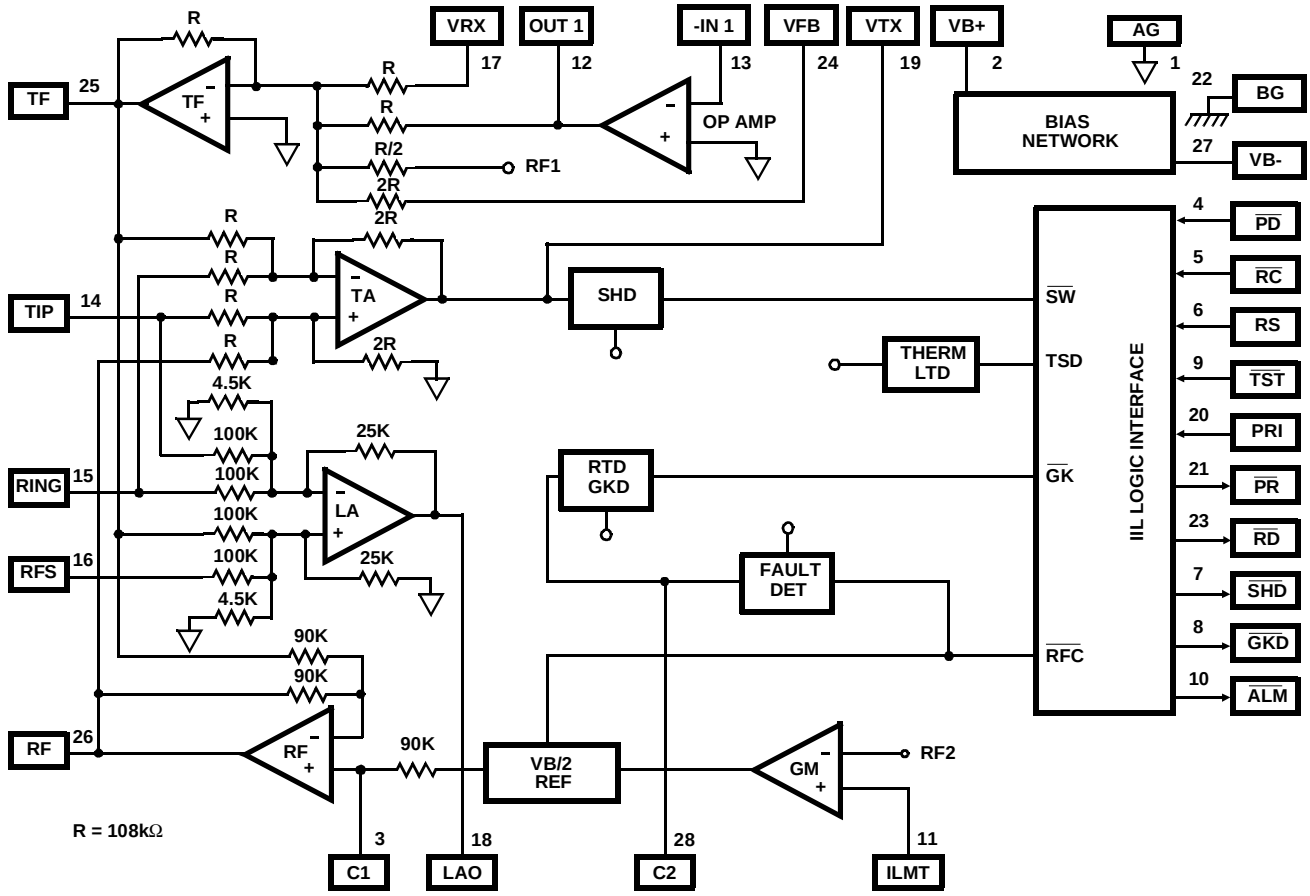
Pinout

HC4P5509A1R3060 (PLCC)
TOP VIEW



Functional Diagram

PLCC



Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

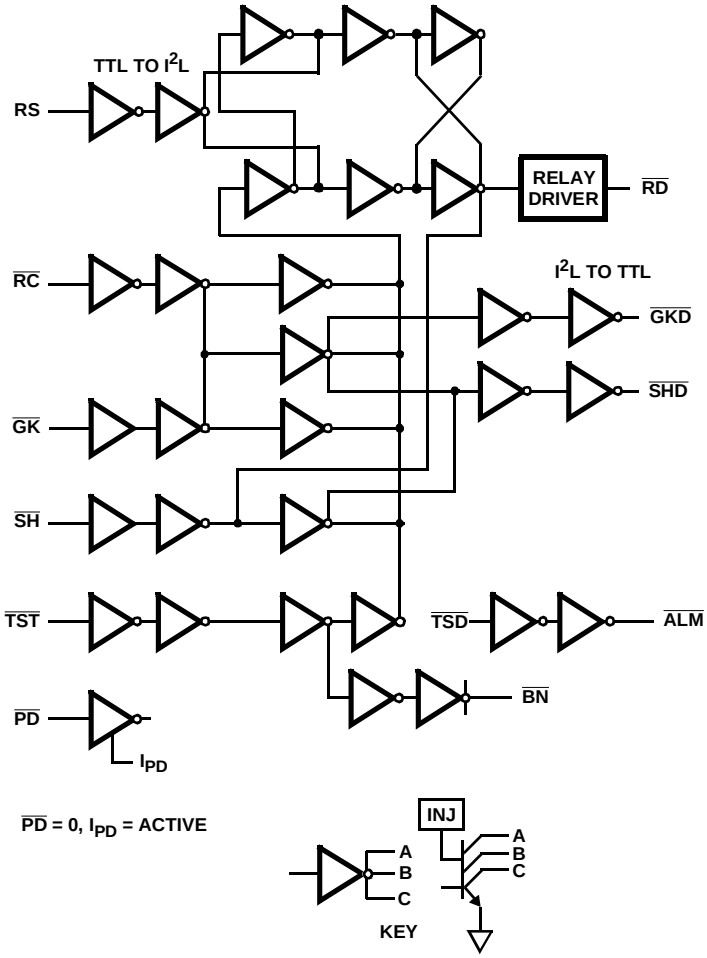
High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or $30mA_{RMS}$, $15mA_{RMS}$ per leg, without any performance degradation.

TABLE 1.

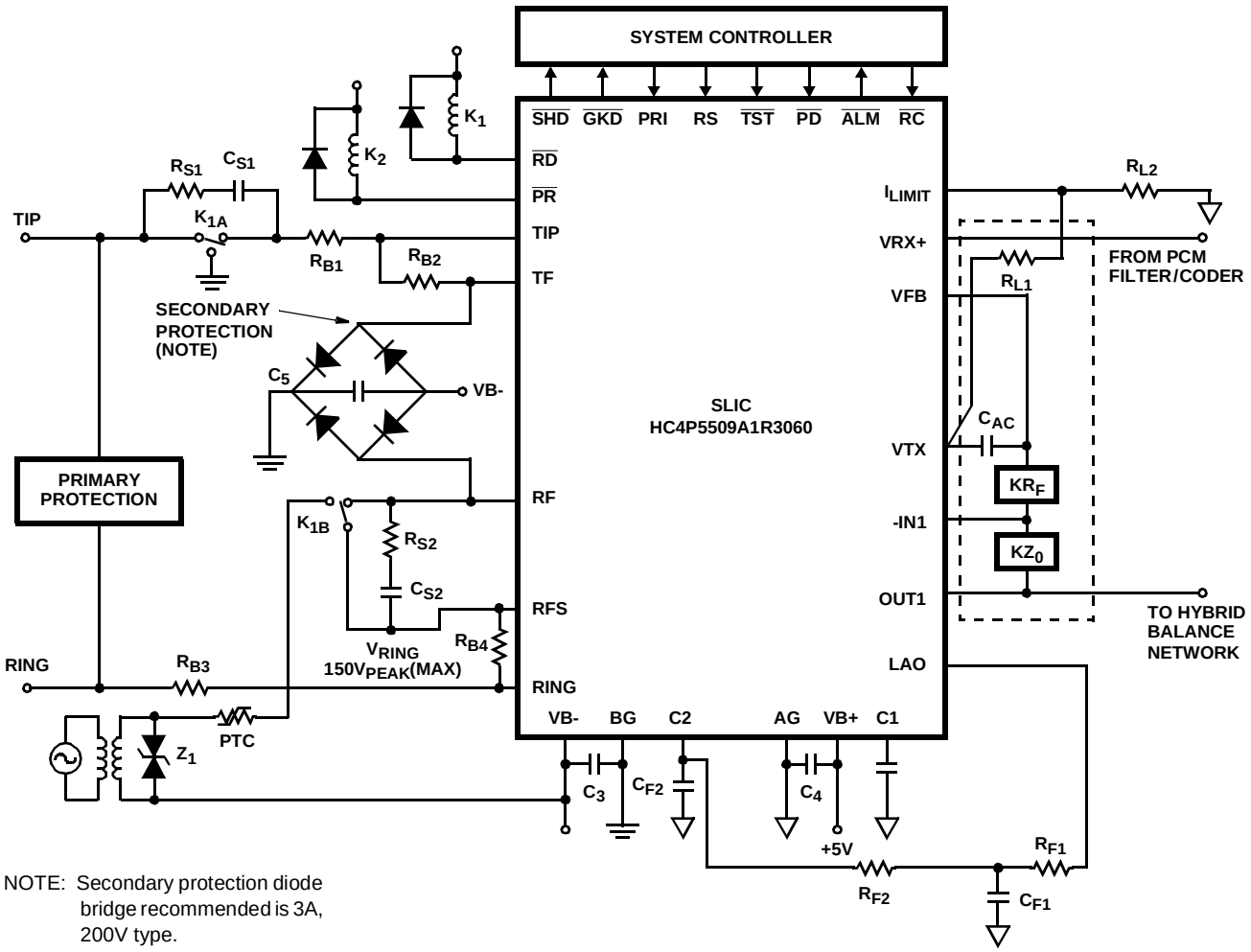
PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
50/60Hz Current T/GND R/GND	11 Cycles Limited to $10A_{RMS}$	700 (Plastic)	V_{RMS}

Logic Diagram



NOTE: PRI and $\overline{PD}$ are independent switch driven by TTL input levels.

Applications Diagram



NOTE: Secondary protection diode bridge recommended is 3A, 200V type.

FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

TYPICAL COMPONENT VALUES

C_1 = 0.5µF, 30V

$R_{F1} = R_{F2}$ = 210kΩ, 1%

$C_{F1} = C_{F2}$ = 0.22µF, 10%, 20V Nonpolarized

C_3 = 0.01µF, 100V, ±20%

C_4 = 0.01µF, 100V, ±20%

C_5 = 0.01µF, 100V, ±20%

C_{AC} = 0.5µF, 20V

KZ_0 = 30kΩ, (Z_0 = 600Ω)

R_{L1}, R_{L2}; Current Limit Setting Resistors:

$I_{LIMIT} = (0.6)(R_{L1} + R_{L2})/(200 \times R_{L2})$, R_{L1} typically 100kΩ

KR_F = 20kΩ

$R_{B1} = R_{B2} = R_{B3} = R_{B4}$ = 50Ω 0.1% absolute matching

$R_{S1} = R_{S2}$ = 1kΩ typically

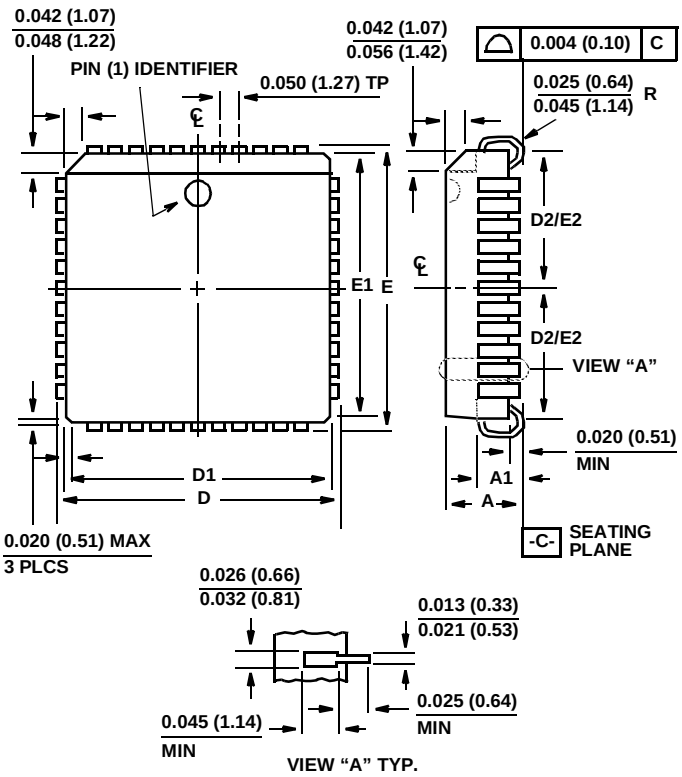
$C_{S1} = C_{S2}$ = 0.1µF, 200V typically, depending on V_{Ring} and line length.

Z_1 = 150V to 200V transient protector. PTC used as ring generator ballast.

NOTES:

1. All grounds (AG, BG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
2. Application shows Ring Injected Ringing, a Balanced or Tip injected configuration may be used.

Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

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