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November 2013

# FDPF13N50FT

# N-Channel UniFET<sup>TM</sup> FRFET<sup>®</sup> MOSFET 500 V, 12 A, 540 m $\Omega$

#### **Features**

- $R_{DS(on)}$  = 420  $m\Omega$  (Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 6 A
- Low Gate Charge (Typ. 30 nC)
- Low C<sub>rss</sub> (Typ. 14.5 pF)
- · 100% Avalanche Tested
- · Improved dv/dt Capability
- · RoHS Compliant

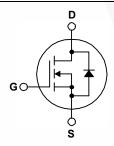
# **Applications**

- LCD/LED/PDP TV
- · Lighting
- · Uninterruptible Power Supply

# **Description**

UniFET<sup>TM</sup> MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its trr is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





# **MOSFET Maximum Ratings** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol		Parameter		FDPF13N50FT	Unit
V <sub>DSS</sub>	Drain to Source Voltage			500	V
V <sub>GSS</sub>	Gate to Source Voltage			±30	V
,	Drain Current	- Continuous (T <sub>C</sub> = 25°C)		12*	Α
ID	Diam Current	- Continuous (T <sub>C</sub> = 100°C)		7.2*	A
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	48*	Α
E <sub>AS</sub>	Single Pulsed Avalanche	e Energy	(Note 2)	684	mJ
I <sub>AR</sub>	Avalanche Current		(Note 1)	12	Α
E <sub>AR</sub>	Repetitive Avalanche En	ergy	(Note 1)	19.5	mJ
dv/dt	Peak Diode Recovery dv	/dt	(Note 3)	20	V/ns
D	Dower Dissination	(T <sub>C</sub> = 25°C)		42	W
$P_{D}$	Power Dissipation	- Derate Above 25°C		0.33	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage T	emperature Range		-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300	°C

<sup>\*</sup>Drain current limited by maximum junction temperature.

### **Thermal Characteristics**

Symbol	Parameter	FDPF13N50FT	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	-0/00

# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDPF13N50FT	FDPF13N50FT	TO-220F	Tube	N/A	N/A	50 units

# **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 25^{\circ} C$	500	-	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C	-	0.7	-	V/°C
1	Zero Gate Voltage Drain Current	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	10	μА
IDSS	Zero Gate Voltage Drain Guirent	$V_{DS} = 400 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	100	μΑ
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 6 \text{ A}$	-	0.42	0.54	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 6 A	-	13.3	-	S

# **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 05.V.V 0.V		-	1450	1930	pF
Coss	Output Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz		-	198	265	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 = 1 WH12		-\	14.5	22	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 13 A,		- \	30	39	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>GS</sub> = 10 V		- \	8	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	(1)	Note 4)	-	12	-	nC

# **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		-	28	65	ns
t <sub>r</sub>		$V_{DD} = 250 \text{ V}, I_D = 13 \text{ A},$	-	54	120	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_G$ = 25 $\Omega$	-	75	160	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	-	47	105	ns

# **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	12	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	48	Α
$V_{SD}$	Drain to Source Diode Forward Voltage V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 12 A		-	-	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 12 A,	-	154	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	0.45	-	μС

#### Notes

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. L = 9.5 mH, I<sub>AS</sub> = 12 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25  $\Omega$ , starting T<sub>J</sub> = 25°C.
- 3.  $I_{SD} \le 12$  A, di/dt  $\le 200$  A/ $\mu$ s,  $V_{DD} \le BV_{DSS}$ , starting  $T_J = 25^{\circ}C$ .
- 4. Essentially independent of operating temperature typical characteristics.

# **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

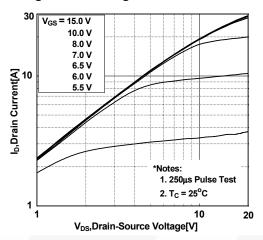


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

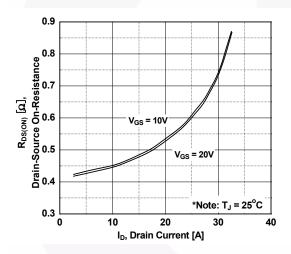


Figure 5. Capacitance Characteristics

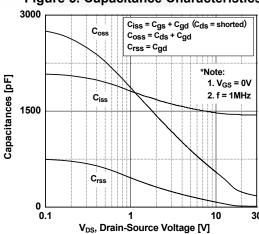


Figure 2. Transfer Characteristics

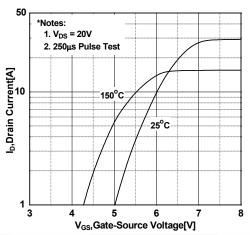


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

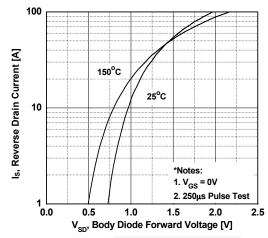
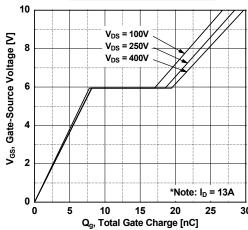


Figure 6. Gate Charge Characteristics



# **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

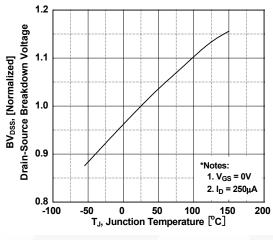


Figure 8. Maximum Safe Operating Area

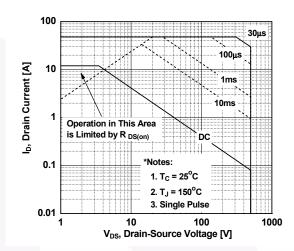


Figure 9. Maximum Drain Current vs. Case Temperature

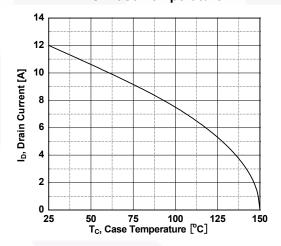
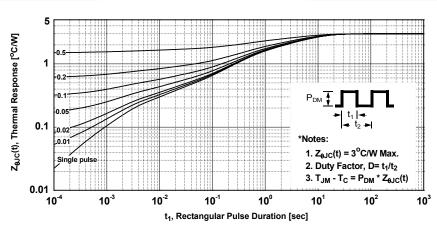


Figure 10. Transient Thermal Response Curve



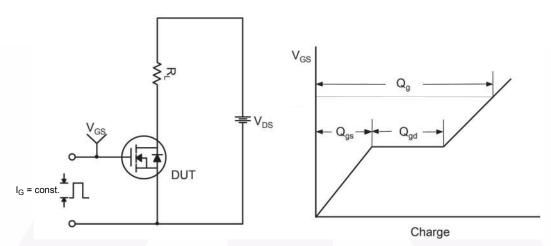


Figure 11. Gate Charge Test Circuit & Waveform

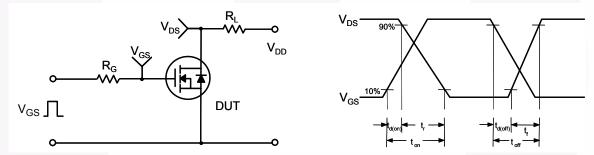


Figure 12. Resistive Switching Test Circuit & Waveforms

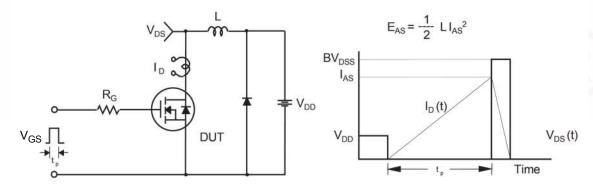


Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms

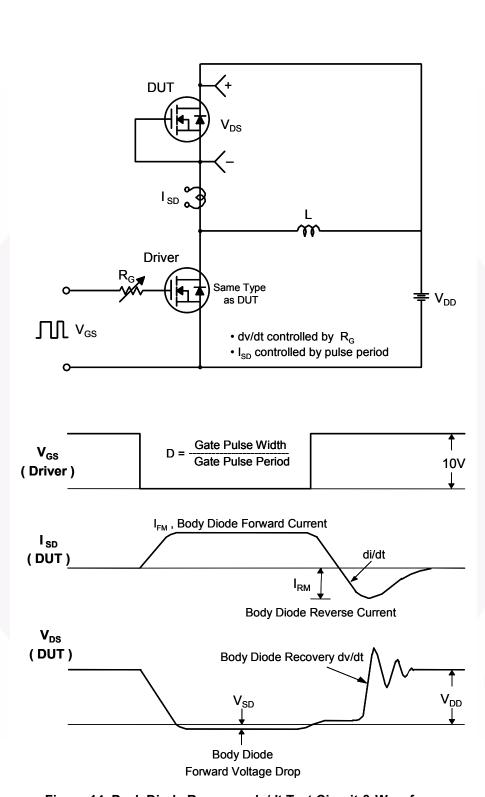


Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms

# **Mechanical Dimensions**

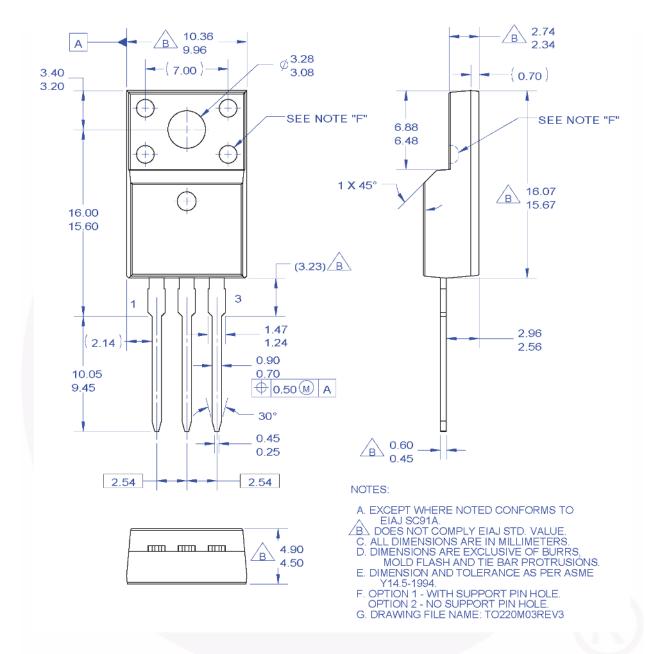


Figure 15. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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