TEXAS INSTRUMENTS

THS3112/22 EVM

User's Guide

May 2002 HPL

SLOU125

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This manual provides information about the evaluation module of the current feedback amplifier under test. Additionally, this document provides a good example of PCB design for high-speed applications. The user should keep in mind the following points.

- The design of the high-speed amplifier PCB is a delicate process.
- The user must approach the PCB design with care and awareness.
- It is recommended that the user initially review the data sheet of the device under test.
- It is also helpful to review the schematic and layout of the THS3112/22 EVM to determine the design techniques used in the evaluation board.
- It is recommended that the user review the application notes *Current Feedback Amplifier Analysis and Compensation,* (literature number SLOA021A) and *Voltage Feedback vs Current Feedback Op Amps*, (literature number SLVA051) to gain more insight about current feedback amplifiers.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction and Description
- Chapter 2—Using the THS3112/22 EVM
- Chapter 3—Circuit Design Examples
- Chapter 4—General High-Speed Amplifier Design Considerations
- Chapter 5—EVM Hardware Description

Information About Cautions and Warnings

This book may contain cautions and warnings.

> This is an example of a caution statement.
>
> A caution statement describes a situation that could potentially damage your software or equipment.
>
> CAUTION

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

WARNING

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The URL's below are correct as of the data of publication of this manual. Texas Instruments applications apologizes if they change over time.

- THS3112/22 data sheet (literature number SLOS385)
- Application report (literature number SLOA021A), *Current Feedback Amplifier Analysis and Compensation*, http://www-s.ti.com/sc/psheets/sloa021a/sloa021a.pdf
- Application report (literature number SLVA051), *Voltage Feedback Vs Current Feedback Op Amps,* http://www-s.ti.com/sc/psheets/slva051/slva051.pdf
- Application report (literature number SLOA069), *How (Not) to Decouple High Speed Op Amp Circuits,* http://www-s.ti.com/sc/psheets/sloa069/sloa069.pdf
- Application report (literature number SLOA072), *Single Supply Differential Op Amp Techniques,* http://www-s.ti.com/sc/psheets/sloa072/sloa072.pdf

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Chapter 1

Introduction and Description

The Texas Instruments THS3112/22 evaluation module (EVM) helps designers evaluate the performance of the THS3112/22 current feedback operational amplifier (CFA). This EVM is also a good example of high-speed PCB design.

This document details the THS3112/22 EVM. It includes a list of EVM features, a brief description of the module illustrated with a series of schematic diagrams, EVM specifications, details on connecting and using the EVM, and a discussion of high-speed amplifier design considerations.

This EVM enables the user to implement various circuits to clarify the available configurations presented in the schematic of the EVM. In addition, when the customer receives the EVM, the schematic of the default circuit has been added to depict the components mounted on the EVM.

Other sample circuits are presented for user implementation. The user is not limited to the circuit configurations presented in this user's guide. The EVM provides enough hardware hooks that the only limitation is the creativity of the user.

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1.1 Description

The THS3112/22 EVM provides a platform for developing high-speed CFA application circuits. It contains the THS3112/22 high-speed CFA, a number of passive components, and various features and footprints that enable the user to experiment, test, and verify various operational amplifier circuit implementations. The PC board measures 2.99 by 3.08 inches.

1.2 Evaluation Module Features

THS3112/22 high-speed operational amplifier EVM features include:

- Wide operating supply voltage range: dual supply ±5 to ±15 Vdc operation (see the device data sheet).
- Unity gain inverting stage (channel 1 of the IC). The user can reconfigure gain as required.
- Noninverting stage with a gain of 2 (channel 2 of the IC). The user can reconfigure gain as required.
- Nominal 50-Ω input termination resistors (R2 and R8). Termination can be configured according to the application requirement.
- Nominal 50-Ω, 1 watt output matching resistors (R5B and R11B). Footprints are provided for lower power resistors (R5A and R11A).
- 100-Ω, 1 watt output load resistors (R6B and R12B). Footprints are provided for lower power resistors (R6A and R12A).
- Power supply ripple rejection capacitors (C1 and C2)
- Decoupling capacitors (C3, C4) populated with 0.1-μF capacitors. Design final decoupling in accordance with SLOA069
- A good example of high-speed amplifier PCB design and layout

1.3 THS3112/22 EVM Operating Conditions

- Supply voltage range, ± VS ±5 V to ±15 V (see the device data sheet)
- Supply current, IS (see the device data sheet)
- Output drive, I_O, at VS = ±15 (see the device data sheet)

For complete THS3112/22 amplifier IC specifications, parameter measurement information, and additional application information, see the THS3112/22 data sheet, TI literature number SLOS385.

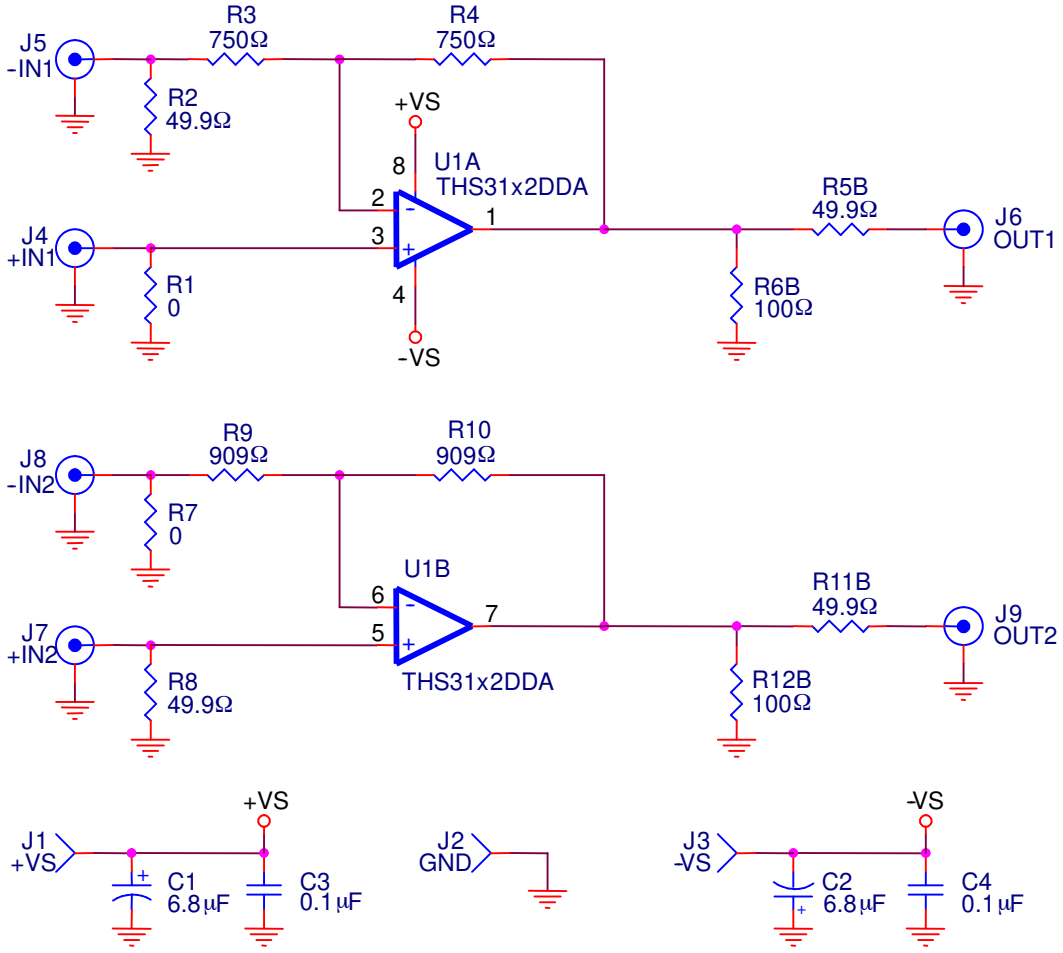
1.4 EVM Default Configuration

As delivered, the EVM has a fully functional example circuit, just add power supplies, a signal source, and monitoring instrument. See Figure 1–1 for the default schematic diagram. The user can change the gain by changing the ratios of the feedback and gain resistors (see the device data sheet for recommended resistor values). The complete EVM schematic—showing all component locations—is shown in Chapter 5.

The default configuration assumes a 50-Ω signal source, and contains a termination resistor R2 or R8 (49.9 Ω) for the source.

Some components such as C1, C2, C3, C4, J1, J2, and J3 are omitted on the application schematics of chapter 4 for clarity. In addition, only the components associated with the section of the IC being used (A or B) are shown.

Figure 1-1. Schematic of the Populated Circuit on the EVM (Default Configuration)



Chapter 2

Using the THS3112/22 EVM

It is recommended that the user perform the following exercises to learn the function of the EVM. This practice helps the user learn about the various terminals on the EVM and their function. In addition, it lists the components and equipment needed to operate the EVM.

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2.1 Required Equipment

- One double-output dc power supply (±15 V, 1-A output minimum)
- Two dc current meters with resolution to 1 mA and capable of the maximum current from the dc power supply. If available, set the current limit on the dc power supply to 100 mA.

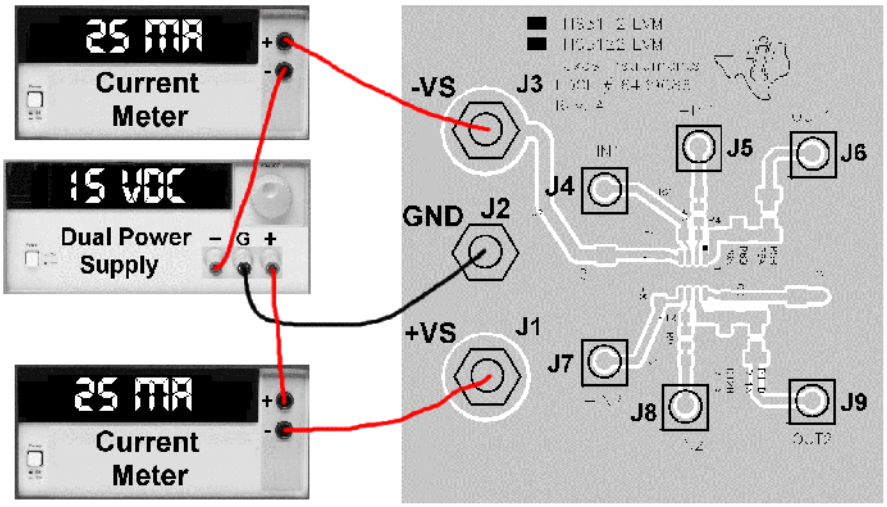
NOTE: Some power supplies incorporate current meters which may be applicable to this test.

- 50-Ω source impedance function generator (1-MHz, 10-V_{PP} sine wave)
- Oscilloscope (50-MHz bandwidth minimum, 50-Ω input impedance).

2.2 Power Supply Setup for ±15 Vdc

1) Set the dc power supply to ±15 V.
2) Make sure the dc power supply is turned off before proceeding to the next step.
3) Connect the positive (+) terminal of the power supply to the positive (+) terminal of the current meter number 1.
4) Connect the negative (–) terminal of the current meter number 1 to the +VS terminal of the EVM (J1).
5) Connect the common ground terminal of the power supply to the ground (GND) terminal on the EVM (J2).
6) Connect the negative (–) terminal of the power supply to the negative (–) terminal of the second current meter.
7) Connect the positive (+) terminal of the current meter number 2 to the –VS of the EVM (J3).

Figure 2–1. Power Supply Connection for ±15 Vdc



2.3 Input and Output Setup for Channel 1

1) Set the function generator to generate a 1-MHz, ±0.5 V (1-V_{PP}) sine wave with no dc offset.

2) Turn off the function generator before proceeding to the next step.

3) Connect a BNC *T* connector to the output of the function generator.

4) Using a BNC-to-SMA cable, connect the function generator to J5 (–IN1) on the EVM.

5) Using a BNC-to-BNC cable, connect the function generator output to the oscilloscope input 1.

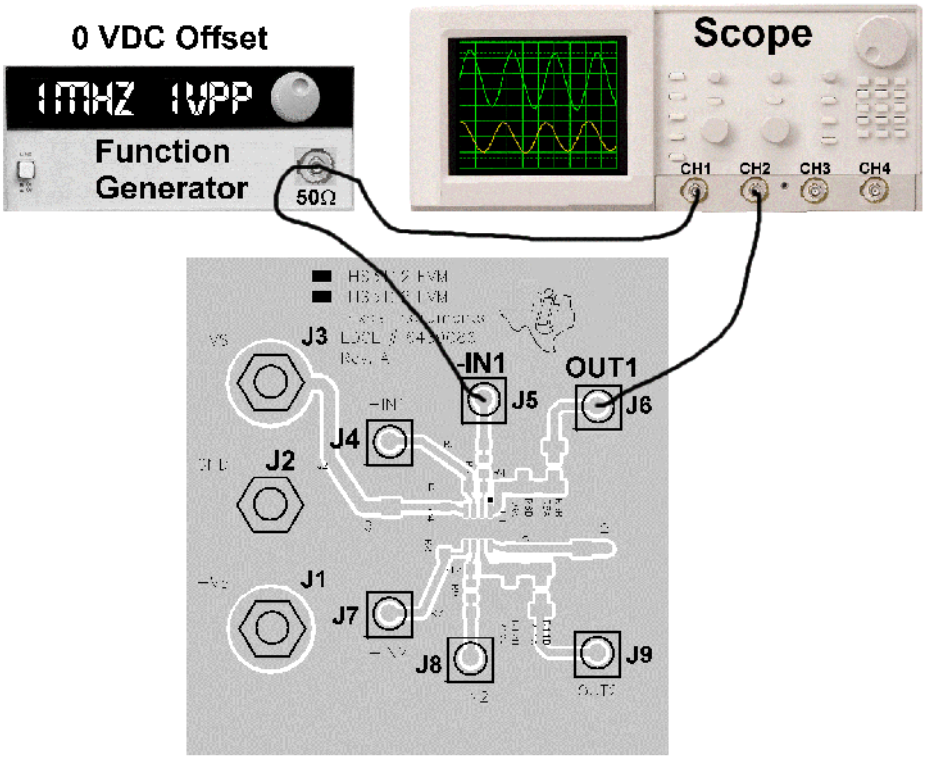
NOTE: The oscilloscope input 1 must be set to use 1-MΩ input impedance for proper results.

6) Using a BNC-to-SMA cable, connect the oscilloscope to J6 (OUT1) on the EVM.

7) Set the oscilloscope to 200 mV/division and a time-base of 0.1 μs/division.

NOTE: The oscilloscope input 2 must be set to use 50-Ω input impedance for proper results.

Figure 2–2. Signal Connections for Channel 1



2.4 Operating the EVM on Channel 1

1) Turn on the dc power supply.

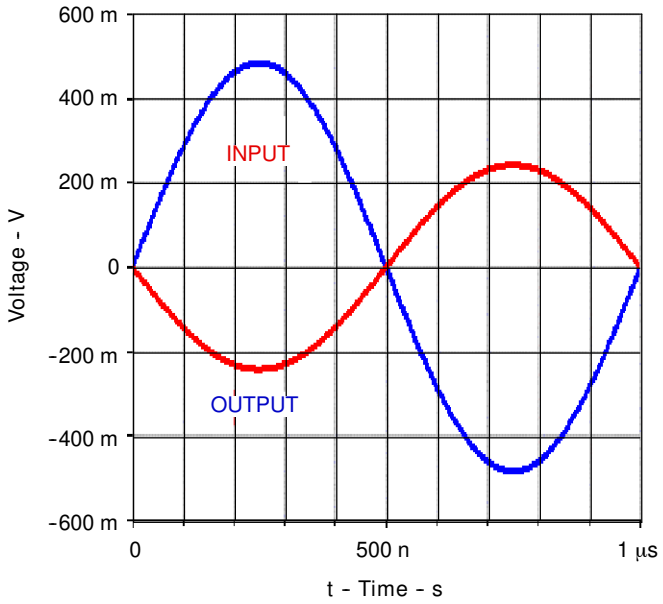
2) Verify that both the +15 V (current meter 1) and the –15 V (current meter 2) currents are below 25 mA.

> **CAUTION**
>
> Currents above the limits stated above indicate a possible short or a wrong resistor value on the PCB. Do not proceed until this situation is correct.

3) Turn on the function generator.

4) Verify the oscilloscope is showing two 1-MHz sine waves, the input with an amplitude of ±0.484 V and the output with an amplitude of ±0.242 V as shown in Figure 2–3. They should be 180° out out of phase. See Section 3.1 for an explanation of these voltage values.

Figure 2–3. Oscilloscope Output for Channel 1



2.5 Input and Output Setup for Channel 2

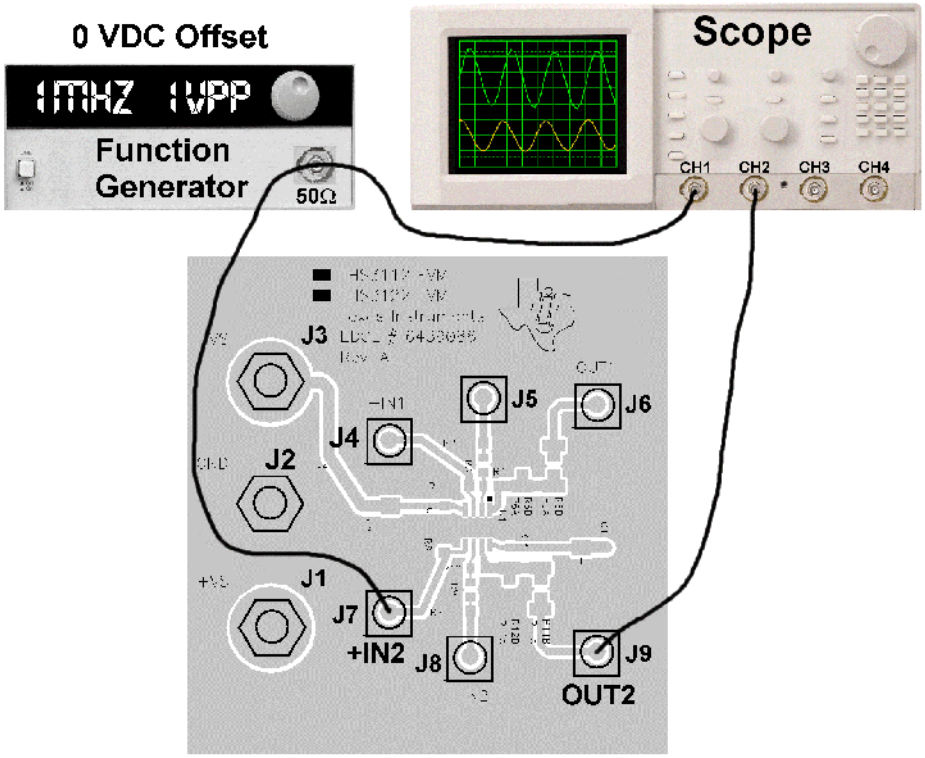
1) Verify that the function generator is still set to generate a 1-MHz, ±0.5 V (1-V_{PP}) sine wave with no dc offset.
2) Turn off the function generator before proceeding to the next step.
3) Connect a BNC *T* connector to the output of the function generator.
4) Using a BNC-to-SMA cable, connect the function generator to J7 (+IN2) on the EVM.
5) Using a BNC-to-BNC cable, connect the function generator output to the oscilloscope input 1.

NOTE: The oscilloscope input 1 must be set to use 1-MΩ input impedance for proper results.

6) Using a BNC-to-SMA cable, connect the oscilloscope input 2 to J9 (OUT2) on the EVM.
7) Set the oscilloscope to 0.2 V/division and a time-base of 0.1 μs/division.

NOTE: The oscilloscope input 2 must be set to use 50-Ω input impedance for proper results.

Figure 2–4. Signal Connections for Channel 2



2.6 Operating the EVM on Channel 2

1) Turn on the dc power supply.

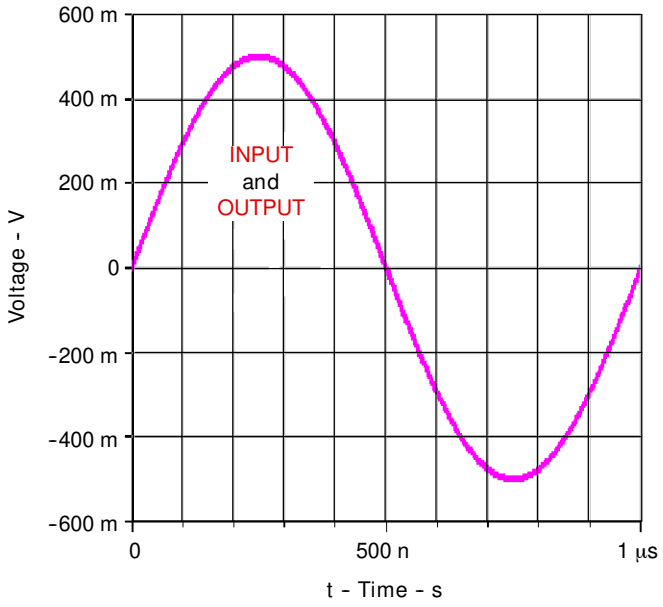
2) Verify that both the +15 V (current meter 1) and the –15 V (current meter 2) currents are below 25 mA.

> **CAUTION**
>
> Currents above the limits stated above indicate a possible short or a wrong resistor value on the PCB. Do not proceed until this situation is correct.

3) Turn on the function generator.

4) Verify the oscilloscope is showing two 1-MHz sine waves as shown in Figure 2–5. Both should have amplitude of ±0.5 V and both should be in phase.

Figure 2–5. Oscilloscope Output for Channel 2



Chapter 3

Circuit Design Examples

Several example applications are presented in this chapter. These applications demonstrate the most popular circuits to the user, but many other circuits can be constructed. The user is encouraged to experiment with different circuits, exploring new and creative design techniques. That, after all, is the function of an evaluation board.

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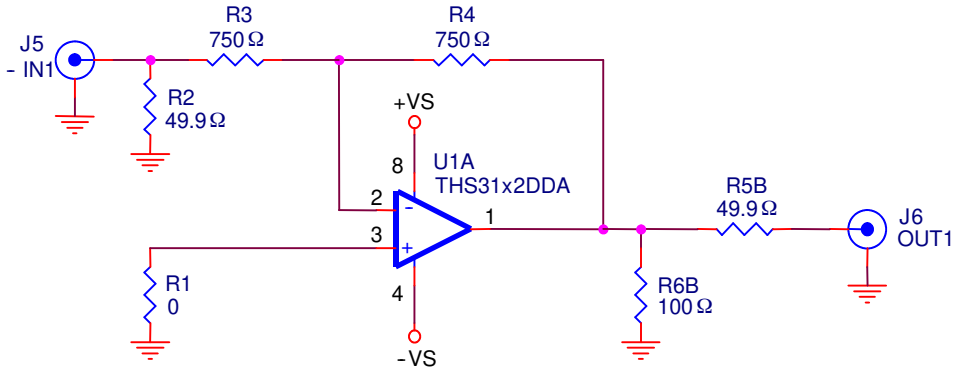
3.1 Inverting Stage (Channel 1) Operation

Inverting stage operation was shown in Chapter 2 of this manual. The default configuration is a 50-Ω terminated input (R2), a 50-Ω matching resistor output (R5B), and a 100-Ω load (R6B). The terminating and matching values can be changed if the user requires different termination and matching—for example, 75-Ω video applications. The load resistor, however, should not be changed because many op amp specifications are measured at this load. Gain of the stage can be modified by changing the values of R3 and R4.

Figure 3-1. Inverting Gain Stage



The gain of this stage is –1 from J5 to J6 for a high impedance load, and –1/2 from J5 to J6 for a 50 Ω load.

> Note:
>
> The inverting configuration affects the level of voltage applied to the EVM. While the function generator indicates a level of ±0.5 V (1 V_{PP}), only ±0.484 V (0.968 V_{PP}) is applied to the board. The user is justified in wondering, where did the rest of the voltage (±0.016 V) go?

There are two ways of looking at this problem:

- From the function generator side. The function generator contains a 50-Ω source resistor. The EVM contains a 49.9-Ω termination resistor, and therefore the output of the function generator may see (approximately) a 2:1 voltage divider. The function generator anticipates this and scales its output accordingly.

  In the inverting configuration, however, the inverting input presents a ground potential to the gain resistor R_g. This is because the ideal op amp model forces both inputs to the same voltage potential. The noninverting input is connected to ground, and therefore the inverting input is also at ground. The resulting impedance resistance for the stage is therefore equal to the termination resistor in parallel to R_g, in this case 750 Ω. Therefore, the instrument output is actually:

$$V_{output} = \frac{\frac{R_{termination} \times R_g}{R_{termination} + R_g}}{R_{source} + \frac{R_{termination} \times R_g}{R_{termination} + R_g}} = \frac{\frac{49.9 \times 750}{49.9 + 750}}{50 + \frac{49.9 \times 750}{49.9 + 750}} = 0.483 \text{ peak}$$

This can also be viewed as the Thevenin equivalent voltage looking into the source at J4 of the EVM.

❑ From the EVM side. The Thevenin equivalent resistance of the EVM plus the source—looking towards the source from the inverting input of the op amp is:

$$R_{th} = R_g + \frac{R_{source} \times R_{termination}}{R_{source} + R_{termination}} = 750 + \frac{50 \times 49.9}{50 + 49.9} = 774.97\ \Omega$$

Therefore, the inverting gain on a 0.5-Vpeak ideal voltage source (assumed to be embedded in the function generator) is:

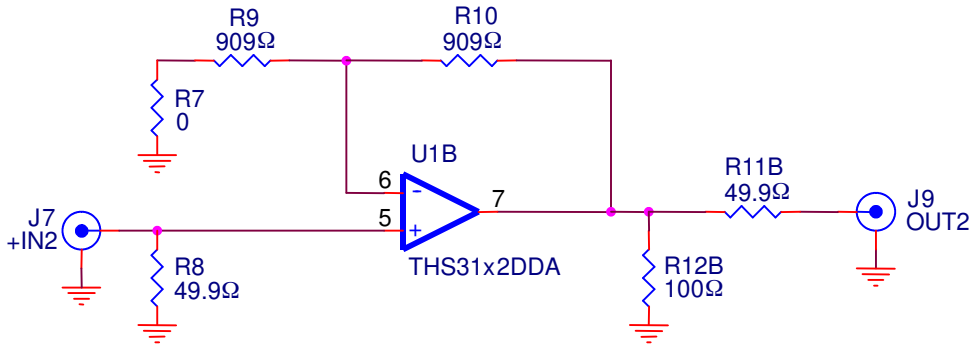
$$V_{output} = -V_{in} \times \frac{R_f}{R_g} = -0.5 \times \frac{750}{774.97} = -0.483 \text{ peak}$$

The two results are identical and therefore equivalent.

3.2 Noninverting Stage (Channel 2) Operation

Noninverting stage operation was shown in Chapter 2 of this manual. The default configuration is a 50-Ω terminated input (R8), a 50-Ω matching resistor output (R11B), and a 100-Ω load (R12B). The terminating and matching values can be changed if the user requires different termination and matching—for example, 75-Ω video applications. The load resistor, however, should not be changed because many op amp specifications are measured at this load. Gain of the stage can be modified by changing the values of R9 and R10.

Figure 3-2. Noninverting Gain Stage



The gain of the circuit as populated is 2 with a high impedance load, and 1 with a 50-Ω load. This circuit does not exhibit the reduction in input voltage level described for the inverting stage—as the input is connected directly to a high impedance input of the op amp.

The circuit of Figure 3-2 can be utilized as a video driver if the 49.9-Ω resistors are removed and 75-Ω resistors are substituted.

Chapter 4

General High-Speed Amplifier Design Considerations

The THS3112/22 EVM layout has been designed for use with high-speed signals and can be used as an example when designing PCBs incorporating the THS3112/22. Careful attention has been given to component selection, grounding, power supply bypassing, and signal path layout. Disregarding these basic design considerations could result in less than optimum performance of the THS3112/22 high-speed operational amplifier. Surface-mount components are selected because of the extremely low lead inductance associated with this technology. This helps minimize both stray inductance and capacitance. Also, because surface-mount components are physically small, the layout can be very compact.

Tantalum power supply bypass capacitors at the power input pads help filter switching transients from the laboratory power supply. The 0.1-μF power supply bypass capacitors are placed as close as possible to the IC power input pins in order to minimize the return path impedance. This improves high frequency bypassing and reduces harmonic distortion. If poor high frequency performance is observed, replace the 0.1-μF capacitors with microwave capacitors with a self-resonance at the frequency that produces trouble. A proper ground plane on both sides of the PCB should be used with high-speed circuit design. This provides low-inductive ground connections for return current paths.

In the area of the amplifier input pins, however, the ground plane is removed to minimize stray capacitance and reduce ground plane noise coupling into these pins. This is especially important for the inverting pin while the amplifier is operating in the noninverting mode in the single-ended to differential mode. Because the voltage at this pin swings directly with the noninverting input voltage, any stray capacitance would allow currents to flow into the ground plane. This could cause possible gain error and/or oscillation. Capacitance variations at the amplifier input pin of greater than 1 pF can significantly affect the response of the amplifier.

In general, it is best to keep signal lines as short and as straight as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω, as required by the application. Such a signal line must also be properly terminated with an appropriate resistor.

Finally, proper termination of all inputs and outputs must be incorporated into the layout. Unterminated lines, such as coaxial cable, can appear to be a reactive load to the amplifier. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears to be purely resistive, and reflections are absorbed at each end of the line. Another advantage of using an output termination resistor is that capacitive loads are isolated from the amplifier output. This isolation helps minimize the reduction in the amplifier's phase-margin and improves the amplifier stability resulting in reduced peaking and settling times.

Chapter 5

EVM Hardware Description

This chapter describes the EVM hardware. It includes the EVM parts list, the printed-circuit board layout, and the schematic.

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5.1 Bill of Materials

Table 5-1. THS3112 EVM Bill of Materials

ITEM	DESCRIPTION	SMD SIZE	REF DESIGNATOR	PCB QTY	MANUFACTURER'S PART NUMBER	DISTRIBUTOR'S PART NUMBER
1	CAP, 6.8 μF, tantalum, 35 V, 10%	D	C1, C2	2	(AVX) TAJD685K035R	(Garrett) TAJD685K035R
2	CAP, 0.1 μF, ceramic, X7R, 50 V	0805	C3, C4	2	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
3	Resistor, 750 Ω, 1/8W, 1%	0805	R3, R4	2	(Phycomp) 9C08052A7500FKHFT	(Garrett) 9C08052A7500FKHFT
4	Resistor, 909 Ω, 1/8W, 1%	0805	R9, R10	2	(Phycomp) 9C08052A9090FKHFT	(Garrett) 9C08052A9090FKHFT
5	OPEN	1206	R5A, R6A, R11A, R12A	4		
6	Resistor, 0 Ω, 1/4W	1206	R1, R7	2	(Phycomp) 9C12063A0R00JLHFT	(Garrett) 9C12063A0R00JLHFT
7	Resistor, 49.9 Ω, 1/4W, 1%	1206	R2, R8	2	(Phycomp) 9C12063A49R9FKRFT	(Garrett) 9C12063A49R9FKRFT
8	Resistor, 49.9 Ω, 1W, 1%	2512	R5B, R11B	2	(Vishay) CRCW251249R9FP (KOA) RK73H3A49R9FP	(TTI) CRCW251249R9FP (TTI) RK73H3A49R9FP
9	Resistor, 100 Ω, 1W, 1%	2512	R6B, R12B	2	(KOA) RK73H3A1000FTE	(Garrett) RK73H3A1000FTE
10	Jack, banana receptance, 0.25" diameter hole		J1, J2, J3	3	(HH Smith) 101	(Newark) 35F865
11	Connector, SMA PCB jack		J4, J5, J6, J7, J8, J9	6	(Amphenol) 901-144-8RFX	(Newark) 01F2208
12	Standoff, 4-40 HEX, 0.625" length			4	(Keystone) 1804	(Allied) 839-2089
13	Screw, Phillips, 4-40, 0.250"			4	SHR-0440-016-SN	
14	IC, THS3122		U1	1	(TI) THS3122DDA	
15	Board, printed-circuit			1	(TI) EDGE # 6439086	

Table 5–2. THS3122 EVM Bill of Materials

ITEM	DESCRIPTION	SMD SIZE	REF DESIGNATOR	PCB QTY	MANUFACTURER'S PART NUMBER	DISTRIBUTOR'S PART NUMBER
1	CAP, 6.8 μF, tantalum, 35 V, 10%	D	C1, C2	2	(AVX) TAJD685K035R	(Garrett) TAJD685K035R
2	CAP, 0.1 μF, ceramic, X7R, 50 V	0805	C3, C4	2	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
3	Resistor, 750 Ω, 1/8W, 1%	0805	R3, R4	2	(Phycomp) 9C08052A7500FKHFT	(Garrett) 9C08052A7500FKHFT
4	Resistor, 909 Ω, 1/8W, 1%	0805	R9, R10	2	(Phycomp) 9C08052A9090FKHFT	(Garrett) 9C08052A9090FKHFT
5	OPEN	1206	R5A, R6A, R11A, R12A	4		
6	Resistor, 0 Ω, 1/4W	1206	R1, R7	2	(Phycomp) 9C12063A0R00JLHFT	(Garrett) 9C12063A0R00JLHFT
7	Resistor, 49.9 Ω, 1/4W, 1%	1206	R2, R8	2	(Phycomp) 9C12063A49R9FKRFT	(Garrett) 9C12063A49R9FKRFT
8	Resistor, 49.9 Ω, 1W, 1%	2512	R5B, R11B	2	(Vishay) CRCW251249R9FP (KOA) RK73H3A49R9FP	(TTI) CRCW251249R9FP (TTI) RK73H3A49R9FP
9	Resistor, 100 Ω, 1W, 1%	2512	R6B, R12B	2	(KOA) RK73H3A1000FTE	(Garrett) RK73H3A1000FTE
10	Jack, banana receptance, 0.25" diameter hole		J1, J2, J3	3	(HH Smith) 101	(Newark) 35F865
11	Connector, SMA PCB jack		J4, J5, J6, J7, J8, J9	6	(Amphenol) 901-144-8RFX	(Newark) 01F2208
12	Standoff, 4-40 HEX, 0.625" length			4	(Keystone) 1804	(Allied) 839-2089
13	Screw, Phillips, 4-40, 0.250"			4	SHR-0440-016-SN	
14	IC, THS3112		U1	1	(TI) THS3112DDA	
15	Board, printed-circuit			1	(TI) EDGE # 6439086	

5.2 Circuit Board Layout

Figure 5–1. Top Layer 1 (Signals) for THS3112 EVM

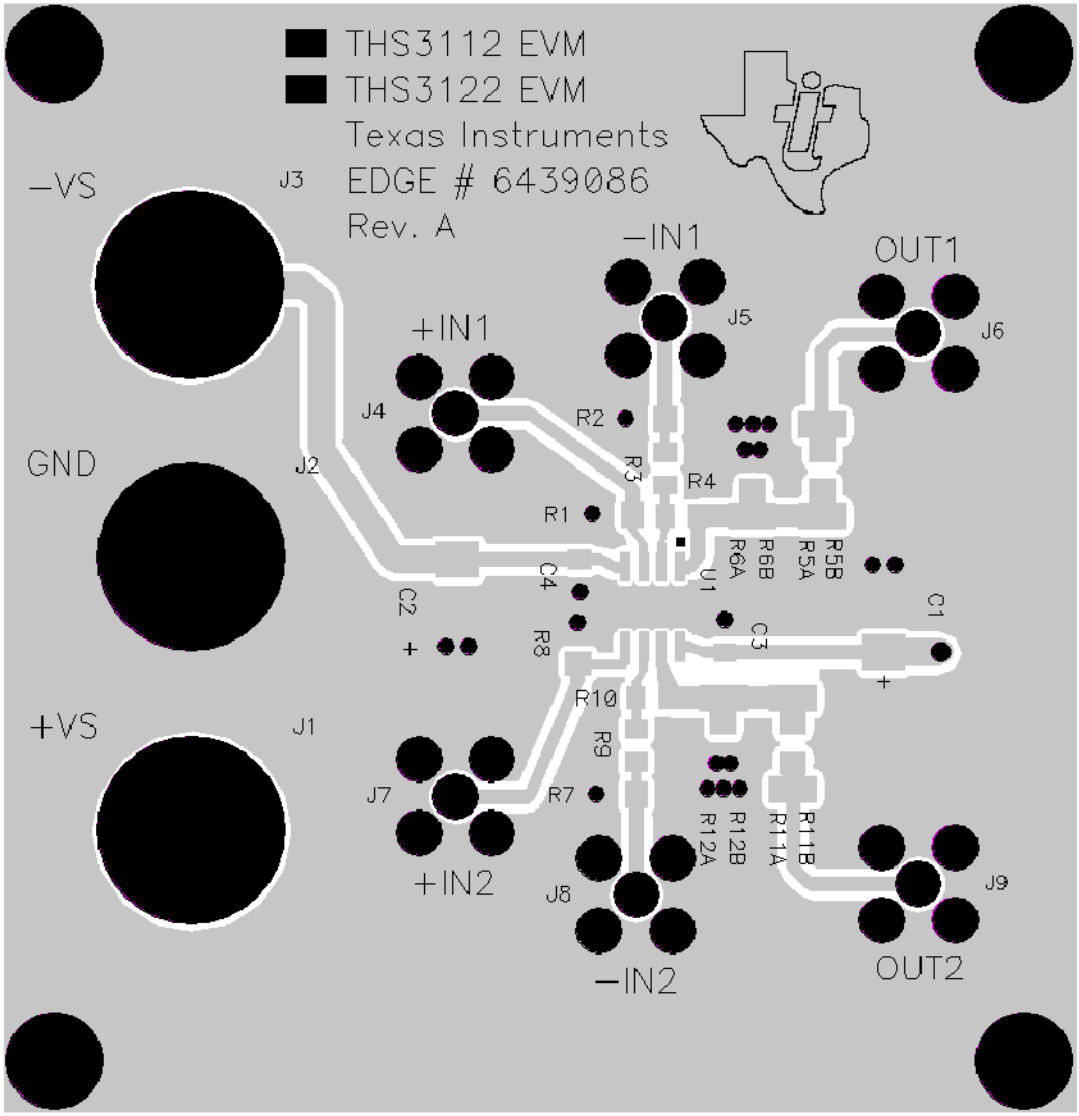
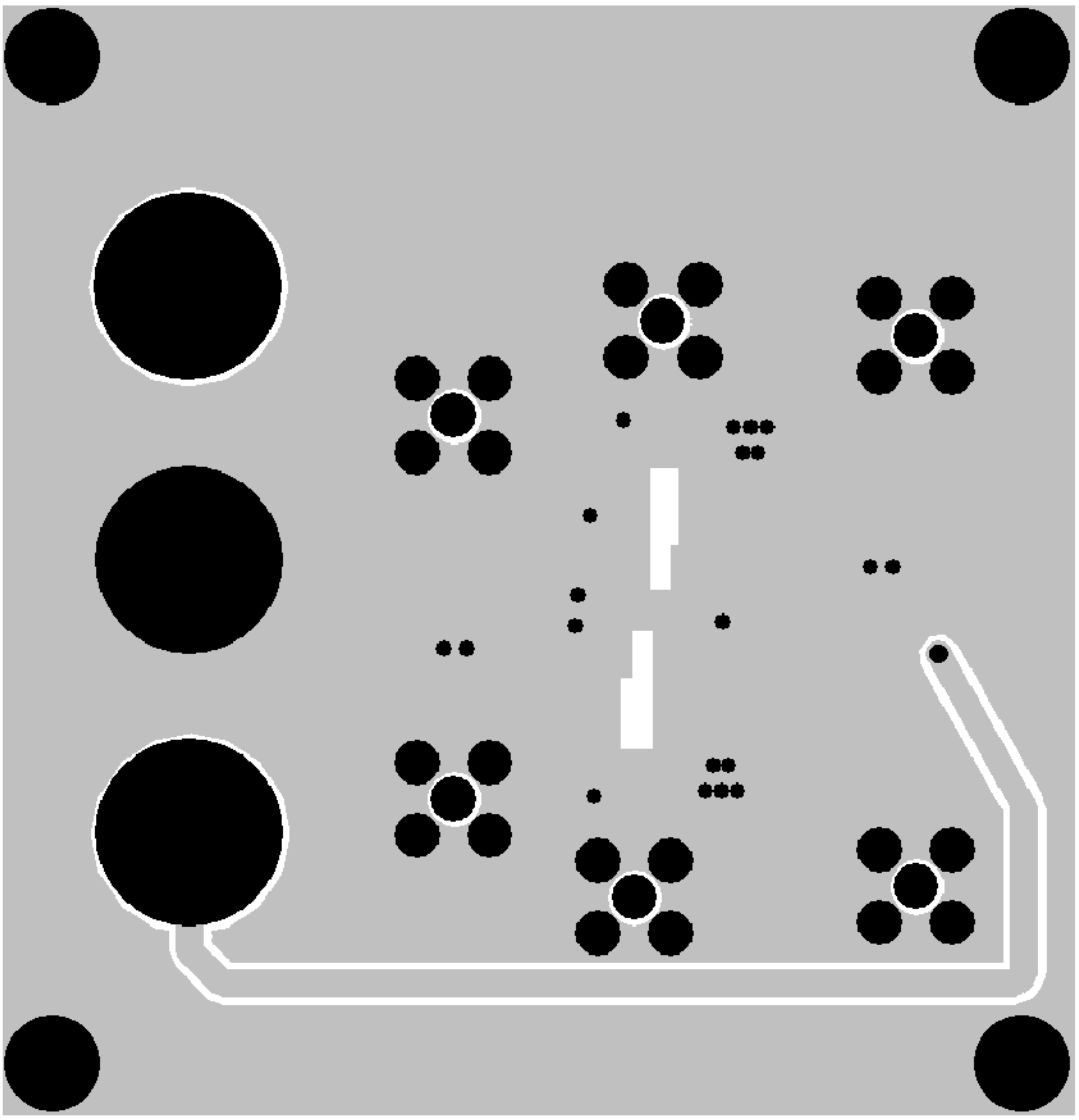


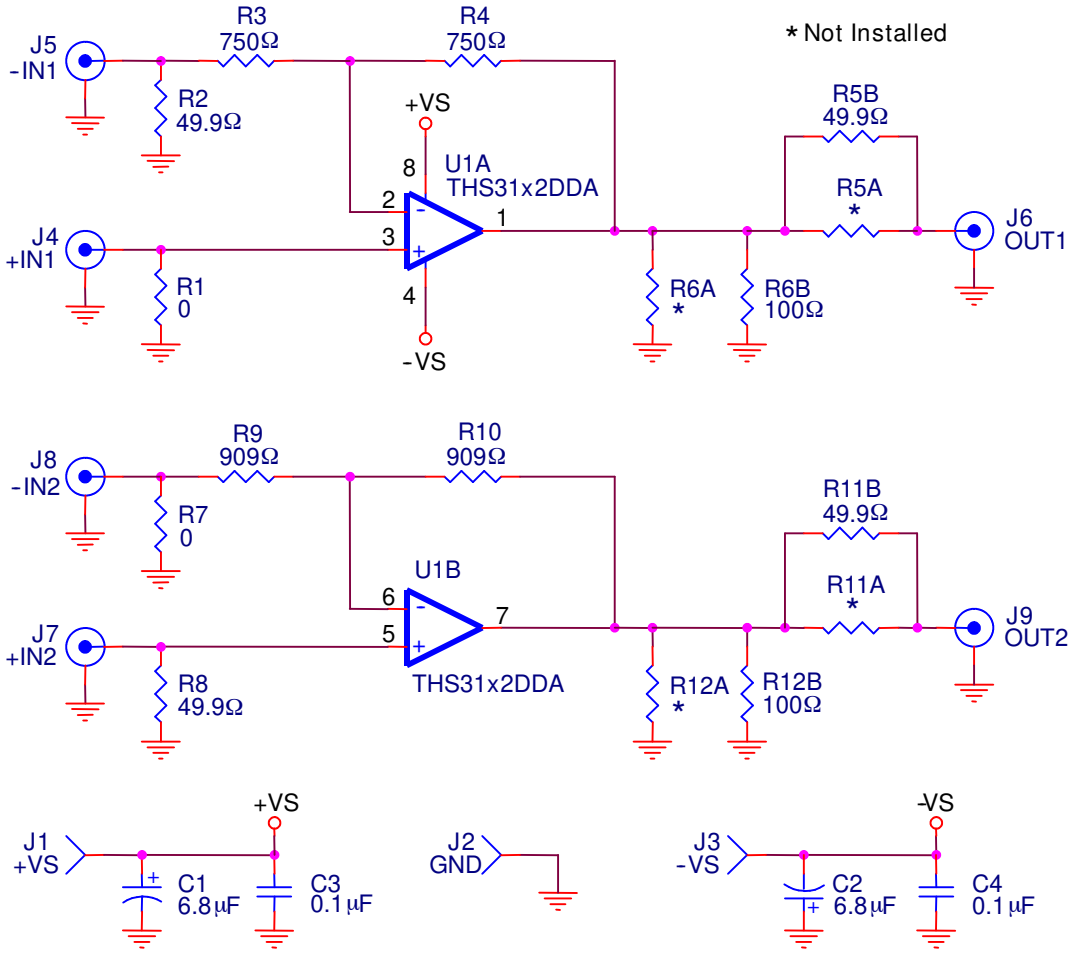
Figure 5-2. Bottom (Layer 2) (Ground and SIgnal) for THS3112 EVM



5.3 Schematic

The full schematic for the THS3112/22 EVM appears below

Figure 5-3. Full Schematic of the EVM



Note: Devices designated with an "*" are not installed on the EVM. The user must supply these components.