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FCP11N60F

N-Channel SuperFET[®] FRFET[®] MOSFET

600 V, 11 A, 380 mΩ

Features

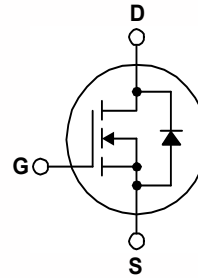
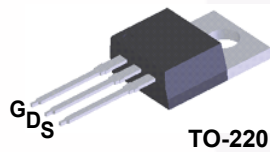
- 650 V @T_J = 150°C
- Typ. R_{DS(on)} = 320 mΩ
- Fast Recovery Type (t_{rr} = 120 ns)
- Ultra Low Gate Charge (Typ. Q_g = 40 nC)
- Low Effective Output Capacitance (Typ. C_{oss,eff} = 95 pF)
- 100% Avalanche Tested
- RoHS compliant

Application

- LCD/LED/PDP TV
- Lighting
- Solar Inverter
- AC-DC Power Supply

Description

SuperFET[®] MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET FRFET[®] MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter	FCP11N60F	Unit
V _{DSS}	Drain to Source Voltage	600	V
I _D	Drain Current	11	A
	- Continuous (T _C = 25°C)	7	
I _{DM}	Drain Current	33	A
	- Pulsed (Note 1)		
V _{GSS}	Gate to Source Voltage	±30	V
E _{AS}	Single Pulsed Avalanche Energy	340	mJ
	(Note 2)		
I _{AR}	Avalanche Current	11	A
	(Note 1)		
E _{AR}	Repetitive Avalanche Energy	12.5	mJ
	(Note 1)		
dv/dt	Peak Diode Recovery dv/dt	4.5	V/ns
	(Note 3)		
P _D	Power Dissipation	125	W
	(T _C = 25°C)		
	- Derate above 25°C	1.0	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	°C

Thermal Characteristics

Symbol	Parameter	FCP11N60F	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max	1.0	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max	62.5	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCP11N60F	FCP11N60F	TO-220	-	-	50

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 25^\circ\text{C}$	600	-	-	V	
		$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 150^\circ\text{C}$	-	650	-	V	
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	0.6	-	$\text{V}/^\circ\text{C}$	
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 11\text{ A}$	-	700	-	V	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA	
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	10		
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA	
On Characteristics							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V	
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}$	-	0.32	0.38	Ω	
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 5.5\text{ A}$	-	6	-	S	
Dynamic Characteristics							
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$	-	1148	1490	pF	
C_{oss}	Output Capacitance		-	671	870	pF	
C_{riss}	Reverse Transfer Capacitance		-	63	82	pF	
C_{oss}	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	35	-	pF	
$C_{oss\text{eff}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	95	-	pF	
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 11\text{ A}$ $R_G = 25\ \Omega$	-	34	80	ns	
t_r	Turn-On Rise Time		-	98	205	ns	
$t_{d(off)}$	Turn-Off Delay Time		-	119	250	ns	
t_f	Turn-Off Fall Time		(Note 4)	-	56	120	ns
$Q_{g(tot)}$	Total Gate Charge at 10V		$V_{DS} = 480\text{ V}, I_D = 11\text{ A},$ $V_{GS} = 10\text{ V}$	-	40	52	nC
Q_{gs}	Gate to Source Gate Charge	(Note 4)	-	7.2	-	nC	
Q_{gd}	Gate to Drain "Miller" Charge		-	21	-	nC	
Drain-Source Diode Characteristics Maximum Ratings							
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	11	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	33	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 11\text{ A}$	-	-	1.4	V	
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 11\text{ A}$	-	120	-	ns	
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$	-	0.8	-	μC	

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. $I_{AS} = 5.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 11\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

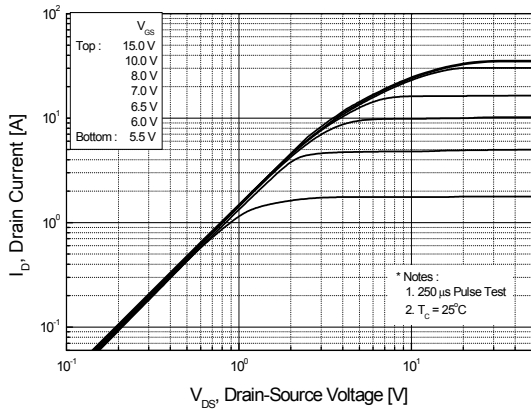


Figure 2. Transfer Characteristics

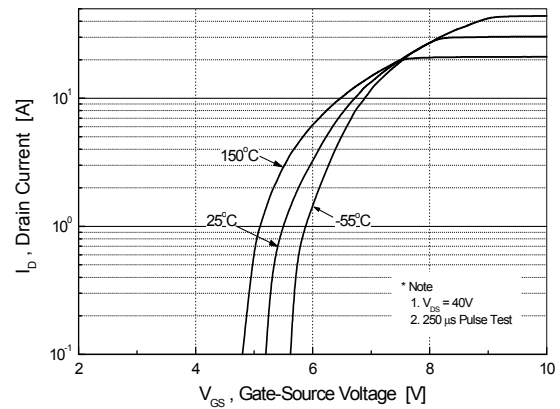


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

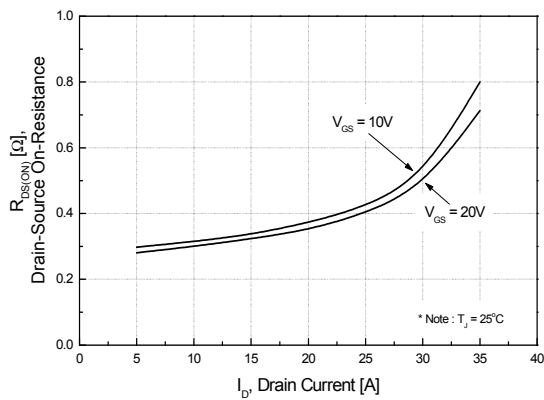


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

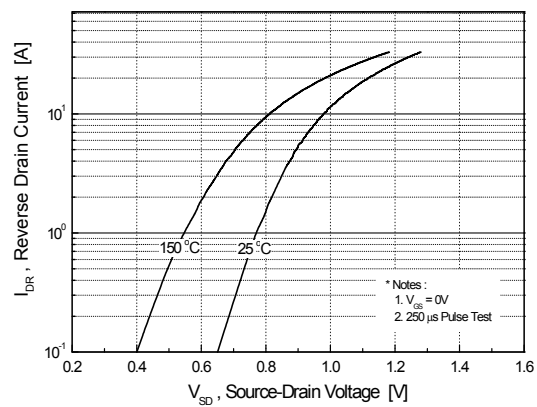


Figure 5. Capacitance Characteristics

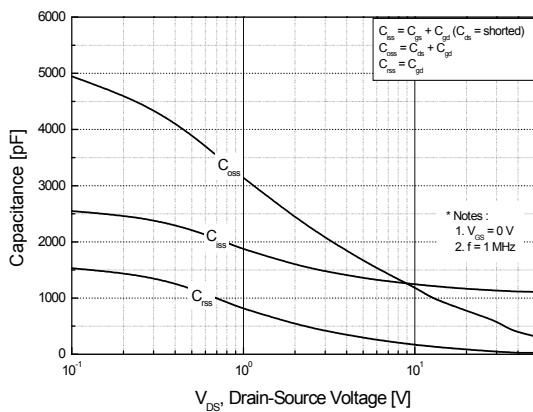
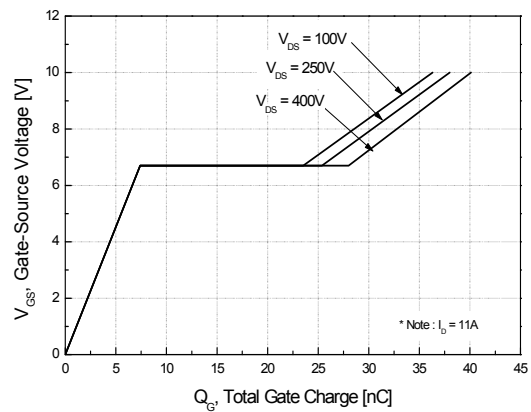


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

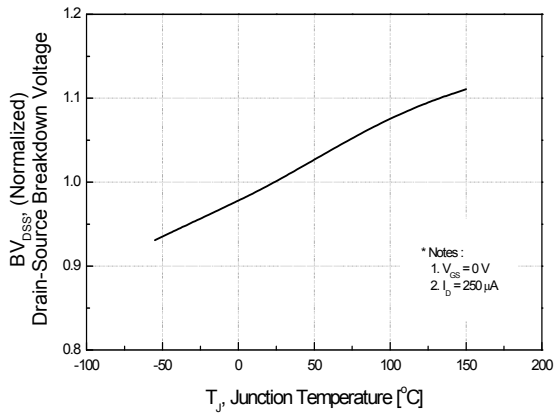


Figure 8. On-Resistance Variation vs. Temperature

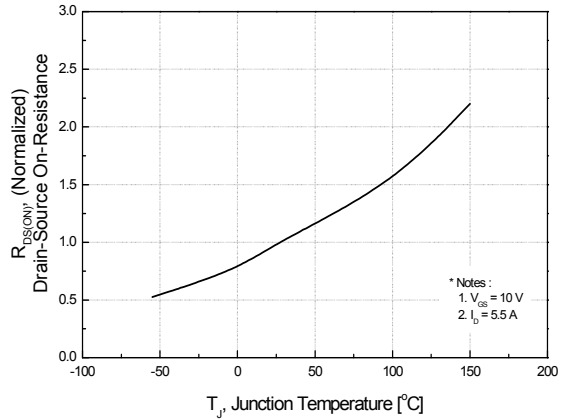


Figure 9. Safe Operating Area

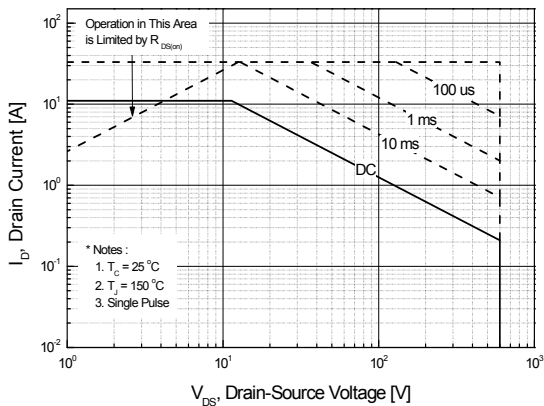


Figure 10. Maximum Drain Current vs. Case Temperature

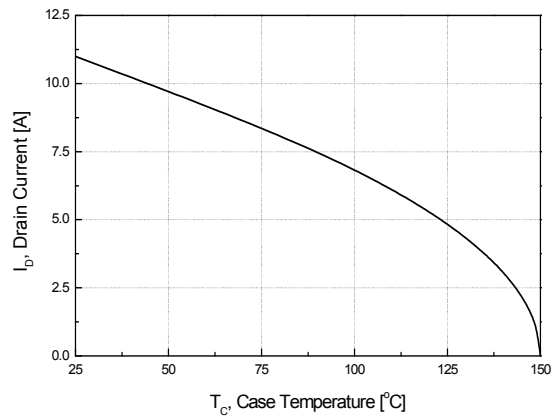


Figure 11. Transient Thermal Response Curve

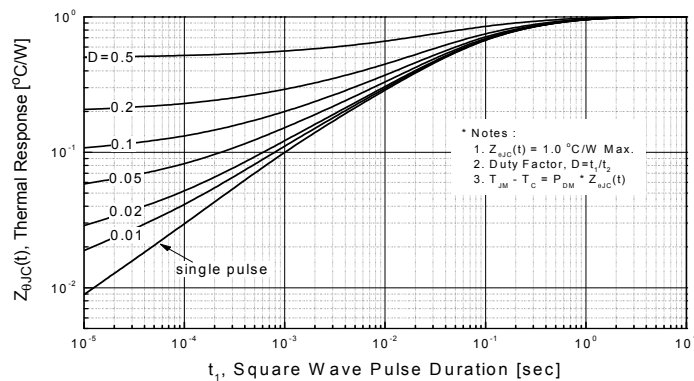


Figure 12. Gate Charge Test Circuit & Waveform

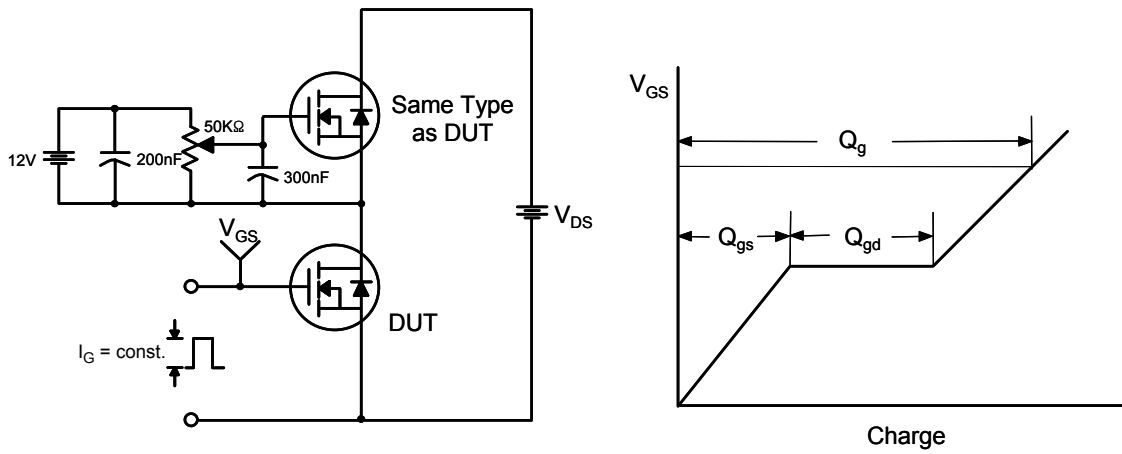


Figure 13. Resistive Switching Test Circuit & Waveforms

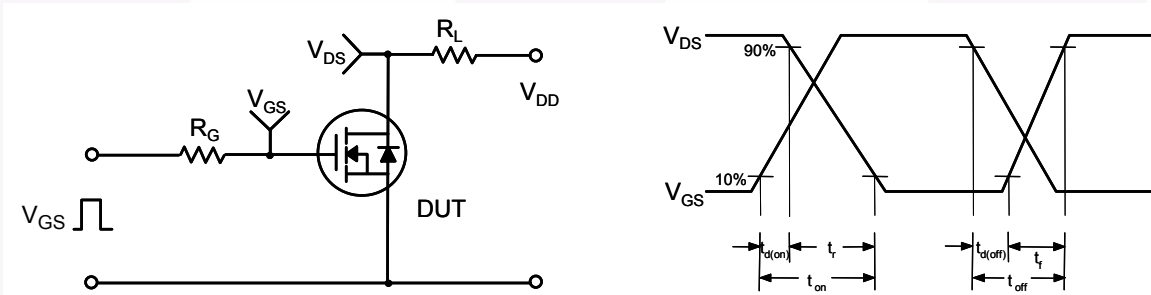


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

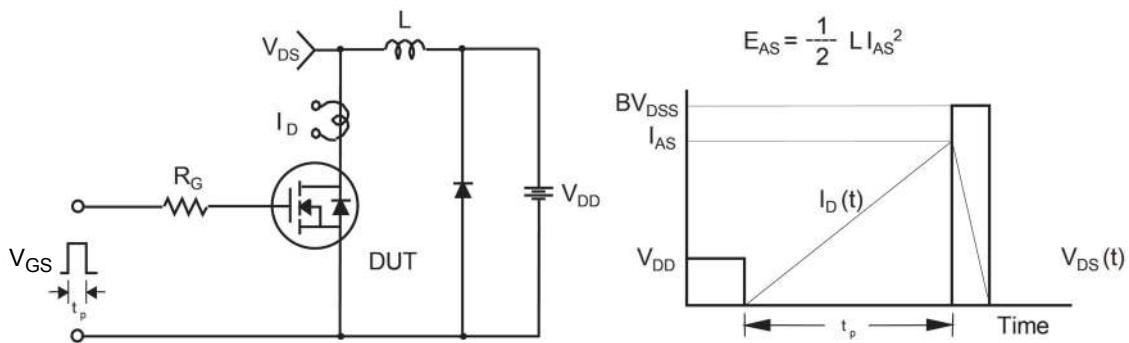
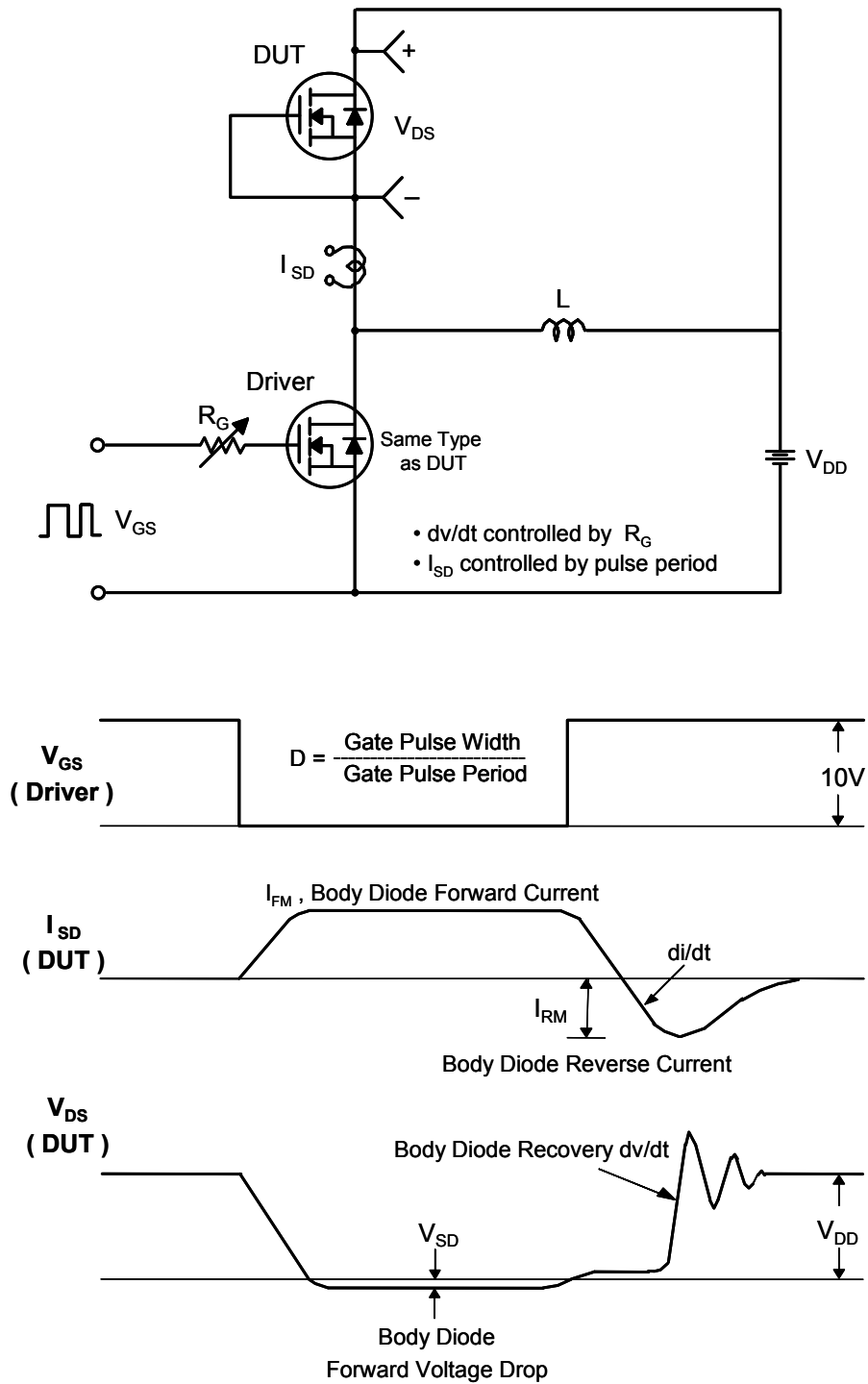
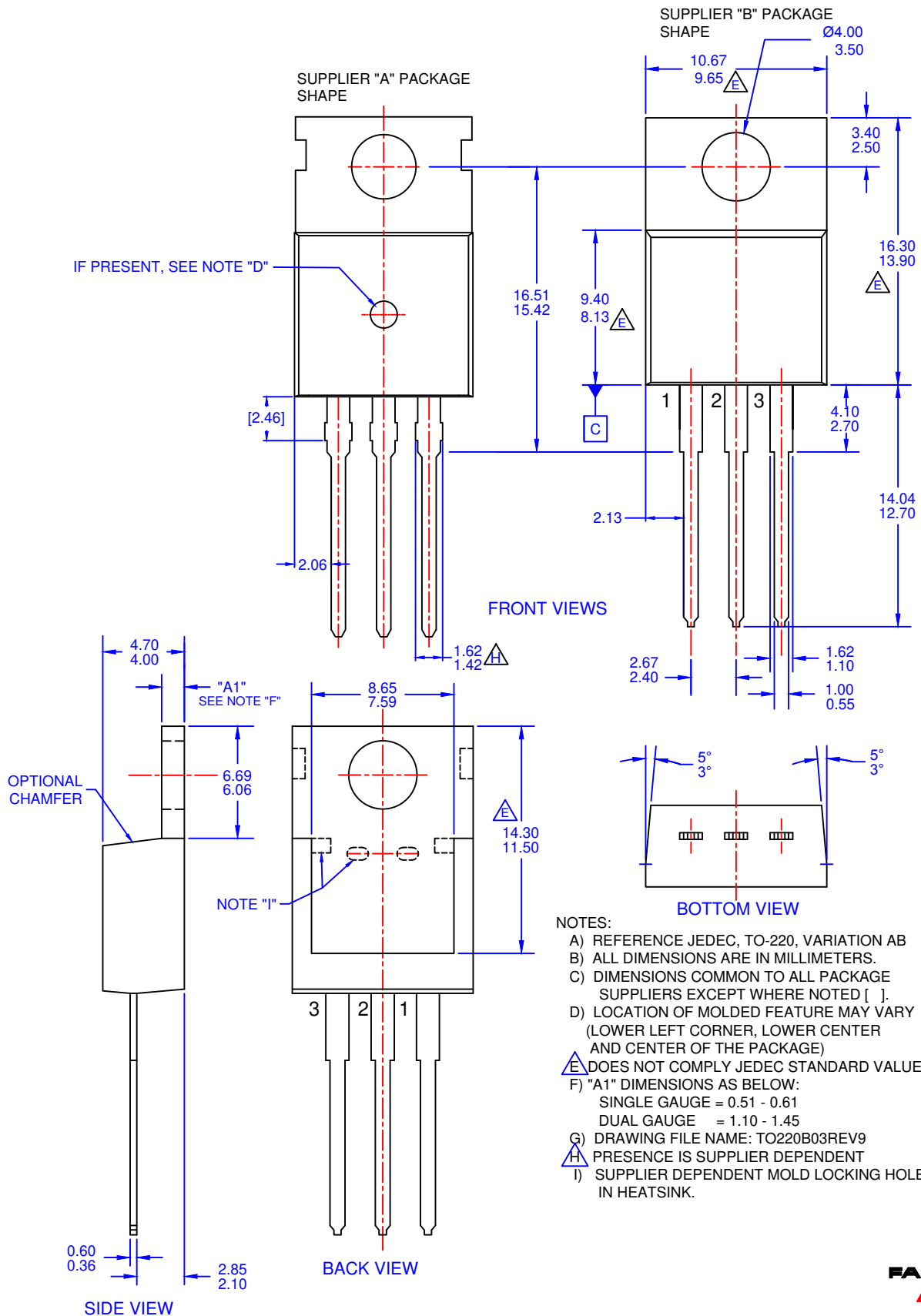


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





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