PRELIMINARY

CY25403
CY25423

Three PLL Programmable Clock Generator with Spread Spectrum

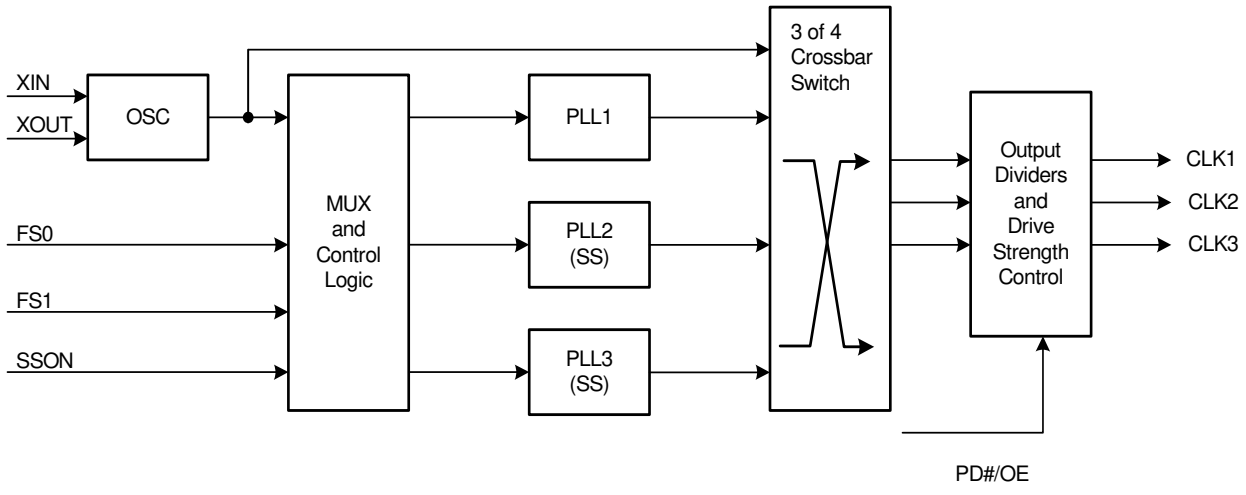
Features

- Three fully integrated phase-locked loops (PLLs)
- Input Frequency range:
  - — External crystal: 8 to 48 MHz
  - — External reference: 8 to 166 MHz clock
- Wide operating output frequency range
  - — 3 to 166 MHz
- Programmable Spread Spectrum modulation frequency range of 30 to 120 kHz with Lexmark profile
- Center Spread: ±0.125% to ±2.5%
- Down Spread: –0.25% to –5%
- Frequency select feature with option to select four different frequencies
- Low-jitter, high-accuracy outputs
- Up to three clock outputs
- Programmable output drive strength
- Glitch-free outputs while frequency switching
- Four independent output voltages: 3.3V, 3.0V, 2.5V, and 1.8V
- 8-pin SOIC package
- Commercial and Industrial temperature range

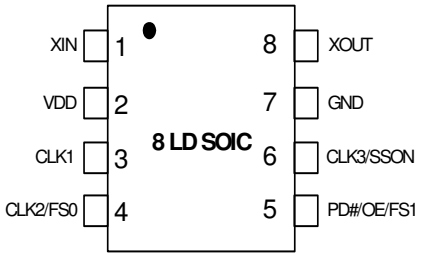
Benefits

- Multiple high-performance PLLs allow synthesis of unrelated frequencies
- Nonvolatile programming for customized PLL frequencies, spread spectrum characteristics, drive strength, crystal load capacitance, and output frequencies
- Two Spread Spectrum capable PLLs with Lexmark profile for maximum for EMI reduction
- Spread Spectrum PLLs can be disabled or enabled separately
- PLLs can be programmed for system frequency margin tests
- Meets critical timing requirements in complex system designs
- Suitable for PC, consumer, and networking applications
- Ability to synthesize standard frequencies with ease
- Application compatibility in standard and low-power systems

Block Diagram



Pin Configuration



Pin Description - Memory Programmable 3-PLL device with 2 Spread Spectrum PLLs

Pin Number	Name	I/O	Description
1	XIN	Input	Crystal or Clock Input
2	VDD	Power	Power Supply
3	CLK1	Output	Programmable Clock Output
4	CLK2/FS0	Output/input	Programmable Clock Output or FS0
5	PD#/OE/FS1	Input	Power Down, Output Enable or FS1
6	CLK3/SSON	Output/Input	Programmable Clock Output or SSON
7	GND	Power	Power Supply Ground
8	XOUT	Output	Crystal Output

General Description

Th CY25403 and CY25423 are three PLL programmable Spread Spectrum Clock Generators used to reduce EMI found in high-speed digital electronic systems. Two of the three PLLs have Spread Spectrum capability. The spread spectrum feature are turned on or off using the control pin SSON.

The advantage of having three PLLs is that a single device can generate up to three independent frequencies from a single crystal or reference input frequency. Generally, a design requires up to three oscillators to achieve the same result with a single CY25403 or CY25423.

The device uses Cypress proprietary PLL and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the input clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies are greatly reduced. This reduction in radiated energy significantly reduces the cost of complying with regulatory agency (EMC) requirements and improves time-to-market without degrading the system performance.

The CY25403 and CY25423 use a factory/field-programmable configuration memory array to provide customization for output frequencies, frequency select options, spread characteristics like spread percentage and modulation frequency, output drive strength and crystal load capacitance. A customized device can be configured using Cyberclocks$_{TM}$ software or by contacting the factory.

The spread percentage is programmed to either center spread or down spread with various spread percentages. The range for center spread is from ±0.125% to ±2.50%. The range for down spread is from –0.25% to –5.0%. Contact the factory for smaller or larger spread percentage amounts, if required.

The input to the CY25403 and CY25423 is either a crystal or a clock signal. The input frequency range for crystals is 8 MHz to 48 MHz, and for clock signals is 8 MHz to 166 MHz.

The CY25403 and CY25423 have up to three clock outputs and each output has four possible input sources.There are two frequency select lines FS(1:0) that provide an option to select four different sets of frequencies among the each of the three PLLs. Each output has programmable output divider options. Output 1 has eight possible divider values and outputs 2–3 have four possible divider values for maximum flexibility. The 2 bit or 3 bit output dividers are programmable providing a wide output frequency range.

The outputs are glitch-free when frequency is switched using output dividers. The outputs have a predictable phase relationship, if the clock source is the same PLL and divider values are 2, 3, 4, or 6.

The CY25403 and CY25423 are 3-PLL memory programmable spread spectrum clock generators with three clock outputs.

Table 1. Supply Voltage Options

Device	V_{DD} Supply Voltage
CY25403	2.5V, 3.0V or 3.3V
CY25423	1.8V

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Supply Voltage		–0.5	4.5	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non Functional	–65	+150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	Volts
UL-94	Flammability Rating	@1/8 in.	V-0		
MSL	Moisture Sensitivity Level	SOIC package	1		

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD1}	Operating Voltage, 3.3V	3.0	–	3.6	V
V_{DD2}	Operating Voltage, 3.0V	2.7	–	3.3	V
V_{DD3}	Operating Voltage, 2.5V	2.25	–	2.75	V
V_{DD4}	Operating Voltage, 1.8V	1.65	–	1.95	V
T_{AC}	Commercial Ambient Temperature	0	–	+70	°C
T_{AI}	Industrial Ambient Temperature	–40	–	+85	°C
C_{LOAD}	Max. Load Capacitance	–	–	15	pF
t_{PU}	Power-up time for all V_{DD} pins to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Output Low Voltage, All CLK pins	All V_{DD} levels, I_{OL} = 8 mA	0	–	0.4	V
V_{OH}	Output High Voltage, All CLK pins	All V_{DD} levels, I_{OH} = –8 mA	V_{DD} – 0.4	–	V_{DD}	V
V_{IL}	All Inputs except XIN	All V_{DD} levels	–0.3	–	0.2 * V_{DD}	V
V_{IH}	All Inputs except XIN	All V_{DD} levels	0.8 * V_{DD}	–	V_{DD} + 0.3	V
V_{ILX}	Input Low Voltage, clock input to XIN pin	All V_{DD} levels	–0.3	–	0.36	V
V_{IHX}	Input High Voltage, clock input to XIN pin	All V_{DD} levels	1.44	–	2.0	V
I_{ILPDOE}	Input Low Current, PD#/OE and FS0,1 pins	V_{IN} = V_{SS} (Internal pull up = 100k typical)	–	–	10	µA
I_{IHPDOE}	Input High Current, PD#/OE and FS0,1 pins	V_{IN} = V_{DD} (Internal pull up = 100k typical)	–	–	1	µA
I_{ILSR}	Input Low Current, SSON pin	V_{IN} = V_{SS} (Internal pull down = 100k typical)	–	–	1	µA
I_{IHSR}	Input High Current, SSON pin	V_{IN} = V_{DD} (Internal pull down = 100k typical)	–	–	10	µA
I_{DD}[1]	Supply Current	All clocks running, CL = 0	–	–	17	mA
C_{IN}	Input Capacitance - All inputs except XIN	SSON, OE, PD# or FS inputs	–	–	7	pF

Note
1. Configuration dependent.

AC Electrical Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
F_{IN} (crystal)	Crystal Frequency		8	–	48	MHz
F_{IN} (clock)	Input Clock Frequency (XIN)		8	–	166	MHz
F_{OUT}	Output Clock Frequency		3	–	166	MHz
DC	Output Duty Cycle All Clocks except Ref Out	Duty Cycle is defined in *Figure 2*; t_1/t_2, 50% of V_{DD}	45	50	55	%
DC	Ref Out Duty Cycle	Ref In Min 45%, Max 55%	40		60	%
E_R	CLK1-3 Rising Edge Rate	V_{DD} = All, 20% to 80% V_{DD}	0.8	–	–	V/ns
E_F	CLK1-3 Falling Edge Rate	V_{DD} = All, 20% to 80% V_{DD}	0.8	–	–	V/ns
T_{CCJ1}	Cycle-to-cycle Jitter	Configuration dependent. See *Table 2*	–	-	–	ps
T_{LTJ}	Long Term Jitter	Configuration dependent. See *Table 2*	–	-	–	ns
T_{10}	PLL Lock Time		–	–	3	ms

Table 2. Configuration Example for Jitter

Reference	Description	Max Jitter (ps) on Output 1(48MHz)	Max Jitter (ps) on Output 2 (27 MHz)	Max Jitter (ps) on Output 3 (166 MHz)
27MHz	T_{CCJ1}	155	255	170
27MHz	T_{LTJ}	770	580	630
48 MHz	T_{CCJ1}	135	225	100
48 MHz	T_{LTJ}	535	575	520

Recommended Crystal Specification for SMD Package

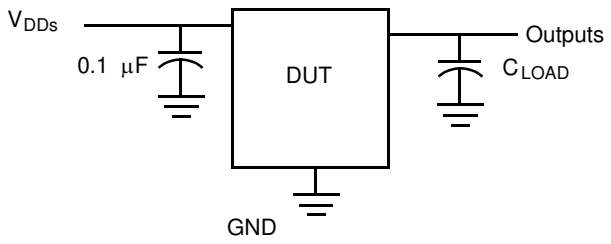
Parameter	Description	Range 1	Range 2	Range 3	Unit
Fmin	Minimum Frequency	8	14	28	MHz
Fmax	Maximum Frequency	14	28	48	MHz
R1(max)	Maximum Motional Resistance (ESR)	135	50	30	Ω
C0(max)	Maximum Shunt Capacitance	4	4	2	pF
CL(max)	Maximum Parallel Load Capacitance	18	14	12	pF
DL(max)	Maximum Crystal Drive Level	300	300	300	µW

Recommended Crystal Specification for Thru-Hole Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
Fmin	Minimum Frequency	8	14	24	MHz
Fmax	Maximum Frequency	14	24	32	MHz
R1(max)	Maximum Motional Resistance (ESR)	90	50	30	Ω
C0(max)	MaximumShunt Capacitance	7	7	7	pF
CL(max)	Maximum Parallel Load Capacitance	18	12	12	pF
DL(max)	Maximum Crystal Drive Level	1000	1000	1000	µW

Test and Measurement Setup

Figure 1. Test and Measurement Setup



Voltage and Timing Definitions

Figure 2. Duty Cycle Definition

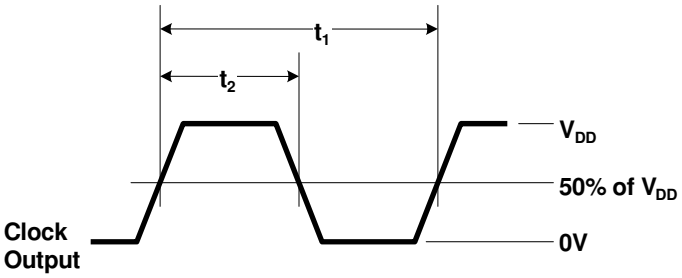
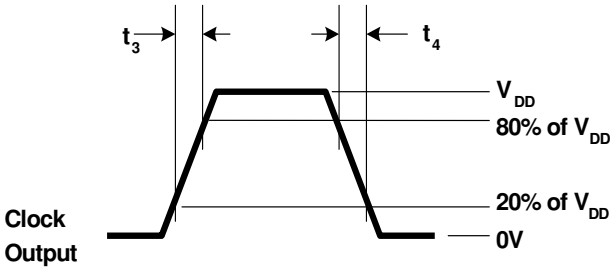


Figure 3. ER = (0.6 x V_{DD}) /t_3, EF = (0.6 x V_{DD}) /t_4



Ordering Information

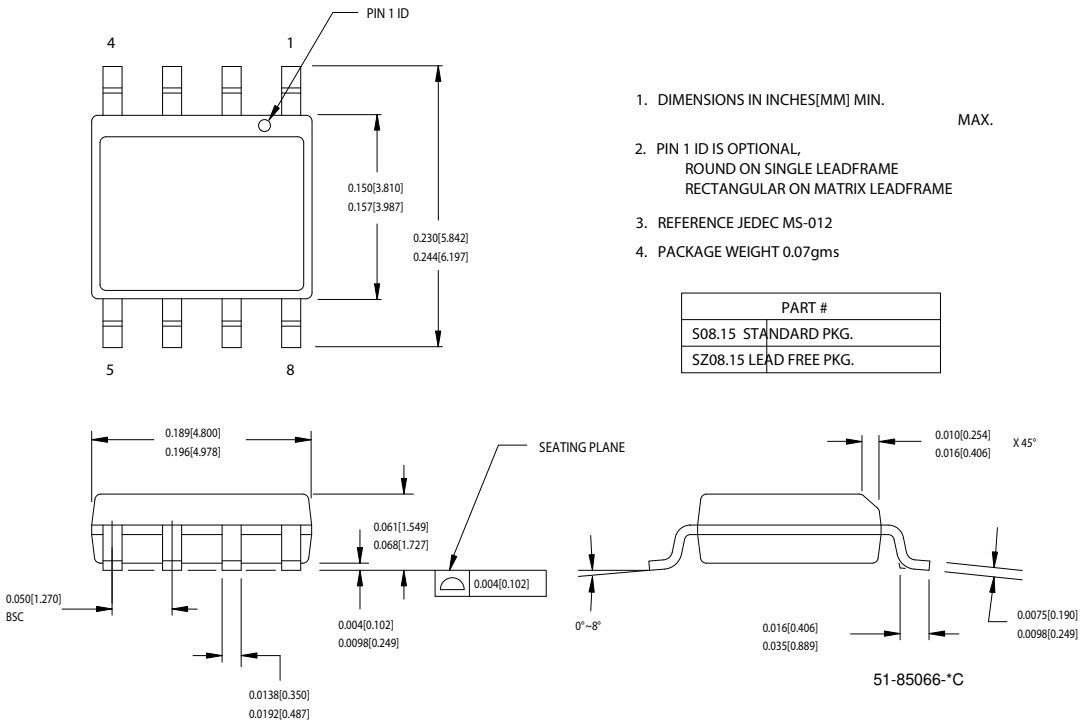
Part Number[2]	Type	VDD(V)	Temperature Range
Lead-free			
CY25403SXC-xxx	8-pin SOIC	3.3, 3.0 or 2.5	Commercial, 0°C to 70°C
CY25403SXC-xxxT	8-pin SOIC-Tape & Reel	3.3, 3.0 or 2.5	Commercial, 0°C to 70°C
CY25403FSXC	8-pin SOIC	3.3, 3.0 or 2.5	Commercial, 0°C to 70°C
CY25403FSXCT	8-pin SOIC-Tape & Reel	3.3, 3.0 or 2.5	Commercial, 0°C to 70°C
CY25423SXC-xxx	8-pin SOIC	1.8	Commercial, 0°C to 70°C
CY25423SXC-xxxT	8-pin SOIC-Tape & Reel	1.8	Commercial, 0°C to 70°C
CY25423FSXC	8-pin SOIC	1.8	Commercial, 0°C to 70°C
CY25423FSXCT	8-pin SOIC-Tape & Reel	1.8	Commercial, 0°C to 70°C
CY25403SXI-xxx	8-pin SOIC	3.3, 3.0 or 2.5	Industrial, -40°C to +85°C
CY25403SXI-xxxT	8-pin SOIC-Tape & Reel	3.3, 3.0 or 2.5	Industrial, -40°C to +85°C
CY25403FSXI	8-pin SOIC	3.3, 3.0 or 2.5	Industrial, -40°C to +85°C
CY25403FSXIT	8-pin SOIC-Tape & Reel	3.3, 3.0 or 2.5	Industrial, -40°C to +85°C
CY25423SXI-xxx	8-pin SOIC	1.8	Industrial, -40°C to +85°C
CY25423SXI-xxxT	8-pin SOIC-Tape & Reel	1.8	Industrial, -40°C to +85°C
CY25423FSXI	8-pin SOIC	1.8	Industrial, -40°C to +85°C
CY25423FSXIT	8-pin SOIC-Tape & Reel	1.8	Industrial, -40°C to +85°C

Note

2. xxx Indicates Factory Programmable are factory programmed configurations. For more details, contact your local Cypress FAE or Cypress Sales Representative. F in the part number indicates field programmable using CyberClocks Online software.

Package Drawing and Dimensions

Figure 4. 8-lead (150-Mil) SOIC S8



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Document History Page

Document Title: CY25403/CY25423 Three PLL Programmable Clock Generator with Spread Spectrum Document Number: 001-12564				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	690339	See ECN	RGL	New Data Sheet
*A	815816	See ECN	RGL	Minor Change: To Post on web