To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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MOS FIELD EFFECT TRANSISTOR
2SK4144

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK4144 is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SK4144-AZ Note	Sn-Ag-Cu	Vinyl bag 200 p/bag	Isolated TO-220 typ. 2.2 g
2SK4144-S12-AZ Note		Tube 50 p/tube	

Note Pb-free (This product does not contain Pb in the external electrode.)

FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 5.8 mΩ MAX. (V_{GS} = 10 V, I_D = 35 A)
  $R_{DS(on)2}$ = 7.3 mΩ MAX. (V_{GS} = 4.5 V, I_D = 35 A)
- Low input capacitance
<R> C_{iss} = 5500 pF TYP. (V_{DS} = 10 V)
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

(Isolated TO-220)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	60	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±70	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±280	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	35	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Repetitive Avalanche Current Note2	I_{AR}	49.5	A
Repetitive Avalanche Energy Note2	E_{AR}	245	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. T_{ch} ≤ 150°C, V_{DD} = 30 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	3.57	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	62.5	°C/W

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Printed in Japan

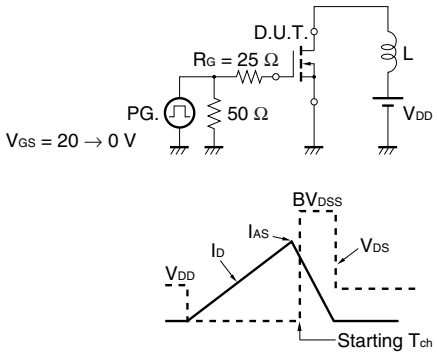
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

<R> **ELECTRICAL CHARACTERISTICS (T_A = 25°C)**

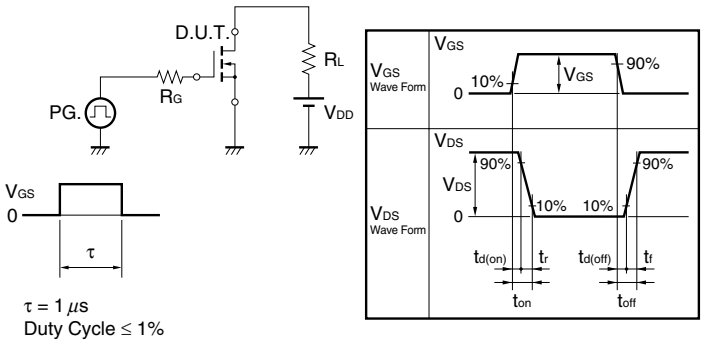
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 35 A	28	56		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 35 A		4.7	5.8	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 35 A		5.3	7.3	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V,		5500		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		1050		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		350		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 35 A,		20		ns
Rise Time	t_r	V_{GS} = 10 V,		12.2		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		100		ns
Fall Time	t_f			9.5		ns
Total Gate Charge	Q_G	V_{DD} = 48 V,		96		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V,		18		nC
Gate to Drain Charge	Q_{GD}	I_D = 70 A		23.5		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 70 A, V_{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 70 A, V_{GS} = 0 V,		48		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		69		nC

Note Pulsed

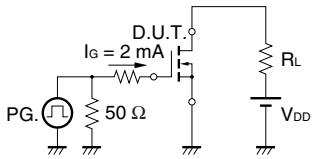
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

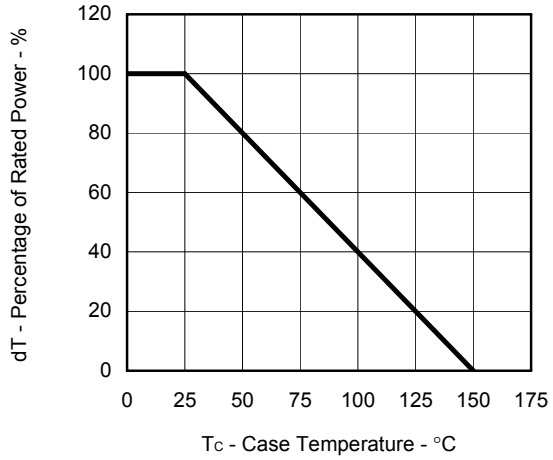


TEST CIRCUIT 3 GATE CHARGE

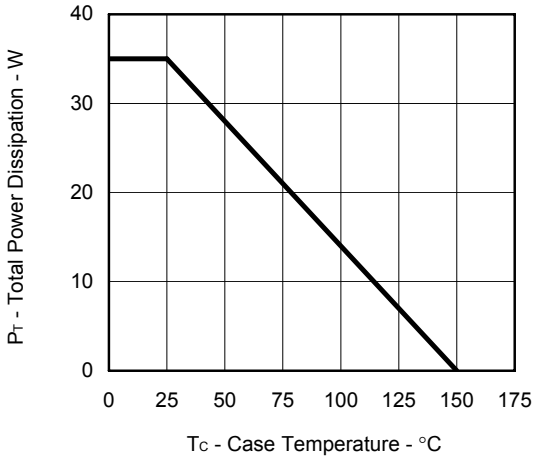


TYPICAL CHARACTERISTICS (T_A = 25°C)

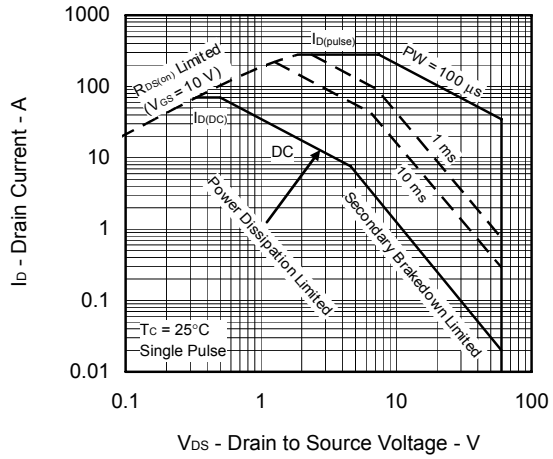
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



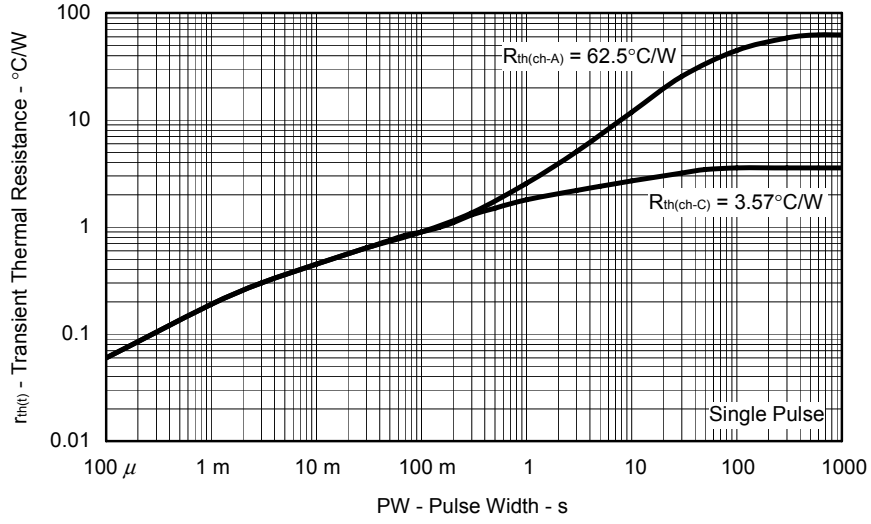
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



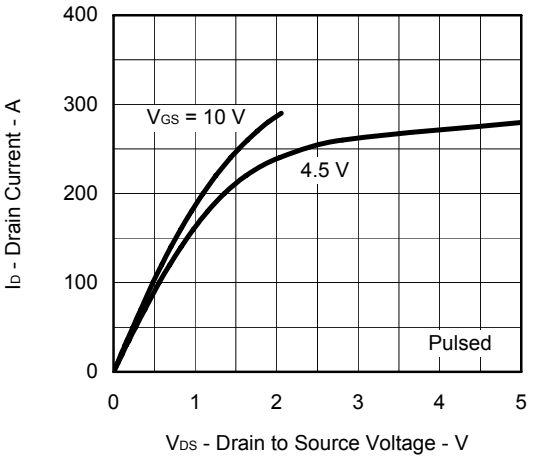
FORWARD BIAS SAFE OPERATING AREA



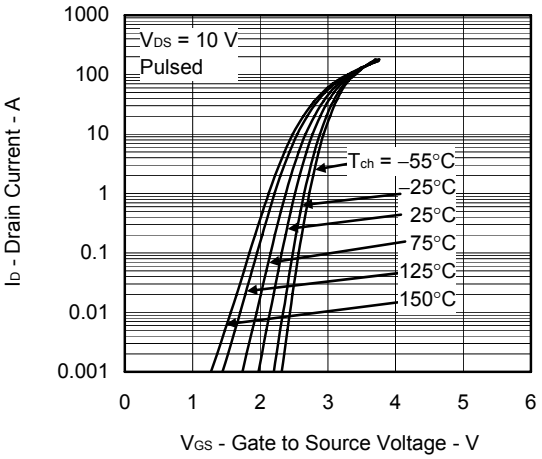
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



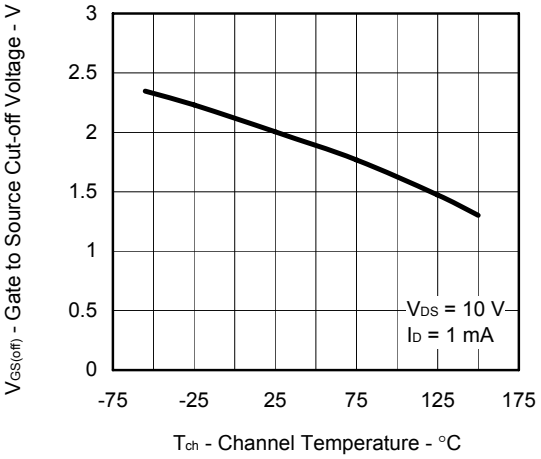
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



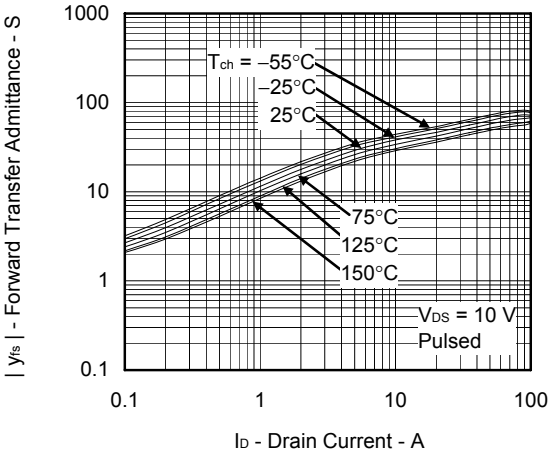
FORWARD TRANSFER CHARACTERISTICS



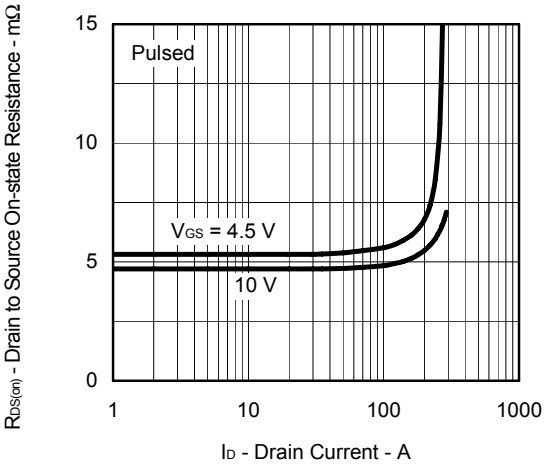
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



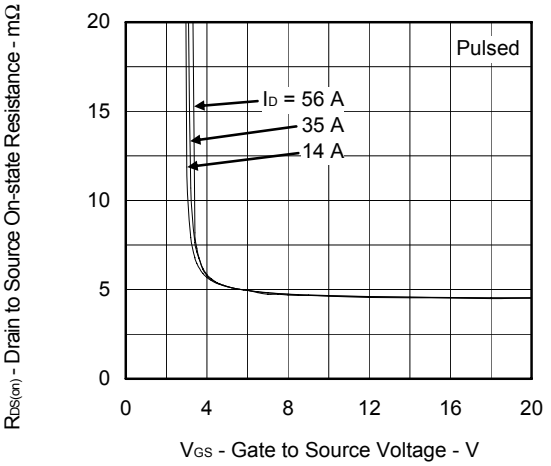
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



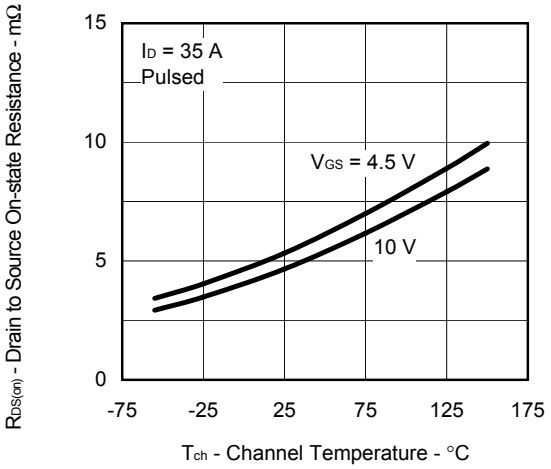
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



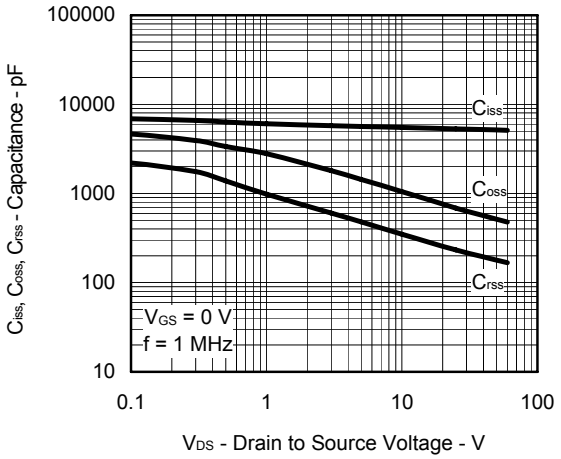
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



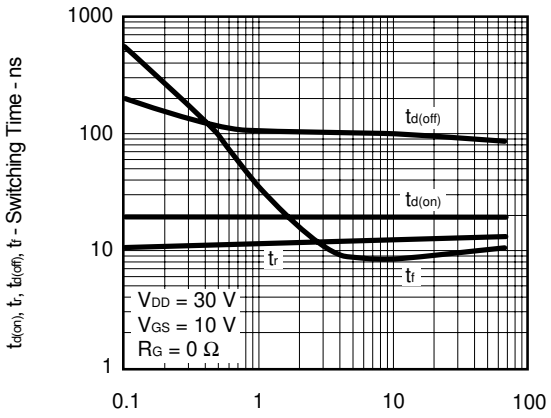
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



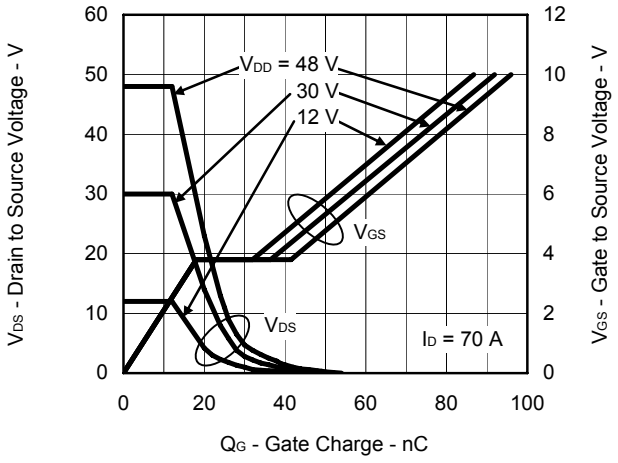
<R> CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



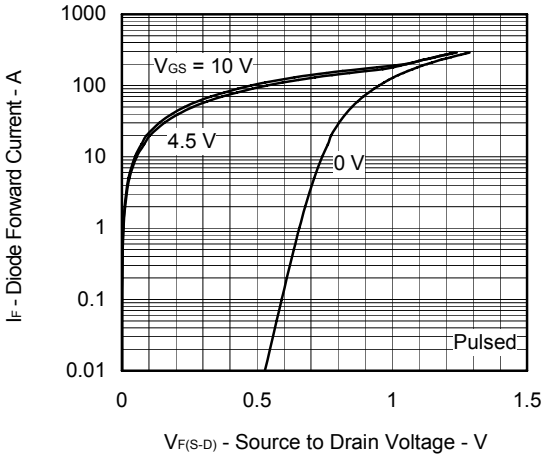
<R> SWITCHING CHARACTERISTICS



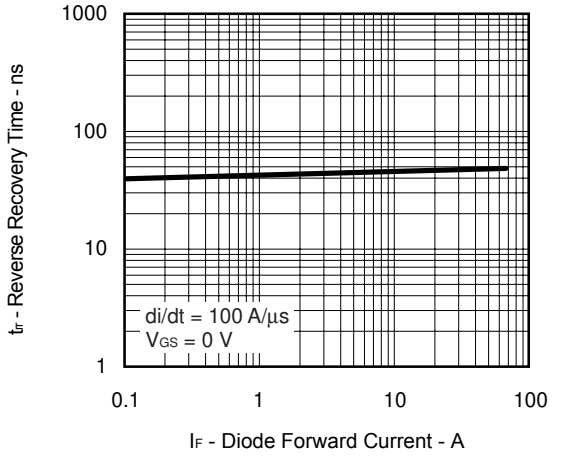
<R> DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

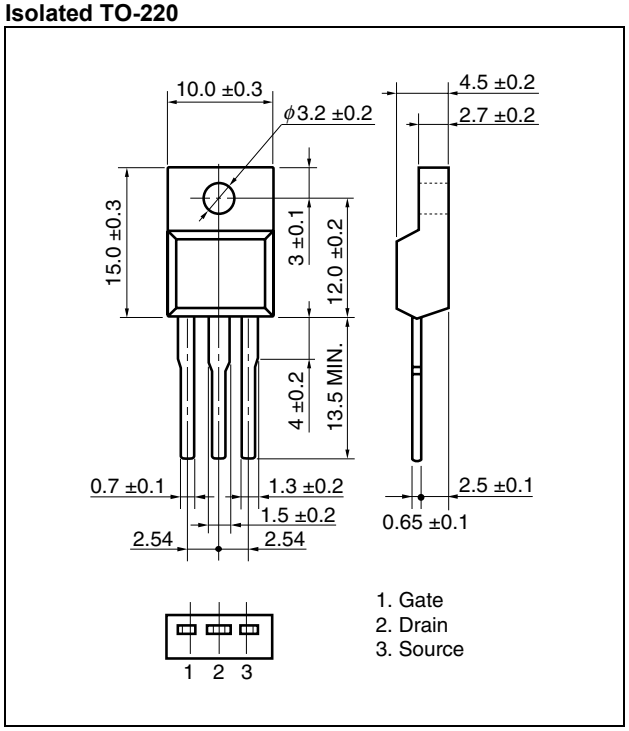


<R> REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

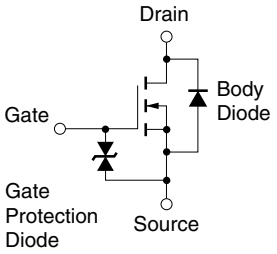


PACKAGE DRAWING (Unit: mm)

Isolated TO-220

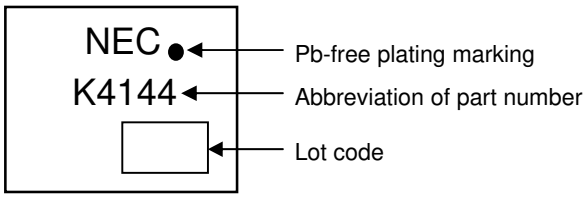


EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The 2SK4144 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Wave soldering	Maximum temperature (Solder temperature): 260°C or below Time: 10 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	THDWS
Partial heating	Maximum temperature (Pin temperature): 300°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P300

Caution Do not use different soldering methods together (except for partial heating).

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