

**FEATURES**

**Alias free: inherent antialias rejection high performance mode 102.5 dB, typical**  
**Excellent ac and dc performance**  
 108 dB dynamic range at ODR = 374 kSPS, FIR filter, typical  
 137 dB dynamic range at ODR = 10 SPS, sinc3 filter, typical  
 THD: -120 dB typical with 1 kHz input tone  
 Offset error drift: 0.7  $\mu\text{V}/^\circ\text{C}$  typical  
 Gain drift: 2 ppm/ $^\circ\text{C}$  typical  
 INL:  $\pm 2$  ppm of FSR typical  
**Dynamic range enhancement: 4:1 and 2:1 averaging mode**  
 126 dB, A weighted dynamic range  
**Resistive ADC and reference input**  
**Easy to sync: asynchronous sample rate converter**  
 Multidevice synchronization with one signal line  
 Programmable data rates from 0.01 kSPS to 1496 kSPS with resolution of 0.01 SPS  
 Option to control output data rate by external signal  
**Linear phase digital filter options**  
 Low ripple FIR filter: 32  $\mu\text{dB}$  pass-band ripple, dc to 161.942 kHz  
 Low latency sinc3 filter and sinc6 filter, dc to 391.5 kHz

Sinc3 filter with 50 Hz/60 Hz rejection  
 Crosstalk: 130.7 dBFS  
 Daisy-chaining  
 CRC error checking on data and SPI interface  
**Two power modes: high performance mode and low power mode**  
**Power supply: 4.5 V to 5.5 V and 1.65 V to 1.95 V**  
 1.8 V IOVDD level  
**External reference: 4.096 V or 5 V**  
 Crystal or external CMOS clock of 48 MHz  
 SPI or pin (standalone) configurable operation  
**Operating temperature range: 0°C to 85°C**  
 Available in **8 mm  $\times$  8 mm, 56-lead LFCSP** with exposed pad

**APPLICATIONS**

Electrical test and measurement  
 Audio test  
 3-phase power quality analysis  
 Control and hardware in loop verification  
 Sonars  
 Condition monitoring for predictive maintenance  
 Acoustic and material science research and development

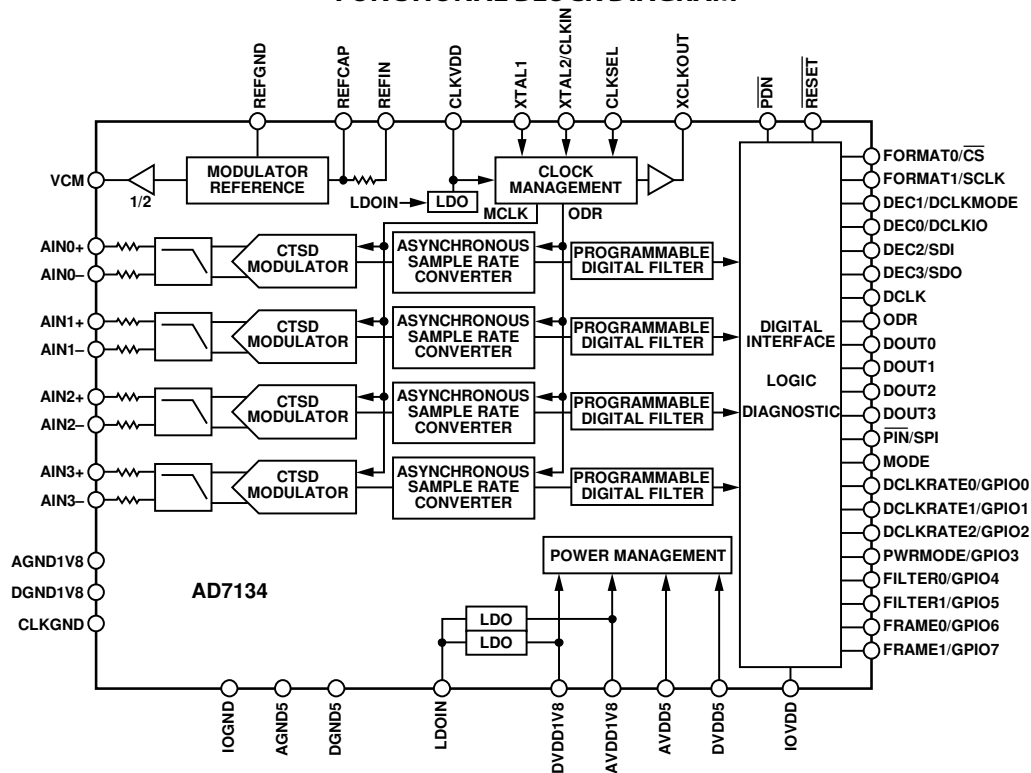
**FUNCTIONAL BLOCK DIAGRAM**


Figure 1.

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Rev. 0

**Document Feedback**

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## TABLE OF CONTENTS

|   |    |  |    |
|---|----|--|----|
| Features .....                                    | 1  | Programming Output Data Rate and Clock .....       | 46 |
| Applications .....                                | 1  | Programming Digital Filter .....                   | 49 |
| Functional Block Diagram .....                    | 1  | Programming Data Interface .....                   | 49 |
| Revision History .....                            | 2  | Power Modes .....                                  | 50 |
| General Description .....                         | 3  | Inherent Antialiasing Filter Modes .....           | 51 |
| Specifications .....                              | 4  | Dynamic Range Enhancement, Channel Averaging ..... | 52 |
| Timing Specifications .....                       | 10 | Calibration .....                                  | 53 |
| Absolute Maximum Ratings .....                    | 12 | Offset Calibration .....                           | 53 |
| Thermal Resistance .....                          | 12 | Gain Calibration .....                             | 53 |
| ESD Caution .....                                 | 12 | Applications Information .....                     | 54 |
| Pin Configuration and Function Descriptions ..... | 13 | Power Supply .....                                 | 54 |
| Typical Performance Characteristics .....         | 17 | Reference Noise Filtering .....                    | 54 |
| Terminology .....                                 | 26 | Multidevice Synchronization .....                  | 55 |
| Theory of Operation .....                         | 28 | Coherent Sampling .....                            | 55 |
| Continuous Time Sigma-Delta Modulator .....       | 28 | Low Latency Digital Control Loop .....             | 55 |
| Easy to Drive Input and Reference .....           | 28 | Automatic Gain Control .....                       | 56 |
| Inherent Antialiasing Filter (AAF) .....          | 29 | Front-End Design Examples .....                    | 56 |
| Analog Front-End Design Simplification .....      | 30 | Digital Interface .....                            | 58 |
| Noise Performance and Resolution .....            | 31 | SPI Interface .....                                | 58 |
| Circuit Information .....                         | 35 | Data Interface .....                               | 59 |
| Core Signal Chain .....                           | 35 | Minimum I/O Mode .....                             | 64 |
| Analog Inputs .....                               | 35 | Diagnostics .....                                  | 65 |
| VCM Output .....                                  | 35 | Internal Fuse Integrity Check .....                | 65 |
| Reference Input .....                             | 36 | Analog Input Overrange .....                       | 66 |
| Clock Input .....                                 | 36 | MCLK Counter .....                                 | 66 |
| XCLKOUT Output .....                              | 36 | SPI Interface Monitoring .....                     | 66 |
| Power Options .....                               | 37 | Memory Map Integrity Check .....                   | 66 |
| Reset .....                                       | 37 | ODR Input Frequency Check .....                    | 66 |
| Asynchronous Sample Rate Converter .....          | 37 | Digital Filter Overflow and Underflow .....        | 67 |
| Digital Filters .....                             | 39 | DCLK Error .....                                   | 67 |
| Quick Start Guide .....                           | 42 | GPIO Functionality .....                           | 68 |
| Standalone Mode .....                             | 43 | Pin Error Reporting .....                          | 68 |
| Low Latency Synchronous Data Acquisition .....    | 43 | Register Map (SPI Control) .....                   | 69 |
| Device Control .....                              | 44 | Register Details .....                             | 71 |
| Pin Control Mode .....                            | 44 | Outline Dimensions .....                           | 86 |
| SPI Control Mode .....                            | 45 | Ordering Guide .....                               | 86 |
| Multifunction Pins .....                          | 45 |  |    |
| Device Configuration .....                        | 46 |  |    |

## REVISION HISTORY

4/2020—Revision 0: Initial Version

## GENERAL DESCRIPTION

The AD7134 is a quad channel, low noise, simultaneous sampling, precision analog-to-digital converter (ADC) that delivers on functionality, performance, and ease of use.

Based on the continuous time sigma-delta (CTSD) modulation scheme, the AD7134 removes the traditionally required switched capacitor circuitry sampling preceding the  $\Sigma$ - $\Delta$  modulator, which leads to a relaxation of the ADC input driving requirement. The CTSD architecture also inherently rejects signals around the ADC aliasing frequency band, giving the device its inherent antialiasing capability, and removes the need for a complex external antialiasing filter.

The AD7134 has four independent converter channels in parallel, each with a CTSD modulator and a digital decimation and filtering path. The AD7134 enables simultaneous sampling of four separate signal sources, each supporting a maximum input bandwidth of 391.5 kHz and achieving tight phase matching between these four signal measurements. The high level of channel integration, together with its simplified analog front-end requirement, enables the AD7134 to provide a high density multichannel data acquisition solution in a small form factor.

The signal chain simplification property of the AD7134 also improves the system level performance through the reduction of noise, error, mismatch, and distortion that is normally introduced by the analog front-end circuitry.

The AD7134 offers excellent dc and ac performance. The bandwidth of each ADC channel ranges from dc to 391.5 kHz, making the device an ideal candidate for universal precision data acquisition solutions supporting a breadth of sensor types, from temperature and pressure to vibration and shock.

The AD7134 offers a large number of features and configuration options, giving the user the flexibility to achieve the optimal balance between bandwidth, noise, accuracy, and power for a given application.

An integrated asynchronous sample rate converter (ASRC) allows the AD7134 to precisely control the decimation ratio and, in turn, the output data rate (ODR) using interpolation and resampling techniques. The AD7134 supports a wide range of ODR frequencies, from 0.01 kSPS to 1496 kSPS with less than 0.01 SPS adjustment resolution, allowing the user to granularly vary sampling speed to achieve coherent sampling. The ODR value can be controlled through the ODR\_VAL\_INT\_x and ODR\_VAL\_FLT\_x registers (Register 0x16 to Register 0x1C, ASRC master mode), or using an external clock source (ASRC slave mode). The ASRC slave mode operation enables synchronous sampling between multiple AD7134 devices to a single system clock. The ASRC simplifies the clock distribution requirement within a medium bandwidth data acquisition system because it

no longer requires a high frequency, low jitter master clock from the digital back end to be routed to each ADC.

The ASRC acts as a digital filter and decimates the oversampled data from the  $\Sigma$ - $\Delta$  modulator to a lower rate to favor higher precision. The ADC data is then further processed by one of the AD7134 user-selectable digital filter profiles to further reject the out of band signals and noises, and reduce the data rate to the final desired ODR value.

The AD7134 offers three main digital filter profile options: a wideband low ripple filter with a brick wall frequency profile and an ODR range from 2.5 kSPS to 374 kSPS that is suitable for frequency domain analysis, a fast responding sinc3 filter with an ODR range from 0.01 kSPS to 1496 kSPS that is suitable for low latency time domain analysis and low frequency high dynamic range input types, and a balanced sinc6 filter with an ODR range from 2.5 kSPS to 1.496 MSPS, offering optimal noise performance and response time.

The AD7134 is also capable of performing on-board averaging between two or four of its input channels. The result is a near 3 dB, if two channels are combined, or 6 dB, if all four channels are combined, improvement in dynamic range while maintaining the bandwidth.

The AD7134 supports two device configuration schemes: serial peripheral interface (SPI) and hardware pin configuration (pin control mode). The SPI control mode offers access to all the features and configuration options available on the AD7134. SPI control mode also enables access to the on-board diagnostic features designed to enable a robust system design. Pin control mode offers the benefit of simplifying the device configuration, enabling the device to operate autonomously after power-up operating in a standalone mode.

In addition to the optional SPI, the AD7134 has a flexible and independent data interface for transmitting the ADC output data. The data interface can act as either a bus master or a slave with various clocking options to support multiple communication bus protocols. The data interface also supports daisy-chaining and an optional minimum input/output (I/O) mode designed to minimize the number of digital isolator channels required in isolated applications.

The AD7134 has an operating ambient temperature range from 0°C to 85°C. The device is housed in an 8 mm × 8 mm, 56-lead lead frame chip scale package (LFCSP).

Note that throughout this data sheet, multifunction pins, such as FORMAT1/SCLK, are referred to either by the entire pin name or by a single function of the pin, for example, SCLK, when only that function is relevant.

## SPECIFICATIONS

AVDD5 = DVDD5 = 4.5 V to 5.5 V, AVDD1V8 = DVDD1V8 = 1.65 V to 1.95 V, CLKVDD = 1.65 V to 1.95 V, LDOIN = 2.6 V to 5.5 V, IOVDD = 1.65 V to 1.95 V, CLKIN = 48 MHz, AGND5 = DGND5 = AGND1V8 = DGND1V8 = IOGND = CLKGND = 0 V, REFIN voltage ( $V_{REF}$ ) = 4.096 V, high performance mode, input common-mode voltage ( $V_{CM}$ ) = 2.048 V, wideband 0.433 Hz × ODR filter, Antialiasing 1 (AA1) mode, unless otherwise noted. Typical values are for  $T_A = 25^\circ\text{C}$ , AVDD5 = DVDD5 = 5 V, AVDD1V8 = DVDD1V8 = CLKVDD = 1.8 V, LDOIN = 5 V, IOVDD = 1.8 V, unless otherwise noted.

Table 1.

| Parameter   | Test Conditions/Comments  | Min                        | Typ   | Max     | Unit |
|---|---|----------------------------|-------|---------|------|
| ADC SPEED AND DATA OUTPUT   |   |                            |       |         |      |
| ODR   |   |                            |       |         |      |
| Wideband 0.10825 Hz × ODR and 0.433 Hz × ODR Filters <sup>1,2</sup> |   | 2.5                        |       | 374     | kSPS |
| Sinc6 Filter <sup>3</sup>   |   | 2.5                        |       | 1496    | kSPS |
| Sinc3 Filter <sup>4</sup>   |   | 0.01                       |       | 1496    | kSPS |
| −3 dB Bandwidth   |   |                            |       |         |      |
| Wideband 0.433 Hz × ODR Filter                                      |   | 1.08                       |       | 161.942 | kHz  |
| Wideband 0.10825 Hz × ODR Filter                                    |   | 0.27                       |       | 40.48   | kHz  |
| Sinc6 Filter  |   | 0.47                       |       | 278.4   | kHz  |
| Sinc3 Filter  |   | 0.003                      |       | 391.5   | kHz  |
| Data Output Coding  |   | Twos complement, MSB first |       |         |      |
| DYNAMIC PERFORMANCE   | More information is available in the Noise Performance and Resolution section |                            |       |         |      |
| Dynamic Range (DR)  | Shorted input   |                            |       |         |      |
| High Performance Mode   | ODR = 374 kSPS  | 105.7                      | 108   |         | dB   |
|   | ODR = 10 SPS, sinc3 filter  |                            | 137   |         | dB   |
|   | A weighted, 1 kHz input, −60 dBFS, ODR = 48 kSPS                              |                            | 120   |         | dB   |
|   | 2:1 channel averaging, A weighted, 1 kHz input, −60 dBFS, ODR = 48 kSPS       |                            | 123   |         | dB   |
|   | 4:1 channel averaging, A weighted, 1 kHz input, −60 dBFS, ODR = 48 kSPS       |                            | 126   |         | dB   |
| Low Power Mode  | ODR = 187 kSPS  | 102.7                      | 106   |         | dB   |
| Signal-to-Noise Ratio   | 1 kHz, −0.5 dBFS, sine wave input   |                            |       |         |      |
| High Performance Mode   | ODR = 374 kSPS  | 105.6                      | 107   |         | dB   |
| Low Power Mode  | ODR = 187 kSPS  | 105.3                      | 106   |         | dB   |
| Signal-to-Noise-and-Distortion Ratio (SINAD)                        | 1 kHz, −0.5 dBFS, sine wave input   |                            |       |         |      |
| High Performance Mode   | ODR = 374 kSPS  |                            | 106.5 |         | dB   |
| Low Power Mode  | ODR = 187 kSPS  |                            | 105.5 |         | dB   |
| Total Harmonic Distortion (THD)                                     | 1 kHz, −0.5 dBFS, sine wave input   |                            |       |         |      |
| High Performance Mode   |   |                            | −120  |         | dB   |
| Low Power Mode  |   |                            | −119  |         | dB   |
| Spurious-Free Dynamic Range <sup>5</sup> (SFDR)                     | 1 kHz, −0.5 dBFS, sine wave input   |                            |       |         |      |
| High Performance Mode   |   |                            | 125   |         | dBc  |
| Low Power Mode  |   |                            | 125   |         | dBc  |
| INTERMODULATION DISTORTION (IMD)                                    | With input tone at 9.7 kHz and 10.3 kHz                                       |                            |       |         |      |
|   | Second-order  |                            | −122  |         | dB   |
|   | Third-order   |                            | −125  |         | dB   |

| Parameter   | Test Conditions/Comments  | Min          | Typ         | Max          | Unit       |
|---|---|--------------|-------------|--------------|------------|
| ACCURACY  |   |              |             |              |            |
| Integral Nonlinearity (INL)                               | End point method<br>High performance mode   |              | ±2          |              | ppm of FSR |
|   | Low power mode  |              | ±2          |              | ppm of FSR |
| Offset Error <sup>6</sup>                                 | High performance mode   |              | ±100        | ±700         | μV         |
|   | Low power mode  |              | ±100        | ±700         | μV         |
| Offset Error Drift  | High performance mode   |              | 0.7         | 3.7          | μV/°C      |
|   | Low power mode  |              | 0.8         | 2.7          | μV/°C      |
| Gain Error <sup>6</sup>                                   | High performance mode, master mode  |              | 350         | 646          | ppm of FSR |
|   | Low power mode, master mode   |              | 150         | 390          | ppm of FSR |
| Gain Drift  |   |              | 2           | 5.4          | ppm/°C     |
| Voltage Noise   | 0.1 Hz to 10 Hz   |              | 1.01        |              | μV p-p     |
| ANALOG INPUTS   |   |              |             |              |            |
| Differential Input Voltage Range ( $V_{IN}$ )             | – $V_{REF}$ is the negative reference voltage and + $V_{REF}$ is the positive reference voltage | – $V_{REF}$  |             | + $V_{REF}$  | V          |
| Input Common-Mode Voltage Range ( $V_{CM}$ )              |   |              | $V_{REF}/2$ | $AV_{DD5}/2$ | V          |
| Input Current   |   |              | 317         |              | μA/V       |
| Input Current Drift                                       |   |              | 8.3         |              | nA/V/°C    |
| Differential Input Resistance                             |   |              | 6.25        |              | kΩ         |
| VCM PIN   |   |              |             |              |            |
| Output Voltage  |   | $V_{REF}/20$ |             | $AV_{DD5}/2$ | V          |
| Load Regulation ( $\Delta V_{OUT}/\Delta I_L$ )           |   |              | 313         |              | μV/mA      |
| Voltage Regulation ( $\Delta V_{OUT}/\Delta V_{AVDD5V}$ ) |   |              | 993         |              | μV/V       |
| Short-Circuit Current                                     |   |              | 45          |              | mA         |
| Loading Capacitance                                       |   |              |             | 200          | pF         |
| Additive Voltage Noise Density                            |   |              | 70          |              | nV/√Hz     |
| EXTERNAL REFERENCE  |   |              |             |              |            |
| REFIN Voltage ( $V_{REF}$ )                               | REFIN to REFGND high performance mode   |              | 4.096 or 5  |              | V          |
|   | REFIN to REFGND low power mode  |              | 4.096 or 5  |              | V          |
| REFIN Current   | All channels on, high performance mode  |              | 5.85        |              | mA         |
|   | All channels on, low power mode   |              | 3.22        |              | mA         |
|   | One channel on, high performance mode   |              | 1.53        |              | mA         |
|   | One channel on, low power mode  |              | 0.9         |              | mA         |
|   | REFIN off   |              | 0.5         |              | μA         |
| REFIN Current Drift                                       |   |              | 40          |              | nA/V/°C    |
| REFIN Resistance  | All channels on   |              | 0.7         |              | kΩ         |
|   | One channel on  |              | 2.66        |              | kΩ         |
|   | All channels on, low power mode   |              | 1.27        |              | kΩ         |
|   | One channel on, low power mode  |              | 4.79        |              | kΩ         |
| MODULATOR MAGNITUDE RESPONSE                              |   |              |             |              |            |
| High Performance Mode                                     | At 100 kHz, ODR = 374 kSPS  |              | –0.0202     |              | dB         |
|   | At 20 kHz, ODR = 374 kSPS   |              | –0.0024     |              | dB         |
| Low Power Mode  | At 50 kHz, ODR = 187 kSPS   |              | –0.0122     |              | dB         |
|   | At 20 kHz, ODR = 187 kSPS   |              | –0.00189    |              | dB         |

| Parameter                                      | Test Conditions/Comments   | Min | Typ           | Max      | Unit  |
|--|--|-----|---------------|----------|-------|
| SYNCHRONIZATION                                | At 20 kHz  |     |               |          |       |
| Channel to Channel Phase Matching <sup>7</sup> |  |     | 1.57          | 3.3      | ns    |
| Channel to Channel Phase Matching Drift        |  |     | 4.17          |          | ps/°C |
| Device to Device Phase Matching <sup>8</sup>   | ODR = 1496 kSPS  |     | 10            |          | ns    |
| DIGITAL FILTER RESPONSE                        |  |     |               |          |       |
| Low Ripple Wideband                            |  |     |               |          |       |
| Group Delay                                    |  |     | 39.8/ODR      |          | sec   |
| Settling Time                                  |  |     | 79.6/ODR      |          | sec   |
| Pass-Band Ripple                               |  |     | 32            |          | µdB   |
| Pass-Band Frequency (f <sub>PASS</sub> )       |  |     |               |          |       |
| Wideband 0.433 Hz × ODR Filter                 | ±32 µdB pass band  |     | 0.4 × ODR     |          | Hz    |
|  | −0.1 dB pass band  |     | 0.401 × ODR   |          | Hz    |
|  | −3 dB bandwidth  |     | 0.433 × ODR   |          | Hz    |
| Wideband 0.10825 Hz × ODR Filter               | ±32 µdB pass band  |     | 0.1 × ODR     |          | Hz    |
|  | −0.1 dB pass band  |     | 0.101 × ODR   |          | Hz    |
|  | −3 dB bandwidth  |     | 0.10825 × ODR |          | Hz    |
| Stop Band Frequency (f <sub>STOP</sub> )       |  |     |               |          |       |
| Wideband 0.433 Hz × ODR Filter                 |  |     | 0.499 × ODR   |          | Hz    |
| Wideband 0.10825 Hz × ODR Filter               |  |     | 0.2 × ODR     |          | Hz    |
| Stop Band Attenuation                          |  |     | 110           |          | dB    |
| Sinc6  |  |     |               |          |       |
| Group Delay                                    |  |     | 3.25/ODR      |          |       |
| Settling Time                                  |  |     | 6.5/ODR       |          |       |
| Pass Band                                      | −3 dB bandwidth  |     | 0.1861 × ODR  |          | sec   |
| Sinc3  |  |     |               |          |       |
| Group Delay (GD)                               | Latency  |     | 1.75/ODR      |          | sec   |
| Settling Time                                  | Complete settling  |     | 3.5/ODR       |          | sec   |
| Pass Band                                      | −3 dB bandwidth  |     | 0.2617 × ODR  |          | sec   |
| Attenuation                                    |  |     |               |          |       |
| At 50 Hz                                       | 50 SPS, 50 Hz ± 1 Hz   |     | 102           |          | dB    |
| At 60 Hz                                       | 60 SPS, 60 Hz ± 1 Hz   |     | 106           |          | dB    |
| At 50 Hz, 60 Hz                                | 10 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz   |     | 102           |          | dB    |
| At 50 Hz, 60 Hz                                | 50 SPS, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz, sinc3 rejection, and 50 Hz/60 Hz rejection filter <sup>1</sup> |     | 67            |          | dB    |
| COMBINED RESPONSE                              |  |     |               |          |       |
| Overall Group Delay                            | Sinc3 filter, slave gated mode   |     |               | 8/ODR    | sec   |
|  | Sinc6 filter, slave gated mode   |     |               | 10.5/ODR | sec   |
| REJECTION                                      | High performance mode  |     |               |          |       |
| Power Supply Rejection Ratio                   |  |     |               |          |       |
| DC   |  |     |               |          |       |
| AVDD5  |  |     | 101.8         |          | dB    |
| DVDD5  |  |     | 80.4          |          | dB    |

| Parameter   | Test Conditions/Comments  | Min           | Typ   | Max           | Unit |
|---|---|---------------|-------|---------------|------|
| AVDD1V8   |   |               | 87.2  |               | dB   |
| DVDD1V8   |   |               | 100   |               | dB   |
| IOVDD   |   |               | 102   |               | dB   |
| LDOIN   |   |               | 116.6 |               | dB   |
| CLKVDD  |   |               | 61    |               | dB   |
| Power Supply Rejection AC                         | 100 mV p-p, 1 MHz signal on supply with no decoupling capacitor, value with respect to full-scale input |               |       |               |      |
| AVDD5   |   |               | 101   |               | dB   |
| DVDD5   |   |               | 102   |               | dB   |
| AVDD1V8   |   |               | 104   |               | dB   |
| DVDD1V8   |   |               | 101   |               | dB   |
| IOVDD   |   |               | 114   |               | dB   |
| CLKVDD  |   |               | 103   |               | dB   |
| Common-Mode Rejection Ratio (CMRR)                | 100 mV p-p on $V_{CM}$ with no decoupling capacitor   |               |       |               |      |
| DC  |   |               | 78.4  |               | dB   |
| AC  | Up to 10 kHz  |               | 74.5  |               | dB   |
| Crosstalk   | -0.5 dBFS, 1 kHz input on adjacent channels   |               | 130.7 |               | dBFS |
| Input Signal Alias Rejection (AA <sub>REJ</sub> ) |   |               |       |               |      |
| High Performance Mode                             | -6 dBFS output of band tone from master clock (MCLK) - 160 kHz to MCLK + 160 kHz, AA1 mode              |               | 85.4  |               | dB   |
|   | -6 dBFS output of band tone from MCLK - 160 kHz to MCLK + 160 kHz, Antialiasing 2 (AA2) mode            |               | 102.5 |               | dB   |
| Low Power Mode                                    | -6 dBFS output of band tone from MCLK - 80 kHz to MCLK + 80 kHz, AA1 mode                               |               | 87.4  |               | dB   |
|   | -6 dBFS output of band tone from MCLK - 80 kHz to MCLK + 80 kHz, AA2 mode                               |               | 97.2  |               | dB   |
| EXTERNAL CLOCK INPUT                              |   |               |       |               |      |
| Frequency   |   | 47.9          | 48    | 48.1          | MHz  |
| Duty Cycle  |   | 40            | 50:50 | 60            | %    |
| Input Voltage High                                |   | 0.65 × CLKVDD |       |               | V    |
| Input Voltage Low                                 |   |               |       | 0.35 × CLKVDD | V    |
| Input Capacitance                                 |   |               | 10    |               | pF   |
| CRYSTAL OSCILLATOR                                |   |               |       |               |      |
| Frequency   | ±100 ppm  |               | 48    |               | MHz  |
| Start-Up Time                                     |   |               | 4.4   |               | ms   |
| CLKSEL INPUT LOGIC                                |   |               |       |               |      |
| Input High Voltage ( $V_{INH}$ )                  |   | 0.7 × IOVDD   |       |               | V    |
| Input Low Voltage ( $V_{INL}$ )                   |   |               |       | 0.3 × IOVDD   | V    |
| Leakage Currents                                  |   | -1            |       | +1            | μA   |
| XCLKOUT PIN                                       |   |               |       |               |      |
| Output Frequency                                  |   |               | 48    |               | MHz  |
| Rise Time/Fall Time (20% to 80%)                  | 45 pF load  |               | 0.85  |               | ps   |
| Duty Cycle  | External clock input duty cycle = 50:50   |               | 53.8  |               | %    |
| Output Voltage High                               | Source current ( $I_{SOURCE}$ ) = 100 μA  | CLKVDD - 0.2  |       |               | V    |
| Output Voltage Low                                | Sink current ( $I_{SINK}$ ) = 100 μA  |               |       | 0.2           | V    |
| ODR PIN   |   |               |       |               |      |
| Output Frequency                                  |   | 0.01          |       | 1496          | kHz  |
| Output Rise Time/Fall Time (20% to 80%)           | 45 pF load  |               | 2.8   |               | ns   |
| Output Voltage High                               | $I_{SOURCE}$ = 100 μA   | IOVDD - 0.2   |       |               | V    |

| Parameter                               | Test Conditions/Comments                             | Min                | Typ   | Max                | Unit    |  |        |     |  |
|---|--|--------------------|-------|--------------------|---------|--|--------|-----|--|
| Output Voltage Low                      | $I_{SINK} = 100 \mu A$                               | 0.01               |       | 0.2                | V       |  |        |     |  |
| Input Frequency ( $f_{IN}$ )            |  |                    |       | 1496               | kHz     |  |        |     |  |
| $V_{INH}$                               |  |                    |       | $0.7 \times IOVDD$ | V       |  |        |     |  |
| $V_{INL}$                               |  |                    |       | $0.3 \times IOVDD$ | V       |  |        |     |  |
| Input Capacitance                       | Pin configured as input                              |                    | 10    |                    | pF      |  |        |     |  |
| DCLK PIN                                | 45 pF load   | 2.93               |       | 48000              | kHz     |  |        |     |  |
| Output Frequency                        |  |                    |       |                    |         |  |        |     |  |
| Output Rise Time/Fall Time (20% to 80%) |  |                    |       |                    |         | 2.8  | ns     |     |  |
| Output Duty Cycle                       |  |                    |       |                    |         | 50:50  | %      |     |  |
| Output Voltage High                     |  |                    |       |                    |         | $IOVDD - 0.2$  | V      |     |  |
| Output Voltage Low                      |  |                    |       |                    |         |  | 0.2    | V   |  |
| $f_{IN}$                                |  |                    |       |                    |         |  | 50,000 | kHz |  |
| $V_{INH}$                               |  |                    |       |                    |         | $0.7 \times IOVDD$   | V      |     |  |
| $V_{INL}$                               |  | $0.3 \times IOVDD$ | V     |                    |         |  |        |     |  |
| Input Capacitance                       | Pin configured as input                              |                    | 10    |                    | pF      |  |        |     |  |
| LOGIC INPUTS                            |  | $0.7 \times IOVDD$ |       |                    | V       |  |        |     |  |
| $V_{INH}$                               |  |                    |       |                    |         |  |        |     |  |
| $V_{INL}$                               |  |                    |       |                    |         |  |        |     |  |
| Leakage Currents                        |  | -10                |       | +10                | $\mu A$ |  |        |     |  |
| LOGIC OUTPUTS                           | $I_{SOURCE} = 100 \mu A$                             | $IOVDD - 0.2$      |       |                    | V       |  |        |     |  |
| Output High Voltage ( $V_{OH}$ )        |  |                    |       |                    |         |  |        |     |  |
| Output Low Voltage ( $V_{OL}$ )         | $I_{SINK} = 100 \mu A$                               |                    |       | 0.2                | V       |  |        |     |  |
| INTEGRATED LOW DROPOUT (LDO) REGULATOR  |  | 2.6                | 1.85  | 5.5                | V       |  |        |     |  |
| Output Voltage                          |  |                    |       |                    |         |  |        |     |  |
| Input Voltage                           |  |                    |       |                    | V       |  |        |     |  |
| POWER SUPPLY VOLTAGE                    |  |                    |       |                    | V       |  |        |     |  |
| AVDD5 to AGND5                          |  |                    |       |                    |         |  |        |     |  |
| DVDD5 to DGND5                          |  |                    |       |                    |         |  |        |     |  |
| AVDD5 to AGND5                          |  |                    |       |                    |         | $V_{REF} = 5 V$  |        |     |  |
| DVDD5 to DGND5                          |  |                    |       |                    |         | $V_{REF} = 5 V$  |        |     |  |
| DVDD1V8 to DGND                         |  |                    |       |                    |         |  |        |     |  |
| AVDD1V8 to AGND1V8                      |  |                    |       |                    |         |  |        |     |  |
| AVDD1V8 to AGND1V8                      |  |                    |       |                    |         | $V_{REF} = 5 V$  |        |     |  |
| DVDD1V8 to DGND                         |  |                    |       |                    |         | $V_{REF} = 5 V$  |        |     |  |
| IOVDD to IOGND                          |  |                    |       |                    |         |  |        |     |  |
| CLKVDD to CLKGND                        |  |                    |       |                    |         |  |        |     |  |
| CLKVDD to CLKGND                        |  |                    |       |                    |         | $V_{REF} = 5 V$  |        |     |  |
| POWER SUPPLY CURRENT                    |  |                    |       |                    |         | 4 channels active, internal LDO regulator bypassed, XCLKOUT disabled |        |     |  |
| High Performance Mode                   |  |                    |       |                    |         |  |        |     |  |
| AVDD5                                   | 8.2  | 10.3               | mA    |                    |         |  |        |     |  |
| DVDD5                                   | 38.6   | 44.8               | mA    |                    |         |  |        |     |  |
| AVDD1V8                                 | 56   | 73.9               | mA    |                    |         |  |        |     |  |
| DVDD1V8                                 | Sinc3 filter, ODR = 1496 kSPS                        | 60                 | 70.6  | mA                 |         |  |        |     |  |
|   | Sinc6 filter, ODR = 1496 kSPS                        | 60.9               | 71.8  | mA                 |         |  |        |     |  |
|   | Wideband $0.433 \text{ Hz} \times \text{ODR}$ filter | 90                 | 105.5 | mA                 |         |  |        |     |  |
| IOVDD                                   |  | 2.25               | 3.17  | mA                 |         |  |        |     |  |
| CLKVDD                                  |  | 2.8                | 3.53  | mA                 |         |  |        |     |  |
| Low Power Mode                          | ODR = 187 kSPS                                       |                    |       |                    |         |  |        |     |  |
| AVDD5                                   |  | 8.2                | 10.3  | mA                 |         |  |        |     |  |
| DVDD5                                   |  | 14.1               | 16.5  | mA                 |         |  |        |     |  |
| AVDD1V8                                 |  | 51                 | 69    | mA                 |         |  |        |     |  |



| Parameter               | Test Conditions/Comments  | Min | Typ  | Max  | Unit |
|-------------------------|---|-----|------|------|------|
| DVDD1V8                 | Sinc3 filter, ODR = 1496 kSPS   |     | 30.6 | 36   | mA   |
|                         | Sinc6 filter, ODR = 1496 kSPS   |     | 38.5 | 45.2 | mA   |
|                         | Wideband 0.433 Hz × ODR filter  |     | 48.5 | 56.8 | mA   |
| IOVDD                   |   |     | 1.27 | 1.7  | mA   |
| CLKVDD                  |   |     | 1.89 | 2.3  | mA   |
| TOTAL POWER CONSUMPTION | External LDO mode: AVDD5 = DVDD5 = 5 V, AVDD1V8 = DVDD1V8 = CLKVDD = IOVDD = LDOIN = 1.8 V, internal LDO regulator bypassed, XCLKOUT disabled |     |      |      |      |
| High Performance Mode   | ODR = 374 kSPS, wideband 0.433 Hz × ODR filter  |     |      |      |      |
|                         | 4 channels active   |     | 504  | 540  | mW   |
|                         | 1 channel active  |     | 201  |      | mW   |
|                         | 2:1 averaging   |     | 472  |      | mW   |
|                         | 4:1 averaging   |     | 450  |      | mW   |
|                         | ODR = 2.5 kSPS, 4 channels active   |     | 418  |      | mW   |
|                         | ODR = 1496 kSPS, 4 channels active, sinc3 filter  |     | 446  |      | mW   |
| Low Power Mode          | ODR = 187 kSPS, wideband 0.433 Hz × ODR filter  |     |      |      |      |
|                         | 4 channels active   |     | 297  | 386  | mW   |
|                         | 1 channel active  |     | 121  |      | mW   |
|                         | 2:1 averaging   |     | 288  |      | mW   |
|                         | 4:1 averaging   |     | 254  |      | mW   |
|                         | ODR = 2.5 kSPS, 4 channels active   |     | 260  |      | mW   |
|                         | ODR = 1496 kSPS, 4 channels active, sinc3 filter  |     | 285  |      | mW   |
| High Performance Mode   | Internal LDO regulator mode: AVDD5 = DVDD5 = 5 V, LDOIN = 2.6 V, XCLKOUT disabled   |     |      |      |      |
|                         | ODR = 270 kSPS, wideband 0.433 Hz × ODR filter  |     |      |      |      |
|                         | 4 channels active   |     | 593  |      | mW   |
|                         | 1 channel active  |     | 246  |      | mW   |
|                         | 2:1 averaging   |     | 555  |      | mW   |
|                         | 4:1 averaging   |     | 530  |      | mW   |
|                         | ODR = 2.5 kSPS, 4 channels active   |     | 484  |      | mW   |
| Low Power Mode          | ODR = 1496 kSPS, 4 channels active, sinc3 filter  |     | 547  |      | mW   |
|                         | ODR = 187 kSPS, wideband 0.433 Hz × ODR filter  |     |      |      |      |
|                         | 4 channels active   |     | 386  |      | mW   |
|                         | 1 channel active  |     | 147  |      | mW   |
|                         | 2:1 averaging   |     | 356  |      | mW   |
|                         | 4:1 averaging   |     | 334  |      | mW   |
|                         | ODR = 2.5 kSPS, 4 channels active   |     | 316  |      | mW   |
| Full Power-Down Mode    | ODR = 1496 kSPS, 4 channels active, sinc3 filter  |     | 355  |      | mW   |
|                         |   |     | 1    |      | mW   |
| Sleep Mode              |   |     | 15   |      | mW   |

<sup>1</sup> For internal LDO regulator mode, the maximum ODR supported for wideband FIR filters is 270 kSPS.

<sup>2</sup> For slave mode, the maximum ODR supported for wideband FIR filters is 365 kSPS.

<sup>3</sup> For slave mode, the maximum ODR supported for the sinc6 filter is 1460 kSPS.

<sup>4</sup> For slave mode, the maximum ODR supported for the sinc3 filter is 1460 kSPS.

<sup>5</sup> Excluding the first five harmonics.

<sup>6</sup> Following a full system calibration, the offset error and the gain error are in the order of the noise for the programmed output data rate selected. The gain error is a function of the output data rate in slave mode. Therefore, a gain error calibration is needed when the output data rate is changed. It is recommended to perform a periodic system calibration to stop aging related drifts.

<sup>7</sup> Between any two channels on the same device.

<sup>8</sup> Between any two channels on any two devices. SPI slave mode with DCLK as gated input only with the DIG\_IF\_RESET SPI write issued simultaneously to both devices.

## TIMING SPECIFICATIONS

AVDD5 = DVDD5 = 4.5 V to 5.5 V, AVDD1V8 = DVDD1V8 = 1.65 V to 1.95 V, CLKVDD = 1.65 V to 1.95 V, IOVDD = 1.65 V to 1.95 V, CLKIN = 48 MHz, AGND5 = DGND5 = AGND1V8 = DGND1V8 = IOGND = CLKGND = 0 V,  $T_A = 0^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 2. Device Clock Timing**

| Parameter           | Description  | Test Conditions/Comments         | Min | Typ                   | Max                 | Unit |
|---------------------|--|----------------------------------|-----|-----------------------|---------------------|------|
| $f_{\text{SYSCLK}}$ | System clock frequency   |                                  |     | 48                    |                     | MHz  |
| MCLK                | Master clock   | High performance mode            |     | $f_{\text{SYSCLK}}/2$ |                     | Hz   |
|                     |  | Low power mode                   |     | $f_{\text{SYSCLK}}/4$ |                     | Hz   |
| $f_{\text{DIGCLK}}$ | Internal digital clock ( $t_{\text{DIGCLK}} = 1/f_{\text{DIGCLK}}$ ) |                                  |     | $f_{\text{SYSCLK}}/2$ |                     | Hz   |
| $f_{\text{DCLK}}$   | Data Interface clock ( $t_{\text{DCLK}} = 1/f_{\text{DCLK}}$ )       | DCLK as output, SPI control mode |     |                       | $f_{\text{SYSCLK}}$ | MHz  |
|                     |  | DCLK as output, pin control mode |     |                       | $f_{\text{SYSCLK}}$ | MHz  |
|                     |  | DCLK as input                    |     |                       | 50                  | MHz  |
| $f_{\text{SCLK}}$   | SPI clock rate ( $t_{\text{SCLK}} = 1/f_{\text{SCLK}}$ )             |                                  |     |                       | 50                  | MHz  |

The signal on DOUTx is driven out on the rising edge of the DCLK.  $t_{\text{ODR\_PERIOD}}$  is  $1/\text{ODR}$ . See Figure 2.

**Table 3. Data Interface Timing with Gated DCLK**

| Parameter | Description                                    | Test Conditions/Comments                              | Min                          | Typ | Max                              | Unit |
|-----------|--|---|------------------------------|-----|----------------------------------|------|
| $t_1$     | ODR high time                                  | Master mode, $t_{\text{DCLK}} > t_{\text{DIGCLK}}$    | $2.5 \times t_{\text{DCLK}}$ |     | $3.5 \times t_{\text{DCLK}}$     | ns   |
|           |  | Master mode, $t_{\text{DCLK}} \leq t_{\text{DIGCLK}}$ | $3 \times t_{\text{DIGCLK}}$ |     | $3 \times t_{\text{DIGCLK}} + 4$ | ns   |
|           |  | Slave mode  | $3 \times t_{\text{DIGCLK}}$ |     |                                  | ns   |
| $t_2$     | ODR low time                                   | Slave mode  | $3 \times t_{\text{DIGCLK}}$ |     |                                  | ns   |
| $t_3$     | ODR falling edge to DCLK rising edge           | Master mode   | $t_{\text{DCLK}} - 2$        |     |                                  | ns   |
|           |  | Slave mode  | 8                            |     |                                  | ns   |
| $t_4$     | Last data DCLK falling edge to ODR rising edge | Master mode   | $0.5 \times t_{\text{DCLK}}$ |     |                                  | ns   |
|           |  | Slave mode  | $2 \times t_{\text{DCLK}}$   |     |                                  | ns   |
| $t_5$     | DCLK rising to DOUTx invalid                   | Master mode   | -4                           |     |                                  | ns   |
|           |  | Slave mode  | 0                            |     |                                  | ns   |
| $t_6$     | DCLK rising to DOUTx valid                     | Master mode   | 0                            |     | 3                                | ns   |
|           |  | Slave mode  |                              |     | 8.2                              | ns   |
| $t_7$     | DCLK low time                                  |   | $t_{\text{DCLK}}/2 - 1$      |     |                                  | ns   |
| $t_8$     | DCLK high time                                 |   | $t_{\text{DCLK}}/2 - 1$      |     |                                  | ns   |

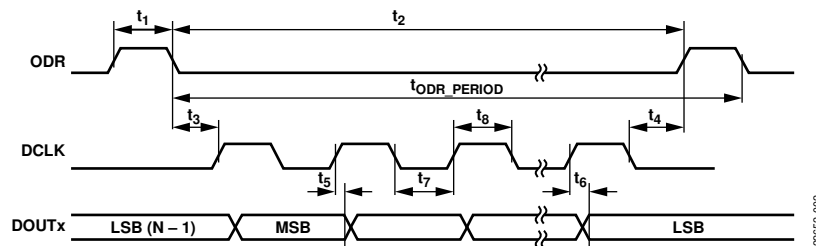


Figure 2. Timing Diagram of Data Interface with Gated DCLK

Signal on DOUTx is driven out on the rising edge of DCLK. See Figure 3.

Table 4. Data Interface Timing with Free Running DCLK

| Parameter       | Description                         | Test Conditions/Comments                             | Min                      | Typ | Max   | Unit |
|-----------------|-------------------------------------|--|--------------------------|-----|---|------|
| t <sub>9</sub>  | ODR high time                       | Master mode, t <sub>DCLK</sub> > t <sub>DIGCLK</sub> | 2.5 × t <sub>DCLK</sub>  |     | 3.5 × t <sub>DCLK</sub> - t <sub>DIGCLK</sub> + 4 | ns   |
|                 |                                     | Master mode, t <sub>DCLK</sub> ≤ t <sub>DIGCLK</sub> | 3 × t <sub>DIGCLK</sub>  |     | 3 × t <sub>DIGCLK</sub> + 4                       | ns   |
|                 |                                     | Slave mode, t <sub>DCLK</sub> > t <sub>DIGCLK</sub>  | 3 × t <sub>DCLK</sub>    |     |   | ns   |
| t <sub>10</sub> | ODR low time                        | Slave mode, t <sub>DCLK</sub> ≤ t <sub>DIGCLK</sub>  | 3 × t <sub>DIGCLK</sub>  |     |   | ns   |
|                 |                                     | Slave mode, t <sub>DCLK</sub> > t <sub>DIGCLK</sub>  | 3 × t <sub>DCLK</sub>    |     |   | ns   |
|                 |                                     | Slave mode, t <sub>DCLK</sub> ≤ t <sub>DIGCLK</sub>  | 3 × t <sub>DIGCLK</sub>  |     |   | ns   |
| t <sub>11</sub> | DCLK rising edge to ODR rising edge | Slave mode   | t <sub>DCLK</sub> /2     |     |   | ns   |
| t <sub>12</sub> | ODR rising edge to DCLK rising edge | Slave mode   | t <sub>DCLK</sub> /2     |     |   | ns   |
| t <sub>13</sub> | ODR sampled high to DOUTx active    |  | 3 × t <sub>DCLK</sub>    |     | 3 × t <sub>DCLK</sub> + 4                         |      |
| t <sub>14</sub> | DCLK rising to DOUTx invalid        | Master mode  | -4                       |     |   | ns   |
| t <sub>15</sub> | DCLK rising to DOUTx valid          | Master mode  | 0                        |     | 2   | ns   |
|                 |                                     | Slave mode   |                          |     | 3   | ns   |
| t <sub>16</sub> | DCLK low time                       |  | t <sub>DCLK</sub> /2 - 1 |     |   | ns   |
| t <sub>17</sub> | DCLK high time                      |  | t <sub>DCLK</sub> /2 - 1 |     |   | ns   |

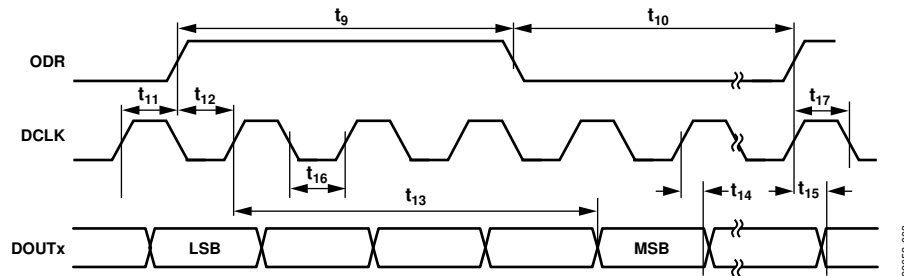


Figure 3. Timing Diagram of Data Interface with Free Running DCLK

SDI is sampled on the rising edge of SCLK. SDO is driven out on the falling edge of SCLK. See Figure 4.

Table 5. SPI Interface Timing

| Parameter       | Description  | Min                        | Typ | Max | Unit |
|-----------------|--|----------------------------|-----|-----|------|
| t <sub>18</sub> | $\overline{CS}$ falling to data out active           | 0                          |     | 7   | ns   |
| t <sub>19</sub> | SCLK falling edge to SDO valid                       |                            |     | 8   | ns   |
| t <sub>20</sub> | SCLK low time  | t <sub>SCLK</sub> /2 - 1   |     |     | ns   |
| t <sub>21</sub> | SDI setup time                                       | 2                          |     |     | ns   |
| t <sub>22</sub> | SDI hold time  | 2                          |     |     | ns   |
| t <sub>23</sub> | SDO hold time after SCLK falling                     |                            |     | 7   | ns   |
| t <sub>24</sub> | SCLK high time                                       | t <sub>SCLK</sub> /2 - 1   |     |     | ns   |
| t <sub>25</sub> | Last SCLK rising edge to $\overline{CS}$ rising edge | t <sub>SCLK</sub>          |     |     | ns   |
| t <sub>26</sub> | $\overline{CS}$ high time                            | 0.9 × t <sub>SCLK</sub> /2 |     |     | ns   |
| t <sub>27</sub> | $\overline{CS}$ falling edge to SCLK rising edge     | 9                          |     |     | ns   |

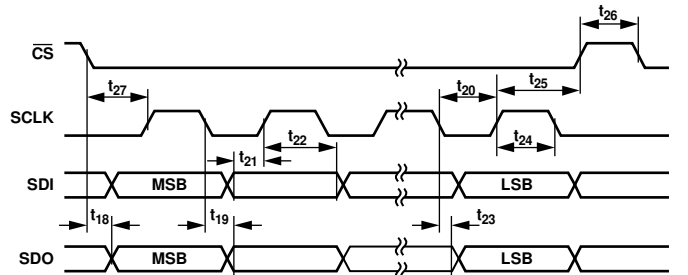


Figure 4. SPI Interface Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

Table 6.

| Parameter  | Rating  |
|--|---|
| AVDD5 to AGND5   | −0.3 V to +6 V  |
| DVDD5 to DGND5   | −0.3 V to +6 V  |
| AVDD1V8 to AGND1V8                                       | −0.3 V to 2.2 V or LDOIN + 0.3 V (whichever is lower) |
| DVDD1V8 to DGND1V8                                       | −0.3 V to 2.2 V or LDOIN + 0.3 V (whichever is lower) |
| CLKVDD to CLKGND   | −0.3 V to 2.2 V or LDOIN + 0.3 V (whichever is lower) |
| IOVDD to IOGND   | −0.3 V to +2.2 V                                      |
| DGND5 to AGND5   | −0.3 V to +0.3 V                                      |
| AGND1V8 to AGND5   | −0.3 V to +0.3 V                                      |
| DGND1V8 to AGND5   | −0.3 V to +0.3 V                                      |
| IOGND to AGND5   | −0.3 V to +0.3 V                                      |
| CLKGND to AGND5  | −0.3 V to +0.3 V                                      |
| LDOIN to AGND5   | AVDD1V8 − 0.3 V to 6 V                                |
| AINx± Inputs to AGND5                                    | −0.3 V to AVDD5 + 0.3 V                               |
| REFIN to AGND5   | −0.3 V to AVDD5 + 0.3 V                               |
| REFCAP to AGND5  | −0.3 V to AVDD5 + 0.3 V                               |
| REFGND to AGND5  | −0.3 V to +0.3 V                                      |
| Digital I/O Pins to IOGND                                | −0.3 V to IOVDD + 0.3 V                               |
| XCLKOUT, XTAL2/CLKIN, and XTAL1 to CLKGND                | −0.3 V to CLKVDD + 0.3 V                              |
| Operating Ambient Temperature Range                      | 0°C to 85°C   |
| Storage Temperature Range                                | −65°C to +150°C                                       |
| Pb-Free Temperature, Soldering Reflow (10 sec to 30 sec) | 260°C   |
| Junction Temperature                                     | 150°C   |
| Package Classification Temperature                       | 260°C   |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$  is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.  $\theta_{JC}$  is the junction to case thermal resistance.

Table 7. Thermal Resistance

| Package Type                         | $\theta_{JA}$   | $\theta_{JC}$    | Unit |
|--------------------------------------|-----------------|------------------|------|
| CP-56-9                              |                 |                  |      |
| 2S2P or 1S Test Board                | 37 <sup>1</sup> | 5.4 <sup>2</sup> | °C/W |
| 2S2P Test Board with 36 Thermal Vias | 27 <sup>3</sup> | N/A <sup>4</sup> | °C/W |

<sup>1</sup> Simulated data based on a JEDEC 2S2P test board in a JEDEC natural convection environment.

<sup>2</sup> Simulated data based on a JEDEC 1S test board, measured at the exposed pad with a cold plate mounted directly to the package surface.

<sup>3</sup> Simulated data based on a JEDEC 2S2P test board with 36 thermal vias in a JEDEC natural convection environment.

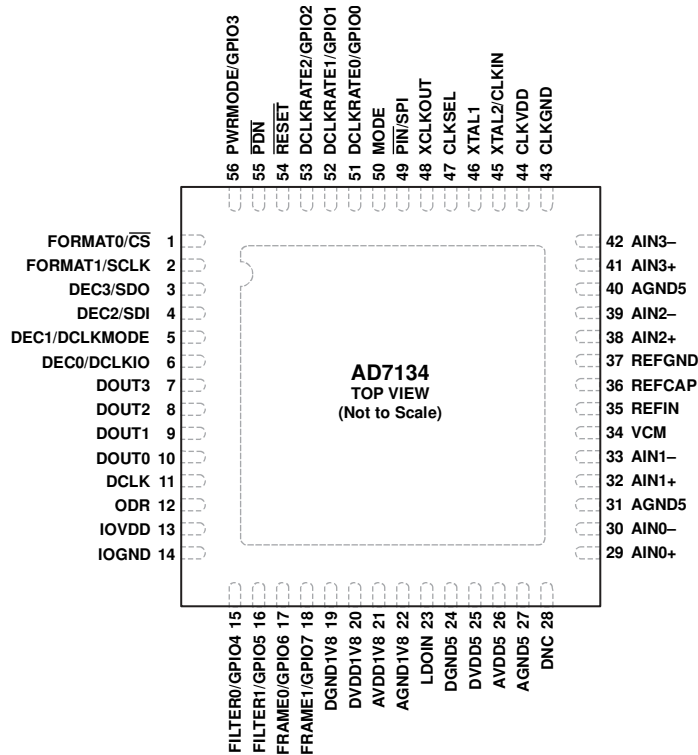
<sup>4</sup> N/A means not applicable.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.
  2. EXPOSED PAD. CONNECT THE EXPOSED PAD TO AGND5.

Figure 5. Pin Configuration

22652-005

Table 8. Pin Function Descriptions

| Pin No. | Mnemonic      | Type <sup>1</sup> | Description   |
|---------|---------------|-------------------|---|
| 1       | FORMAT0/CS    | DI                | ADC Output Data Format Selection Input 0 in Pin Control Mode (FORMAT0). Tie this pin to IOVDD or to IOGND to set the number of DOUTx pins used to output ADC conversion data. See the Output Channel Format section for more details.<br>Chip Select Input in SPI Control Mode (CS).  |
| 2       | FORMAT1/SCLK  | DI                | ADC Output Data Format Selection Input 1 in Pin Control Mode (FORMAT1). Tie this pin to IOVDD or to IOGND to set the number of DOUTx pins used to output ADC conversion data. See the Output Channel Format section for more details.<br>Serial Clock Input in SPI Control Mode (SCLK).   |
| 3       | DEC3/SDO      | DI/O              | Decimation Ratio Selection Input 3 in Pin Control Master Mode or PLL Lock Status Output in Pin Control Slave Mode (DEC3). Tie this pin to IOVDD or to IOGND to set the output data rate. See the Programming Output Data Rate and Clock section for more details. In pin control slave mode, this pin is output high to indicate the internal PLL is in lock.<br>Serial Data Output in SPI Control Mode (SDO).                            |
| 4       | DEC2/SDI      | DI                | Master Mode Decimation Ratio Selection Input 2 in Pin Control Master Mode (DEC2). Tie this pin to IOVDD or to IOGND to set the output data rate. See the Programming Output Data Rate and Clock section for more details.<br>Serial Data Input in SPI Control Mode (SDI).   |
| 5       | DEC1/DCLKMODE | DI                | Decimation Ratio Selection Input 1 in Pin Control Master Mode (DEC1). Tie this pin to IOVDD or to IOGND to set the output data rate. See the Programming Output Data Rate and Clock section for more details.<br>DCLK Mode Control in Pin Control Slave Mode and in SPI Control Mode (DCLKMODE). Tie this pin high to IOVDD to set DCLK to operate in free running mode. Tie this pin low to ground to set DCLK to operate in gated mode. |

| Pin No. | Mnemonic      | Type <sup>1</sup> | Description   |
|---------|---------------|-------------------|---|
| 6       | DEC0/DCLKIO   | DI                | Decimation Ratio Selection Input 0 in Pin Control Master Mode (DEC0). Tie this pin to IOVDD or to IOGND to set the output data rate. See the Programming Output Data Rate and Clock section for more details.<br>DCLK Pin I/O Direction Control in Pin Control Slave Mode and in SPI Control Mode (DCLKIO). In master mode, tie this pin to IOVDD to configure DCLK as an output. In slave mode, tie this pin low to ground to set DCLK as an input. When the DEC1/DCLKMODE pin is high (DCLK is in free running mode), the DCLKIO input is ignored and the DCLK direction is always the same as the ODR pin. |
| 7       | DOUT3         | DO                | Data Output 3. The output data is synchronous to DCLK and framed by the ODR pin.  |
| 8       | DOUT2         | DO                | Data Output 2. The output data is synchronous to DCLK and framed by the ODR pin.  |
| 9       | DOUT1         | DO                | Data Output 1. The output data is synchronous to DCLK and framed by the ODR pin.  |
| 10      | DOUT0         | DO                | Data Output 0. The output data is synchronous to DCLK and framed by the ODR pin.  |
| 11      | DCLK          | DI/O              | ADC Conversion Data Clock. Conversion data on the DOUT0 pin to the DOUT3 pin is clocked out synchronously by DCLK. In pin control master mode, DCLK is configured as an output operating in gated mode. In pin control slave mode or in SPI control mode, the DCLK direction and mode of operation are determined by the DEC1/DCLKMODE pin and DCLKIO pin. Refer to Table 29 for details. In master mode, DCLK frequency is programmable through DCLKRATEx in pin control mode or the DATA_PACKET_CONFIG register in SPI control mode.  |
| 12      | ODR           | DI/O              | Output Data Rate Control and Framing. The frequency of the ODR signal matches the ADC output data rate. The edges of the ODR signal can be used to frame the conversion output data bit stream. In master mode, the ODR pin is configured as an output with the pin-programmable and register-programmable frequency derived from the device master clock. In slave mode, the ODR pin is configured as an input to allow the external clock to control the ADC output data rate.  |
| 13      | IOVDD         | P                 | Digital I/O Supply. This pin sets the logic levels for all interface I/O pins.  |
| 14      | IOGND         | GND               | I/O Interface Ground Reference.   |
| 15      | FILTER0/GPIO4 | DI/O              | Digital Filter Type Selection Input 0 in Pin Control Mode (FILTER0). Tie this pin to IOVDD or to IOGND to select the digital filter options. See the Programming Digital Filter section for more details. General-Purpose Input/Output 4 in SPI Control Mode (GPIO4).   |
| 16      | FILTER1/GPIO5 | DI/O              | Digital Filter Type Selection Input 1 in Pin Control Mode (FILTER1). Tie this pin to IOVDD or to IOGND to select the digital filter options. See the Programming Digital Filter section for more details. General-Purpose Input/Output 5 in SPI Control Mode (GPIO5).   |
| 17      | FRAME0/GPIO6  | DI/O              | Conversion Output Data Frame Control Input 0 in Pin Control Mode (FRAME0). Tie this pin to IOVDD or to IOGND to select the conversation output data frame. See the Data Frame section for more details. General-Purpose Input/Output 6 in SPI Control Mode (GPIO6).   |
| 18      | FRAME1/GPIO7  | DI/O              | Conversion Output Data Frame Control Input 1 in Pin Control Mode (FRAME1). Tie this pin to IOVDD or to IOGND to select the conversation output data frame. See the Data Frame section for more details. General-Purpose Input/Output 7 in SPI Control Mode (GPIO7).   |
| 19      | DGND1V8       | GND               | Ground Reference for Digital Supply Voltage, 1.8 V.   |
| 20      | DVDD1V8       | P                 | Digital Supply Voltage, 1.8 V. The pin is supplied from an external source or the internal LDO regulator. In either case, a decoupling capacitor of 10 $\mu$ F is required between DVDD1V8 and DGND1V8.   |
| 21      | AVDD1V8       | P                 | Analog Supply Voltage 1.8 V. The pin is supplied from an external source or the internal LDO regulator. In either case, a decoupling capacitor of 10 $\mu$ F is required between AVDD1V8 and AGND1V8.   |
| 22      | AGND1V8       | GND               | Ground Reference for Analog Supply Voltage, 1.8 V.  |
| 23      | LDOIN         | P                 | Input for Three Internal 1.8 V LDO Regulators Powering AVDD1V8, DVDD1V8, and CLKVDD. Tie this pin to DVDD1V8 if an external power supply is used to power AVDD1V8, DVDD1V8, and CLKVDD. A 10 $\mu$ F decoupling capacitor is required between LDOIN and DGND1V8. See the On-Board LDO Regulators section for more details.  |
| 24      | DGND5         | GND               | Ground Reference for Digital Supply Voltage, 5 V.   |
| 25      | DVDD5         | P                 | Digital Supply Voltage, 5 V. A decoupling capacitor of 10 $\mu$ F is required between DVDD5 and DGND5.  |
| 26      | AVDD5         | P                 | Analog Supply Voltage, 5 V. A decoupling capacitor of 10 $\mu$ F is required between AVDD5 and AGND5.   |
| 27      | AGND5         | GND               | Ground Reference for Analog Supply Voltage, 5 V.  |
| 28      | DNC           | DNC               | Do Not Connect. Do not connect to this pin.   |
| 29      | AIN0+         | AI                | Positive Analog Input to ADC Channel 0.   |
| 30      | AIN0-         | AI                | Negative Analog Input to ADC Channel 0.   |
| 31      | AGND5         | GND               | Ground Reference for Analog Supply Voltage, 5 V.  |
| 32      | AIN1+         | AI                | Positive Analog Input to ADC Channel 1.   |
| 33      | AIN1-         | AI                | Negative Analog Input to ADC Channel 1.   |

| Pin No. | Mnemonic                           | Type <sup>1</sup> | Description  |
|---------|------------------------------------|-------------------|--|
| 34      | VCM                                | AO                | Common-Mode Voltage Output. The VCM output can be used to provide a common-mode voltage for the analog front-end circuit. The VCM pin provides a buffered voltage output. The level is fixed to 1/2 of the voltage on the REFCAP pin in pin control mode, and is programmable in SPI control mode. When driving capacitive loads larger than 0.2 nF, it is recommended to place a 50 $\Omega$ series resistor between the pin and the capacitive load for stability. |
| 35      | REFIN                              | AI                | ADC Reference Filter Input. Use an internal 20 $\Omega$ resistor together with an external capacitor on the REFCAP pin to filter the reference source noise.   |
| 36      | REFCAP                             | AO                | ADC Reference Direct Input. Connect this pin to the external reference source for a direct reference input. Alternatively, connect the reference source to the REFIN pin and place a filter capacitor between the REFCAP pin and REFGND pin to limit the reference noise bandwidth. See the Reference Input section for more details.  |
| 37      | REFGND                             | GND               | ADC Reference Ground Reference.  |
| 38      | AIN2+                              | AI                | Positive Analog Input to ADC Channel 2.  |
| 39      | AIN2-                              | AI                | Negative Analog Input to ADC Channel 2.  |
| 40      | AGND5                              | GND               | Ground Reference for Analog Supply Voltage, 5 V.   |
| 41      | AIN3+                              | AI                | Positive Analog Input to ADC Channel 3.  |
| 42      | AIN3-                              | AI                | Negative Analog Input to ADC Channel 3.  |
| 43      | CLKGND                             | GND               | Clock Management Circuit Ground Reference.   |
| 44      | CLKVDD                             | P                 | Clock Management Circuit Power Supply, 1.8 V. This pin is supplied from an external source or internal LDO regulator. In either case, a decoupling capacitor of 2.2 $\mu$ F is required between the CLKVDD pin and CLKGND pin.   |
| 45      | XTAL2/CLKIN                        | DI                | Input 2 for Internal Crystal Oscillator (XTAL2). Connect an external crystal between the XTAL1 pin and XTAL2/CLKIN pin for on-chip clock generation.<br>Clock Input (CLKIN). For operations using an external clock signal, connect this pin to the external clock source. See the Clock Input section for more details.   |
| 46      | XTAL1                              | DI                | Input 1 for Internal Crystal Oscillator. Connect an external crystal between the XTAL1 pin and XTAL2/CLKIN pin for on-chip clock generation. Leave this pin floating if the device is to operate from a single-ended external clock signal.  |
| 47      | CLKSEL                             | DI                | Clock Source Selection Input. Connect this pin to IOVDD to enable on-chip clock generation from an external crystal. Connect this pin to IOGND if the clock signal is provided externally on the XTAL2/CLKIN pin.  |
| 48      | XCLKOUT                            | DO                | Crystal Oscillator Buffered Output. A buffered clock signal generated by the internal crystal oscillator is available on this pin. This signal can be used to drive other AD7134 devices working in parallel. The XCLKOUT output is enabled by default in pin control mode only if the crystal clock option is selected. The XCLKOUT output is disabled by default in SPI control mode. See the XCLKOUT Output section for more details.                             |
| 49      | $\overline{\text{PIN}}/\text{SPI}$ | DI                | Device Configuration Mode Control Input. Tie this pin to IOVDD to enable device configuration through register access over the SPI interface. Tie this pin to ground to enable device configuration through the configuration input pins.  |
| 50      | MODE                               | DI                | ASRC Mode Of Operation Control Input. Tie this pin to IOVDD for master mode operation. Tie this pin to IOGND for slave mode operation.   |
| 51      | DCLKRATE0/GPIO0                    | DI/O              | DCLK Frequency Control Input 0 in Pin Control Mode (DCLKRATE0). When DCLK is configured as an output, tie this pin to IOVDD or to IOGND to set the frequency ratio between DCLK and the device master clock. See Table 30 for more details.<br>General-Purpose Input/Output 0 in SPI Control Mode (GPIO0).   |
| 52      | DCLKRATE1/GPIO1                    | DI/O              | DCLK Frequency Control Input 1 in Pin Control Mode (DCLKRATE1). When DCLK is configured as an output, tie this pin to IOVDD or to IOGND to set the frequency ratio between DCLK and the device master clock. See Table 30 for more details.<br>General-Purpose Input/Output 1 in SPI Control Mode (GPIO1).   |
| 53      | DCLKRATE2/GPIO2                    | DI/O              | DCLK Frequency Control Input 2 in Pin Control Mode (DCLKRATE2). When DCLK is configured as an output, tie this pin to IOVDD or to IOGND to set the frequency ratio between DCLK and the device master clock. See Table 30 for more details.<br>General-Purpose Input/Output 2 in SPI Control Mode (GPIO2).   |
| 54      | $\overline{\text{RESET}}$          | DI                | Hardware Asynchronous Reset Input, Active Low. Pull this pin to IOVDD through a 10 k $\Omega$ pull-up resistor during normal operation. Pull this pin low to IOGND to force the device into reset. See the Reset section for more details.   |
| 55      | $\overline{\text{PDN}}$            | DI                | Full Power-Down Mode Control Input, Active Low. Pull this pin to IOVDD through a 10 k $\Omega$ pull-up resistor during normal operation. Pull this pin to IOGND to force the device into full power-down mode. See the Power Modes section for more details.   |

| Pin No. | Mnemonic      | Type <sup>1</sup> | Description  |
|---------|---------------|-------------------|--|
| 56      | PWRMODE/GPIO3 | DI/O              | Power Mode Selection Input in Pin Control Mode (PWRMODE). Tie this pin to IOVDD for high performance mode. Tie this pin to IOGND for low power mode. |
|         | EPAD          |                   | General-Purpose Input/Output 3 in SPI Control Mode (GPIO3).<br>Exposed Pad. Connect the exposed pad to AGND5.  |

<sup>1</sup> DI is digital input, DI/O is bidirectional digital input/output, DO is digital output, P is power, GND is ground, DNC is do not connect, AI is analog input, and AO is analog output.



# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{REF} = 4.096\text{ V}$ , AA1 mode,  $V_{CM} = 2.048\text{ V}$ , wideband  $0.433 \times \text{ODR}$  filter, high performance mode, wideband filter plots at  $\text{ODR} = 374\text{ kSPS}$ , sinc3 and sinc6 plots at  $\text{ODR} = 1496\text{ kSPS}$ , unless otherwise noted.

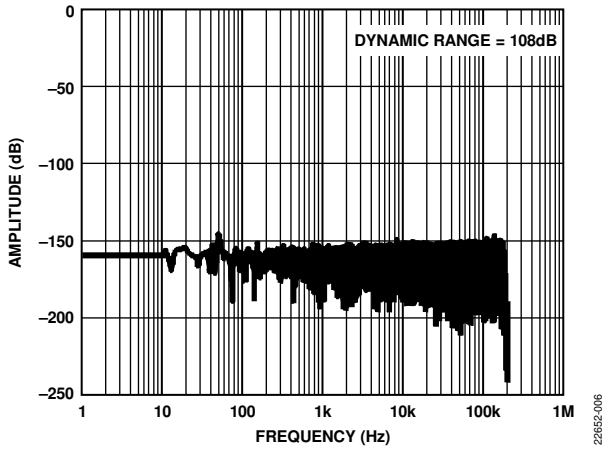


Figure 6. Dynamic Range Performance, High Performance Mode, Wideband  $0.433\text{ Hz} \times \text{ODR}$  Filter,  $\text{ODR} = 374\text{ kSPS}$

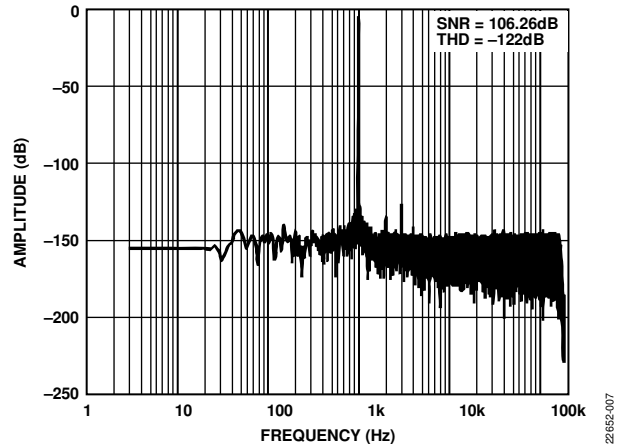


Figure 9. FFT, High Performance Mode,  $-0.5\text{ dBFS}$ , Wideband  $0.433\text{ Hz} \times \text{ODR}$  Filter,  $\text{ODR} = 374\text{ kSPS}$

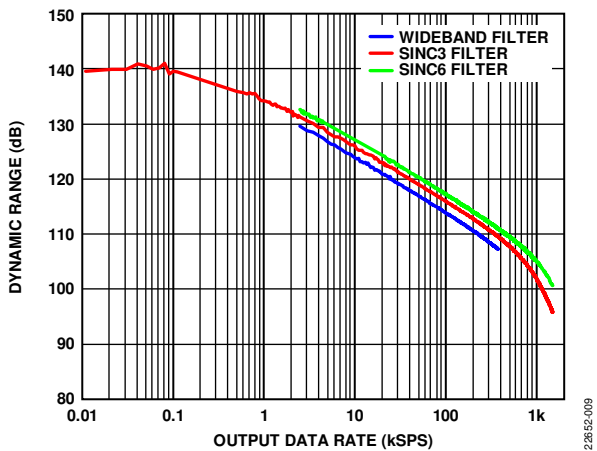


Figure 7. Dynamic Range vs. Output Data Rate in High Performance Mode for Wideband FIR, Sinc3 and Sinc6 Filters

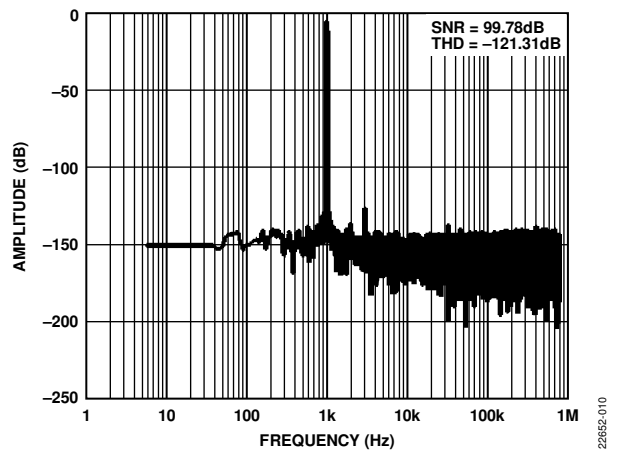


Figure 10. FFT, High Performance Mode, Sinc6 Filter,  $-0.5\text{ dBFS}$ ,  $\text{ODR} = 1496\text{ kSPS}$

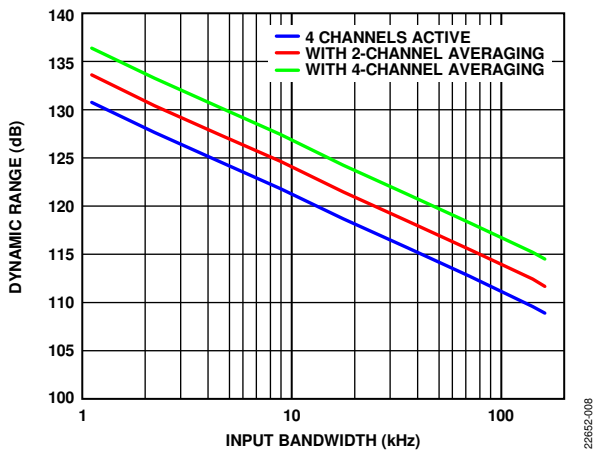


Figure 8. Dynamic Range vs. Input Bandwidth, Wideband  $0.433\text{ Hz} \times \text{ODR}$  Filter

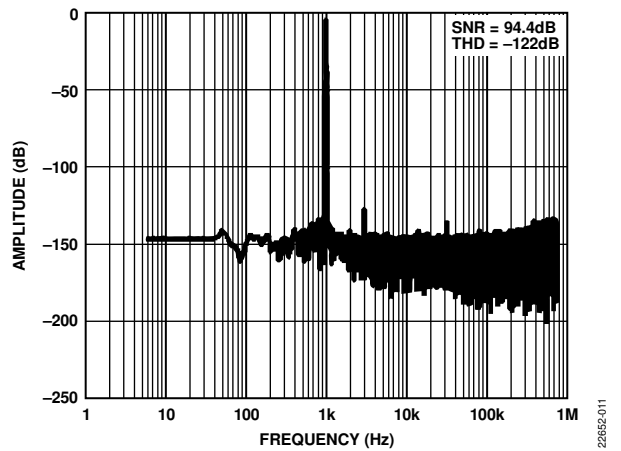


Figure 11. FFT, High Performance Mode, Sinc3 Filter,  $-0.5\text{ dBFS}$ ,  $\text{ODR} = 1496\text{ kSPS}$

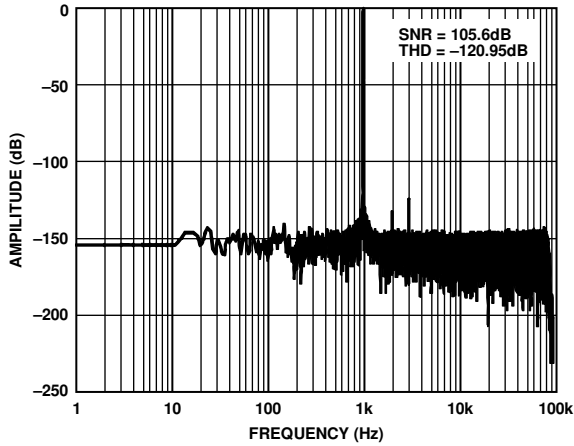


Figure 12. FFT, Low Power Mode, Wideband  $0.433 \times \text{ODR}$  Filter,  $-0.5 \text{ dBFS}$ ,  $\text{ODR} = 187 \text{ kSPS}$

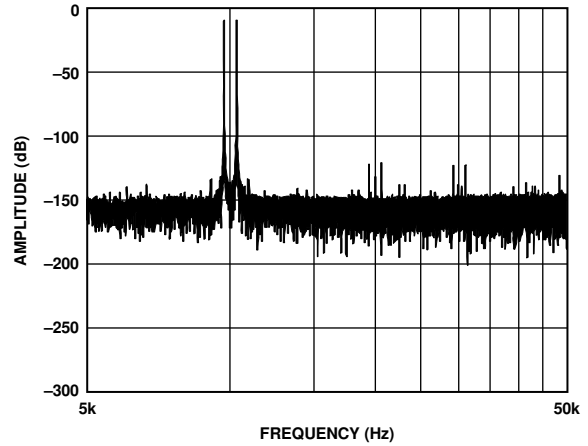


Figure 15. IMD with Input Signals at 9.7 kHz and 10.3 kHz, Wideband  $0.433 \times \text{ODR}$  Filter

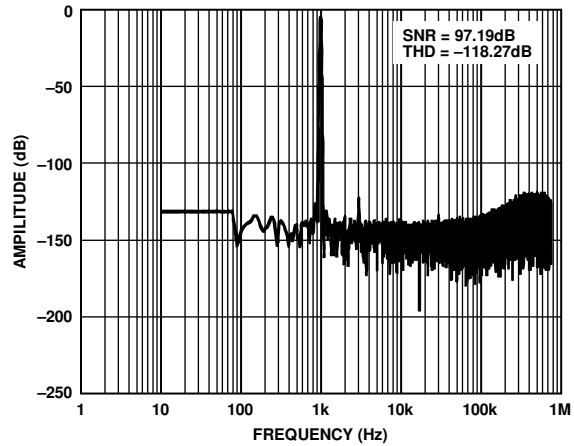


Figure 13. FFT, Low Power Mode, Sinc6 Filter,  $-0.5 \text{ dBFS}$ ,  $\text{ODR} = 750 \text{ kSPS}$

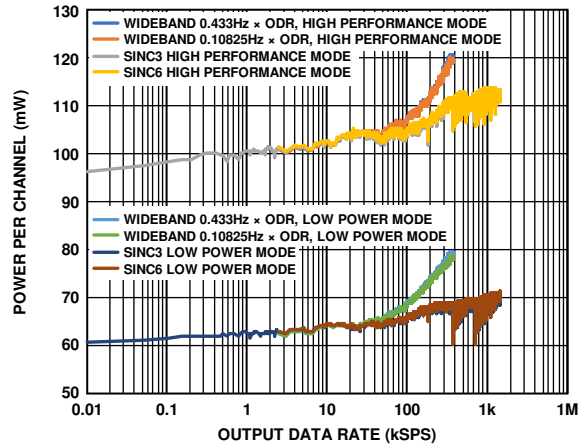


Figure 16. Power per Channel vs. Output Data Rate

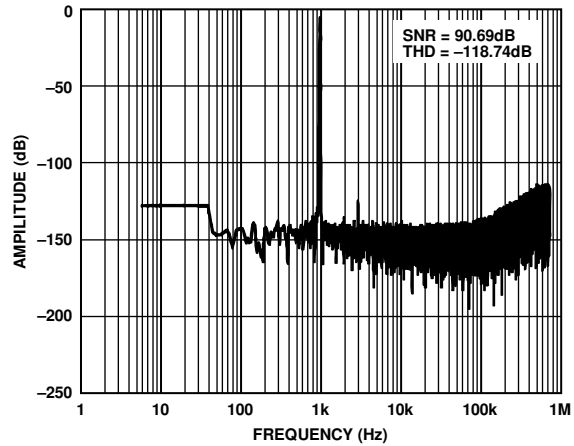


Figure 14. FFT, Low Power Mode, Sinc3 Filter,  $-0.5 \text{ dBFS}$ ,  $\text{ODR} = 750 \text{ kSPS}$

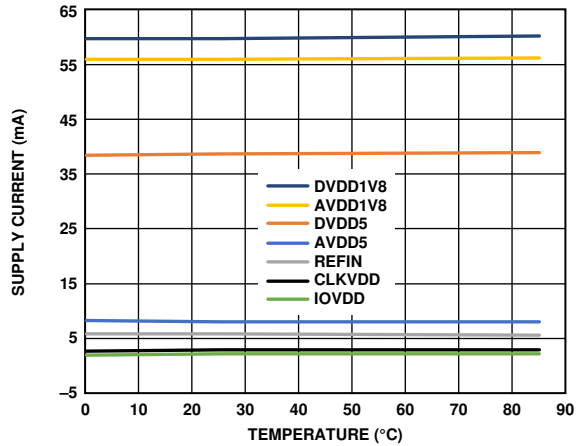


Figure 17. Supply Current vs. Temperature, Wideband  $0.433 \text{ Hz} \times \text{ODR}$  Filter

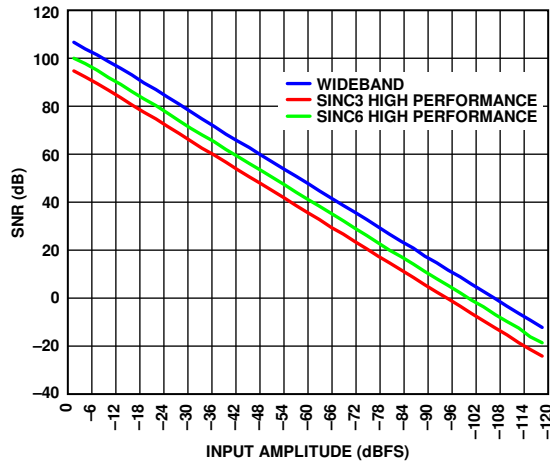


Figure 18. SNR vs. Input Amplitude, Tone at 1 kHz

22652-017

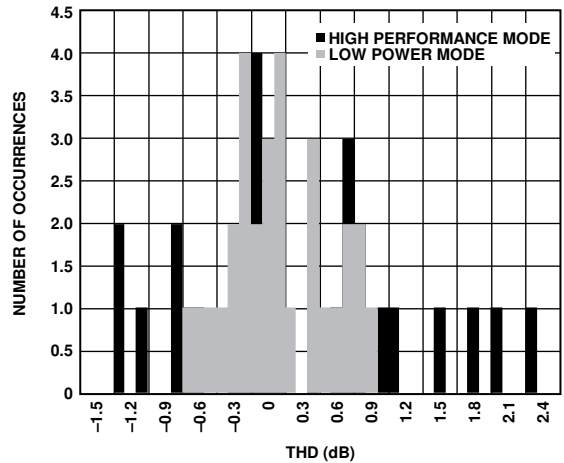


Figure 21. THD Histogram

22652-274

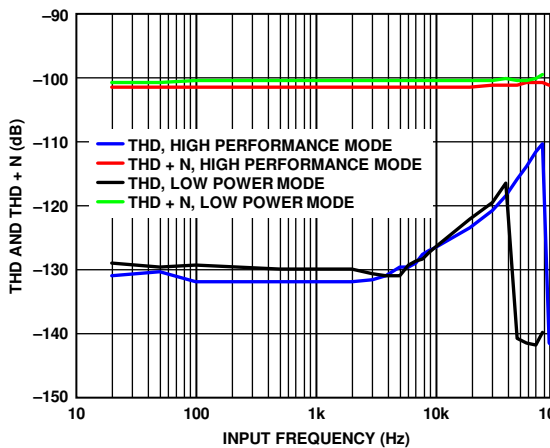


Figure 19. THD and THD + N vs. Input Frequency, -6 dBFS Input, 0.433 x ODR Filter

22652-221

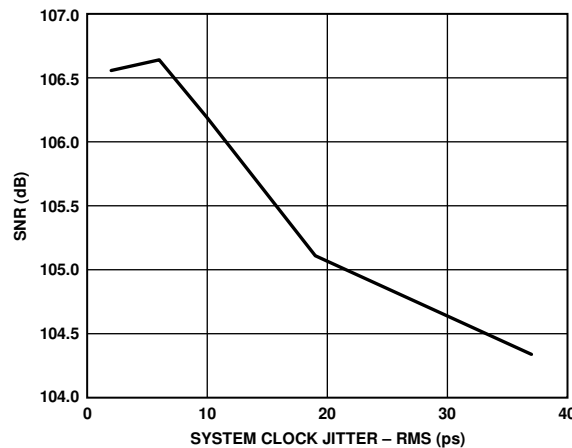


Figure 22. SNR vs. System Clock Jitter, Wideband 0.433 Hz x ODR Filter

22652-039

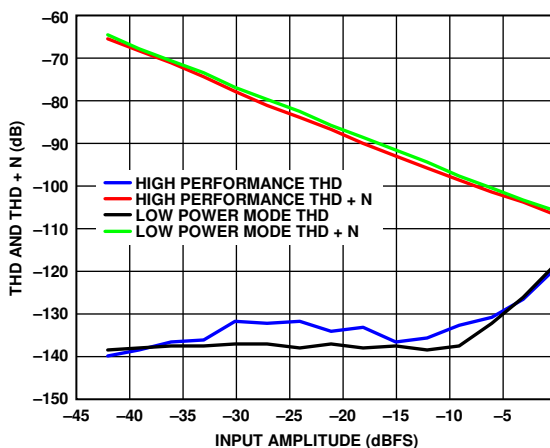


Figure 20. THD and THD + N vs. Input Amplitude, Wideband Filter, Tone at 1 kHz

22652-222

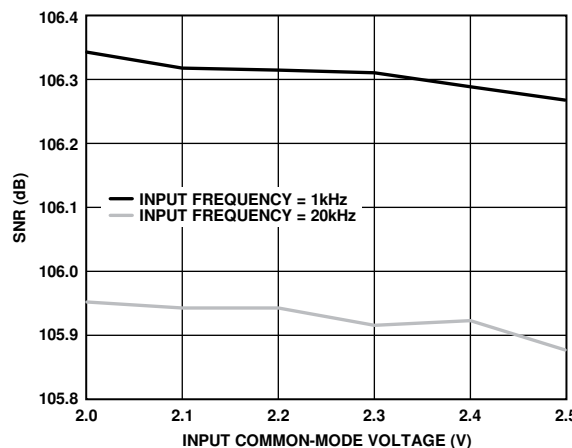


Figure 23. SNR vs. Input Common-Mode Voltage, Wideband 0.433 Hz x ODR Filter

22652-040

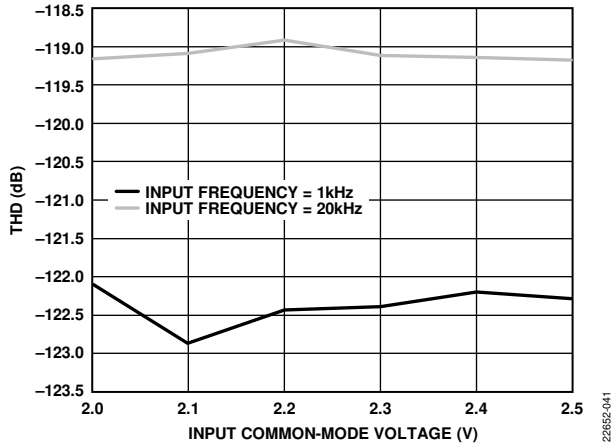


Figure 24. THD vs. Input Common-Mode Voltage, 0.5 dBFS Input Tone, Wideband 0.433 Hz × ODR Filter, Full-Scale Input Tone

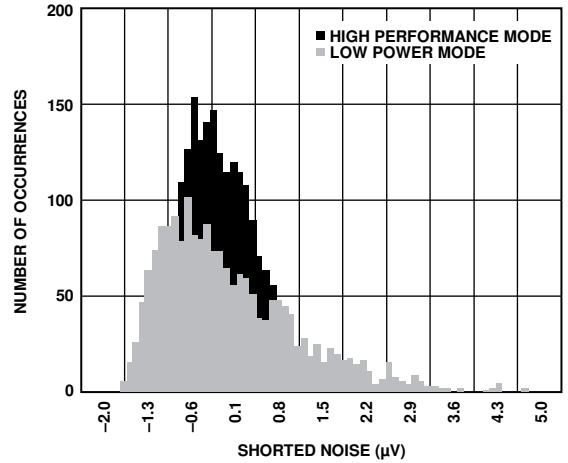


Figure 27. Shorted Noise, 0.433 × ODR Filter

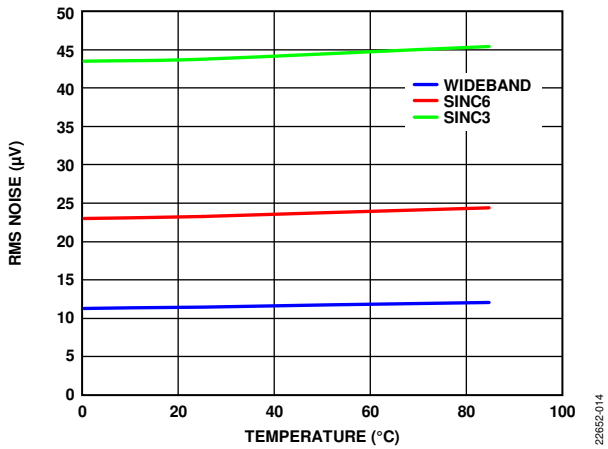


Figure 25. RMS Noise vs. Temperature, for Wideband 0.433 Hz × ODR, Sinc6 and Sinc3 Filters

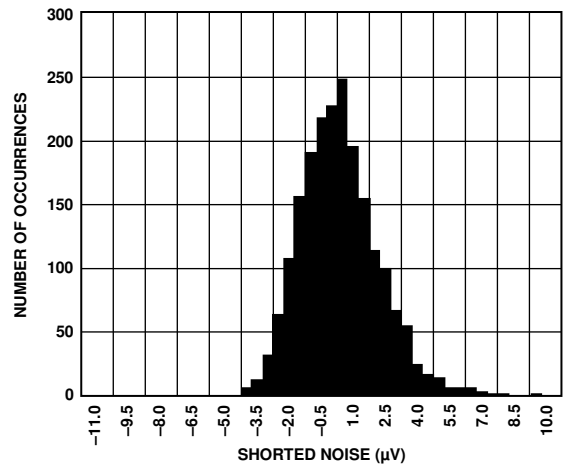


Figure 28. Shorted Noise, Sinc3 Filter

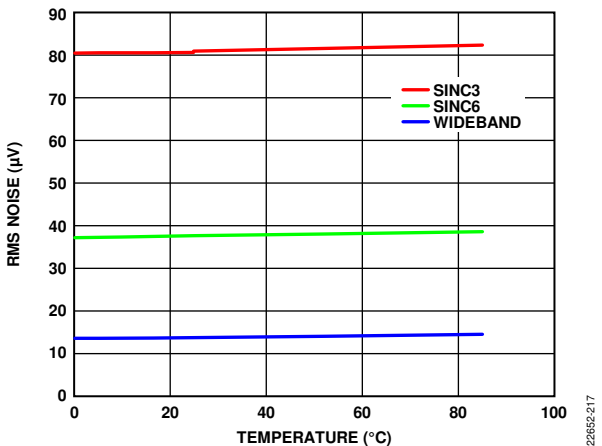


Figure 26. RMS Noise vs. Temperature, Low Power Mode for Wideband 0.433 × ODR Filter, Sinc6, Sinc3

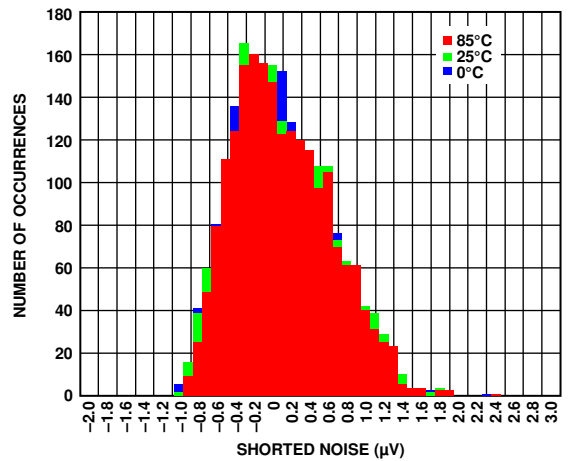


Figure 29. Shorted Noise Histogram, 0.433 × ODR Filter at Different Temperatures

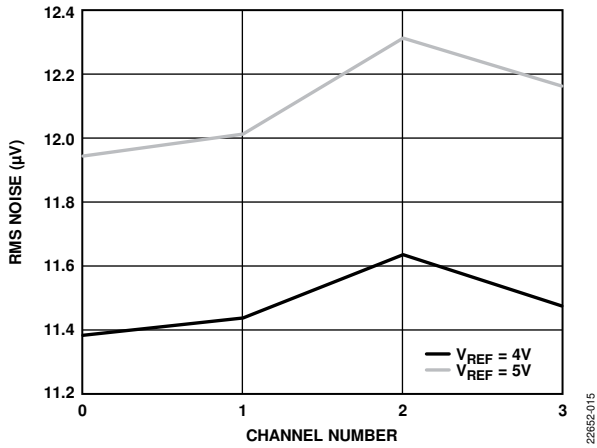


Figure 30. RMS Noise per Channel for Various  $V_{REF}$  Values, Wideband  $0.433 \times$  ODR Filter

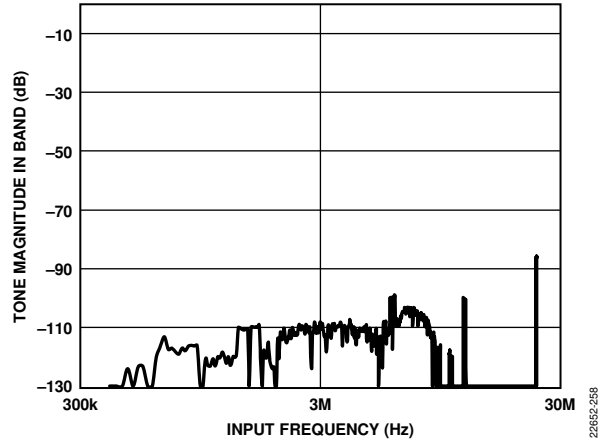


Figure 33. Tone Magnitude In Band vs. Input Frequency

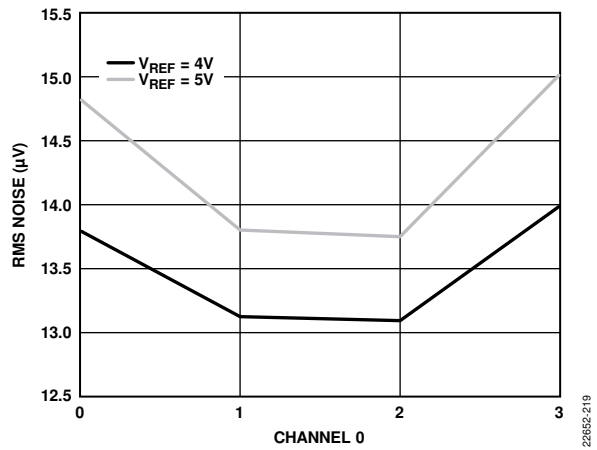


Figure 31. RMS Noise per Channel for Various  $V_{REF}$  Values, Low Power Mode

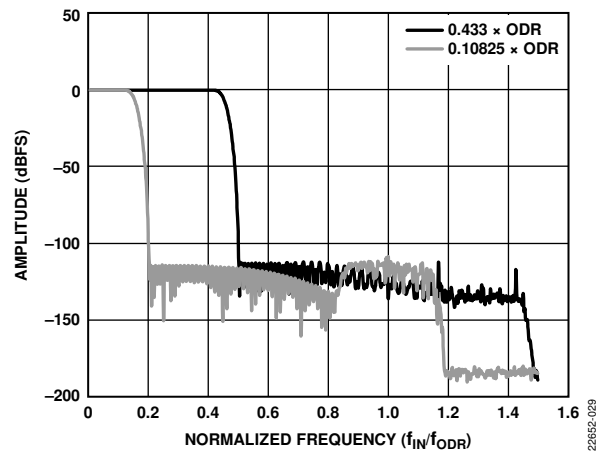


Figure 34. Amplitude vs. Normalized Frequency ( $f_{IN}/f_{ODR}$ )

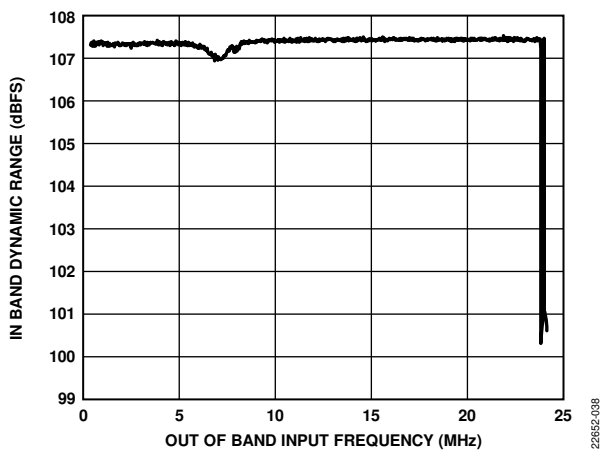


Figure 32. In Band Dynamic Range vs. Out of Band Input Frequency of  $1\text{ V p-p}$  Input Signal Wideband  $0.433\text{ Hz} \times$  ODR Filter

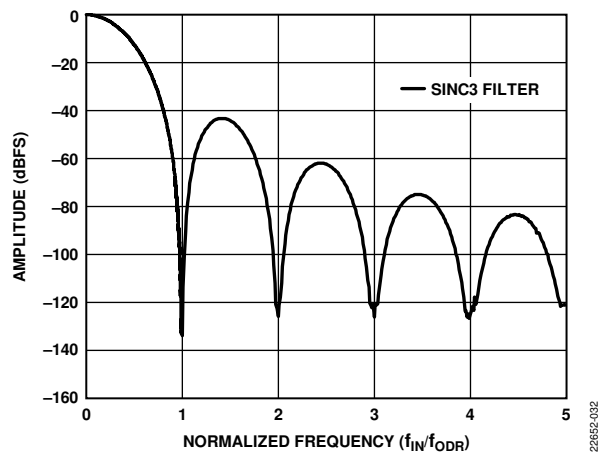


Figure 35. Amplitude vs. Normalized Frequency ( $f_{IN}/f_{ODR}$ ), Sinc Filter Profile

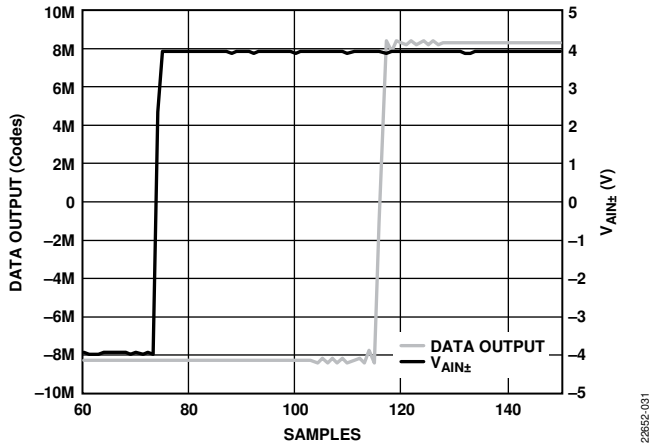


Figure 36. Step Response, Wideband Filter

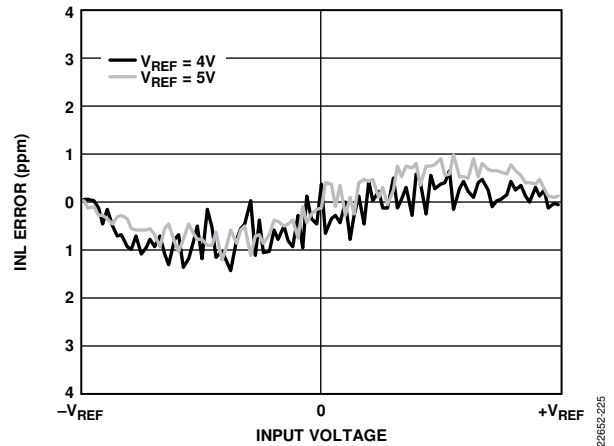


Figure 39. INL Error vs. Input Voltage for Various  $V_{REF}$  Levels, Low Power Mode

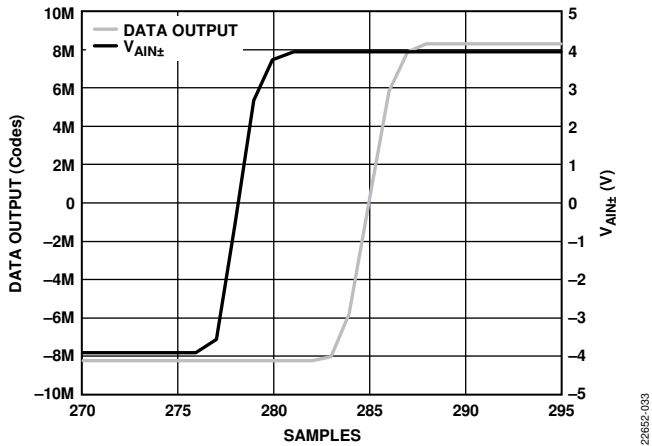


Figure 37. Step Response, Sinc3 Filter

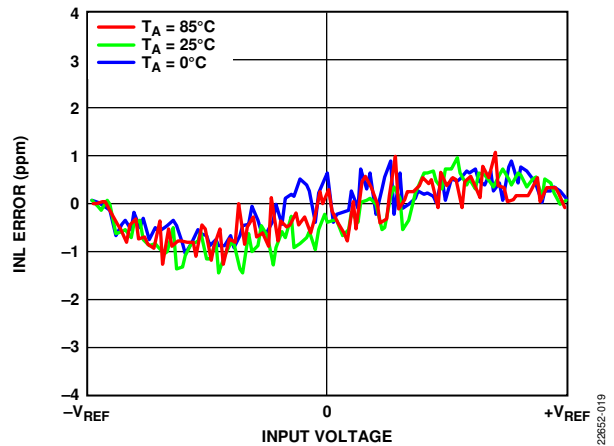


Figure 40. INL Error vs. Input Voltage, Wideband  $0.433 \times ODR$  Filter

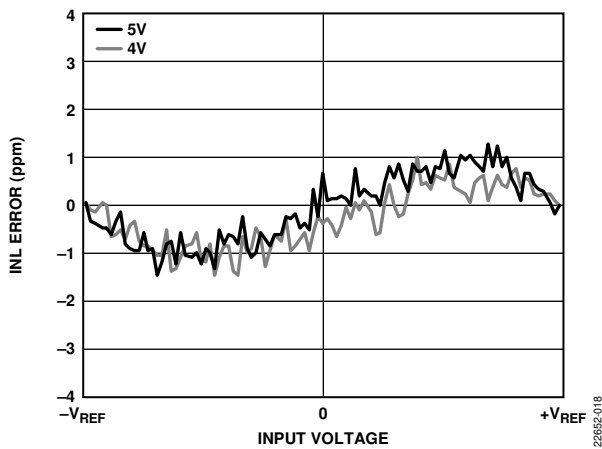


Figure 38. INL Error vs. Input Voltage, Wideband  $0.433 \times ODR$  Filter

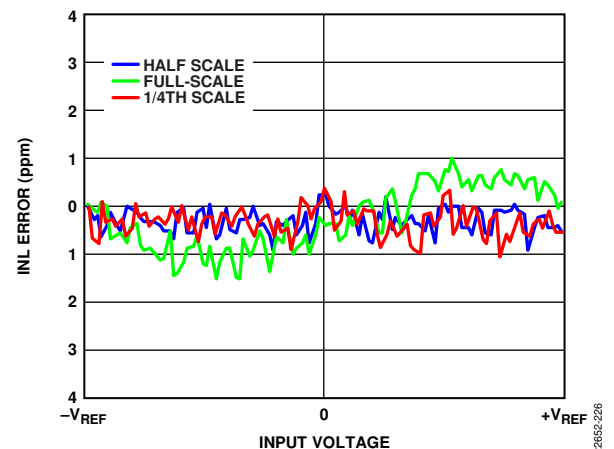


Figure 41. INL Error vs. Input Voltage, Full-Scale, Half Scale, and Quarter Scale Inputs

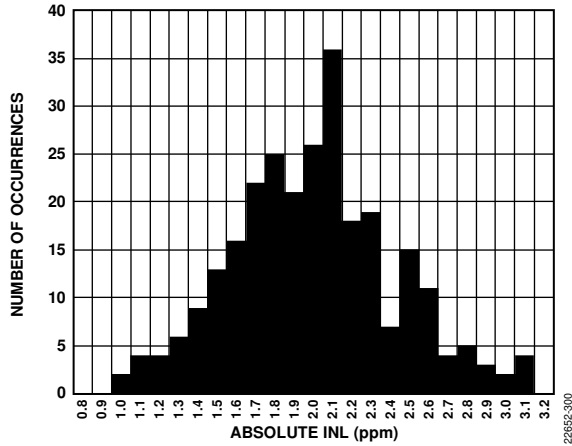


Figure 42. INL Distribution

228652-300

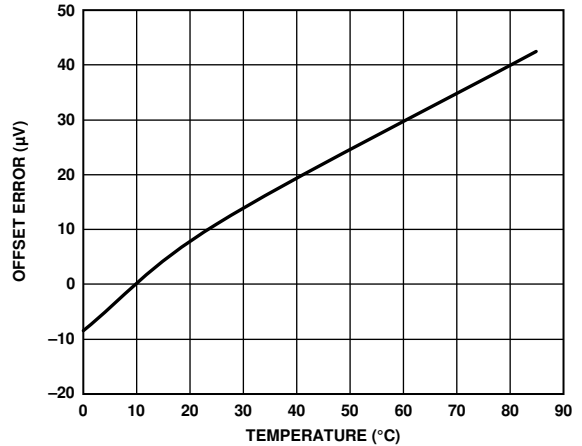


Figure 45. Offset Error vs. Temperature

228652-177

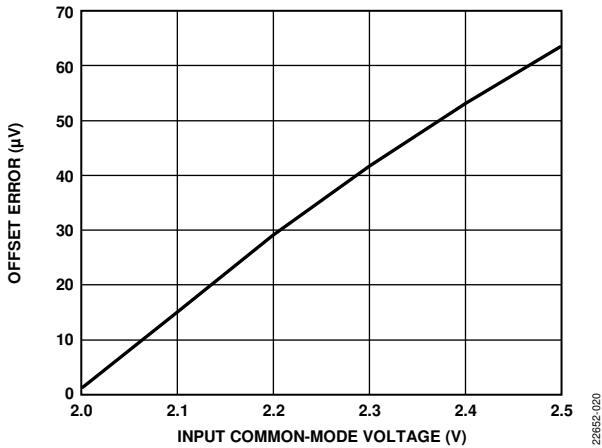


Figure 43. Offset Error vs. Input Common-Mode Voltage, Wideband 0.433 Hz  $\times$  ODR Filter

228652-020

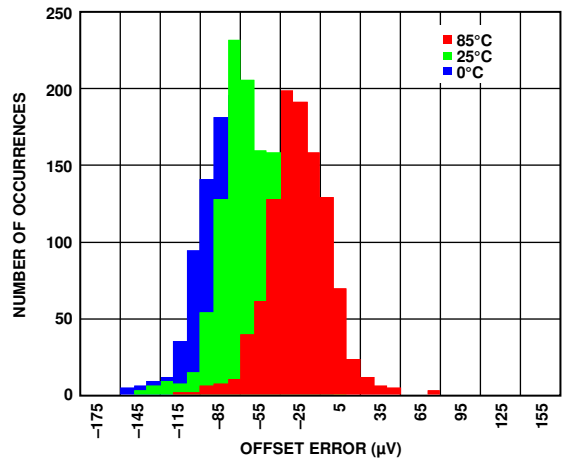


Figure 46. Offset Error Distribution, High Performance Mode

228652-228

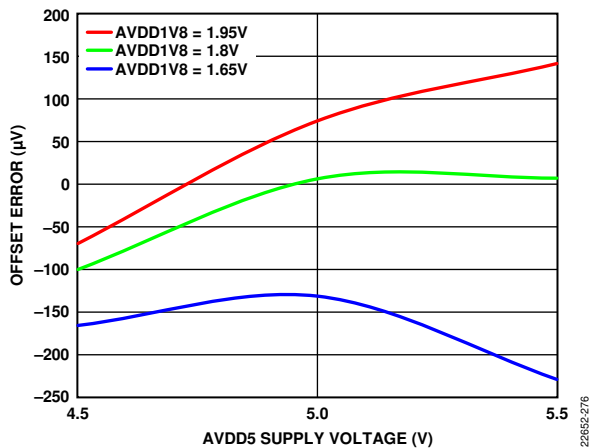


Figure 44. Offset Error vs. AVDD5 Supply Voltage

228652-276

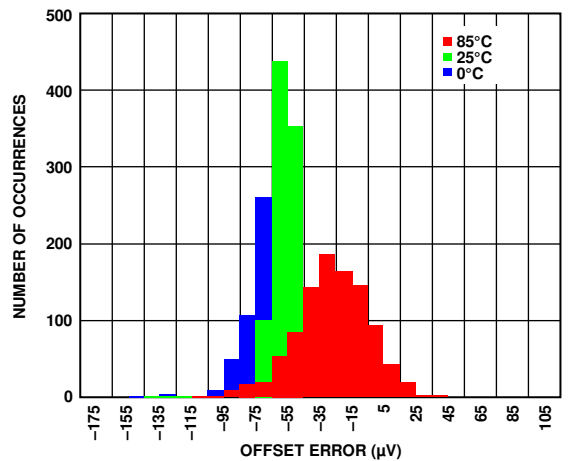


Figure 47. Offset Error Distribution, Low Power Mode

228652-229

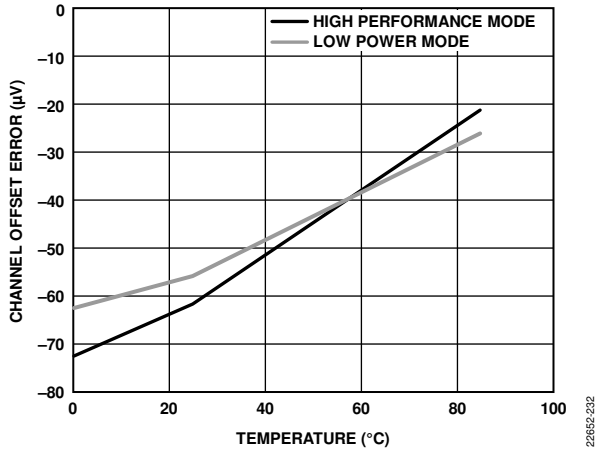


Figure 48. Channel Offset Error Matching

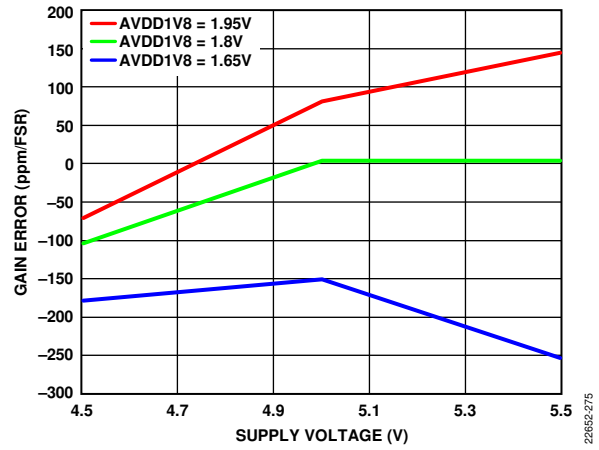


Figure 51. Gain Error vs. Supply Voltage

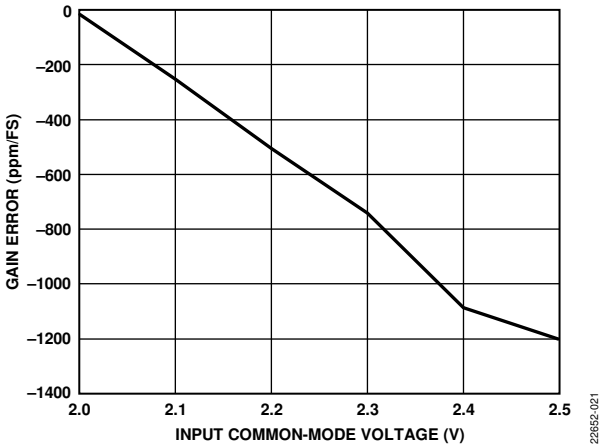


Figure 49. Gain Error vs. Input Common-Mode Voltage, Wideband 0.433 x ODR Filter

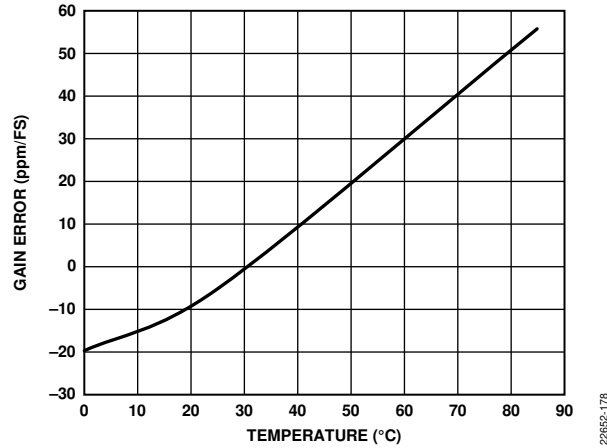


Figure 52. Gain Error vs. Temperature

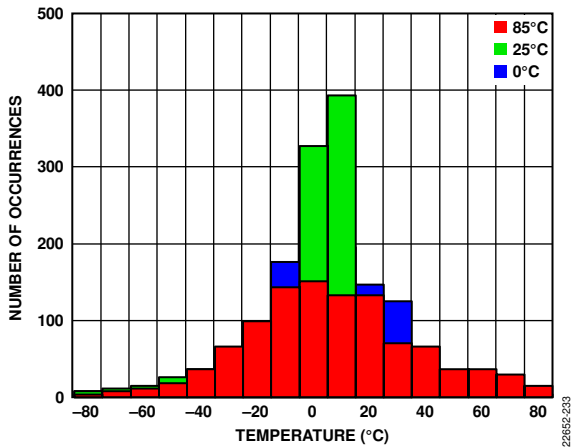


Figure 50. Gain Error Distribution

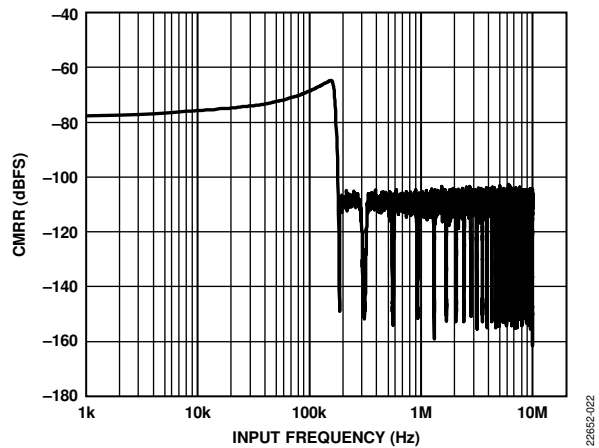


Figure 53. CMRR vs. Input Frequency, Wideband 0.433 x ODR Filter



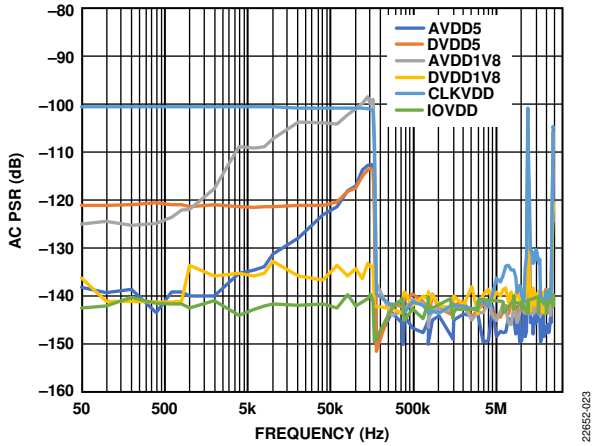


Figure 54. AC Power Supply Rejection (PSR) vs. Frequency, Wideband 0.433 x ODR Filter

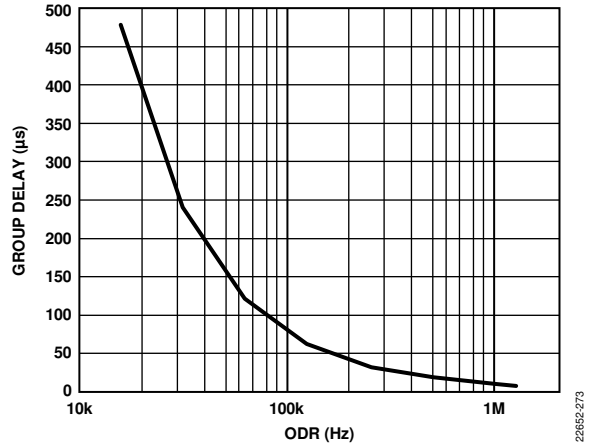


Figure 57. Group Delay vs. ODR, Sinc3 Filter

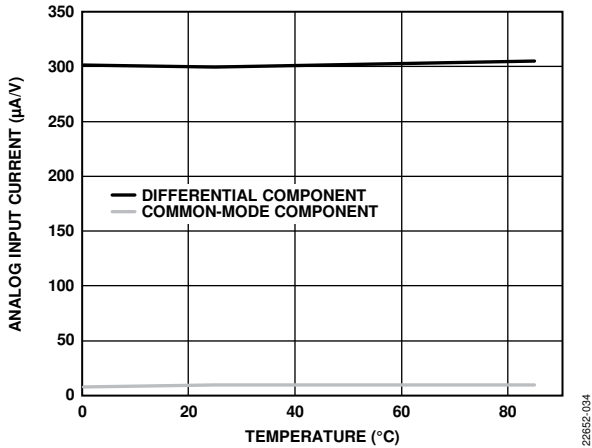


Figure 55. Analog Input Current vs. Temperature, Wideband 0.433 Hz x ODR Filter

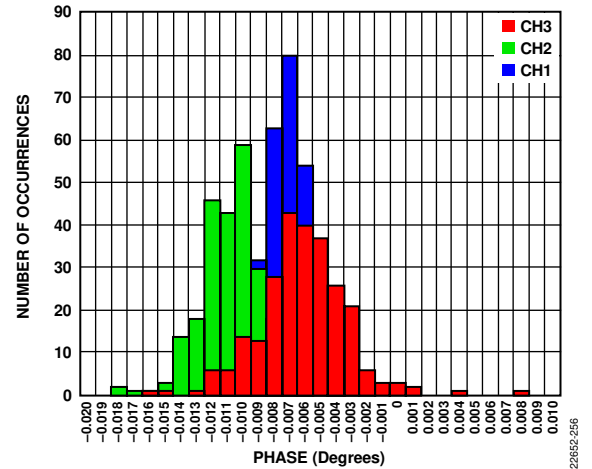


Figure 58. Channel Phase Matching Distribution for Input Tone at 20 kHz

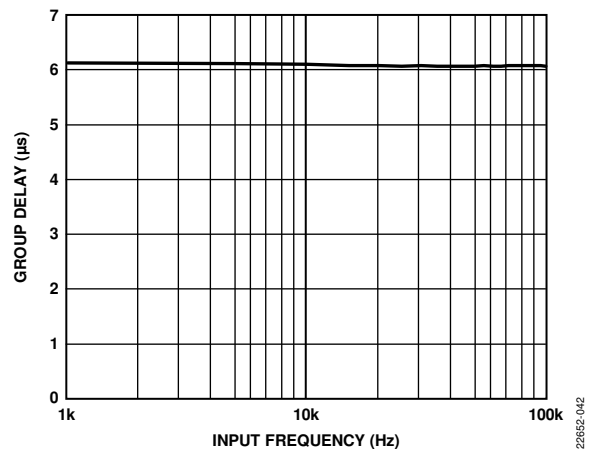


Figure 56. Group Delay vs. Input Frequency, Sinc3 Filter ODR = 1250 kSPS

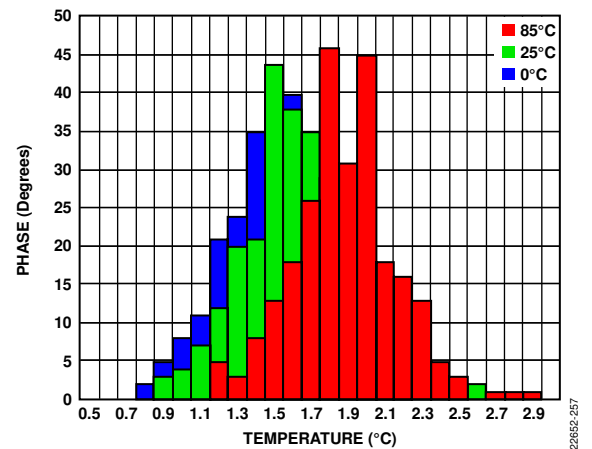


Figure 59. Channel Phase Matching vs. Temperature

## TERMINOLOGY

### AC Common-Mode Rejection Ratio (CMRR)

AC CMRR is defined as the ratio of the power in the ADC output at frequency,  $f$ , to the power of a 100 mV p-p sine wave applied as the common-mode voltage to the AINx+ pin and AINx- pin at sampling frequency ( $f_s$ ).

$$AC\ CMRR\ (dB) = 10 \log(P_f/P_{f_s})$$

where:

$P_f$  is the power at frequency,  $f$ , in the ADC output.

$P_{f_s}$  is the power at frequency,  $f_s$ , in the ADC output.

### Integral Nonlinearity (INL) Error

INL error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs  $\frac{1}{2}$  LSB before the first code transition. Positive full scale is defined as a level  $1\frac{1}{2}$  LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

### Intermodulation Distortion

With inputs consisting of sine waves at two frequencies,  $f_a$  and  $f_b$ , any active device with nonlinearities creates distortion products at the sum and difference frequencies of  $m f_a$  and  $n f_b$ , where  $m, n = 0, 1, 2, 3$ , and so on. Intermodulation distortion terms are those for which neither  $m$  nor  $n$  is equal to 0. For example, the second-order terms include  $(f_a + f_b)$  and  $(f_a - f_b)$ , and the third-order terms include  $(2f_a + f_b)$ ,  $(2f_a - f_b)$ ,  $(f_a + 2f_b)$ , and  $(f_a - 2f_b)$ .

The AD7134 is tested using the International Telephonic Consultative Committee (CCIF) standard, where two input frequencies near to each other are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second-order and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

### Gain Error

The first transition (from 100 ... 000 to 100 ... 001) occurs at a level  $\frac{1}{2}$  LSB above nominal negative full scale ( $-4.0959375$  V for the  $\pm 4.096$  V range). The last transition (from 011 ... 110 to 011 ... 111) occurs for an analog voltage  $1\frac{1}{2}$  LSB below the nominal full scale ( $+4.0959375$  V for the  $\pm 4.096$  V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

### Gain Drift

Gain drift is the ratio of the gain error change due to a temperature change of  $1^\circ\text{C}$  and the full-scale range ( $2^N$ ). Gain drift is expressed in parts per million.

### Least Significant Bit (LSB)

The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with  $N$  bits of resolution, the LSB expressed in volts is

$$LSB = 2 \times \frac{V_{REFCAP}}{2^N}$$

where:

$V_{REFCAP}$  is the voltage measured on the REFCAP pin.

$N = 24$  for the AD7134.

### DC Power Supply Rejection Ratio (DC PSRR)

Variations in power supply affect the full-scale transition but not the linearity of the converter. DC PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

### AC Power Supply Rejection (AC PSR)

AC PSR is the amplitude of the tone observed when a 100 mV p-p signal is injected on the supply.

For example, if a 100 mV p-p signal injected on the supply at a frequency of 1 kHz and a  $-108$  dB tone is observed at 1 kHz in the FFT output, then  $-108$  dB is the ac power supply rejection.

### Alias Rejection

Alias rejection is defined as the ratio of the power in the ADC output at frequency,  $f_{IN}$ , to the power of a  $-6$  dBFS input signal at frequency,  $MCLK \pm f_{IN}$ .

$$Alias\ rejection = 10 \log(P_{f_{IN}}/P_{MCLK \pm f_{IN}})$$

where:

$P_{f_{IN}}$  is the power at frequency,  $f_{IN}$ , in the ADC output.

$P_{MCLK \pm f_{IN}}$  is the power at frequency,  $MCLK \pm f_{IN}$ , in the ADC output.

### Group Delay

Group delay is defined as the difference of phase delays measured at the ADC output and full-scale sine wave ADC input.

### Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the ODR/2 frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

### Signal-to-Noise-and-Distortion Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the ODR/2 frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

### Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal (excluding the first five harmonics).

**Total Harmonic Distortion (THD)**

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

**Offset Error**

Offset error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

**Offset Error Drift**

Offset error drift is the ratio of the offset error change due to a temperature change of 1°C. For this calculation, observe the change in output code when the temperature varies over the full range and take the ratio. Offset error drift is expressed in microvolts per degree Celsius.

**Crosstalk**

Crosstalk is measured as tone amplitude observed at Frequency X on Channel 1 when Channel 0 and Channel 2 are driven simultaneously with a full-scale tone at Frequency X.

## THEORY OF OPERATION

Figure 60 illustrates a simplified signal path of one of the four  $\Sigma$ - $\Delta$  ADC channels of the AD7134. In a typical operation, the CTSD modulator oversamples the analog input signal at the modulator sampling frequency at MCLK. The ADC quantization noise is modulated to the higher frequency band during this process. The oversampled modulator output is then decimated through an ASRC and digital filter. The decimation removes the additional bandwidth caused by oversampling along with the shaped quantization. The result is a high precision data output from the digital filter at the user defined ODR.

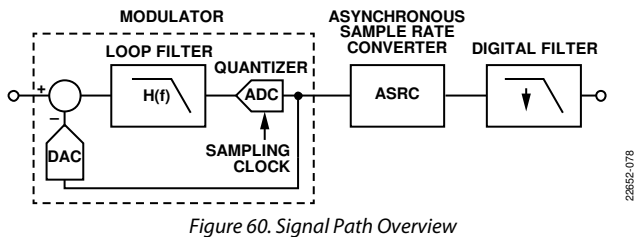


Figure 60. Signal Path Overview

## CONTINUOUS TIME SIGMA-DELTA MODULATOR

Almost all of the contemporary precision ADCs are designed with a switched capacitor-based sample-and-hold circuit. The sample-and-hold circuit is an essential part of the successive approximation register (SAR) ADC architecture, for example, where it is used to reduce the aperture time and maintain a steady input level during conversion. The discrete time  $\Sigma$ - $\Delta$  ADCs also use the sample-and-hold circuit in both the input path and the feedback loop, which simplifies the design. Because the analog input signal is converted to a discrete time signal by the sample-and-hold circuit, the ADCs with the sample-and-hold circuit are also known as discrete time ADCs.

The sample-and-hold circuit offers many benefits to the ADC design. However, some side effects of using the sample-and-hold circuit, such as charge kickback and signal aliasing, require additional effort in designing the ADC into a system.

The CTSD modulator employs the same  $\Sigma$ - $\Delta$  modulation principle, such as oversampling and noise shaping, as the discrete time sigma-delta (DTSD) modulator, with the key difference being the CTSD does not use the sample-and-hold circuit.

The CTSD modulator design used on the AD7134 uses both a continuous time integrator and a continuous time DAC. This architecture offers some unique system benefits to the precision data acquisition systems design over the discrete time ADCs.

## EASY TO DRIVE INPUT AND REFERENCE

The switching action of the sample-and-hold circuit used on the discrete time ADCs creates disturbances on the input node. There are two main impacts of the disturbance. The first is the sudden loading of the input node by the sampling capacitor, for which the magnitude of the disturbance is proportional to the input differential voltage/differential time. The second impact is from the charges stored in the parasitic capacitance of the switches being pushed out to the input node when the switch is closed, a

phenomenon known as charge injection or charge kickback. In either case, the sudden change of current flow at the input of the ADC reacts with the finite impedance of the driving circuit to create a disturbance in the form of voltage variation. The profile of the variation depends on the bandwidth and the impedance of the driving circuit.

To achieve the required level of accuracy, at the end of each sampling period, the disturbed input signal must settle to the actual source value within 1 LSB of the ADC target effective resolution, which is particularly challenging with a higher precision or higher input bandwidth requirement.

A common solution to overcome the input settling challenge is to buffer the input with a high bandwidth amplifier with high output driving capability, as shown in Figure 61.

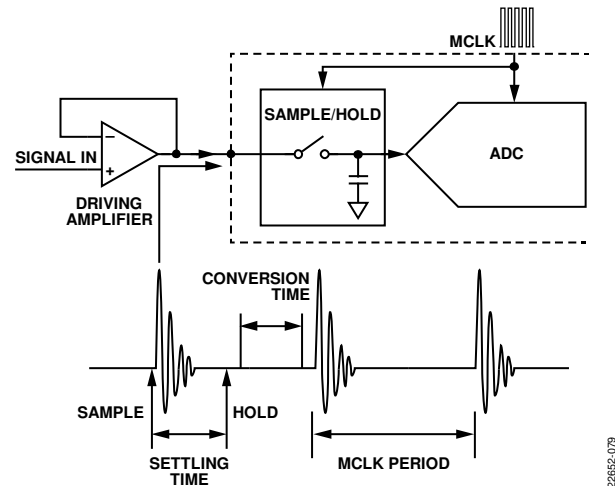


Figure 61. Driving the Input of a Discrete Time ADC

The sample-and-hold circuit is also used by the discrete time ADC on the reference input. A high bandwidth amplifier is also required to drive the ADC reference input.

The drawbacks of using an ADC driving amplifier include the following:

- The amplifier bandwidth must be much higher than the input signal bandwidth, leading to higher power consumption
- The additional components in the signal chain lead to more noise and error
- Additional design complexity to ensure stability when driving the dynamic capacitive load of a discrete time ADC

CTSD architecture allows the AD7134 to have a constant resistive input characteristic. This behavior simplifies the front-end circuit design, allowing lower bandwidth, and low power high performance precision amplifiers to directly drive the ADC.

Similarly, due to the continuous time DAC used in the modulator feedback loop, the AD7134 reference input also has a constant resistive input characteristic, making it possible to drive the ADC reference input directly with a voltage reference IC.

**INHERENT ANTIALIASING FILTER (AAF)**

When sampling an analog sinusoid signal at less than twice of its frequency, reconstruction through interpolation results in a lower frequency signal than the original. This phenomenon is known as aliasing. Figure 62 shows an example of signal aliasing viewed in both the time and frequency domains. The example shows the digital discrete time representations of a 3 kHz, 17 kHz, and 23 kHz signal sampled at 20 kHz are identical. When interpolating the result, the output is always a 3 kHz sine wave, which means that, in this sampling system, the frequency component of the input signal at 17 kHz and 23 kHz appear at 3 kHz in the output.

The aliasing occurs at the point of sampling of the analog signal. The only way to guarantee the matching between input and output signal frequency is to limit the input signal bandwidth before sampling. In the previous example of the frequency component input signal, if the signal is low-pass filtered with a bandwidth of 10 kHz, the interpolated output always matches the filtered input signal. Because the purpose of the low-pass filter is to prevent high frequency signals from aliasing down, the filter is also known as an antialiasing filter.

The signal sampling occurs at the very front of the discrete time ADC in the sample-and-hold circuit. An external antialiasing filter is required in front of the discrete time ADC to protect it against signal aliasing.

The antialiasing filter design requires a fine balance between the aliasing rejection level and the phase and magnitude distortion of the input signal. The extra components also introduce error, noise, and additional power consumption to the signal chain.

Other than being easy to drive, the other major advantage of the CTSD architecture is its inherent antialiasing property. Without the sample-and-hold circuit, the sampling of the analog signal takes place inside the CTSD modulator at the quantizer, after the integrator. This sampling scheme allows the device to take advantage of the low-pass response of the integrator and intrinsically reject signals around the sampling frequency of the modulator. This property provides an inherent aliasing rejection of up to 102.5 dB for the AD7134. As shown in Figure 63, combining the inherent antialiasing response of the CTSD modulator with the low ripple wideband digital filter, the AD7134 is fully protected from the out of band frequency tones.

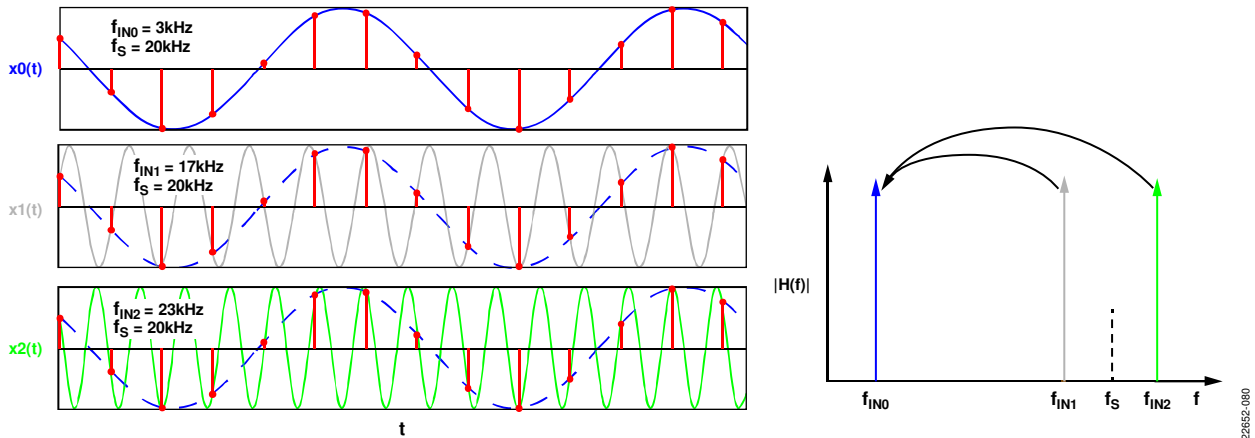


Figure 62. Aliasing Explained with an Example Shown in Both Time and Frequency Domains

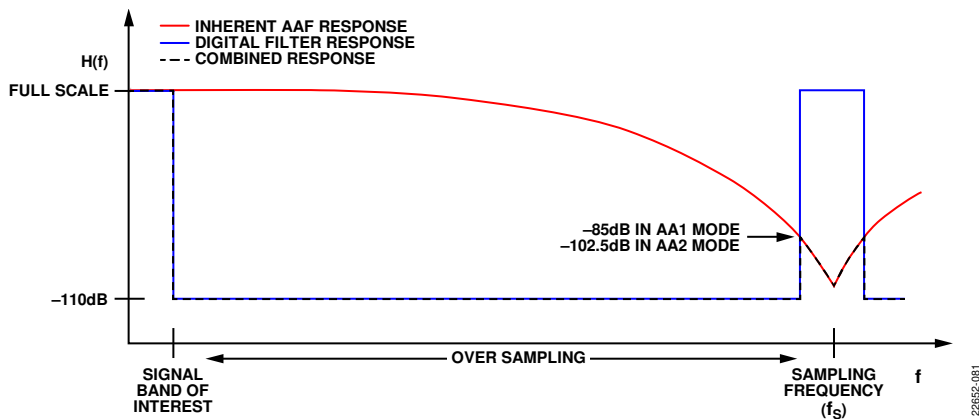


Figure 63. Combined Magnitude Response of the Inherent Antialiasing Filter and the Digital Filter of the AD7134

## ANALOG FRONT-END DESIGN SIMPLIFICATION

The result from the two major benefits of the CTSD architecture described in the Easy to Drive Input and Reference section and the Inherent Antialiasing Filter section is a major simplification of the analog front-end design of the precision medium bandwidth data acquisition signal chain.

Figure 64 shows the analog front-end circuit for a discrete time ADC. For discrete time ADC, in between the precision instrumentation amplifier and the ADC is a third-order antialiasing filter plus an ADC driving circuit based on a fully differential ADC driving amplifier. An additional RC circuit is required at the ADC input to ensure stability of the driver and to help further suppress the kickback. A reference driving circuit based on an operation amplifier is placed between the reference IC and the ADC. The circuit incorporates a second-order low-pass filter to help reduce the wideband noise from the reference source.

Figure 65 shows the signal chain of the AD7134. For the continuous time-based AD7134, the easy to drive and inherent antialiasing property results in significant simplification of the analog front-end design. Other than the apparent area and cost saving, the front-end simplification also removes the noise, error, and instability introduced by the removed circuit, improving the overall performance of the signal chain. As shown in Figure 65, the instrumentation amplifier can directly drive the resistive inputs of the AD7134, and the bandwidth of the amplifier adds to the antialias rejection, making the signal chain an alias free signal chain.

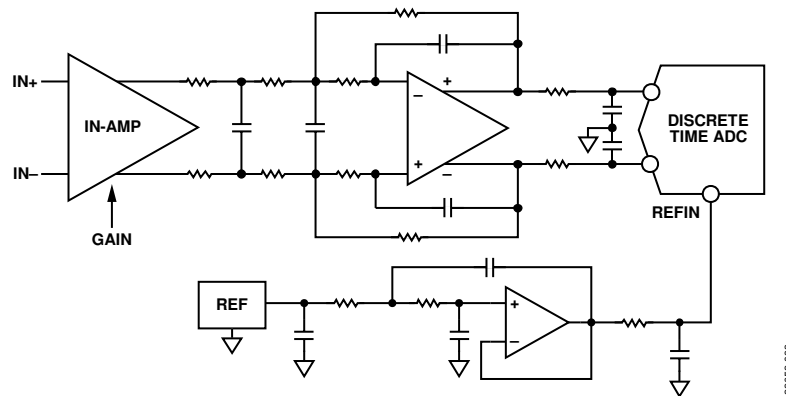


Figure 64. Example Analog Front-End Circuit Design of the Discrete Time-Based ADC

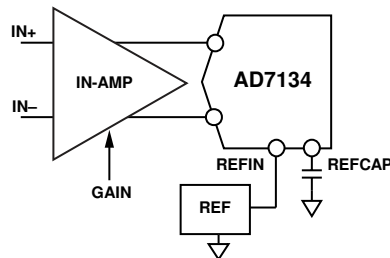


Figure 65. Example Analog Front-End Circuit Design of the AD7134

## NOISE PERFORMANCE AND RESOLUTION

Table 9 to Table 16 contain the data of the noise performance for the wideband 0.433 Hz × ODR filter, wideband 0.10825 Hz × ODR filter, sinc6 filter, and the sinc3 digital filter of the AD7134 for various output data rates and channel averaging settings. The noise values and dynamic range specified are typical for the bipolar input range with an external 4.096 V reference ( $V_{REF}$ ).

The rms noise is measured with shorted analog inputs. The dynamic range is calculated as

$$\text{Dynamic Range (dB)} = 20\log_{10}((2 \times V_{REF}/2\sqrt{2})/(\text{RMS Noise}))$$

The LSB size is calculated as follows:

$$\text{LSB Size} = (2 \times V_{REF})/2^{24}$$

where *LSB Size* is 488 nV with a 4.096 V reference.

**Table 9. Wideband 0.433 Hz × ODR Filter, High Performance Mode Noise Performance vs. Output Data Rate ( $V_{REF} = 4.096$  V)**

| Output Data Rate (kSPS) | −3 dB Bandwidth (kHz) | Single Channel     |                | 2:1 Channel Averaging |                | 4:1 Channel Averaging |                |
|-------------------------|-----------------------|--------------------|----------------|-----------------------|----------------|-----------------------|----------------|
|                         |                       | Dynamic Range (dB) | RMS Noise (μV) | Dynamic Range (dB)    | RMS Noise (μV) | Dynamic Range (dB)    | RMS Noise (μV) |
| 374                     | 161.94                | 107.21             | 12.63          | 110.46                | 8.68           | 113.46                | 6.15           |
| 325                     | 140.73                | 108.09             | 11.41          | 111.21                | 7.96           | 114.25                | 5.61           |
| 285                     | 123.41                | 108.65             | 10.69          | 111.81                | 7.43           | 114.8                 | 5.27           |
| 256                     | 110.85                | 109.21             | 10.03          | 112.5                 | 6.87           | 115.26                | 4.99           |
| 235                     | 101.76                | 109.71             | 9.47           | 112.79                | 6.63           | 115.85                | 4.67           |
| 200                     | 86.60                 | 110.58             | 8.57           | 113.63                | 6.02           | 116.57                | 4.29           |
| 175                     | 75.78                 | 111.12             | 8.05           | 114.27                | 5.6            | 117.25                | 3.97           |
| 128                     | 55.42                 | 112.72             | 6.70           | 115.66                | 4.77           | 118.68                | 3.37           |
| 100                     | 43.30                 | 113.71             | 5.97           | 116.81                | 4.17           | 119.83                | 2.95           |
| 80                      | 34.64                 | 114.80             | 5.27           | 117.9                 | 3.68           | 120.78                | 2.64           |
| 64                      | 27.71                 | 115.83             | 4.68           | 118.87                | 3.29           | 121.87                | 2.33           |
| 32                      | 13.86                 | 118.91             | 3.28           | 121.82                | 2.34           | 124.89                | 1.65           |
| 16                      | 6.93                  | 121.94             | 2.32           | 124.81                | 1.66           | 127.8                 | 1.17           |
| 10                      | 4.33                  | 123.80             | 1.87           | 126.67                | 1.34           | 129.76                | 0.94           |
| 5                       | 2.17                  | 126.68             | 1.34           | 129.55                | 0.96           | 132.34                | 0.69           |
| 2.5                     | 1.08                  | 129.36             | 0.99           | 132.32                | 0.7            | 135.08                | 0.51           |

**Table 10. Wideband 0.433 Hz × ODR Filter, Low Power Mode Noise Performance vs. Output Data Rate ( $V_{REF} = 4.096$  V)**

| Output Data Rate (kSPS) | −3 dB Bandwidth (kHz) | Single Channel     |                | 2:1 Channel Averaging |                | 4:1 Channel Averaging |                |
|-------------------------|-----------------------|--------------------|----------------|-----------------------|----------------|-----------------------|----------------|
|                         |                       | Dynamic Range (dB) | RMS Noise (μV) | Dynamic Range (dB)    | RMS Noise (μV) | Dynamic Range (dB)    | RMS Noise (μV) |
| 374                     | 161.94                | 100.42             | 27.61          | 103.41                | 19.55          | 106.33                | 13.96          |
| 325                     | 140.73                | 102.03             | 22.93          | 105.04                | 16.21          | 107.96                | 11.57          |
| 285                     | 123.41                | 103.21             | 20.01          | 106.37                | 13.9           | 109.21                | 10.03          |
| 256                     | 110.85                | 104.08             | 18.10          | 107.12                | 12.75          | 110.12                | 9.03           |
| 235                     | 101.76                | 104.67             | 16.91          | 107.89                | 11.68          | 110.64                | 8.50           |
| 200                     | 86.60                 | 105.80             | 14.85          | 108.97                | 10.31          | 111.76                | 7.47           |
| 175                     | 75.78                 | 106.64             | 13.48          | 109.79                | 9.37           | 112.55                | 6.82           |
| 128                     | 55.42                 | 108.29             | 11.15          | 111.32                | 7.87           | 114.31                | 5.57           |
| 100                     | 43.30                 | 109.49             | 9.71           | 112.55                | 6.83           | 115.51                | 4.85           |
| 80                      | 34.64                 | 110.58             | 8.57           | 113.54                | 6.09           | 116.47                | 4.34           |
| 64                      | 27.71                 | 111.63             | 7.59           | 114.68                | 5.34           | 117.61                | 3.81           |
| 32                      | 13.86                 | 114.72             | 5.32           | 117.75                | 3.75           | 120.64                | 2.68           |
| 16                      | 6.93                  | 117.69             | 3.78           | 120.78                | 2.64           | 123.71                | 1.88           |
| 10                      | 4.33                  | 119.73             | 2.99           | 122.72                | 2.11           | 125.76                | 1.49           |
| 5                       | 2.17                  | 122.79             | 2.10           | 125.66                | 1.50           | 128.61                | 1.07           |
| 2.5                     | 1.08                  | 125.64             | 1.51           | 128.58                | 1.07           | 131.48                | 0.77           |

Table 11. Wideband 0.10825 Hz × ODR Filter, High Performance Mode Noise Performance vs. Output Data Rate ( $V_{REF} = 4.096\text{ V}$ )

| Output Data Rate (kSPS) | –3 dB Bandwidth (kHz) | Single Channel     |                             | 2:1 Channel Averaging |                             | 4:1 Channel Averaging |                             |
|-------------------------|-----------------------|--------------------|-----------------------------|-----------------------|-----------------------------|-----------------------|-----------------------------|
|                         |                       | Dynamic Range (dB) | RMS Noise ( $\mu\text{V}$ ) | Dynamic Range (dB)    | RMS Noise ( $\mu\text{V}$ ) | Dynamic Range (dB)    | RMS Noise ( $\mu\text{V}$ ) |
| 374                     | 40.49                 | 112.80             | 6.63                        | 116.03                | 4.57                        | 119.01                | 3.24                        |
| 325                     | 35.18                 | 113.57             | 6.07                        | 116.84                | 4.16                        | 119.67                | 3.00                        |
| 285                     | 30.85                 | 114.20             | 5.65                        | 117.37                | 3.91                        | 120.12                | 2.85                        |
| 256                     | 27.71                 | 114.71             | 5.33                        | 117.63                | 3.80                        | 120.71                | 2.66                        |
| 235                     | 25.44                 | 115.14             | 5.07                        | 118.13                | 3.59                        | 121.16                | 2.53                        |
| 200                     | 21.65                 | 115.72             | 4.74                        | 118.88                | 3.29                        | 121.61                | 2.40                        |
| 175                     | 18.94                 | 116.44             | 4.36                        | 119.62                | 3.02                        | 122.37                | 2.20                        |
| 128                     | 13.86                 | 117.76             | 3.75                        | 120.88                | 2.61                        | 123.85                | 1.86                        |
| 100                     | 10.83                 | 118.82             | 3.32                        | 121.9                 | 2.32                        | 124.79                | 1.66                        |
| 80                      | 8.66                  | 119.76             | 2.98                        | 123.06                | 2.03                        | 125.85                | 1.47                        |
| 64                      | 6.93                  | 120.85             | 2.63                        | 123.78                | 1.87                        | 126.78                | 1.32                        |
| 32                      | 3.46                  | 123.64             | 1.91                        | 126.56                | 1.36                        | 129.61                | 0.95                        |
| 16                      | 1.73                  | 126.50             | 1.37                        | 129.30                | 0.99                        | 132.36                | 0.69                        |
| 10                      | 1.08                  | 128.44             | 1.10                        | 131.23                | 0.79                        | 134.15                | 0.56                        |
| 5                       | 40.49                 | 130.91             | 0.83                        | 133.54                | 0.60                        | 136.31                | 0.44                        |
| 2.5                     | 35.18                 | 133.59             | 0.61                        | 136.13                | 0.45                        | 138.84                | 0.33                        |

Table 12. Wideband 0.10825 Hz × ODR Filter, Low Power Mode Noise Performance vs. Output Data Rate ( $V_{REF} = 4.096\text{ V}$ )

| Output Data Rate (kSPS) | –3 dB Bandwidth (kHz) | Single Channel     |                             | 2:1 Channel Averaging |                             | 4:1 Channel Averaging |                             |
|-------------------------|-----------------------|--------------------|-----------------------------|-----------------------|-----------------------------|-----------------------|-----------------------------|
|                         |                       | Dynamic Range (dB) | RMS Noise ( $\mu\text{V}$ ) | Dynamic Range (dB)    | RMS Noise ( $\mu\text{V}$ ) | Dynamic Range (dB)    | RMS Noise ( $\mu\text{V}$ ) |
| 374                     | 40.49                 | 108.46             | 10.94                       | 111.64                | 7.58                        | 114.53                | 5.43                        |
| 325                     | 35.18                 | 109.29             | 9.94                        | 112.34                | 6.99                        | 115.20                | 5.03                        |
| 285                     | 30.85                 | 110.05             | 9.11                        | 113.09                | 6.41                        | 115.90                | 4.64                        |
| 256                     | 27.71                 | 110.46             | 8.69                        | 113.61                | 6.04                        | 116.42                | 4.37                        |
| 235                     | 25.44                 | 110.80             | 8.35                        | 113.97                | 5.79                        | 116.96                | 4.01                        |
| 200                     | 21.65                 | 111.45             | 7.75                        | 114.69                | 5.33                        | 117.66                | 3.79                        |
| 175                     | 18.94                 | 112.26             | 7.06                        | 115.35                | 4.94                        | 118.24                | 3.54                        |
| 128                     | 13.86                 | 113.51             | 6.12                        | 116.6                 | 4.28                        | 119.63                | 3.02                        |
| 100                     | 10.83                 | 114.69             | 5.34                        | 117.6                 | 3.81                        | 120.61                | 2.69                        |
| 80                      | 8.66                  | 115.64             | 4.78                        | 118.64                | 3.38                        | 121.76                | 2.36                        |
| 64                      | 6.93                  | 116.73             | 4.22                        | 119.66                | 3.01                        | 122.54                | 2.16                        |
| 32                      | 3.46                  | 119.81             | 2.96                        | 122.58                | 2.15                        | 125.64                | 1.51                        |
| 16                      | 1.73                  | 122.60             | 2.15                        | 125.58                | 1.52                        | 128.61                | 1.07                        |
| 10                      | 1.08                  | 124.75             | 1.68                        | 127.41                | 1.23                        | 130.45                | 0.86                        |
| 5                       | 40.49                 | 127.37             | 1.24                        | 130.32                | 0.88                        | 133.14                | 0.63                        |
| 2.5                     | 35.18                 | 130.14             | 0.90                        | 132.99                | 0.64                        | 135.84                | 0.46                        |



Table 13. Sinc6 Filter, High Performance Mode Noise Performance vs. Output Data Rate ( $V_{REF} = 4.096\text{ V}$ )

| Output Data Rate (kSPS) | –3 dB Bandwidth (kHz) | Single Channel     |                             | 2:1 Channel Averaging |                             | 4:1 Channel Averaging |                             |
|-------------------------|-----------------------|--------------------|-----------------------------|-----------------------|-----------------------------|-----------------------|-----------------------------|
|                         |                       | Dynamic Range (dB) | RMS Noise ( $\mu\text{V}$ ) | Dynamic Range (dB)    | RMS Noise ( $\mu\text{V}$ ) | Dynamic Range (dB)    | RMS Noise ( $\mu\text{V}$ ) |
| 1496                    | 278.406               | 100.66             | 26.85                       | 104.13                | 18.01                       | 107.07                | 12.83                       |
| 1250                    | 232.63                | 102.98             | 20.56                       | 106.34                | 13.95                       | 109.24                | 10.00                       |
| 1000                    | 186.10                | 105.15             | 16.01                       | 108.48                | 10.90                       | 111.44                | 7.75                        |
| 750                     | 139.58                | 107.33             | 12.46                       | 110.57                | 8.57                        | 113.52                | 6.10                        |
| 500                     | 93.05                 | 109.64             | 9.54                        | 112.87                | 6.57                        | 115.85                | 4.66                        |
| 375                     | 69.79                 | 111.09             | 8.08                        | 114.27                | 5.59                        | 117.32                | 3.94                        |
| 325                     | 60.48                 | 111.94             | 7.32                        | 115.02                | 5.13                        | 118.02                | 3.63                        |
| 256                     | 47.64                 | 113.20             | 6.34                        | 116.20                | 4.48                        | 119.16                | 3.19                        |
| 175                     | 32.57                 | 114.82             | 5.26                        | 117.97                | 3.65                        | 120.90                | 2.61                        |
| 128                     | 23.82                 | 116.32             | 4.42                        | 119.35                | 3.12                        | 122.29                | 2.22                        |
| 80                      | 14.89                 | 118.34             | 3.50                        | 121.50                | 2.43                        | 124.26                | 1.77                        |
| 64                      | 11.91                 | 119.38             | 3.11                        | 122.36                | 2.20                        | 125.46                | 1.54                        |
| 32                      | 5.96                  | 122.38             | 2.20                        | 125.33                | 1.56                        | 128.24                | 1.12                        |
| 10                      | 1.86                  | 126.98             | 1.30                        | 129.87                | 0.92                        | 132.90                | 0.65                        |
| 5                       | 0.93                  | 129.69             | 0.95                        | 132.47                | 0.68                        | 135.29                | 0.49                        |
| 2.5                     | 0.47                  | 131.97             | 0.73                        | 135.31                | 0.49                        | 137.57                | 0.383                       |

Table 14. Sinc6 Filter, Low Power Mode Noise Performance vs. Output Data Rate ( $V_{REF} = 4.096\text{ V}$ )

| Output Data Rate (kSPS) | –3 dB Bandwidth (kHz) | Single Channel     |                             | 2:1 Channel Averaging |                             | 4:1 Channel Averaging |                             |
|-------------------------|-----------------------|--------------------|-----------------------------|-----------------------|-----------------------------|-----------------------|-----------------------------|
|                         |                       | Dynamic Range (dB) | RMS Noise ( $\mu\text{V}$ ) | Dynamic Range (dB)    | RMS Noise ( $\mu\text{V}$ ) | Dynamic Range (dB)    | RMS Noise ( $\mu\text{V}$ ) |
| 1496                    | 278.406               | 84.11              | 180.40                      | 87.30                 | 124.98                      | 90.05                 | 91.06                       |
| 1250                    | 232.63                | 87.78              | 118.22                      | 90.93                 | 82.3                        | 93.92                 | 58.31                       |
| 1000                    | 186.10                | 92.28              | 70.43                       | 95.42                 | 49.04                       | 98.36                 | 34.99                       |
| 750                     | 139.58                | 97.65              | 37.96                       | 100.78                | 26.48                       | 103.61                | 19.12                       |
| 500                     | 93.05                 | 103.33             | 19.74                       | 106.53                | 13.65                       | 109.33                | 9.89                        |
| 375                     | 69.79                 | 101.17             | 25.32                       | 103.98                | 18.32                       | 104.34                | 17.57                       |
| 325                     | 60.48                 | 107.19             | 12.65                       | 110.22                | 8.93                        | 113.13                | 6.38                        |
| 256                     | 47.64                 | 108.60             | 10.76                       | 111.58                | 7.63                        | 114.51                | 5.44                        |
| 175                     | 32.57                 | 110.53             | 8.62                        | 113.63                | 6.03                        | 116.51                | 4.33                        |
| 128                     | 23.82                 | 112.05             | 7.23                        | 115.08                | 5.10                        | 118.06                | 3.62                        |
| 80                      | 14.89                 | 114.25             | 5.61                        | 117.28                | 3.96                        | 120.16                | 2.84                        |
| 64                      | 11.91                 | 115.17             | 5.05                        | 118.21                | 3.56                        | 121.20                | 2.52                        |
| 32                      | 5.96                  | 118.22             | 3.55                        | 121.30                | 2.49                        | 124.23                | 1.78                        |
| 10                      | 1.86                  | 123.03             | 2.04                        | 126.15                | 1.42                        | 129.02                | 1.02                        |
| 5                       | 0.93                  | 125.99             | 1.45                        | 129.11                | 1.01                        | 131.99                | 0.72                        |
| 2.5                     | 0.47                  | 128.91             | 1.04                        | 131.75                | 0.74                        | 134.57                | 0.54                        |

Table 15. Sinc3 Filter, High Performance Mode Noise Performance vs. Output Data Rate ( $V_{REF} = 4.096\text{ V}$ )

| Output Data Rate (kSPS) | –3 dB Bandwidth (kHz) | Single Channel     |                             | 2:1 Channel Averaging |                             | 4:1 Channel Averaging |                             |
|-------------------------|-----------------------|--------------------|-----------------------------|-----------------------|-----------------------------|-----------------------|-----------------------------|
|                         |                       | Dynamic Range (dB) | RMS Noise ( $\mu\text{V}$ ) | Dynamic Range (dB)    | RMS Noise ( $\mu\text{V}$ ) | Dynamic Range (dB)    | RMS Noise ( $\mu\text{V}$ ) |
| 1496                    | 391.503               | 95.32              | 49.64                       | 98.67                 | 33.74                       | 101.46                | 24.48                       |
| 1000                    | 261.70                | 101.62             | 24.03                       | 105.05                | 16.18                       | 107.97                | 11.56                       |
| 750                     | 196.28                | 104.72             | 16.82                       | 108.01                | 11.51                       | 110.97                | 8.19                        |
| 375                     | 98.14                 | 109.56             | 9.63                        | 112.64                | 6.76                        | 115.59                | 4.81                        |
| 187.5                   | 49.07                 | 112.88             | 6.58                        | 116.11                | 4.53                        | 119.04                | 3.23                        |
| 128                     | 33.50                 | 114.76             | 5.29                        | 117.81                | 3.72                        | 120.72                | 2.66                        |
| 64                      | 16.75                 | 117.83             | 3.72                        | 120.91                | 2.60                        | 123.88                | 1.85                        |
| 32                      | 8.37                  | 120.91             | 2.61                        | 124.10                | 1.80                        | 126.87                | 1.31                        |
| 16                      | 4.19                  | 125.74             | 1.50                        | 128.66                | 1.06                        | 131.54                | 0.76                        |
| 5                       | 1.31                  | 128.29             | 1.11                        | 131.34                | 0.78                        | 134.17                | 0.56                        |
| 2.5                     | 0.654                 | 130.89             | 0.83                        | 133.60                | 0.60                        | 136.30                | 0.44                        |
| 1.25                    | 0.327                 | 132.91             | 0.66                        | 135.52                | 0.48                        | 138.08                | 0.36                        |
| 0.625                   | 0.164                 | 134.66             | 0.54                        | 137.28                | 0.39                        | 139.79                | 0.29                        |
| 0.06                    | 0.016                 | 137.59             | 0.38                        | 139.89                | 0.29                        | 142.62                | 0.21                        |
| 0.05                    | 0.013                 | 137.46             | 0.39                        | 139.49                | 0.30                        | 141.81                | 0.23                        |
| 0.01                    | 0.003                 | 137.22             | 0.40                        | 140.07                | 0.28                        | 141.65                | 0.23                        |

Table 16. Sinc3 Filter, Low Power Mode Noise Performance vs. Output Data Rate ( $V_{REF} = 4.096\text{ V}$ )

| Output Data Rate (kSPS) | –3 dB Bandwidth (kHz) | Single Channel     |                             | 2:1 Channel Averaging |                             | 4:1 Channel Averaging |                             |
|-------------------------|-----------------------|--------------------|-----------------------------|-----------------------|-----------------------------|-----------------------|-----------------------------|
|                         |                       | Dynamic Range (dB) | RMS Noise ( $\mu\text{V}$ ) | Dynamic Range (dB)    | RMS Noise ( $\mu\text{V}$ ) | Dynamic Range (dB)    | RMS Noise ( $\mu\text{V}$ ) |
| 1496                    | 391.503               | 76.68              | 424.32                      | 79.72                 | 299.01                      | 82.62                 | 214.21                      |
| 1000                    | 261.70                | 85.34              | 156.58                      | 88.44                 | 109.66                      | 91.26                 | 79.17                       |
| 750                     | 196.28                | 91.30              | 78.89                       | 87.19                 | 126.6                       | 97.41                 | 39.00                       |
| 375                     | 98.14                 | 98.67              | 33.77                       | 101.30                | 24.94                       | 103.42                | 19.52                       |
| 187.5                   | 49.07                 | 108.35             | 11.08                       | 111.42                | 7.78                        | 114.42                | 5.50                        |
| 128                     | 33.50                 | 110.49             | 8.65                        | 113.50                | 6.12                        | 116.36                | 4.40                        |
| 64                      | 16.75                 | 113.73             | 5.96                        | 116.70                | 4.23                        | 119.69                | 3.00                        |
| 32                      | 8.37                  | 116.75             | 4.21                        | 119.73                | 2.98                        | 122.74                | 2.11                        |
| 16                      | 4.19                  | 121.75             | 2.37                        | 124.65                | 1.69                        | 127.7                 | 1.19                        |
| 5                       | 1.31                  | 124.63             | 1.70                        | 127.59                | 1.20                        | 130.54                | 0.86                        |
| 2.5                     | 0.654                 | 127.47             | 1.23                        | 130.24                | 0.89                        | 133.21                | 0.63                        |
| 1.25                    | 0.327                 | 130.07             | 0.91                        | 133.05                | 0.64                        | 135.59                | 0.48                        |
| 0.625                   | 0.164                 | 132.59             | 0.68                        | 135.23                | 0.50                        | 137.85                | 0.37                        |
| 0.06                    | 0.016                 | 137.95             | 0.37                        | 140.07                | 0.28                        | 141.77                | 0.23                        |
| 0.05                    | 0.013                 | 137.87             | 0.37                        | 139.98                | 0.29                        | 141.97                | 0.23                        |
| 0.01                    | 0.003                 | 138.06             | 0.36                        | 140.67                | 0.26                        | 141.78                | 0.23                        |

## CIRCUIT INFORMATION

### CORE SIGNAL CHAIN

Each ADC channel on the AD7134 has an identical signal path from the analog input pins to the data interface. Each ADC channel has its own CTSD modulator that oversamples the analog input and passes the digital representation to the digital filter block. The data is filtered, scaled for gain and offset (depending on user settings), and then output on the data interface. Control of the flexible settings for the signal chain is provided by either using the  $\overline{\text{pin}}$  control or the SPI control set at power-up by the state of the  $\overline{\text{PIN}}$ /SPI input pin.

The ADC can use up to a 5 V reference and converts the differential voltage between the analog inputs ( $\text{AINx+}$  and  $\text{AINx-}$ ) into a digital output. The analog input accepts only differential input. The ADC converts the voltage difference between the analog input pins into a digital code on the output. Using a common-mode voltage of  $V_{\text{REF}}/2$  for the analog inputs,  $\text{AINx+}$  and  $\text{AINx-}$ , maximizes the ADC input range. The 24-bit conversion result is in twos complement, MSB first format. See Table 17 for more details.

### ANALOG INPUTS

#### Input Structure

Due to the CTSD architecture, the AD7134 has a pure resistive input, with a simplified input structure diagram, as shown in Figure 66. The ADC supports only fully differential input signals. The input impedance has a differential resistance value of 6.25 k $\Omega$ . Internally, both  $\text{AINx+}$  and  $\text{AINx-}$  are biased to  $V_{\text{REF}}/2$  through the internal resistor network. The AD7134 achieves optimal performance with a differential input signal that has a common-mode voltage equal to  $V_{\text{REF}}/2$ . In Figure 66,  $C_{\text{IN}}$  means input capacitance and  $R_{\text{IN}}$  means input resistance.

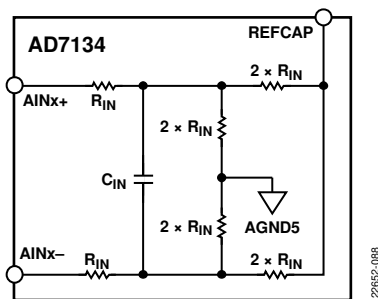


Figure 66. ADC Input Structure

Table 17. Output Codes and Ideal Input Voltages

| Description             | Analog Input ( $\text{AINx+} - \text{AINx-}$ ), $V_{\text{REF}} = 4.096 \text{ V}$ | Digital Output Code, Twos Complement (Hex) |
|-------------------------|--|--|
| Full Scale (FS) – 1 LSB | 4.095999512 V  | 0x7FFFFFFF                                 |
| Midscale + 1 LSB        | 488 nV   | 0x000001                                   |
| Midscale                | 0 V  | 0x000000                                   |
| Midscale – 1 LSB        | –488 nV  | 0xFFFFF7                                   |
| –FS + 1 LSB             | –4.095999512 V   | 0x800001                                   |
| –FS                     | –4.096 V   | 0x800000                                   |

When the device is powered down, with the  $\overline{\text{PDN}}$  pin low, in sleep mode, or with the  $\text{PWRDN\_CHx}$  bits, the input behaves with high impedance.

#### Input Voltage Range

The resistive input structure of the AD7134 allows its input pins to tolerate wide input voltage swings without damaging the device. With the ADC full-scale input being  $\pm V_{\text{REF}}$ , each of the ADC input pins can accept absolute input voltages from 0 V to 5 V.

When the individual ADC input channel is powered down, the input is high impedance.

#### Input Common-Mode Range

The AD7134 supports an input common-mode range from  $V_{\text{REF}}/2$  to  $\text{AVDD5}/2$ . Optimal performance is achieved with the input common-mode level equal to half of the reference input voltage.

### VCM OUTPUT

The AD7134 provides a buffered common-mode voltage output on the VCM pin. This output can shift the level of the analog input signals. By incorporating the VCM buffer into the ADC, the AD7134 reduces component count and board space.

In pin control mode, the VCM potential is fixed to  $V_{\text{REF}}/2$  and is enabled by default.

In SPI control mode, the user has the option to program the VCM output voltage level from  $V_{\text{REF}}/20$  to  $19 \times V_{\text{REF}}/20$ , or  $\text{AVDD5}/2$ . The user can also choose to disable the VCM output if not used in SPI control mode.

The VCM output level can be configured through the  $\text{VCMBUF\_REF\_DIV\_SEL}$  bits and the  $\text{VCMBUF\_REF\_SEL}$  bit. The VCM output can be enabled or disabled using the  $\text{PWRDN\_VCMBUF}$  bit. When disabled, the VCM behaves with high impedance.

When driving capacitive loads larger than 0.1  $\mu\text{F}$ , it is recommended to place a 50  $\Omega$  series resistor between the VCM pin and the capacitive load to ensure the stability of the output buffer.

## REFERENCE INPUT

Similar to the ADC inputs, the AD7134 reference input is also resistive, which allows the external reference IC to drive the AD7134 directly without the need of a reference buffer. The user can directly connect the external reference source to the REFCAP pin of the AD7134.

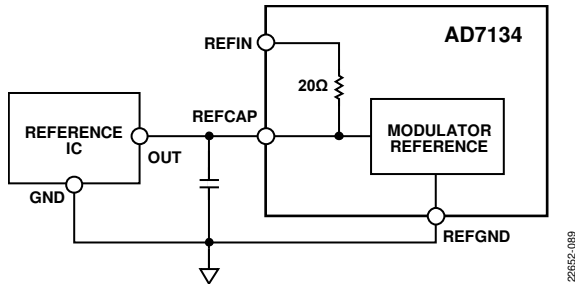


Figure 67. Direct Reference Input Connection to REFCAP Pin

The user can reduce the noise on the reference source by filtering the reference signal. An internal  $20\ \Omega$  resistor between the REFIN pin and the REFCAP pin enables the user to form a first-order RC filter by connecting a capacitor on the REFCAP pin.

See the Reference Noise Filtering section for examples on how to design the reference filter.

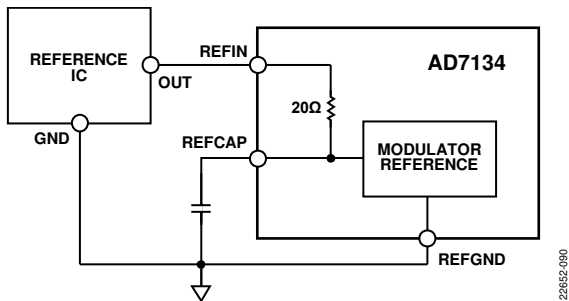


Figure 68. Reference Input Connection Using REFIN Pin

The series resistor creates a small voltage drop that varies with the device mode of operation. In SPI control mode, the user can configure the device to autocorrect this drop in different operating modes by setting the REFIN\_GAIN\_CORR\_EN bit to 1. The reference input current reduces by 1/4 with the disable of each individual ADC channel. This reduction in current is also accounted for with the reference autocorrection function.

The autocorrection function is disabled in pin control mode.

The reference input behaves with high impedance when the device is powered down or in power down mode with the PDN pin low.

## CLOCK INPUT

The AD7134 use an internal oscillator during the initial power-up configuration. After the AD7134 has completed the start-up routine, a clock handover to the externally applied CLKIN occurs.

The AD7134 supports two master clock input options. The device can accept an external CMOS clock signal or generate the clock signal using an external crystal. The clock source is determined at power-on by the state of the CLKSEL pin.

Tie the CLKSEL pin to the IOVDD pin and connect an external crystal between the XTAL1 pin and the XTAL2/CLKIN pin to enable the crystal clock option. Tie the CLKSEL pin to the IOGND pin and connect an external CMOS clock signal to the XTAL2/CLKIN pin to enable the CMOS clock option.

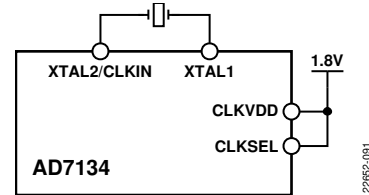


Figure 69. Master Clock Provided by a Crystal

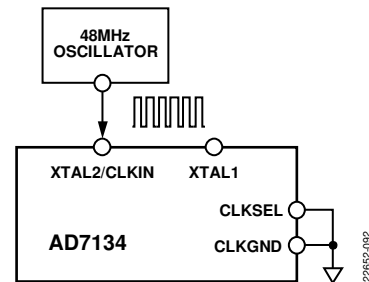


Figure 70. Master Clock Provided by an Oscillator

## XCLKOUT OUTPUT

When using the crystal clock option, a buffered output from the internal crystal oscillator can be made available on the XCLKOUT pin. Distribute this CMOS clock signal to other AD7134 devices in the same system to allow multiple AD7134 devices to operate from a single external crystal. The XCLKOUT pin can drive 45 pF of load.

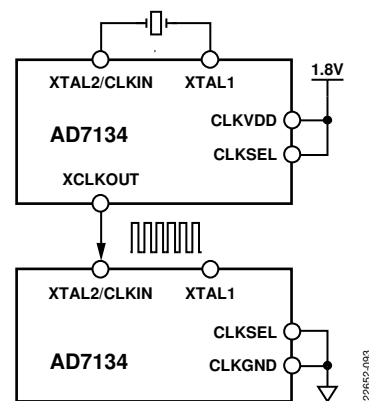


Figure 71. Provide Master Clock to Multiple Devices from a Single Crystal

The XCLKOUT output is enabled by default in pin control mode if the crystal clock options are selected. The XCLKOUT output is disabled in pin control mode if the CMOS clock option is selected.

The XCLKOUT output is disabled by default in SPI control mode and can be enabled by writing 1 to the XCLKOUT\_EN bit.

**POWER OPTIONS**

**Operating Power Modes**

Depending on the bandwidth of interest for the measurement, the AD7134 allows the user to trade measurement bandwidth with power consumption or resolution through its two selectable power modes: high performance and low power. The low power mode operates with half the modulator clock frequency, resulting in comparable noise performance to the high performance mode at half of the output data rate and 40% of power saving. For details of the performance difference between the two modes, see the Noise Performance and Resolution section.

**Channel Power-Down**

In SPI control mode, the four ADC channels can be individually powered down to save power when not used. The PWRDN\_CHx bits control the power-down of each channel. Powering down an ADC channel reduces the supply current and the input current. The input of a powered down channel goes high-Z. The reference input current reduces by 1/4 with the power-down of each ADC channel.

**Sleep Mode**

Sleep mode can be activated in SPI control mode by setting the SLEEP\_MODE\_EN bit to 1. In this mode, the device powers down all the blocks except the digital LDO regulator and it retains its on-chip register values. The typical power consumption in this mode is 15 mW. The device can resume full operation within 100 μs after exiting this mode. Both the reference input and input channels go high-Z in sleep mode.

**Full Power-Down**

The full power-down mode is activated by holding the PDN pin low. All internal blocks are powered down in this mode. The typical power consumption in this mode is 1 mW. The device requires a power-up time of 10 ms after exiting this mode. After exiting this mode, the device registers are reset to the default value. Both the reference input and input channels go high-Z in sleep mode.

**RESET**

When reset, the AD7134 restores the internal register values to the default and resets the internal logics and functional blocks. Two methods exist for the user to reset the AD7134: through a hard reset by pulling the RESET pin low, or through a software reset by writing 1 to SOFT\_RESET (self clears).

**ASYNCHRONOUS SAMPLE RATE CONVERTER**

One unique property of the CTSD modulator architecture is having a fixed time constant. As a result, the AD7134 device operates at a fixed modulator clock frequency.

To facilitate the accurate adjustment of the output data rate, the AD7134 features a digitally programmable ASRC.

The ASRC is placed between the modulator and the digital filter of each ADC channel. The ASRC has the following two inputs:

- Data that comes at the MCLK rate from the modulator
- ODR input, which is either an external asynchronous signal (slave) or a fractional value (master)

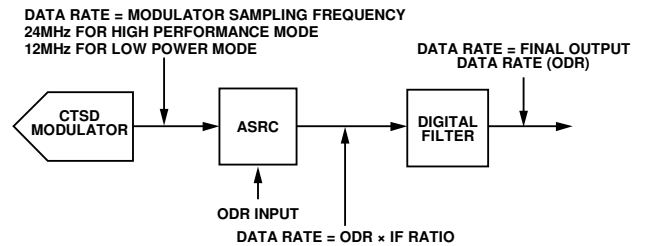


Figure 72. Data Rate at Each Stage of Conversion Path

The digital PLL present in the ASRC block tracks and locks on the ODR input and generates a fractional ratio. The ASRC works through interpolation and resampling of the modulator output at a fractional ratio to the sampling frequency of the modulator. The interpolation factor depends on the ODR selected. The fractional sample rate conversion of the ASRC allows the final ODR to be asynchronous to the sampling clock of the modulator. The output of the ASRC is then decimated by an integer in the digital filter to produce the final ODR.

The ASRC only response depends on the ODR selected and has a notch at the value of interpolation factor × ODR frequency. The interpolation factor values for the various ODRs are shown in Table 18.

**Table 18. Interpolation Factor Values for Different ODR Ranges**

| ODR Range                  | Interpolation Factor Value |
|----------------------------|----------------------------|
| 750 kSPS to 1.496 MSPS     | 8                          |
| 375 kSPS to 749.999 kSPS   | 16                         |
| 366.99 SPS to 374.999 kSPS | 32                         |
| 10 SPS to 366.99 SPS       | 1024                       |

For example, the ASRC response for an ODR of 374 kSPS shows a notch at 32 × 374 kHz = 11.968 MHz, as shown in Figure 73.

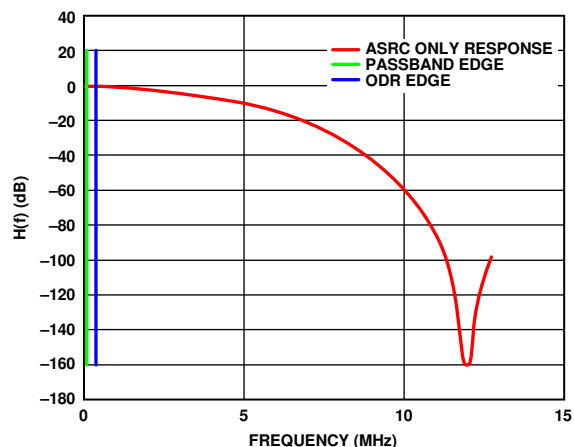


Figure 73. ASRC Only Response for ODR = 374 kSPS

Similarly, the ASRC response for an ODR of 1496 kSPS shows a notch at  $8 \times 1496 \text{ kHz} = 11.968 \text{ MHz}$ , as shown in Figure 74.

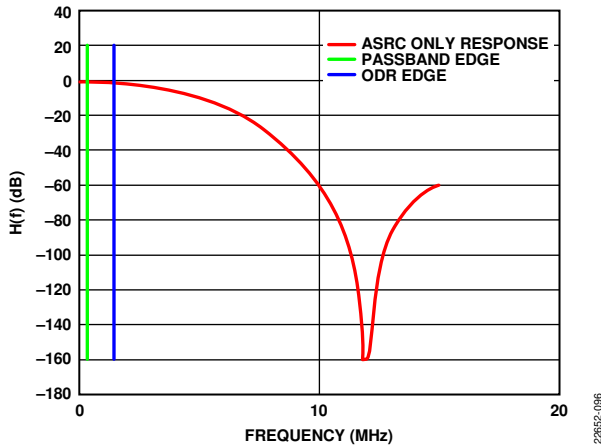


Figure 74. Response for ODR of 1496 kSPS

The available output data rate range varies based on the digital filter type and the ASRC mode selected (see the Digital Filters section for more information).

The ASRC on the AD7134 has the following two modes of operation:

- In master mode, the ODR pin is output and the ODR is set through the pin configuration or a register write.
- In slave mode, the ODR pin is input to the AD7134 and the ODR is set with an external clock source.

**ASRC Master Mode**

In master mode, the ASRC resamples the interpolated modulator output at a fixed ratio to the modulator clock (see Figure 75). The ratio is internally calculated based on the user setting of the final ODR. The user can configure the ODR through configuration of the ODR pin in pin control mode or through register configuration in SPI control mode.

In ASRC master mode, the ODR pin behaves as an output. It produces a pulse train signal in the frequency of the output data rate. The ADC output data is made available for sampling with respect to the ODR signal.

For details of the ASRC master mode output data rate setting, see the ASRC Master Mode section.

**ASRC Slave Mode**

In slave mode, the ODR pin behaves as an input (see Figure 76). The user sets the ODR by providing a clock or pulse train at the desired ODR frequency ( $f_{ODR}$ ) to the ODR pin. The AD7134 measures the ODR frequency using the input signal rising edge. An internal digital PLL tracks the ODR pin input signal frequency and uses it to set the resampling rate of the ASRC. The ADC output data is made available for sampling with respect to the ODR signal.

The user must provide continuous cycles of the ODR signal until the PLL is locked by checking the STAT\_PLL\_LOCK bit and then reading the data. Any change in the ODR value causes the PLL to unlock and lock back again and requires a wait time before reading data.

The user must also ensure that the jitter on the ODR pin is not more than 100 ns p-p to ensure that the performance is not degraded.

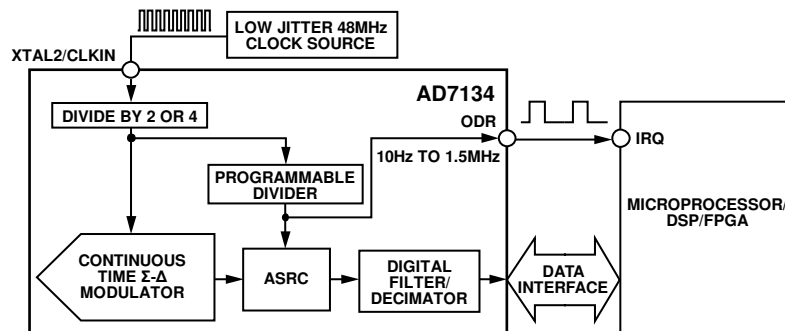


Figure 75. ASRC Master Mode Functional Diagram

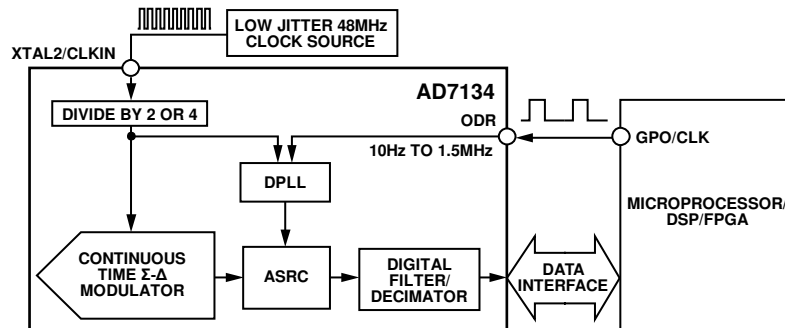


Figure 76. ASRC Slave Mode Functional Diagram

**DIGITAL FILTERS**

The AD7134 offers four types of digital filters: sinc3, sinc6, and two wideband filters. The sinc3 filter type includes an additional setting with 50 Hz/60 Hz rejection (see Table 19). In SPI control mode, these filters can be chosen on a per channel basis. In pin control mode, only one filter can be selected for all channels.

The digital filters available can be operated at any output data rate within the range mentioned in Table 19, allowing the user to choose the optimal input bandwidth and speed of the conversion vs. the desired power mode or resolution.

**Sinc Filters**

The sinc filters on the AD7134 employ a cascaded integrator comb (CIC) topology to produce a response similar to a sinc function, equivalent to a running averaging operation on the output samples from the ASRC. The sinc filters enable a low latency signal path, useful for applications such as time domain analysis, measurement of dc inputs, and for control loops. Two types of sinc filters are available on the AD7134. The sinc6 filter offers a balance between noise rejection and latency, whereas the sinc3 filter offers the minimum latency path and supports a wide ODR range down to 10 SPS.

The sinc6 filter has a -3 dB bandwidth of  $0.1861 \times \text{ODR}$ , and the sinc3 filter has a -3 dB bandwidth of  $0.2617 \times \text{ODR}$ . The Noise Performance and Resolution section contains the noise performance for the sinc filters across power modes and ODR values.

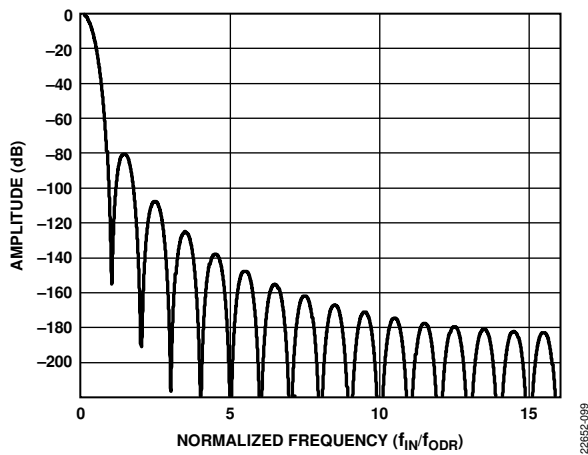


Figure 77. Sinc6 Filter Frequency Response

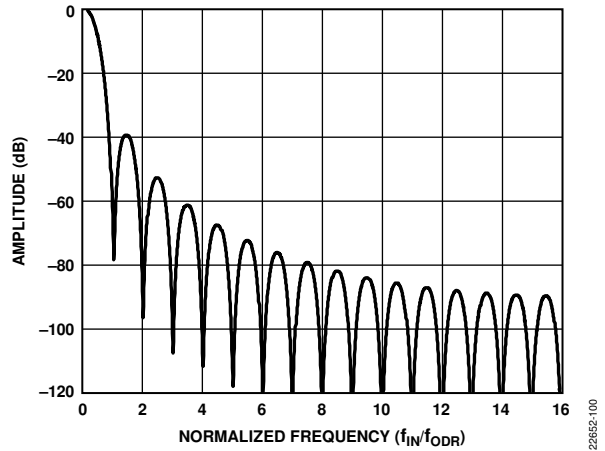


Figure 78. Sinc3 Filter Frequency Response

The settling of the sinc6 filter is  $6.5/\text{ODR}$ . For a 374 kSPS ODR, the time to fully settled data is  $17.37 \mu\text{s}$ .

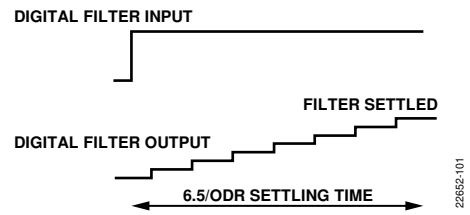


Figure 79. Sinc6 Filter Step Response

The settling of the sinc3 filter is  $3.5/\text{ODR}$  cycles. Therefore, for a 374 kSPS ODR, the time to fully settled data is  $9.35 \mu\text{s}$ .

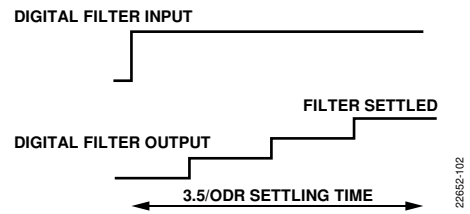


Figure 80. Sinc3 Filter Step Response

**Table 19. Digital Filter Options**

| Filter Name  | -3 dB Bandwidth (Hz)       | ODR Range              | Description   |
|--|----------------------------|------------------------|---|
| Sinc3 Filter   | $0.2617 \times \text{ODR}$ | 0.01 kSPS to 1496 kSPS | Fast settling   |
| Sinc3 Filter with 50 Hz/60 Hz Rejection  | $0.2753 \times \text{ODR}$ | 0.01 kSPS to 1496 kSPS | Fast settling with simultaneous 50 Hz and 60 Hz rejection when ODR = 50 SPS |
| Sinc6 Filter   | $0.1861 \times \text{ODR}$ | 2.5 kSPS to 1.496 MSPS | Balancing settling with rejection   |
| Wideband $0.433 \text{ Hz} \times \text{ODR}$ Filter   | $0.433 \times \text{ODR}$  | 2.5 kSPS to 374 kSPS   | Wideband low ripple filter  |
| Wideband $0.10825 \text{ Hz} \times \text{ODR}$ Filter<br>(Available Only in SPI Control Mode) | $0.108 \times \text{ODR}$  | 2.5 kSPS to 374 kSPS   | Wideband low ripple filter with lower bandwidth                             |

### Simultaneous 50 Hz and 60 Hz Rejection

Because the sinc filter rejects signals at the frequency around integer multiples of the ODR, it can be used to reject undesired interference at a specific frequency higher than the input band of interest. Because the sinc3 filter supports an ODR down to 10 SPS, a typical application for the sinc3 filter is to make dc to low bandwidth measurements while rejecting line frequencies at 50 Hz or 60 Hz.

Figure 81 shows the frequency response of the sinc3 filter when the output data rate is programmed to 50 SPS. The sinc3 filter provides 102 dB rejection at 50 Hz  $\pm$  1 Hz.

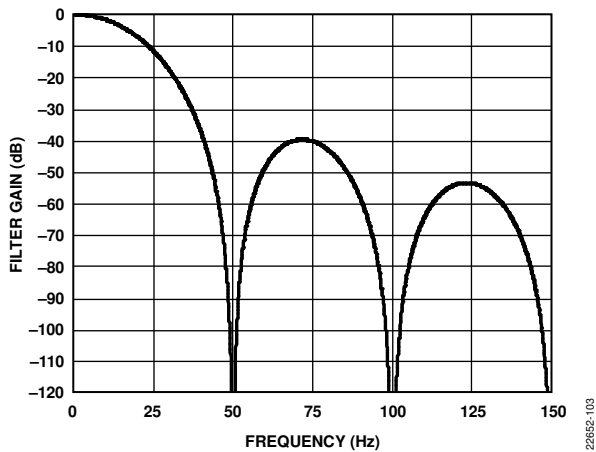


Figure 81. Sinc3 and Sinc6 Filter Response (ODR = 50 SPS)

Figure 82 shows the frequency response of the sinc3 filter when the output data rate is programmed to 60 SPS. The sinc3 filter provides 106 dB rejection at 60 Hz  $\pm$  1 Hz.

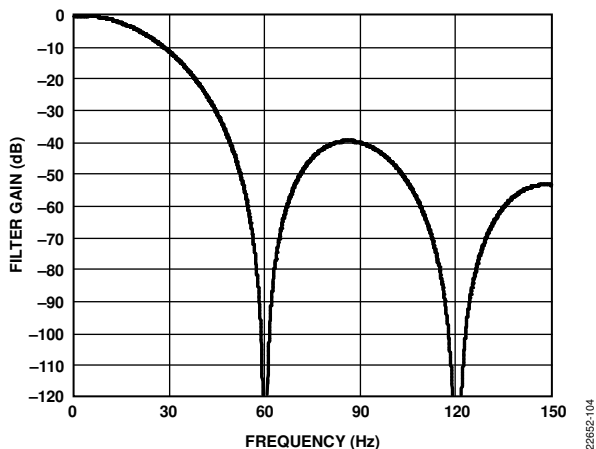


Figure 82. Sinc3 and Sinc6 Filter Response (ODR = 60 SPS)

When the output data rate is 10 SPS, simultaneous 50 Hz and 60 Hz rejection is obtained. The sinc3 filter provides 102 dB rejection at 50 Hz  $\pm$  1 Hz and 105 dB at 60 Hz  $\pm$  1 Hz.

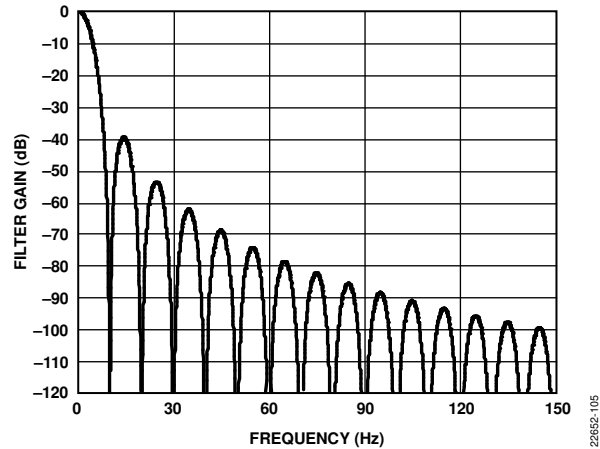


Figure 83. Sinc3 and Sinc6 Filter Response (ODR = 10 SPS)

Simultaneous 50 Hz and 60 Hz rejection can also be achieved by selecting the sinc3 and 50 Hz/60 Hz rejection filter path. When the sinc3 filter places a notch at 50 Hz, the 50 Hz/60 Hz rejection postfilter places a first-order notch at 60 Hz. The output data rate is 50 SPS. Figure 84 shows the frequency response of the sinc3 and 50 Hz/60 Hz rejection filter path. The rejection at 50 Hz and 60 Hz ( $\pm$  1 Hz) is in excess of 67 dB.

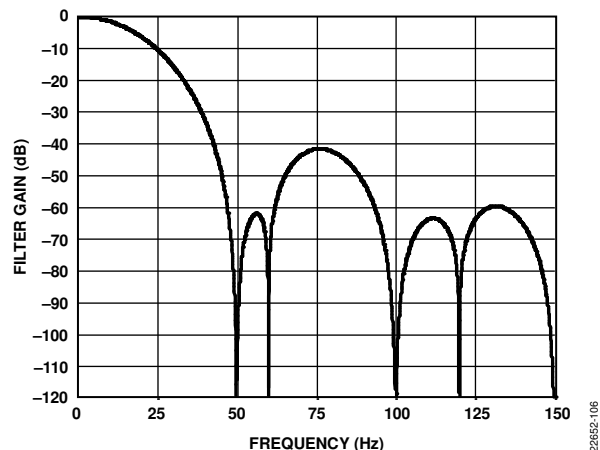


Figure 84. Sinc3 and 50 Hz/60 Hz Rejection Filter Response (ODR = 50 SPS)

### Wideband Low Ripple Filter

The wideband low ripple filter has a low ripple pass band, narrow transition band, and high stop band rejection. The filter response is close to an ideal brick wall filter, making it ideal for frequency domain measurement and analysis.

Two wideband low ripple filter options are available on the AD7134: one filter has a  $-3$  dB corner at  $0.433 \text{ Hz} \times \text{ODR}$ , and the other filter has a  $-3$  dB corner at  $0.10825 \text{ Hz} \times \text{ODR}$ .

Both wideband low ripple filter options offer a pass-band ripple of  $32 \mu\text{dB}$  and a stop band attenuation of  $-110$  dB. For noise performance and resolution, see the Noise Performance and Resolution section.



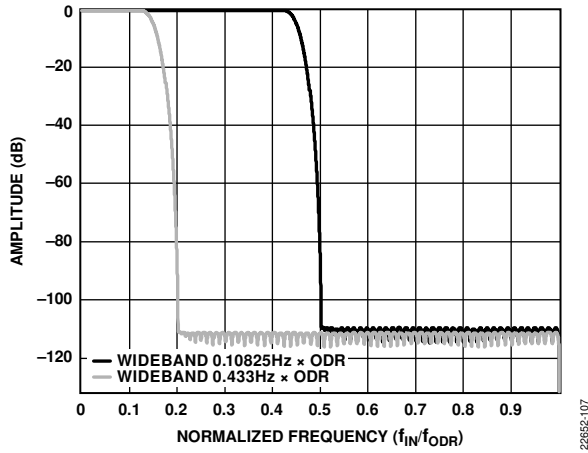


Figure 85. Low Ripple Wideband 0.433 Hz × ODR Filter and Wideband 0.10825 Hz × ODR Filter Frequency Response

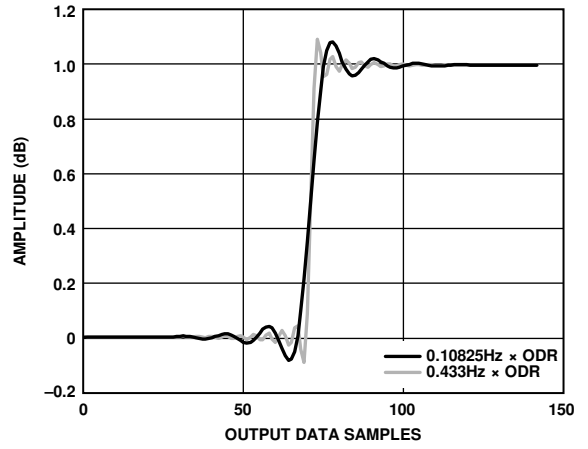


Figure 87. Low Ripple Wideband 0.433 Hz × ODR Filter and Wideband 0.10825 Hz × ODR Filter Step Response

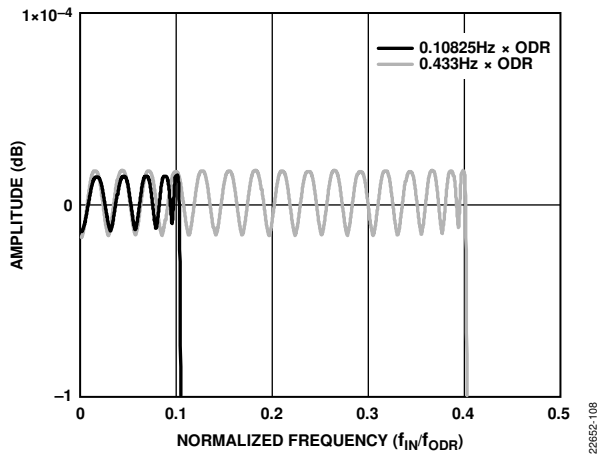


Figure 86. Low Ripple Wideband 0.433 Hz × ODR Filter and Wideband 0.10825 Hz × ODR Filter Pass-Band Ripple

## QUICK START GUIDE

The AD7134 offers users a multichannel platform measurement solution for ac and dc signal processing. Flexible filtering allows the AD7134 to be configured to simultaneously sample ac and dc signals on a per channel basis. The ASRC allows users to granularly set the output data rate controlling the input bandwidth of the measurement. This ability, coupled with the flexibility of the digital filter, allows the user to choose the right application settings and meet latency, bandwidth, and performance targets. Key capabilities that allow users to choose the AD7134 as their platform high resolution ADC are highlighted as follows:

- Four fully differential analog inputs
- Fast throughput simultaneous sampling ADCs catering for input signals up to 391 kHz
- Two selectable power modes (high performance and low power) for scaling the current consumption and input bandwidth of the ADC to achieve optimal measurement efficiency

- Wideband, low ripple, digital filter for ac measurement
- Fast sinc3 filter for precision low frequency, low latency measurement
- Two ASRC modes (master mode and slave mode) allow user flexibility in digital interface
- Two antialias modes enabling the user to choose higher levels of alias rejection
- Choice of SPI or pin strapped configuration option
- Offset, gain, and phase calibration registers per channel
- Common-mode voltage output buffer to set the common-mode voltage of the input
- On-board 1.8 V LDO regulators for single-supply operation

Refer to Figure 88 and Table 20 for the typical connections and minimum requirements to start using the AD7134.

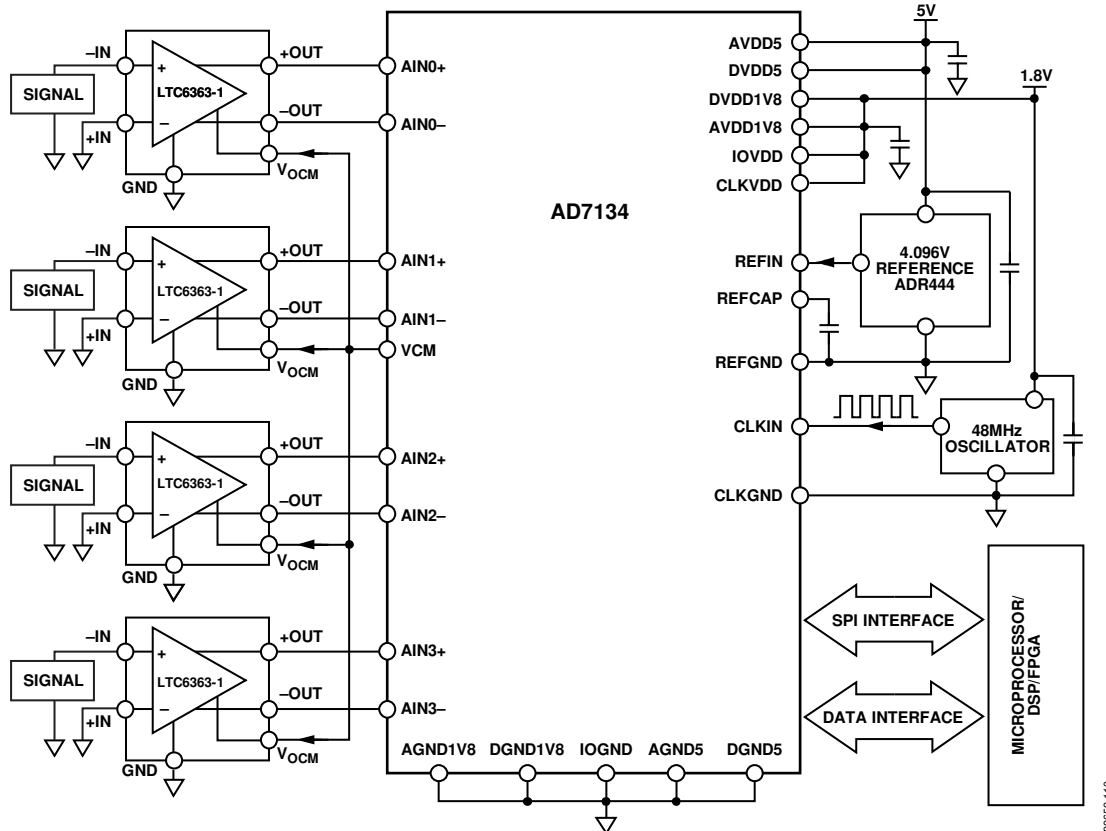


Figure 88. Typical Connections Diagram

Table 20. Requirements to Operate the AD7134

| Requirement        | Description  |
|--------------------|--|
| Power Supplies     | 5 V AVDD5 and DVDD5 supply, 1.8 V – IOVDD, CLKVDD, AVDD1V8, and DVDD1V8 (LT8606, LT8607) |
| External Reference | 4.096 V or 5 V (ADR444/ADR445)   |
| Input Stage        | AD8421, ADA4075-2, ADA4945-1, LTC6363  |
| External Clock     | Crystal or a CMOS/LVDS clock for the ADC modulator sampling                              |
| FPGA or DSP        | 1.65 V to 1.95 V digital I/O level   |

## STANDALONE MODE

The user has a digital host without an SPI interface and needs a –3 dB input bandwidth of 102.4 kHz. The user also desires a flat pass-band response with robust data interface. The recommended scheme is pin controlled master mode. The 102.4 kHz input bandwidth with flat pass band can be achieved by using a  $0.433 \times \text{ODR}$  FIR filter. The minimum ODR needed can be calculated as input bandwidth =  $0.433 \times \text{ODR}$ . Therefore, the minimum ODR needed is 237 kSPS. From Table 28, the closest ODR value of 256 kSPS can be programmed.

The robust interface calls for using the CRC. Therefore, the frame size is 24 data bits + 8-bit header that includes a 6-bit CRC and a 2-bit status.

The DCLK value required is  $>(\text{Frame Size} + 6) \times \text{ODR}$ , giving the user a value of 9.7 MHz. From Table 30, the closest DCLK option is 12 MHz.

The settings to be configured are pin control mode control, ASRC master, high performance mode, gated DCLK output, 32-bit data output, 256 kSPS ODR, 12 MHz DCLK,  $0.433 \times \text{ODR}$  filter, external LDO regulator, and 4-channel output.

Refer to the Device Configuration section for programming these settings.

**Table 21. Configuration 1 Hardware Settings**

| Pin Function                           | Supply/Level         | Comments                         |
|--|----------------------|----------------------------------|
| AVDD5, DVDD5                           | 5 V                  | Supply                           |
| IOVDD, LDOIN, AVDD1V8, DVDD1V8, CLKVDD | 1.8 V                | Supply                           |
| $\overline{\text{PIN}}/\text{SPI}$     | Low                  | Pin control                      |
| CLKSEL                                 | High                 | Crystal input                    |
| MODE                                   | High                 | ASRC master                      |
| DCLKMODE                               | Low                  | Gated DCLK                       |
| DCLKIO                                 | High                 | DCLK output                      |
| FILTER1, FILTER0                       | Low, low             | $0.433 \times \text{ODR}$ filter |
| FORMAT1, FORMAT0                       | High, low            | 4-channel output                 |
| FRAME1, FRAME0                         | High, high           | 32-bit output                    |
| PWRMODE                                | High                 | High performance                 |
| DCLKRATE2, DCLKRATE1, DCLKRATE0        | Low, low, high       | 12 MHz DCLK                      |
| DEC3, DEC2, DEC1, DEC0                 | Low, low, high, high | 256 kSPS ODR                     |

## LOW LATENCY SYNCHRONOUS DATA ACQUISITION

The user has an input signal bandwidth of 250 kHz and needs a 24-bit output with minimum latency. There are eight channels and the user needs tight synchronization between the channels.

The recommended scheme is to use two devices in SPI controlled slave mode. The external ODR signal can synchronize both devices with a digital interface reset issued simultaneously. See the Multidevice Synchronization section for more details.

The 250 kHz input bandwidth with minimum latency can be achieved by the sinc3 filter. The minimum ODR needed can be calculated as input bandwidth =  $0.2617 \times \text{ODR}$ . Therefore, the ODR required is 956 kSPS.

The external DCLK value required is  $>(\text{Frame Size} + 6) \times \text{ODR}$ , giving the user a value of 29 MHz. Provide the DCLK and ODR values as per the timing specifications listed in Table 3.

The settings to be configured are SPI control mode control, ASRC slave, high performance mode, gated DCLK input, 24-bit data output, 956 kSPS ODR, 29 MHz DCLK, sinc3 filter, external LDO regulator, and 4-channel output.

Refer to the Device Configuration section for programming these settings. After power-on, verify the hardware configuration by reading the DEVICE\_STATUS register.

**Table 22. Configuration 2 Hardware Settings**

| Pin Function                           | Supply/Level | Comments         |
|--|--------------|------------------|
| AVDD5, DVDD5                           | 5 V          | Supply           |
| IOVDD, CLKVDD, AVDD1V8, LDOIN, DVDD1V8 | 1.8 V        | Supply           |
| $\overline{\text{PIN}}/\text{SPI}$     | High         | SPI control mode |
| CLKSEL                                 | High         | Crystal input    |
| MODE                                   | Low          | ASRC slave       |
| DCLKMODE                               | Low          | Gated DCLK       |
| DCLKIO                                 | Low          | DCLK input       |

Program the registers in Table 23 with the values listed and leave the all the other registers at their default values.

**Table 23. Software Settings**

| SPI Register             | Value | Comments              |
|--------------------------|-------|-----------------------|
| DATA_PACKET_CONFIG       | 0x20  | 24-bit frame          |
| DEVICE_CONFIG            | 0x01  | High performance mode |
| CHAN_DIG_FILTER_SEL      | 0xAA  | Sinc3 filter          |
| DIGITAL_INTERFACE_CONFIG | 0x03  | 4-channel parallel    |

## DEVICE CONTROL

The AD7134 has independent paths for reading data from the ADC conversions and for controlling the device functionality.

For control, the device can be configured in either of the following two modes:

- Pin control mode: pin strapped digital logic inputs (allowing a subset of the configurability options to be used)
- SPI control mode: over a 3-wire or 4-wire SPI interface (complete configurability)

On power-up, the state of the  $\overline{\text{PIN}}/\text{SPI}$  pin determines the mode used. SPI control mode offers a full set of configurability, including access to the AD7134 internal diagnostic features. Pin control mode offers a subset of selectable features in exchange for easy configurability. The user can choose the mode of operation by the voltage level applied to the  $\overline{\text{PIN}}/\text{SPI}$  pin

Along with the  $\overline{\text{PIN}}/\text{SPI}$  pin, four additional pins must be configured to ensure the correct operation of either SPI or pin control mode. Table 24 shows a list of pin controlled functions that are common to pin control mode and SPI control mode operation. The pins listed in Table 24 are sampled only when the AD7134 is powered on.

**Table 24. Common Control Pin Function Summary**

| Pin Mnemonic                       | Pin Function  |
|------------------------------------|---|
| $\overline{\text{PIN}}/\text{SPI}$ | Controls the mode selection, pin or SPI.                          |
| MODE                               | ASRC mode of operation selection, master or slave mode operation. |
| CLKSEL                             | Input clock source selection, crystal or CMOS.                    |
| DEC0/DCLKIO                        | DCLK direction selection.   |
| DEC1/DCLKMODE                      | Gated or Free Running DCLK selection.                             |

## PIN CONTROL MODE

Pin control mode eliminates the need for an SPI communication interface. When a single known configuration is required by the user, or when only limited reconfiguration is required, the number of signals that require routing to the digital host can be reduced using this mode. Pin control mode is useful in digitally isolated applications where minimal adjustment of the configuration is needed. Pin control mode helps save on PCB design and eliminates routing of digital lines.

Pin control offers a subset of the core functionality and ensures a known state of operation after power-up or reset. Pin control mode selectable options include the following:

- Digital filter
- Frame size
- Data interface format
- Decimation rate and DCLK frequency
- High performance mode or low power mode

Figure 89 shows pin configurable functions. All the pins except the ones listed in Table 24 can be changed dynamically.

Refer to Figure 90 for more details. A limited set of diagnostics are available and CLKOUT is enabled by default in pin control mode only when the crystal option is selected.

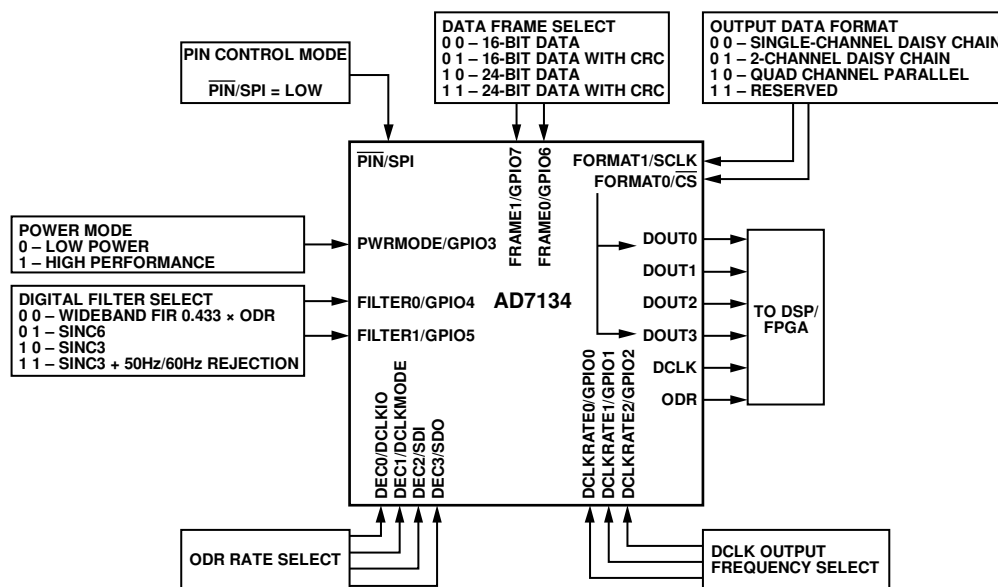


Figure 89. Pin Control Mode Configurable Functions

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## SPI CONTROL MODE

The AD7134 has a 4-wire SPI interface that is compatible with QSPI™, MICROWIRE®, and DSPs. Using the SPI interface, the user can access the ADC register map and control the AD7134.

To use SPI control mode, the  $\overline{\text{PIN}}/\text{SPI}$  pin of the AD7134 must be set to logic high. The SPI control operates as a 16-bit, 4-wire interface, allowing read and write access. The SPI serial control interface of the AD7134 is an independent path for controlling and monitoring the AD7134. There is no direct link to the data interface. The timing of ODR and DCLK is not directly related to the timing of the SPI control interface. Refer to the SPI Interface section for more details.

The SPI control mode allows the user to configure more features than the pin control mode and use the device fully. The additional features available in SPI control mode are the following:

- Full suite of diagnostic features
- More options for ODR select and DCLK frequency select in master mode
- XCLKOUT disable

- Option for wideband digital filter FIR  $0.108 \times \text{ODR}$
- Digital interface reset
- Programmable gain, offset, and channel delay
- Sleep mode
- 2-channel averaging
- Additional inherent alias mode (AA2)
- Programmable ODR, ODR/2, ODR/4, and ODR/8
- VCM pin output voltage programmability
- Per channel phase delay

## MULTIFUNCTION PINS

The AD7134 has multifunction pins where the function of these pins change depending on the selected control mode. Table 25 shows a summary of the multifunction pin functions in each mode of operation.

**Table 25. Multifunction Pin Function Summary**

| Pin Mnemonic  | Pin Function in Pin Control Mode  | Pin Function in SPI Control Mode               |
|---|---|--|
| FORMAT0/CS<br>FORMAT1/SCLK                            | ADC output channel format selection   | SPI interface                                  |
| DEC3/SDO<br>DEC2/SDI                                  | ASRC master mode decimation ratio selection   |  |
| DEC1/DCLKMODE   | ASRC master mode: decimation ratio selection<br>ASRC slave mode: DCLK mode selection (free running or gated)    | DCLK mode selection (free running or gated)    |
| DEC0/DCLKIO   | ASRC master mode: decimation ratio selection, DCLK is output<br>ASRC slave mode: tie pin low to set it as input | DCLK I/O direction selection (input or output) |
| DCLKRATE0/GPIO0<br>DCLKRATE1/GPIO1<br>DCLKRATE2/GPIO2 | DCLK output frequency selection in ASRC master mode   | General-purpose I/O                            |
| PWRMODE/GPIO3   | Device power mode selection (high performance or low power mode)  |  |
| FILTER0/GPIO4<br>FILTER1/GPIO5                        | Digital filter type selection   |  |
| FRAME0/GPIO6<br>FRAME1/GPIO7                          | Output data frame selection   |  |
|   |   |  |

## DEVICE CONFIGURATION

### PROGRAMMING OUTPUT DATA RATE AND CLOCK

#### Output Data Rate

AD7134 can be programmed to any output data rate from 10 SPS to 1496 kSPS. Depending on the MODE pin configuration, the ODR can be generated by the AD7134 or provided externally. When the AD7134 generates the ODR, the mode is called master mode, and when ODR is provided externally, the mode is called slave mode.

**Table 26. Mode Pin Configuration**

| MODE Pin | ASRC Mode of Operation | ODR Pin Direction |
|----------|------------------------|-------------------|
| 0        | Slave                  | Input             |
| 1        | Master                 | Output            |

#### ASRC Slave Mode

In ASRC slave mode, the ODR is controlled by a continuous external pulse signal connected to the ODR pin, with the ODR equal to the pulse frequency. This feature gives the user the flexibility to update the frequency of the external pulse dynamically, which changes the ODR value, but there is a loss of data during a change over time plus the filter settling time. The change over time is dominated by the unlocking and locking of the phase-locked loop (PLL) that tracks the ODR. For ODR values of >10 kSPS, a change of ODR value to less than 500 SPS does not cause the PLL to unlock and lock back again, allowing seamless data. Refer to Table 27 for change over time for ODR ranges for various filters in slave mode.

For Example 1, if the user changes the ODR value from 300 kSPS to 2500 SPS while using the digital FIR filter, the change over time is  $22 \text{ ms} + 512/2500 = 226.8 \text{ ms}$ .

For Example 2, if the user changes the ODR value from 1 MSPS to 500 kSPS while using a sinc3 digital filter, the change over time is  $11 \text{ ms} + 512/500,000 = 12 \text{ ms}$ .

The supported ODR range varies by the power mode and the digital filter type selected (see Table 19 for more details).

**Table 27. ODR Change Over Time in Slave Mode**

| ODR Range            | FIR                                   | Sinc6                             | Sinc3                              |
|----------------------|---------------------------------------|-----------------------------------|------------------------------------|
| 750 kHz to 1.46 MHz  | Not applicable                        | $5.5 \text{ ms} + 512/\text{ODR}$ | $5.5 \text{ ms} + 512/\text{ODR}$  |
| 374 kHz to 750 kHz   | Not applicable                        | $11 \text{ ms} + 512/\text{ODR}$  | $11 \text{ ms} + 512/\text{ODR}$   |
| 365 kHz to 374 kHz   | ODR range not supported in slave mode | $22 \text{ ms} + 512/\text{ODR}$  | $22 \text{ ms} + 512/\text{ODR}$   |
| 1.46 kHz to 365 kHz  | $22 \text{ ms} + 512/\text{ODR}$      | $22 \text{ ms} + 512/\text{ODR}$  | $22 \text{ ms} + 512/\text{ODR}$   |
| 1.46 kHz to 2.5 kHz  | Not applicable                        | $22 \text{ ms} + 512/\text{ODR}$  | $22 \text{ ms} + 512/\text{ODR}$   |
| 732 SPS to 1.46 kHz  | Not applicable                        | Not applicable                    | $44 \text{ ms} + 512/\text{ODR}$   |
| 366 SPS to 732 SPS   | Not applicable                        | Not applicable                    | $88 \text{ ms} + 512/\text{ODR}$   |
| 183 SPS to 366 SPS   | Not applicable                        | Not applicable                    | $6 \text{ sec} + 512/\text{ODR}$   |
| 91.5 SPS to 183 SPS  | Not applicable                        | Not applicable                    | $12 \text{ sec} + 512/\text{ODR}$  |
| 45.7 SPS to 91.5 SPS | Not applicable                        | Not applicable                    | $24 \text{ sec} + 512/\text{ODR}$  |
| 22.8 SPS to 45.7 SPS | Not applicable                        | Not applicable                    | $48 \text{ sec} + 512/\text{ODR}$  |
| 11.4 SPS to 22.8 SPS | Not applicable                        | Not applicable                    | $96 \text{ sec} + 512/\text{ODR}$  |
| 10 SPS to 11.4 SPS   | Not applicable                        | Not applicable                    | $192 \text{ sec} + 512/\text{ODR}$ |

**ASRC Master Mode**

In ASRC master mode, the AD7134 device generates the output data at a programmable decimation ratio. The user can program the decimation ratio in both pin control and SPI control mode to achieve the desired output data rate.

In pin control mode, the decimation rate is fixed as per the predefined pin control options. Sixteen decimation ratio options are available through the configuration of the DEC0/DCLKIO pin to DEC3/SDO pin. The final ODR value also depends on the digital filter type. Table 28 summarizes the ODR values available in master mode.

In SPI control mode, the ODR is available at the full range described in Table 19. The ODR can be programmed via the ODR\_VAL\_INT, Bits[23:0] bits and ODR\_VAL\_FLT, Bits[31:0] bits with a resolution of 0.01 SPS.

In Example 1, for an ODR to be 187.23 kSPS, calculate the decimation rate as follows:

$$\begin{aligned} \text{Decimation Rate} &= \text{MCLK}/187.23 \text{ kHz} = \\ &24 \text{ MHz}/187.23 \text{ kHz} = 128.1846 = 0x0000802F4103E5 \end{aligned}$$

Program ODR\_VAL\_INT, Bits[23:0] with 0x80.

Program ODR\_VAL\_FLT, Bits[31:0] with 0x2F4103E5.

In Example 2, for an ODR to be 375 kSPS, calculate the decimation rate as follows:

$$\begin{aligned} \text{Decimation Rate} &= \text{MCLK}/375 \text{ kHz} = 24 \text{ MHz}/375 \text{ kHz} = \\ &64 = 0x00004000000000 \end{aligned}$$

Program ODR\_VAL\_INT, Bits[23:0] with 0x000040.

Program ODR\_VAL\_FLT, Bits[31:0] with 0x00000000.

Every time the ODR\_VAL\_INT, Bits[23:0] and ODR\_VAL\_FLT, Bits[31:0] are changed, the MASTER\_SLAVE\_TX\_BIT in the TRANSFER\_REGISTER must be set to update the ODR to the new value.

The user has the flexibility to change the ODR value, but that means a loss of data of about 2 μs plus the filter settling time. The 2 μs time, t<sub>DELAY</sub>, is constant across the ODR range. See Figure 90 for more details.

The SPI control mode also allows the user to set a different ODR rate for each of the four ADC channels using the ODR\_RATE\_SEL\_CHx bits. The ODR options are limited to 1, ½, ¼, or ⅛ of the ODR frequency.

**Table 28. Output Data Rate Configuration in Pin Control Master Mode**

| DEC3 | DEC2 | DEC1 | DEC0 | Wideband 0.433 Hz × ODR Filter (kSPS) | Sinc6 Filter (kSPS) | Sinc3 Filter (kSPS) |
|------|------|------|------|---------------------------------------|---------------------|---------------------|
| 0    | 0    | 0    | 0    | 374                                   | 1496                | 1496                |
| 0    | 0    | 0    | 1    | 325                                   | 1250                | 1000                |
| 0    | 0    | 1    | 0    | 285                                   | 1000                | 750                 |
| 0    | 0    | 1    | 1    | 256                                   | 750                 | 375                 |
| 0    | 1    | 0    | 0    | 235                                   | 500                 | 187.5               |
| 0    | 1    | 0    | 1    | 200                                   | 375                 | 128                 |
| 0    | 1    | 1    | 0    | 175                                   | 325                 | 64                  |
| 0    | 1    | 1    | 1    | 128                                   | 256                 | 32                  |
| 1    | 0    | 0    | 0    | 100                                   | 175                 | 16                  |
| 1    | 0    | 0    | 1    | 80                                    | 128                 | 5                   |
| 1    | 0    | 1    | 0    | 64                                    | 80                  | 2.5                 |
| 1    | 0    | 1    | 1    | 32                                    | 64                  | 1.25                |
| 1    | 1    | 0    | 0    | 16                                    | 32                  | 0.625               |
| 1    | 1    | 0    | 1    | 10                                    | 10                  | 0.06                |
| 1    | 1    | 1    | 0    | 5                                     | 5                   | 0.05                |
| 1    | 1    | 1    | 1    | 2.5                                   | 2.5                 | 0.01                |

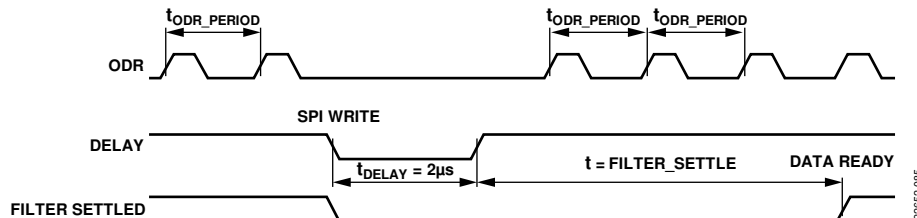


Figure 90. Master Mode ODR Change Over

**Data Clock (DCLK)**

The data clock can be either an input or an output depending on the direction of the ODR pin. When ODR is output for master mode, set the DEC0/DCLKIO pin high to configure DCLK as an output. When ODR is input for slave mode, tie the DEC0/DCLKIO pin low to configure DCLK as an input. The data clock can be operated in gated mode or free running mode controlled by the DEC1/DCLKMODE pin.

When operated in pin control mode with the ASRC set to master mode, the DCLK operation is limited to gated output only. When operating in pin control mode with the ASRC set to slave mode, or when operating in SPI control mode, the DCLK

mode of operation is controlled by the DEC1/DCLKMODE pin and DEC0/DCLKIO pin, as shown in Table 29.

In master mode, the DCLK pin is configured as an output. The DCLK frequency is derived from the AD7134 device master clock and can be configured using the DCLKRATE0/GPIO0 pin to DCLKRATE2/GPIO2 pin in pin control mode, or DCLK\_FREQ\_SEL (Bits[3:0]) in Register 0x11 in SPI control mode. SPI control mode offers 16 DCLK output frequency options, and pin control mode offers eight. Table 30 lists all the DCLK output frequency options.

In slave mode, the DCLK pin is an external signal.

**Table 29. DCLK Mode of Operation in Pin Control Mode or in SPI Control Mode**

| DEC1/DCLKMODE | DEC0/DCLKIO | MODE | DCLK Direction | DCLK Mode    |
|---------------|-------------|------|----------------|--------------|
| 0             | 0           | 0    | Input          | Gated        |
| 0             | 0           | 1    | Reserved       | Reserved     |
| 0             | 1           | 0    | Reserved       | Reserved     |
| 0             | 1           | 1    | Output         | Gated        |
| 1             | 0           | 0    | Input          | Free running |
| 1             | 0           | 1    | Reserved       | Reserved     |
| 1             | 1           | 0    | Reserved       | Reserved     |
| 1             | 1           | 1    | Output         | Free running |

**Table 30. DCLK Output Frequency Configuration**

| DCLKRATE2 or Register 0x11, Bit 3 | DCLKRATE1 or Register 0x11, Bit 2 | DCLKRATE0 or Register 0x11, Bit 1 | Register 0x11, Bit 0 | DCLK Output Frequency Options         |
|-----------------------------------|-----------------------------------|-----------------------------------|----------------------|---------------------------------------|
| 0                                 | 0                                 | 0                                 | 0                    | 48 MHz (SPI/pin control mode default) |
| 0                                 | 0                                 | 0                                 | 1                    | 24 MHz <sup>1</sup>                   |
| 0                                 | 0                                 | 1                                 | 0                    | 12 MHz                                |
| 0                                 | 0                                 | 1                                 | 1                    | 6 MHz <sup>1</sup>                    |
| 0                                 | 1                                 | 0                                 | 0                    | 3 MHz                                 |
| 0                                 | 1                                 | 0                                 | 1                    | 1.5 MHz <sup>1</sup>                  |
| 0                                 | 1                                 | 1                                 | 0                    | 750 kHz                               |
| 0                                 | 1                                 | 1                                 | 1                    | 375 kHz <sup>1</sup>                  |
| 1                                 | 0                                 | 0                                 | 0                    | 187.5 kHz                             |
| 1                                 | 0                                 | 0                                 | 1                    | 93.75 kHz <sup>1</sup>                |
| 1                                 | 0                                 | 1                                 | 0                    | 46.875 kHz                            |
| 1                                 | 0                                 | 1                                 | 1                    | 234.375 kHz <sup>1</sup>              |
| 1                                 | 1                                 | 0                                 | 0                    | 11.71875 kHz                          |
| 1                                 | 1                                 | 0                                 | 1                    | 5.859375 kHz <sup>1</sup>             |
| 1                                 | 1                                 | 1                                 | 0                    | 2.929688 kHz                          |
| 1                                 | 1                                 | 1                                 | 1                    | 1.464844 kHz <sup>1</sup>             |

<sup>1</sup> Not available in pin control mode.



**PROGRAMMING DIGITAL FILTER**

In pin control mode, four digital filter types are available through the configuration of the FILTER1/GPIO5 pin and FILTER0/GPIO4 pin. All four ADC channels share the same digital filter type.

One additional digital filter type, wideband 0.10825 Hz × ODR filter, is available only in SPI control mode. In SPI control mode, the digital filter type can be configured independently for each ADC channel via the DIGFILTER\_SEL\_CHx bits and the additional digital filter type (wideband 0.10825 Hz × ODR filter or wideband 0.433 Hz × ODR filter) via the WB\_FILTER\_SEL\_CHx bits, where x is the channel number from 0 to 3. Table 31 lists all the digital filter options.

To configure the digital filter dynamically, change the digital filter first and then change the output data rate to ensure proper operation.

**PROGRAMMING DATA INTERFACE**

The digital interface consists of setting up the format, the frame, and the averaging options.

**Output Channel Format**

The data interface format is determined by setting the FORMAT0/ $\overline{\text{CS}}$  pin and FORMAT1/SCLK pin. The logic state of the FORMAT0/ $\overline{\text{CS}}$  pin and FORMAT1/SCLK pin is read on power-up and determine how many data lines (DOUTx) the ADC conversions are output on.

Because the FORMAT0/ $\overline{\text{CS}}$  pin and FORMAT1/SCLK pin are read on power-up of the AD7134 and the device remains in this output configuration, this function must always be hardwired and cannot be altered dynamically. Figure 91 and Figure 92 show the formatting configuration for the digital output pins on the AD7134.

**Table 31. Digital Filter Configuration**

| FILTER1 or DIGFILTER_SEL_CHx, Bit 1 | FILTER0 or DIGFILTER_SEL_CHx, Bit 0 | WB_FILTER_SEL_CHx, Bit 0 | Digital Filter Type                           |
|-------------------------------------|-------------------------------------|--------------------------|---|
| 0                                   | 0                                   | 0                        | Wideband 0.433 Hz × ODR filter                |
| 0                                   | 0                                   | 1                        | Wideband 0.10825 Hz × ODR filter <sup>1</sup> |
| 0                                   | 1                                   | X <sup>2</sup>           | Sinc6   |
| 1                                   | 0                                   | X <sup>2</sup>           | Sinc3   |
| 1                                   | 1                                   | X <sup>2</sup>           | Sinc3 with additional 60 Hz rejection         |

<sup>1</sup> Available in SPI control mode only.

<sup>2</sup> X means don't care.

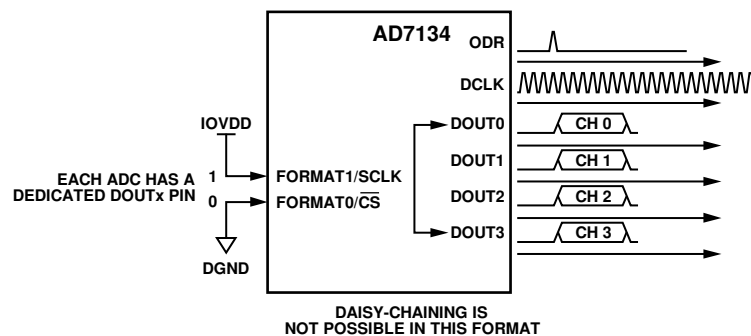


Figure 91. FORMAT1, FORMAT0 = 10, Four Data Output Pins

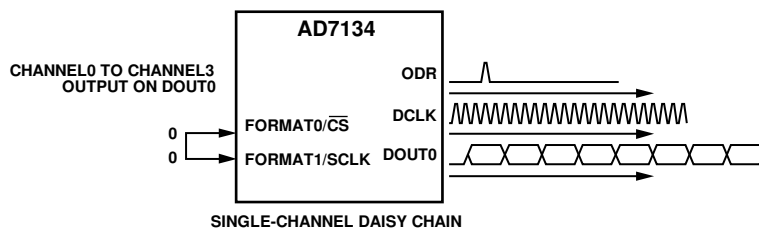


Figure 92. FORMAT1, FORMAT0 = 00, One Data Output Pin

Calculate the minimum required DCLK rate for a given data interface configuration as follows:

$$DCLK \text{ (Minimum)} = \text{Output Data Rate} \times \text{Channels per DOUTx} \times (\text{Frame Size} + 6)$$

For example, if data size = 24 and 6-bit CRC is enabled with one DOUTx line, single-channel daisy-chaining,

$$DCLK \text{ (Minimum)} = 374 \text{ kSPS} \times 4 \text{ Channels per DOUTx} \times (24 + 8 + 6) = 44.88 \text{ Mbps}$$

The AD7134 can output the data from four ADC channels in parallel using four output pins, or serialize the data and output them using fewer pins. Paralleling the output enables a higher output data rate for a given DCLK frequency. In addition to using fewer I/Os, serializing the data allows data from multiple AD7134 devices to be daisy-chained.

The output channel format is controlled by the FORMAT0/ $\overline{\text{CS}}$  pin and FORMAT1/SCLK pin in pin control mode and the format bits in the DIGITAL\_INTERFACE\_CONFIG register in SPI control mode.

Table 33 lists all the output channel format options.

#### Data Frame

The frame of each ADC sample output data consists of the data followed by an optional status/CRC header.

The AD7134 supports two data length options: 16-bit and 24-bit. The AD7134 also supports one CRC-6 header option. Table 34 lists all the output data frame options.

#### Data Delay

The data output of each channel of the AD7134 can be individually delayed by 0, 1, or 2 MCLK cycles using the MPC\_CONFIG register. The front-end signal chain components can add varying amounts of phase delay depending on factors like gain setting

**Table 33. Output Channel Format Configuration**

| FORMAT1/SCLK Pin or Bit 1, DIGITAL_INTERFACE_CONFIG Register | FORMAT0/ $\overline{\text{CS}}$ Pin or Bit 0, DIGITAL_INTERFACE_CONFIG Register | Output Channel Format  |
|--|---|--|
| 0  | 0   | Single-channel daisy-chain mode. DOUT0 acts as an output and DOUT2 acts as a daisy-chain input. DOUT1 and DOUT3 are disabled. Data from all four ADC channels are serialized and output on DOUT0 (SPI default mode).   |
| 0  | 1   | Dual-channel daisy-chain mode. DOUT0 and DOUT1 act as outputs, and DOUT2 and DOUT3 act as daisy-chain inputs. Data from Channel 0 and Channel 1 are serialized and output on DOUT0. Data from Channel 2 and Channel 3 are serialized and output on DOUT1.                    |
| 1  | 0   | Quad-channel parallel output mode. Each ADC channel has a dedicated data output pin.   |
| 1  | 1   | Channel data averaging mode. In pin control mode, data from all four channels are averaged and output on DOUT0. DOUT2 acts as daisy-chain input. DOUT1 and DOUT3 are disabled. In SPI control mode, the averaging operation is defined by the AVG_SEL bits in Register 0x12. |

**Table 34. Data Frame Options**

| FRAME1/GPIO7 Pin or Bit 1, DATA_PACKET_CONFIG Register | FRAME0/GPIO6 Pin or Bit 0, DATA_PACKET_CONFIG Register | Data Frame             | Frame Length |
|--|--|------------------------|--------------|
| 0  | 0  | 16-bit ADC data        | 16           |
| 0  | 1  | 16-bit data with CRC-6 | 24           |
| 1  | 0  | 24-bit ADC data        | 24           |
| 1  | 1  | 24-bit data with CRC-6 | 32           |

and filtering. This feature gives the user flexibility to match the delays on different channels and thus achieving tight phase matching between channels.

#### POWER MODES

The AD7134 offers two power modes, high performance mode and low power mode. These modes are available in both pin control mode and SPI control mode. In pin control mode, the PWRMODE/GPIO3 pin controls the AD7134 operating power mode. In SPI control mode, the POWER\_MODE bit controls the power mode. Additional sleep mode is available in SPI control mode. Table 32 summarizes the power mode configurations. In both pin control mode and SPI control mode, a full device power-down can be initiated through the  $\overline{\text{PDN}}$  pin.

**Table 32. Power Mode Configuration**

| PWRMODE/GPIO3 or POWER_MODE Bit | SLEEP_MODE_EN | Device Power Mode     |
|---------------------------------|---------------|-----------------------|
| 0                               | 0             | Low power mode        |
| 1                               | 0             | High performance mode |
| X                               | 1             | Sleep mode            |

To operate the device correctly in low power mode, the user must toggle the setting from low power mode to high performance mode and back to low power mode.

In pin control mode, to set the AD7134 in low power mode, toggle the PWRMODE/GPIO3 pin to high and after a delay of 10 ms toggle it back to low. In SPI control mode after power up, change the POWER\_MODE bit from low to high and after a delay of 10 ms change it back to low.

Also, in pin slave mode, first provide the ODR signal and then change the power mode to ensure dynamic sampling of the PWRMODE/GPIO3 pin.

### INHERENT ANTIALIASING FILTER MODES

The CTSD architecture allows the AD7134 to reject signals around the integer multiples of the modulator sampling frequency, protecting its input band of interest from aliasing. The AD7134 offers two antialiasing modes. The default antialiasing mode, AA1, offers a typical 85 dB of aliasing rejection.

The other antialiasing mode, AA2, improves the rejection to 102.5 dB with the cost of a higher offset drift of 1.03  $\mu\text{V}/^\circ\text{C}$ , additional power consumption of 3 mW per channel, and higher noise level with dynamic range reduction.

The AA2 mode is only available in SPI control mode and can be enabled by setting the AA\_MODE bit to 1.

Table 35 shows typical performance differences in inherent antialias modes. The filter is wideband  $0.433 \times \text{ODR}$  FIR filter, and the ODR value is  $\text{ODR} = 374 \text{ kSPS}$ .

**Table 35. Performance Difference in Inherent Antialias Modes**

| Parameter         | AA1 Mode                         | AA2 Mode                          |
|-------------------|----------------------------------|-----------------------------------|
| Dynamic Range     | 107.4 dB                         | 105.9 dB                          |
| SNR               | 106.6 dB                         | 105.4 dB                          |
| Alias Rejection   | 85 dB                            | 102.5 dB                          |
| Offset Drift      | 0.5 $\mu\text{V}/^\circ\text{C}$ | 1.03 $\mu\text{V}/^\circ\text{C}$ |
| Power per Channel | 126 mW                           | 129 mW                            |

## DYNAMIC RANGE ENHANCEMENT, CHANNEL AVERAGING

The AD7134 is equipped with built in 4-channel and 2-channel averaging functions that increase the performance by 6 dB and 3 dB. The device performs on-board averaging of the output data from two or four of its ADC channels to improve the dynamic range.

Averaging is a digital postprocessing option after the digital filter, which performs averaging of the output data from multiple ADC channels. This averaging feature allows the user to measure a signal with multiple ADC channels and average the result to achieve higher dynamic range.

In 4:1 averaging mode, a single input signal is applied to all four input channels, as shown in Figure 93. In this mode with averaging enabled, the AD7134 is a single-channel device with the dynamic range improved by 6 dB.

In 2:1 averaging mode, a single input signal is applied to two input channels, as shown in Figure 94. In this mode with averaging enabled, the AD7134 behaves as a 2-channel device with each channel dynamic range improved by 3 dB.

For noise performance of channel averaging, see the Noise Performance and Resolution section.

Figure 93 and Figure 94 show the connection diagrams for using these functions. For 4:1 channel averaging, short all four inputs together, but for 2:1 channel averaging short two inputs together.

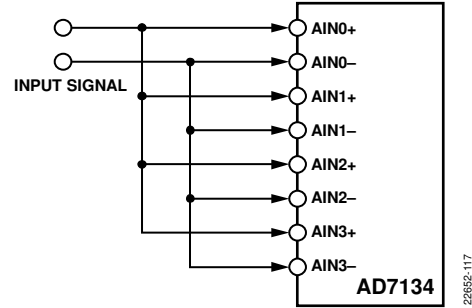


Figure 93. 4:1 Channel Averaging

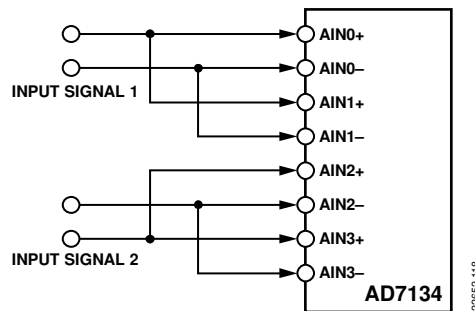


Figure 94. 2:1 Channel Averaging

In pin control mode, only 4:1 averaging is available through the configuration of the  $\overline{\text{FORMAT0}}/\overline{\text{CS}}$  pin and  $\overline{\text{FORMAT1}}/\text{SCLK}$  pin, as shown in Table 33.

In SPI control mode, set the format bits, Bits[1:0] in Register 0x12 to 11 to enable the output averaging function. Then use Bits[3:2] in Register 0x12 to select the channel averaging options.

## CALIBRATION

In SPI control mode, the AD7134 offers the ability to calibrate offset and gain individually for each channel. The user can alter the gain and offset of the AD7134 and subsystem.

Each channel of the ADC has an associated gain and offset coefficient that is stored for each ADC after factory programming. The user can overwrite these gain and offset coefficients using the gain and offset correction registers. However, after a reset or power cycle, the gain and offset register values revert to the hard coded, programmed factory setting.

These options are available in SPI control mode only.

### OFFSET CALIBRATION

The offset correction registers provide 23-bit, signed, twos complement registers for channel offset adjustment. The offset setting for each channel is enabled using the OFFSET\_CAL\_EN\_CHx bits. The offset range is  $\pm V_{REF}$  with a step size of

$V_{REF}/2^{22}$ . An LSB of offset register adjustment changes the digital output by 2 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by 200 LSBs.

For additional register information, see the OFFSET\_CAL\_EN\_CHx bit descriptions in Table 81, Table 87, Table 93, and Table 99.

### GAIN CALIBRATION

The gain register is 20 bits with a range of  $\pm 50\%$  and the LSB applying a gain of 0.95 ppm. The gain setting for each channel is enabled using the GAIN\_CAL\_SEL\_CHx bits.

For additional register information, see the GAIN\_CAL\_SEL\_CHx bit descriptions in Table 78, Table 84, Table 90, and Table 96.

# APPLICATIONS INFORMATION

## POWER SUPPLY

The AD7134 has a total of seven power supply input pins: AVDD5, DVDD5, LDOIN, AVDD1V8, DVDD1V8, CLKVDD, and IOVDD.

Refer to the power supply voltages in Table 1 for operating supply voltage values for 4.096 V and 5 V reference inputs.

To simplify the power supply design, the user can supply the AVDD5 pin and DVDD5 pin together with a single, low noise 5 V supply, and supply the AVDD1V8, DVDD1V8, CLKVDD, and IOVDD pins together with a single low noise 1.8 V supply.

To generate 5 V and 1.8 V rails, the power circuits using [LT8606](#) or [LT8607](#) provide a low EMI, small size solution supporting a wide range of input voltages.

### On-Board LDO Regulators

To simplify the power supply design, the AD7134 provides three internal LDO regulators to generate the 1.8 V required for the AVDD1V8, DVDD1V8, and CLKVDD pins from a single 2.6 V to 5.5 V supply connected to the LDOIN pin, as shown in Figure 95.

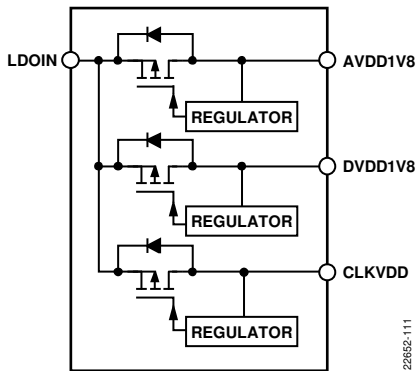


Figure 95. Internal LDO Regulator Connections

If the internal LDO regulators are used, the AVDD1V8, DVDD1V8, and CLKVDD pins must be decoupled with a 10 μF, 10 μF, and 2.2 μF capacitor, respectively, to their respective grounds, as shown in Figure 96.

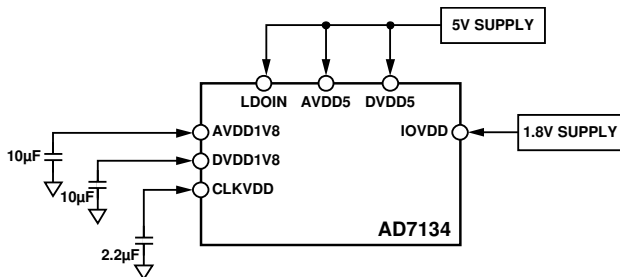


Figure 96. Internal LDO Regulator Mode Power Connections

The internal LDO regulators are enabled only when the IOVDD supply is powered up first by an external 1.8 V supply.

The internal LDO regulators work properly if the power supply sequence in Figure 97 is followed. Ensure that the IOVDD and LDOIN pins are powered after DVDD5, as shown in Figure 97.

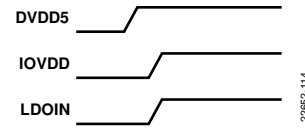


Figure 97. Power Sequencing in Internal LDO Mode

If the internal LDO regulators are not used, tie the LDOIN pin to DVDD1V8, as shown in Figure 98.

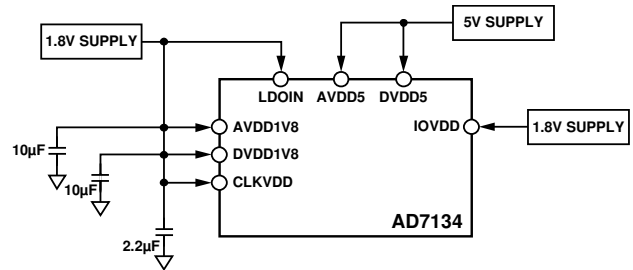


Figure 98. External Power Mode Connections

If AVDD1V8, DVDD1V8, and CLKVDD are powered from a separate external supply, take caution on the supply sequencing. All three supplies are connected internally through the back diode of the regulator. If one supply powers up first, it can supply power to other supplies through the back diode and the other LDO regulators.

### REFERENCE NOISE FILTERING

The user can reduce the noise contribution of the reference source to the overall ADC conversion accuracy by filtering the reference signal. An internal 20 Ω resistor between the REFIN pin and the REFCAP pin enables the user to form a first-order RC filter by connecting a capacitor on the REFCAP pin.

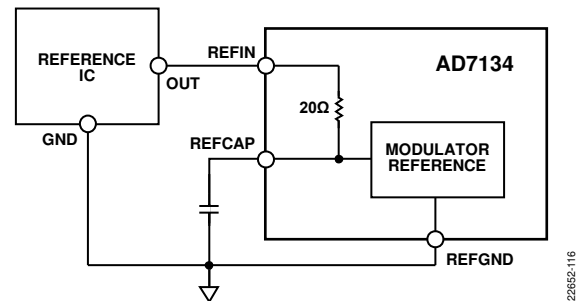


Figure 99. Reference Input Connection Using REFIN pin

The equivalent noise bandwidth of a first-order filter is 0.25/RC in Hz.

The noise contribution of the reference source is proportional to the ADC input signal. The reference noise contribution is at the highest when the input signal is at full scale. The reference noise has no impact on the output when the ADC inputs are shorted.

As a general rule, limit the reference noise to ¼ of the noise of the ADC to have a minimal effect on the overall SNR.

The total reference noise is the root sum square of its 1/f noise and its wideband noise.

The  $1/f$  noise of the reference can be estimated by its peak-to-peak noise specification over the 0.1 Hz to 10 Hz frequency range. The wideband noise can be calculated from the voltage noise density specification of the reference and the reference noise bandwidth.

An example to calculate the reference noise requirement based on the ADC mode of operation follows.

Consider the AD7134 device that is operating in high performance mode,  $ODR = 374$  kSPS, and wideband  $0.433 \text{ Hz} \times ODR$  filter with a reference voltage of 4.096 V.

According to Table 9, the ADC noise in this setup is  $12.63 \mu\text{V rms}$ . The reference noise is  $1/4$ , equal to  $3.16 \mu\text{V rms}$ .

An [ADR444](#) reference IC is chosen to provide the reference voltage for the AD7134. The [ADR444](#) has a 0.1 Hz to 10 Hz peak noise of  $1.8 \mu\text{V p-p}$ , and a noise spectrum density of  $78.6 \text{ nV}/\sqrt{\text{Hz}}$ . The [ADR444](#)  $1/f$  noise is  $1.8 \mu\text{V p-p}$  or  $1.8/6.6 = 0.273 \mu\text{V rms}$ .

The total reference noise is the root sum square of its  $1/f$  noise and its wideband noise. Therefore,

$$\sqrt{(0.273^2 + n_{WB}^2)} < 3.16$$

Solving the equation yields the wideband noise,  $n_{WB}$ , of the [ADR444](#), which must be less than  $3.14 \mu\text{V rms}$ .

The wideband noise of the [ADR444](#) can be calculated by multiplying its noise spectrum density by the square root of the noise bandwidth.

$$78.6 \text{ nV}/\sqrt{\text{Hz}} \times \sqrt{NBW} < 3.14 \mu\text{V rms}$$

where  $NBW$  is the noise bandwidth.

The calculation shows that the noise bandwidth must be less than 1.6 kHz. The equivalent noise bandwidth of a first-order filter is  $0.25/RC$ , in Hz.

The AD7134 has an internal  $20 \Omega$  resistor between the REFIN pin and the REFCAP pin. By connecting the output of the [ADR444](#) to the REFIN input, a capacitor  $> 7.9 \mu\text{F}$  on the REFCAP pin is sufficient to limit the reference noise to the desired value. It is recommended to place a  $10 \mu\text{F}$  capacitor on the REFCAP pin.

## MULTIDEVICE SYNCHRONIZATION

The integrated ASRC of the AD7134 helps achieve multidevice synchronization with a single low speed ODR line, giving less than 10 ns of phase matching between channels on different devices, which makes it easy to synchronize. Applications like condition-based monitoring, power quality analyzer, and sonar system demand tight phase matching across high numbers of channels, making the digital interface design complex.

The devices can be clocked with their own local clock sources yet can achieve tight phase matching without the need of routing high speed clock lines that adds to EMI issues. This clocking also means that for applications demanding isolation, the user can pass fewer low speed lines across the isolation barrier, as shown in Figure 100.

The AD7134 does not require the system clock across isolation to synchronize isolated devices, which enables higher ODR in isolated simultaneous sampling applications.

To achieve tight synchronization, the user must configure all the devices in slave mode and use the SPI to set the DIG\_IF\_RESET bit to reset the digital interface before the data capture. This DIG\_IF\_RESET command must be given to all the slaves simultaneously using one single SPI write command.

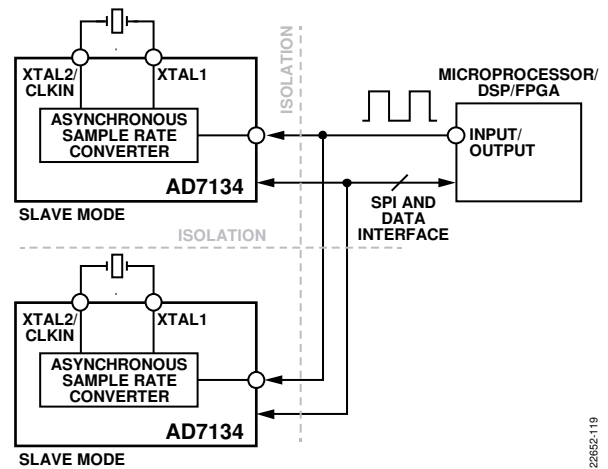


Figure 100. Simplified Clocking in AD7134

## COHERENT SAMPLING

The integrated ASRC of the AD7134 allows the user to set granular sampling speeds from 0.01 kSPS to 1496 kSPS with a resolution of 0.01 SPS. The ASRC allows the user to detect the line frequency and change the ODR so that there is a rational relationship between the input signal frequency and the sampling speed.

Mathematically, coherent sampling is expressed as  $f_{IN}/f_{ODR} = \text{number of cycles in sampling window} \div \text{number of data points for FFT}$ . For example,  $f_{ODR}$  is 32 kSPS,  $f_{IN}$  is 1 kHz, and the number of samples is 512.

Number of cycles in the sampling window =  $512 \times 1000/32 \text{ kSPS} = 16$ .

If the input frequency is 1.01 kHz, the ODR change is  $4096 \times 1010/16 = 258.56 \text{ kSPS}$  to achieve coherent sampling.

In applications like power metering and analysis, it is necessary to achieve the required accuracy on the harmonic data and metering parameters and ensure coherency between the ADC sampling rate and the power line frequency.

## LOW LATENCY DIGITAL CONTROL LOOP

The control loop demands low latency, but the antialias filter for noise reduction adds significant delay, increasing the loop latency. The inherent antialias rejection of the AD7134 removes the need of the antialias filter, significantly reducing the signal chain latency.

The AD7134 supports throughput rates up to 1496 kSPS, making it an optimal choice for low latency, 24-bit digital control loops.

**AUTOMATIC GAIN CONTROL**

The AD7134 has additional GPIO functionality when operated in SPI control mode. One of the diagnostic features of the AD7134 enables GPIO7 to report any of the diagnostic errors by enabling the ERR\_PIN\_OUT\_EN bit.

The user can use GPIO7 to report any input overrange detection, and based on the report the user can control the gain of the front-end amplifier. Configure GPIO7 as an output and set the ERR\_PIN\_EN\_OR\_AIN bit, which enables errors from input overrange and enables error reporting on GPIO7. Wire the FRAME1/GPIO7 pin to gain control of the amplifier.

Any input overrange above  $\pm V_{REF}$  on the input lines causes GPIO7 to go high, which brings down gain of the PGA, which reduces its output below  $\pm V_{REF}$ . This control happens automatically without any intervention of the digital host.

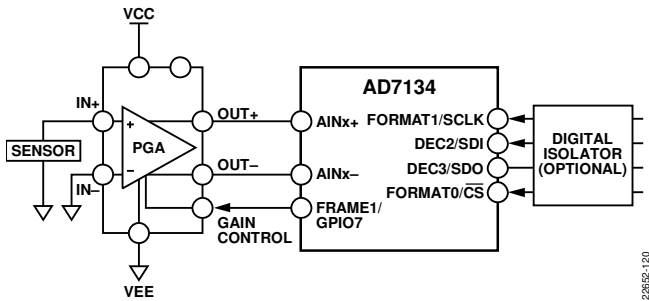


Figure 101. Automatic Gain Control

**FRONT-END DESIGN EXAMPLES**

The analog front-end circuit of the AD7134 must perform the following sequence:

1. Provide adequate input impedance to match the source.
2. Provide reasonably low output impedance to drive the 6 kΩ differential input resistance of the ADC.
3. Convert the input signal to a balanced, fully differential signal with fixed common-mode voltage of 2 V to 2.5 V.
4. Provide the necessary gain or attenuation to match the maximum source signal amplitude to the full-scale input range of the ADC.

The following low noise amplifiers are recommended for various types of system challenges. Example operational amplifiers include the ADA4625-2, ADA4610-2, AD8605, and the ADA4075-2. Examples of fully differential amplifiers include the ADA4940-2, LTC6363, and the ADA4945-1. Example instrumentation amplifiers include the AD8421.

**Differential Input Signal with Controlled Common-Mode and High Impedance Source**

An example of a high impedance source includes a Wheatstone bridge type of configuration for strain and pressure monitoring. The input common mode is well controlled, needing no common-mode rejection, and a dual op amp configuration works properly. The circuit in Figure 102 can also provide gain to the signal. Because of the easy to drive nature of the AD7134, the op amps

do not need to have a high bandwidth and a strong output drive to overcome kickbacks from traditional ADCs. The ADA4610-2 is an optimal choice because it offers wide input range, low noise, suitable bandwidth, and high linearity. The AD8605 is another optimal choice for rail to rail, low voltage, single-supply operation.

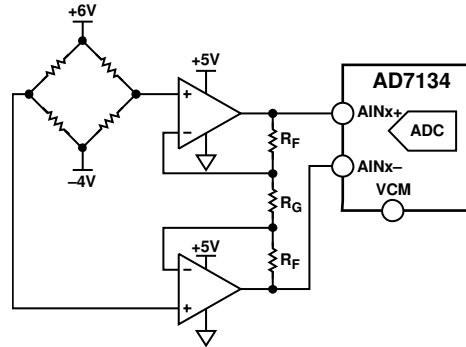


Figure 102. Buffered Input with Gain and No Additional Common-Mode Rejection

**Differential Input with Unregulated Common-Mode Voltage Low Impedance Source**

If a wider input common-mode range is required, a fully differential amplifier can be used, as shown in Figure 103.

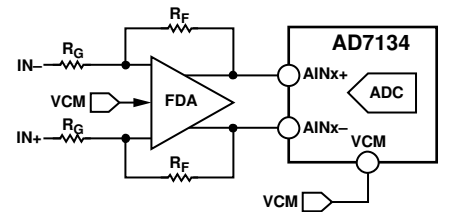


Figure 103. Use a Fully Differential Amplifier to Extend Input Common-Mode Voltage and Signal Gain/Attenuation

This circuit can also provide gain or attenuation of the signal and is responsible for rejecting the input common mode.

Fully differential amplifiers such as the ADA4940-2, ADA4945-1, and LTC6363 are all suitable choices. Devices such as the LTC6363-0.5, LTC6363-1, and LTC6363-2 with a highly matched integrated resistor network offer unmatched CMRR at 94 dB minimum.

**Fully Differential Amplifier with Single Unipolar Supply**

The circuit in Figure 104 has no passive components, but it offers fixed gain for single-ended or differential inputs having a low impedance source. Single unipolar 5 V supply operation relaxes the power design.

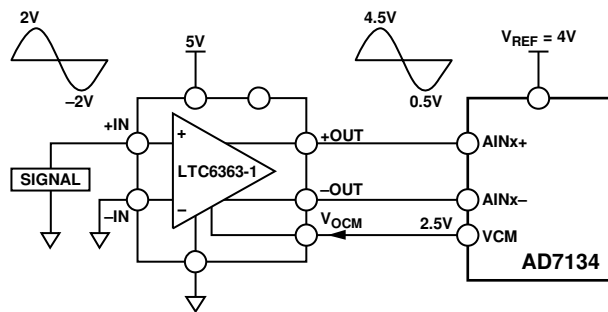


Figure 104. Fully Differential Amplifier with Single Supply



**Single-Ended or Pseudo Differential Input with High Source Impedance**

The single-ended or pseudo differential input signals must be converted into fully differential signals before driving into the AD7134. All the circuit examples given in the Front-End Design Examples section for interfacing with differential signals can work with interfacing with single-ended or pseudo differential signals. Connect the second input to signal ground or a common-mode voltage source.

A number of other circuits can be used to perform single-ended to differential conversions.

**Instrumentation Amplifier with Single-Ended to Differential Output Conversion**

The circuit configuration in Figure 105 is suitable for single-ended input signal, high common-mode range, and low input current suitable for a high impedance source for gain  $\geq 1$ .

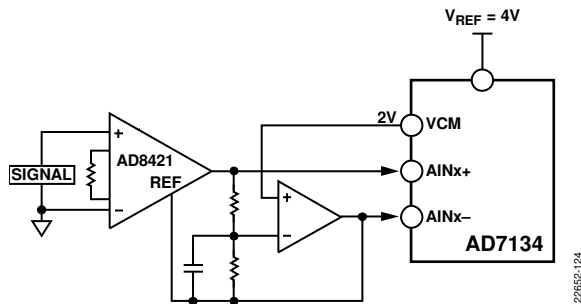


Figure 105. Instrumentation Amplifier in Differential Output Configuration

**Precision Dual Amplifier**

The circuit in Figure 106 is suitable for a high impedance source, which can add gain or attenuation. Example operational amplifiers are the ADA4941-1, LT6350, ADA4805-2, and ADA4004-2.

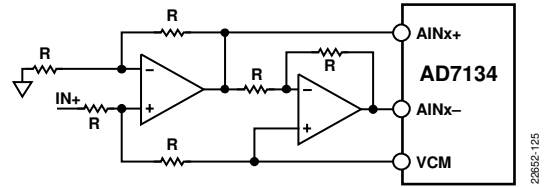


Figure 106. Dual Operation Amplifier Configuration

**Operational Amplifier and Fully Differential Amplifier**

The circuit in Figure 107 is a low input bias operational amplifier with a fully differential amplifier, like the ADA4945-1, is suitable for high impedance sources. The fully differential amplifier circuit can add gain or attenuation.

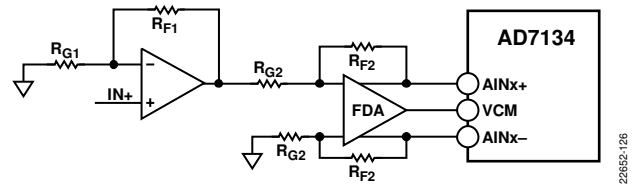


Figure 107. Op Amp and Fully Differential Amplifier

## DIGITAL INTERFACE

The AD7134 digital interface consists of two independent parts: an SPI interface for register access and device configuration, and a data interface for sending out conversion data.

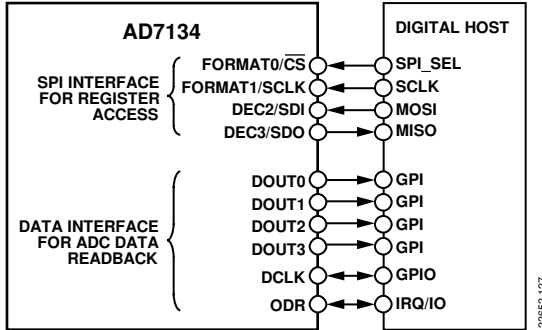


Figure 108. Communication Interface of AD7134

### SPI INTERFACE

The SPI control mode is one of the two control modes supported on the AD7134. The other mode is pin control mode. The user can choose which mode to operate the device in by setting the logic level on the PIN/SPI pin. Set the PIN/SPI pin high to enable the SPI control mode, which enables the SPI interface of the device.

The AD7134 has a 4-wire SPI interface that is compatible with QSPI, MICROWIRE, and DSPs. The interface operates in SPI Control Mode 0. In SPI Control Mode 0, the SCLK idles low,

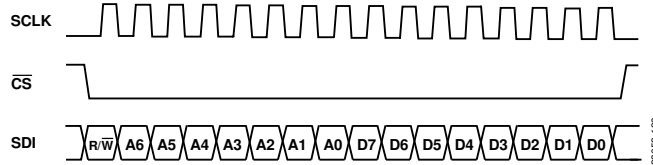


Figure 110. 3-Wire Mode Write/Read Command

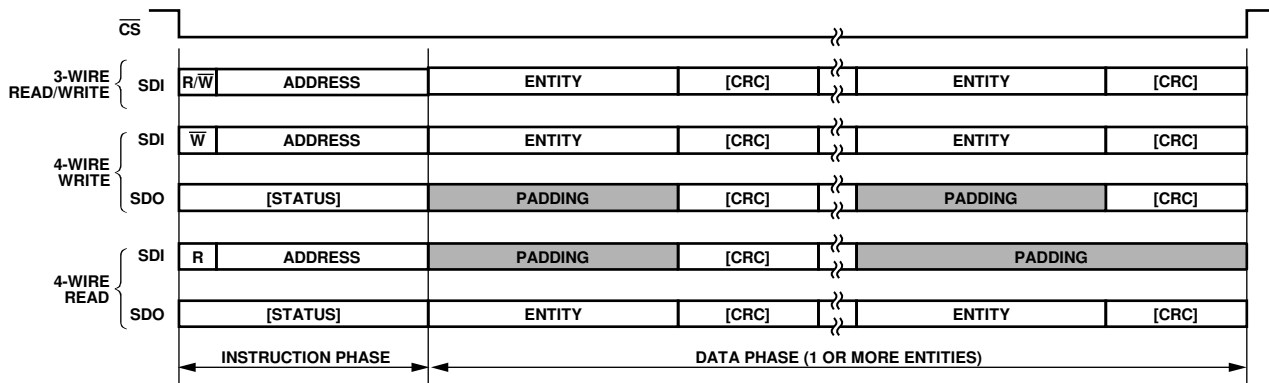


Figure 111. 3-Wire and 4-Wire SPI Transaction Protocols

the falling edge of the SCLK is the driving edge, and the rising edge of the SCLK is the sampling edge. The output data on the SDO pin is clocked out on the falling edge of SCLK and the input data on the SDI pin is sampled on the rising edge of SCLK.

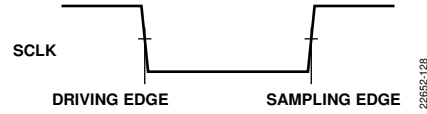


Figure 109. SCLK Edges

The SPI interface uses a 7-bit addressing scheme and supports three modes of operation: 3-wire mode, 4-wire mode, and minimum I/O mode. An optional CRC function is also available for improving communication robustness.

#### 3-Wire Mode

In this mode, SDO is disabled and read data is available on the DEC2/SDI pin. SDO is high impedance in the command, and the data is shorted to SDI (see Figure 110).

#### 4-Wire Mode

The standard SPI interface consists of four signals, as shown in Figure 111.

**SPI CRC**

The SPI CRC code is an optional feature. Enabling it allows the user to improve transaction robustness on the SPI bus, for example, in a noisy environment.

The SPI CRC is calculated with the  $x^8 + x^2 + x + 1$  polynomial with an initial seed value of 0xA5.

The SPI CRC achieves a Hamming distance of 4 with a maximum word length of 119 bits.

**3-Wire Isolated Mode**

The AD7134 powers up in 3-wire isolated mode and a toggle on the chip select line makes the AD7134 exit this mode. The chip select line is not used and must be connected to ground. The SPI packet is 24 bits, consisting of an 8-bit command and address, 8-bit data (entity), and 8-bit CRC. See Figure 112 for 3-wire isolated mode. Also note that a streaming register read or write is not supported in this mode.

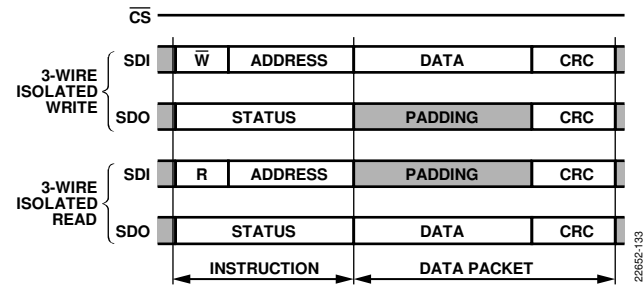


Figure 112. 3-Wire Isolated Mode

**Additional SPI Features**

The AD7134 provides the user several options to control the SPI interface. Some of the features are listed in the following sections.

**Single Instruction Mode**

When the SINGLE\_INSTR bit is set, streaming is disabled and only one read or write operation is performed regardless of the state of the CS line. If this bit is set and CS remains asserted, the state machine resets after the data byte as if CS was deasserted and awaits the next instruction. Single instruction mode forces each data byte to be preceded with a new instruction even though the CS line has not been deasserted. Single instruction mode also allows additional flexibility in the usage of the CS pin if it is required for an application. The default for this bit is set, resulting in streaming being enabled.

**SPI Interface Lock/Unlock**

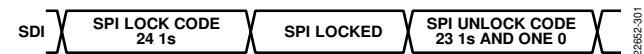


Figure 113. SPI Lock/Unlock and Reset

The AD7134 provides the user an option to lock the SPI interface by performing an SPI write of 24 consecutive 1s. This write blocks the SPI read/write access to registers. To unlock and reset, the user must perform an SPI write of 23 1s and one 0. The status of the SPI interface can be read by completing an SPI read to an SPI register whose value is known. If the SPI interface is out of sync, the user initiates an unlock and resets the SPI interface. At any point, if

the SPI interface is not responding, execute a lock and unlock. This unlock/lock does not affect any data transaction in progress on the data interface and does not affect the SDO behavior.

**Stream Mode**

Stream mode allows the user to consecutively access one or more registers repeatedly without having to carry the overhead associated with setting up the address each cycle. At the end of the loop, the autogenerated address resets to the beginning address and resumes counting until the last address is reached again. The process continues as long as the CS is not deactivated. When CS is deactivated, stream mode is terminated until started again by the user.

The STREAM\_MODE register is used to tell the device how many consecutive registers are to be accessed in the stream mode. If this register is 0x00, the default, streaming is not enabled. If the value in this register is not zero, when streaming is initiated, the value in this register tells the address generator how many consecutive addresses are to be written to or read from before looping back to the beginning address. If the value in this address is 0x01, the same address is written to or read from for the duration of the stream event. If the value is 0x02, two consecutive addresses are written (or read) for the duration. If, for example, the stream entry point is Address 0x10, Address 0x10 is the first address. Address 0x11 is the second address. After this loop is complete, the next autogenerated address is 0x10 and so on. This cycle continues until terminated by the user by deasserting the CS line.

To initiate stream mode, the user must first set this register, 0x000E, with a nonzero value indicating how many addresses are to be accessed. Any value between 0x01 and 0xFF is valid. Take care that all addresses within this scope are suitable for streaming because some addresses may be specified as do not change. Next, begin the read or write cycle as usual.

**Master Slave Transfer Bit**

Bit 0 of the TRANSFER\_REGISTER is used as the master slave transfer bit, which is useful when a register is composed of multiple bytes that must all be written simultaneously to prevent erroneous device operation. In master mode, the ODR\_VAL\_INT\_x and ODR\_VAL\_FLT\_x registers need this implementation. When this bit is set, multiple bytes of data that have been transferred using the SPI are written at one time to the slave. Upon completion of the transfer, the slave device clears this bit (autoclear), indicating to the SPI master that the transfer completed and the slave data can be read back if desired by the control program.

**DATA INTERFACE**

The AD7134 has a flexible data interface designed to support the different digital host types and applications requirements.

The AD7134 can act as the data interface master or slave. The data interface supports both gated and free running clock signals, parallel or serial output data steaming modes, and daisy-chain configuration.

The data interface consists of three signal types: clock, data, and data framing signal.

### Data Interface Clock

The AD7134 supports both gated and free running DCLK signals. The ADC output data is clocked out on the DCLK rising edge.

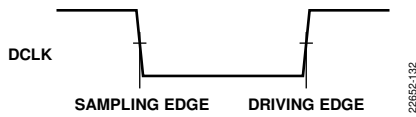


Figure 114. DCLK Edges

DCLK is a bidirectional pin. The AD7134 can act as an interface master and generate the DCLK signal, or act as an interface slave and clock out data based on a received DCLK signal.

When the DCLK pin is configured as an output, the user can choose the DCLK output frequency through the DATA\_PACKET\_CONFIG register or configuration of the DCLKRATEx/GPIOx pins in pin control mode.

Refer to the Programming Output Data Rate and Clock section for more information on how to configure the DCLK frequency.

### Data Bus

The ADC output data appears on the DOUTx pins. Each AD7134 device has four data output pins: DOUT0, DOUT1, DOUT2, and DOUT3. The user has the option to parallel output the ADC conversion result on the four DOUTx pins or to serialize the data from multiple channels and output them using one or two of the DOUTx pins.

Parallel output configuration allows a high data rate at a low DCLK frequency. A serialized output configuration requires fewer I/Os from the digital host and can reduce the number of digital isolator channels required in an isolation application. The daisy-chain mode is available only with a serialized output configuration.

### Data Framing Signal

The ODR control signal is dual purposed to act as the framing signal for the AD7134 data interface.

The ODR pin is bidirectional with its signal direction dependent on the ASRC mode of operation.

The output data can be driven out with respect to the ODR falling or rising edge depending on the mode of DCLK used.

### Choosing the Data Interface Mode of Operation

The direction of the ODR signal depends on the choice of the ASRC mode of operation. See the Asynchronous Sample Rate Converter section for more information on the ASRC.

### Data Interface Status and CRC Header

The user has the option to append a byte width header to each output data sample for additional status information and/or error checking. The header consists of 6-bit CRC code with two status bits, as shown in Table 36.

Table 36. Details of the Header

| Bit   | Bit Description               |
|-------|-------------------------------|
| 7     | Chip error                    |
| 6     | Filter settled and PLL locked |
| [5:0] | 6-bit CRC                     |

Bit 7 is set if an error is detected by the on-chip diagnostic circuitry of the AD7134. See the Diagnostics section for more details of the diagnostic features of the device.

Bit 6 is set if the digital filter on the corresponding channel is fully settled and, when operating in ASRC slave mode, the PLL is locked after an ODR input frequency change.

The data sample value does not reflect the correct conversion result when Bit 6 of the header has a value of zero.

### Data CRC Calculation

The CRC is calculated with the polynomial and initial seed value as shown in Table 37.

Table 37. Data CRC Calculation

| CRC Mode | Polynomial                | Default Seed Value |
|----------|---------------------------|--------------------|
| CRC-6    | $x^6 + x^5 + x^2 + x + 1$ | 0x25               |

### Alternative CRC Mode of Operation

The AD7134 uses a linear feedback shift register (LFSR) to calculate the CRC. In pin control mode and in SPI control mode, by default, the LFSR is reset after each data sample with the default seed value (see Table 37). In SPI control mode, the user has the option to alter the LFSR resetting behavior. Configure CRC\_POLY\_RST\_SEL to 1 to disable the reset of the LFSR after each sample, making the current CRC result in the seed value of the next calculation. This mode allows the processor-based digital host to check the CRC less frequently and still be able to detect an error in the bit transfer.

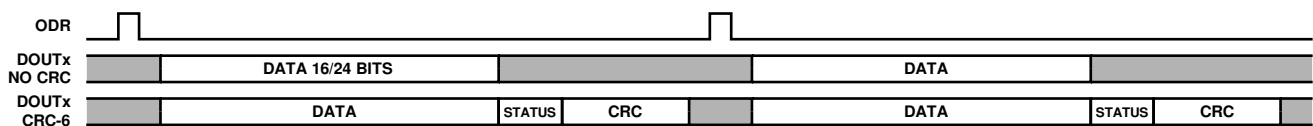


Figure 115. Data CRC Options

**ASRC Master Mode Data Interface**

When the ASRC is in master mode, the ODR pin behaves as an output. The user has the choice to operate the DCLK pin in gated mode or in free running mode.

With the DCLK pin configured as an output, the AD7134 acts as the data interface master, providing the DCLK signals and the output data stream synchronously to the ODR signal.

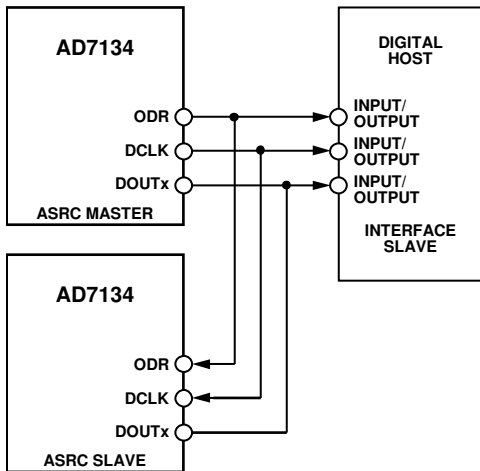


Figure 116. Data Interface Example 1, First AD7134 Device in ASRC Master Mode with the Digital Host as Interface Slave

**ASRC Slave Mode Data Interface**

When the ASRC is in slave mode, the ODR pin behaves as an input. The user has the choice to operate the DCLK pin in gated mode or in free running mode.

With the DCLK pin configured as an input, the AD7134 acts as the data interface slave, providing the output data stream on the input DCLK driving edge.

If the DCLK pin is configured as a free running input, the user must ensure that the DCLK pin is synchronized to the ODR signal for proper data framing.

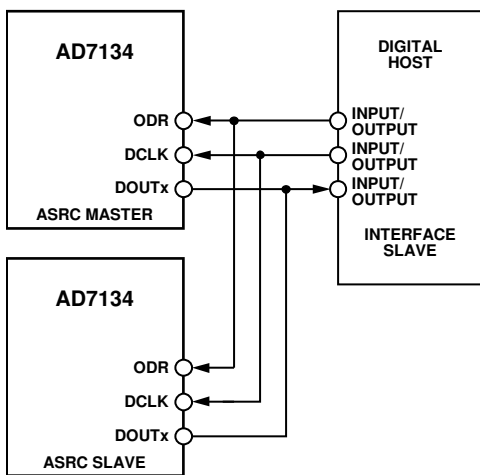


Figure 117. Data interface Example 2, Two AD7134 Devices in ASRC Slave Mode with Digital Host as Interface Master

**Daisy-Chaining**

Daisy-chaining allows numerous devices to use the same data interface lines by cascading the outputs of multiple ADCs from separate AD7134 devices. The data interface of only one ADC device is in direct connection with the digital host.

For the AD7134, implement this connection by cascading DOUT0 and DOUT1 through a number of devices, or using only DOUT0.

This feature is especially useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity.

When daisy-chaining with two channels, DOUT2 and DOUT3 become serial data inputs, and DOUT0 and DOUT1 remain as serial data outputs.

Figure 118 shows an example of daisy-chaining the AD7134 devices with two channels. In this case, the DOUT0 pin and DOUT1 pin of the AD7134 devices are cascaded to the DOUT2 and DOUT3 pins of the next device in the chain. Data readback is analogous to clocking a shift register.

The scheme operates by passing the output data of the DOUT0 pin and DOUT1 pin of an AD7134 downstream device to the DOUT2 and DOUT3 inputs of the next AD7134 device upstream in the chain. The data then continues through the chain until it is clocked onto the DOUT0 pin and DOUT1 pin of the final upstream device in the chain.

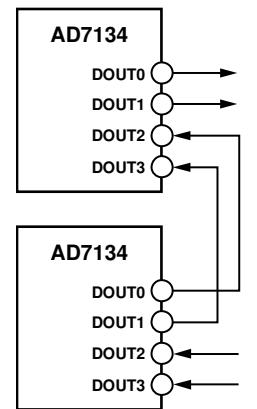


Figure 118. Data Interface Connection with 2-Channel Daisy-Chaining Configuration

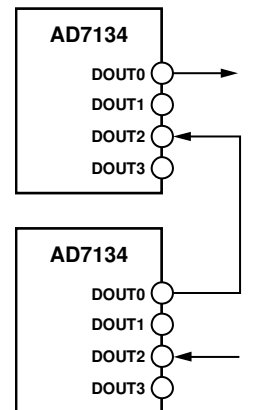


Figure 119. Data Interface Connection with 1-Channel Daisy-Chaining Configuration

Daisy-chaining can be achieved in a similar manner on the AD7134 when using only the DOUT0 pin. In this case, only the DOUT2 pin is used as the serial data input pin, as shown in Figure 119.

If the AD7134 is used in the chain as a master for generating the ODR and DCLK, the user must program the DAISY\_CHAIN\_DEV\_NUM bits to let the device know how many devices are connected to it. Programming the DAISY\_CHAIN\_DEV\_NUM bits ensures that the AD7134 generates a sufficient number of DCLK cycles to clock the data out from all the devices in the chain. For example, in Figure 120, program the DAISY\_CHAIN\_DEV\_NUM bits in the master device to 0x01 so that the AD7134 can generate the number of DCLK cycles to clock out data from both the devices.

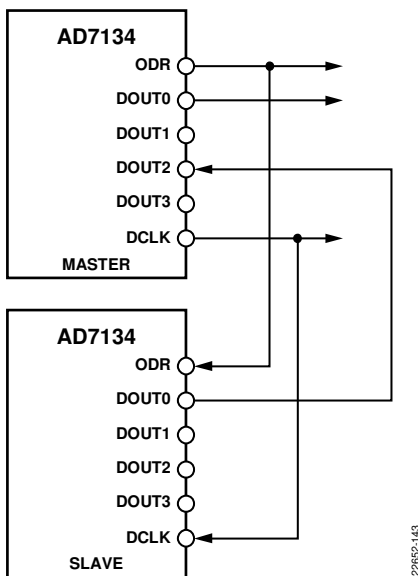


Figure 120. Single Channel Daisy Chain for Master Slave Configuration

The number of devices supported on a chain is limited by the DCLK frequency chosen for a given output data rate.

The maximum usable DCLK frequency allowed when daisy-chaining devices is limited by the combination of timing specifications and the DCLK mode of operation.

### Data Interface Frame Length

The AD7134 data interface operates with the byte-based transfer scheme. That is, the transactions are in multiples of eight bits.

The data frame length, defined as the number of data bytes per ODR cycle per DOUTx pin, depends on the following factors:

- Conversion output word size
- Status or CRC header
- Data output format configuration
- Daisy-chain configuration
- Data averaging

The conversion output word size can be 16 bits or 24 bits.

It is optional to include a status or CRC header byte with each conversion result to improve the communication robustness and to receive real-time error status.

The user can choose to parallel or serialize the output data. Serializing the output data from four ADC channels to one DOUTx pin increases the data frame length by 4×

If multiple devices are daisy-chained, the total data frame length is equal to the sum of the data frame length of the individual devices on the chain.

### Frame Length Examples

In Case 1, the following conditions apply:

- 16-bit output format
- No status or CRC header
- Parallel output on all four DOUTx pins
- No daisy chain
- Averaging disabled

The output data frame length is  $16/8 = 2$  bytes per ODR period on each of the four DOUTx pins.

In Case 2, the following conditions apply:

- 24-bit data format
- Status and CRC header enabled
- Output on two DOUTx pins
- Daisy chain three devices
- Averaging disabled

The output data frame length is  $(24/8 + 1) \times 2 \times 3 = 24$  bytes per ODR period on each of the two DOUTx pins.

In Case 3, the following conditions apply:

- 24-bit output format
- Status/CRC header enabled
- Output on one DOUTx pins
- Daisy-chain two devices
- 4:1 averaging

The output data frame length is  $(24/8 + 1) \times 4 \times 2/4 = 8$  bytes per ODR period.

### DCLK Frequency Selection

The user must ensure an adequate DCLK frequency is used to clock out the full length of the data frame in time.

The maximum supported DCLK frequency on the AD7134 is 48 MHz as an output and 50 MHz as an input.

### Gated DCLK Output Cycles

When DCLK is configured as a gated output, the AD7134 uses an internal counter to control the number of DCLK cycles to output after each ODR pulse. The device automatically adjusts the number of DCLK cycles to output according to its data frame and format configuration.

However, in daisy-chain mode, the device has no inherent knowledge of the number of devices connected on the chain.

In pin control mode, unless the device is configured to operate in quad channel parallel output mode, it assumes a daisy-chain configuration. If the DCLK pin is configured as a gated output, the device assumes that four devices are on the daisy chain. The number of DCLK cycles it generates after each ODR pulse is equal to four times the data frame length of the devices.

In SPI control mode, the user has the flexibility to program the number of devices on the daisy chain through the DAISY\_CHAIN\_DEV\_NUM bits. The value acts as a multiplier to the number of DCLK cycles the device outputs after each ODR pulse when the DCLK is configured as a gated output.

**Gated DCLK Output Cycles Examples**

In Case 1, the following conditions apply:

- 16-bit output format
- No status or CRC header
- Single-channel daisy-chain mode
- Pin control mode operation
- DCLK configured as gated output

The device outputs  $16 \times 4 = 64$  DCLK cycles after each ODR pulse.

In Case 2, the following conditions apply:

- 24-bit output format
- Status and CRC header enabled
- Dual-channel daisy-chain mode

- Averaging disabled
- SPI control mode operation
- DAISY\_CHAIN\_DEV\_NUM = 3 (decimal)

The device outputs  $(24 + 8) \times 2 \times 3 = 192$  DCLK cycles after each ODR pulse.

**Channel Dependent ODR**

In SPI control mode, the AD7134 supports the configuration of different ODR rates on each channel using the CHANNEL\_ODR\_SELECT register. The rate must be a power of two fraction of the signal frequency on the ODR pin and is limited to a minimum of 1/8 of the main ODR frequency.

Each channel updates its conversion output based on the ODR rate of the channel. For example, if a channel is configured to have an output data rate of ODR/4, its output data updates once every four ODR cycles. Figure 121 shows an example of the data interface timing of a device with different output data rate settings on each channel.

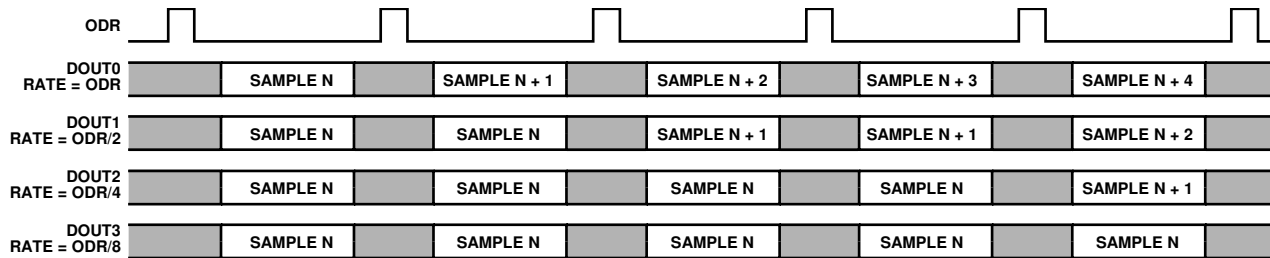


Figure 121. Data Interface Timing Example of a Device with Different ODR Settings on Each Channel

22652-144

### Digital Interface Reset

Bit 1 of the INTERFACE\_CONFIG\_B register (DIG\_IF\_RESET) resets the data interface. In multidevice configuration, this bit synchronizes data channel outputs to achieve device to device channel phase matching. This bit is self clearing and only available for use in SPI slave mode operation. Refer to the Multidevice Synchronization section.

### MINIMUM I/O MODE

Certain applications require a minimum number of I/O lines to be used for interfacing with the AD7134. This requirement may be due to the limited number of I/Os available on the digital host, or for cost reasons, to minimize the number of digital isolation channels required in an isolated application.

The AD7134 is designed to support both register and data access using as few as only four unidirectional I/O lines.

The minimum I/O mode configuration essentially combines the register and data access interface on the AD7134 and allows the digital host to interface with the AD7134 with only one SPI port as master.

The trade-off of minimizing the number of I/O ports is more complicated firmware design and a potentially higher CPU processing load.

On power-on, the AD7134 boots up in minimum I/O mode and a toggle on  $\overline{\text{CS}}$  pin makes the device exit the minimum I/O mode. Also, SPI CRC is enabled in minimum I/O mode and

cannot be disabled. All SPI packets must be 24 bits, which is R/W + Address (8-bit), data (8-bit), and CRC (8-bit), as described in Figure 114. To configure the AD7134 to operate with a minimum number of IO lines, perform the following sequence:

1. Connect the FORMAT0/ $\overline{\text{CS}}$  pin to ground.
2. Externally connect DCLK to the FORMAT1/SCLK pin.
3. Configure DCLK to be a gated input.
4. Set ASRC slave mode.
5. Set FORMATx to 00 wherein data from all four ADC channels are converged and output through DOUT0.
6. Set the SDO\_PIN\_SRC\_SEL bit to 1.

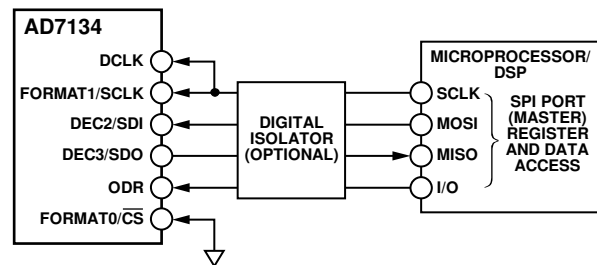


Figure 122. Signal Connection Diagram of Minimum I/O Configuration

In minimum I/O mode, the user can use the DEC3/SDO pin for both register content and ADC conversion data readback. Only one of the SDO and DOUT0 outputs are allowed to be enabled at any given time. Setting the SDO\_PIN\_SRC\_SEL bit to 1 causes the signal on DOUT0 to be duplicated on the DEC3/SDO pin.



## DIAGNOSTICS

The AD7134 has numerous diagnostic functions on chip that monitor and report errors for the following functional blocks:

- Internal fuses
- Analog input range
- MCLK frequency
- SPI communication
- Memory map value
- ODR input frequency
- Digital filters

In SPI control mode, the user can enable or disable the following diagnostic features through the diagnostic control register:

- Fuse cyclic redundancy check (CRC)
- Memory map CRC
- SPI CRC
- MCLK counter
- Analog input range

Figure 123 shows all the different types of blocks monitored, as well as blocks that are enabled using the diagnostic control register.

The remaining diagnostic features run continuously on the device and all the bits except the NO\_CHIP\_ERR bit are cleared on a read.

As shown in Figure 123, the NO\_CHIP\_ERR bit in the device configuration register is the master error status bit. This bit is cleared if any of the other status error bits are set. This bit sets back to 1 when all the status bits are cleared, indicating no chip error.

### INTERNAL FUSE INTEGRITY CHECK

The AD7134 uses a fuse type memory to store the factory programmed calibration values that are unique to each device. When leaving the factory, a CRC code is calculated based on the final fuse values of the device and is stored in the device memory.

On each power-up, the device reads the fuse memory for self configuration. The device also performs a CRC calculation based on the fuse values read and compares the calculation against the factory programmed value to detect a fuse reading error.

The device sets the ERR\_FUSE\_CRC bit if a fuse CRC error is detected.

The user can also initiate a fuse check by using the FUSE\_CRC\_CHECK bit in the diagnostic control register. This bit is cleared when the check is complete. When this check is executed, the data output is interrupted.

The fuse CRC supports 1-bit error correction. The device tries to correct the error when detected. The AD7134 sets the STAT\_FUSE\_ECC bit if the error is corrected and sets the ERR\_FUSE\_CRC bit if the fuse CRC error correction is not completed.

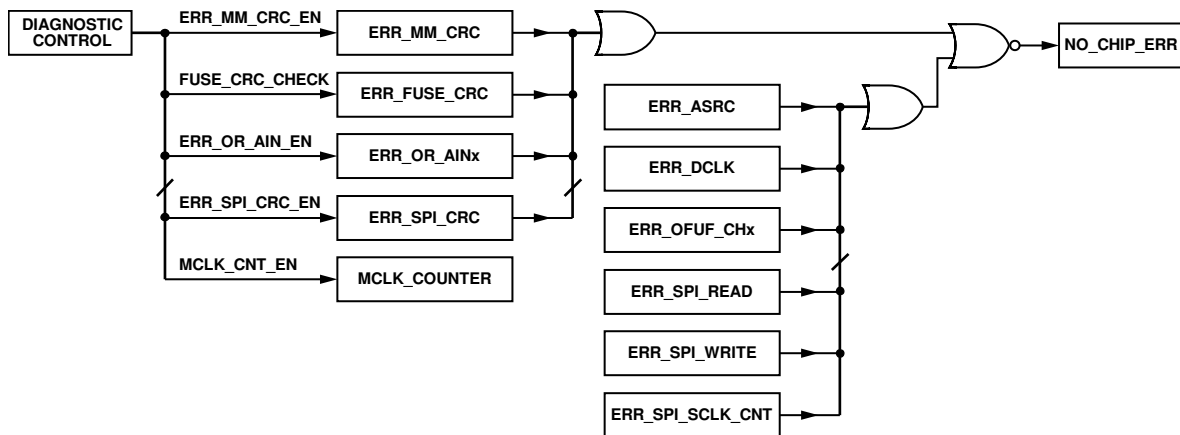


Figure 123. Errors

22852-148

## ANALOG INPUT OVERRANGE

An on-chip, full-scale overrange detection monitor flags a bit on detection of a positive full-scale input voltage between the AINx+ pins and AINx- pins. This detection is enabled on each channel by using the ERR\_OR\_AIN\_EN bit in the diagnostic control register, and an overvoltage bit corresponding to the particular channel is set if the voltage exceeds the full scale corresponding to that channel.

Four overvoltage flags in the AIN\_OR\_ERROR register corresponding to the four input channels are cleared on a read.

## MCLK COUNTER

A stable MCLK is important because the output data rate, filter settling time, and the filter notch frequencies are dependent on the master clock. The AD7134 allows the user to monitor the master clock. When the MCLK\_CNT\_EN bit in the diagnostic control register is set, the MCLK\_COUNTER register increments by one every 12,000 master clock cycles. The user can monitor this register over a fixed period by running a timer in the controller, and the master clock frequency can be determined from the result in the MCLK\_COUNTER register.

$$MCLK = \text{Register Data} \times 12,000 / \text{Timer Value}$$

where *Register Data* is in decimal format.

For example, if MCLK is 24 MHz and the timer is set to 100 ms, the expected MCLK\_COUNTER value is 0xC8. This register wraps around after it reaches its maximum value.

## SPI INTERFACE MONITORING

The AD7134 supports a number of diagnostic measures to improve the robustness of its SPI interface.

### Accessing Undefined Register Address

When the user tries to access an undefined register address, the device ignores the instruction and flags an error in the ERR\_SPI\_READ bit or the ERR\_SPI\_WRITE bit. These bits are cleared on a read.

### SCLK Counter

The AD7134 uses an SCLK counter to count the number of SCLK cycles supplied in each of the read and write transactions framed by the CS signal. The device flags an error in the ERR\_SPI\_SCLK\_CNT bit if the number of SCLK cycles at the end of each SPI transaction is not an integer multiple of 8. This bit is cleared on a read. The SCLK counter is not available in minimum I/O mode.

### SPI CRC

When the ERR\_SPI\_CRC\_EN bit in the diagnostic control register is set, a CRC check for all SPI read and write operations is enabled. The ERR\_SPI\_CRC bit in the SPI error register is set if the CRC check fails. This bit is cleared on a read.

For CRC checksum calculations, the polynomial used is  $x^8 + x^2 + x + 1$  and has a reset seed of 0xA5.

The 8-bit checksum is appended to the end of each read and write transaction. The checksum calculation for the write

transaction is calculated using the 8-bit command word and data. For a read transaction, the checksum is calculated using the command word and the data output.

For write or read operation, the host sends the R/W bit, the address (eight bits), the data (eight bits), and the 8-bit CRC (on R/W, address, and data).

In a write operation, while the host is sending the CRC on the SDI line, the slave simultaneously transmits the CRC calculated on the write + address + data that the slave has received. The slave executes a write operation only when the received CRC sent by the host matches with its calculated CRC. The slave sends a 1-bit status followed by 15 zeros and the 8-bit CRC (see Figure 124).



Figure 124. SPI Write with CRC

In a read operation, while the host is sending the CRC on the SDI line, the slave simultaneously transmits the CRC calculated on the command and the read data. The slave sends a 1-bit status followed by seven zeros, 8-bit read data, and 8-bit CRC (see Figure 125).

The 1-bit status sent by the slave is the error bit, which indicates that the previous frame had a read, write, or CRC error.

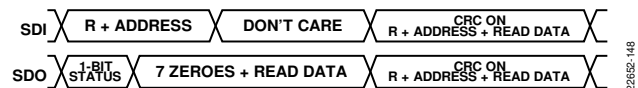


Figure 125. SPI Read with CRC

## MEMORY MAP INTEGRITY CHECK

When the ERR\_MM\_CRC\_EN bit is set in the diagnostic control register, a CRC of the data from all the on-board registers with write access is calculated and the results are stored in memory. The device then continuously performs the CRC calculation at a frequency of 2.4 kHz, and compares each output with the CRC value stored in memory. The device sets the ERR\_MM\_CRC bit if the two values are different. This bit is cleared on a read. The CRC value stored in the memory is also recalculated after each SPI write transaction.

This feature is useful for detecting a soft error in the memory map.

## ODR INPUT FREQUENCY CHECK

An ODR input frequency check applies only to device operation in ASRC slave mode.

The device checks the input ODR signal frequency after the PLL locks and sets the ERR\_ASRC bit if the ODR frequency detected is outside the range for the particular type of filter selected as specified in Table 19. This bit is cleared on a read.

For example, if the ODR input is set to 600 kSPS and the type of filter set is wideband, this error is flagged. There is no data output in this scenario.

**DIGITAL FILTER OVERFLOW AND UNDERFLOW**

The digital filter overflow/underflow occurs when the input is overrange or due to an incorrect setting of the gain and calibration register. The AD7134 monitors the digital filter path and sets the corresponding channel bit in the DIG\_FILTER\_OFUF register when an overflow or underflow condition is detected.

For proper usage of this diagnostic feature, it is recommended to read back these flags after power-up.

**DCLK ERROR**

The device has a built in feature to flag insufficient numbers of data clocks needed to clock out the complete frame.

The user must program or provide a data clock that is fast enough to clock out the complete frame for the given ODR and ensure that for the gated mode,

$ODR\ Time > t_{DCLK} \times Frame\ Size + 6 \times t_{DCLK}/t_{DIGCLK}$  (whichever is higher)

And for free mode,

$ODR\ Time > t_{DCLK} \times Frame\ Size + 4 \times t_{DCLK}/t_{DIGCLK}$  (whichever is higher) (1)

The ERR\_DCLK flag sets if the programmed or provided DCLK frequency is such that Equation 1 is not met, resulting in an insufficient number of data clocks to clock out the entire frame. This bit is cleared on a read.

## GPIO FUNCTIONALITY

The AD7134 has additional GPIO functionality when operated in SPI control mode. This fully configurable mode allows the device to operate eight GPIOs, thus making the AD7134 work as an SPI-based GPIO expander. The GPIO pins can be set as inputs or outputs (read or write) on a per pin basis.

In write mode, these GPIO pins can be used to control other circuits such as switches, amplifiers, multiplexers, and buffers over the same SPI interface as the AD7134. Sharing the SPI interface in this way allows the user to use a lower overall number of data lines from the controller, compared to a system where multiple control signals are required. This sharing is especially useful in systems where reducing the number of control lines across an isolation barrier is important. Similarly, a GPIO read is a useful feature because it allows a peripheral device to send information to the input GPIO and then this information can be read from the SPI interface of the AD7134.

The GPIO pins can be used as general-purpose inputs or outputs. The GPIO\_DIR\_CTRL register configures the individual pin as an input or output. The GPIO\_DATA register reflects the status of the pins when configured as inputs or the user can write to this register to set the pins when configured as outputs (see Figure 126).

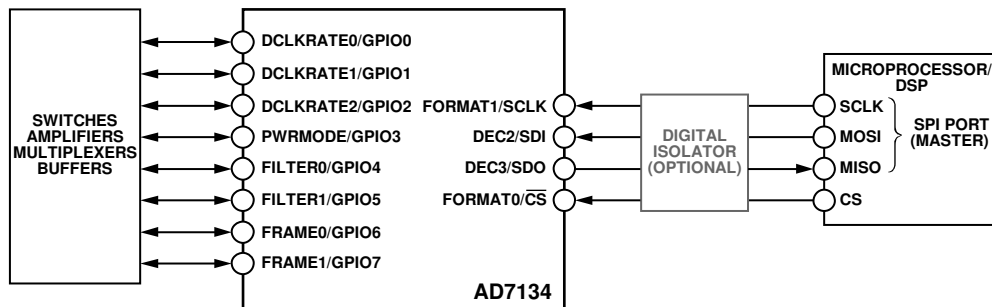


Figure 126. AD7134 as SPI GPIO Expander

22852-149

## PIN ERROR REPORTING

Additionally, GPIO7 can be used as an output to report any of the diagnostic errors by enabling Bit ERR\_PIN\_OUT\_EN. Register ERROR\_PIN\_SRC\_CONTROL controls the type of errors that can be reported on this pin. If multiple types are selected, the output is a logical OR of all the selected errors.

GPIO6 can be used as an error input from any other device by enabling the ERR\_PIN\_IN\_EN bit. The status of this bit can be read using the ERR\_PIN\_IN\_STATUS bit.

The GPIO7 output is a logical OR of all the selected errors, as per the ERROR\_PIN\_SRC\_CONTROL register and the ERR\_PIN\_IN\_STATUS bit.

## REGISTER MAP (SPI CONTROL)

See Table 38 for the register map for the device (SPI control).

**Table 38. Register Map**

| Reg  | Name                     | Bit 7               | Bit 6             | Bit 5                 | Bit 4               | Bit 3                 | Bit 2                        | Bit 1              | Bit 0               | Reset | RW               |     |
|------|--------------------------|---------------------|-------------------|-----------------------|---------------------|-----------------------|------------------------------|--------------------|---------------------|-------|------------------|-----|
| 0x0  | INTERFACE_CONFIG_A       | SOFT_RESET          | Reserved          | ADDRESS_ASCENSION_BIT | SDO_ACTIVE_BIT      | SDO_ACTIVE_BIT_MIRROR | ADDRESS_ASCENSION_BIT_MIRROR | Reserved           | SOFT_RESET_MIRROR   | 0x18  | R/W              |     |
| 0x1  | INTERFACE_CONFIG_B       | SINGLE_INSTR        | Reserved          | MASTER_SLAVE_RD_CTRL  | Reserved            |                       |                              | DIG_IF_RESET       | Reserved            | 0x80  | R/W              |     |
| 0x2  | DEVICE_CONFIG            | Reserved            |                   | OP_IN_PROGRESS        | NO_CHIP_ERR         | Reserved              |                              |                    | POWER_MODE          | 0xD0  | R/W              |     |
| 0x3  | CHIP_TYPE                | CHIP_TYPE           |                   |                       |                     |                       |                              |                    |                     |       | 0x07             | R   |
| 0x4  | PRODUCT_ID_LSB           | PRODUCT_ID[7:0]     |                   |                       |                     |                       |                              |                    |                     |       | N/A <sup>1</sup> | R   |
| 0x5  | PRODUCT_ID_MSB           | PRODUCT_ID[15:8]    |                   |                       |                     |                       |                              |                    |                     |       | N/A <sup>1</sup> | R   |
| 0x6  | CHIP_GRADE               | PRODUCT_GRADE       |                   |                       |                     | DEVICE_VERSION        |                              |                    |                     | 0x00  | R                |     |
| 0x7  | SILICON_REV              | SILICON_REVISION_ID |                   |                       |                     |                       |                              |                    |                     |       | 0x02             | R   |
| 0xA  | SCRATCH_PAD              | SCRATCH_PAD         |                   |                       |                     |                       |                              |                    |                     |       | 0x00             | R/W |
| 0xB  | SPI_REVISION             | SPI_REVISION_NUMBER |                   |                       |                     |                       |                              |                    |                     |       | 0x02             | R   |
| 0xC  | VENDOR_ID_LSB            | VENDOR_ID[7:0]      |                   |                       |                     |                       |                              |                    |                     |       | 0x56             | R   |
| 0xD  | VENDOR_ID_MSB            | VENDOR_ID[15:8]     |                   |                       |                     |                       |                              |                    |                     |       | 0x04             | R   |
| 0xE  | STREAM_MODE              | STREAM_MODE_BITS    |                   |                       |                     |                       |                              |                    |                     |       | 0x00             | R/W |
| 0xF  | TRANSFER_REGISTER        | Reserved            |                   |                       |                     |                       |                              |                    | MASTER_SLAVE_TX_BIT | 0x00  | R/W              |     |
| 0x10 | DEVICE_CONFIG_1          | Reserved            |                   |                       |                     | AA_MODE               | SDO_PIN_SRC_SEL              | REFIN_GAIN_CORR_EN | XCLKOUT_EN          | 0x00  | R/W              |     |
| 0x11 | DATA_PACKET_CONFIG       | CRC_POLY_RST_SEL    | Reserved          | Frame                 |                     | DCLK_FREQ_SEL         |                              |                    |                     | 0x00  | R/W              |     |
| 0x12 | DIGITAL_INTERFACE_CONFIG | DAISY_CHAIN_DEV_NUM |                   |                       |                     | AVG_SEL               |                              | Format             |                     | 0x00  | R/W              |     |
| 0x13 | POWER_DOWN_CONTROL       | Reserved            | PWRDN_CH3         | PWRDN_CH2             | PWRDN_CH1           | PWRDN_CH0             | Reserved                     | PWRDN_LDO          | SLEEP_MODE_EN       | 0x00  | R/W              |     |
| 0x14 | RESERVED                 | Reserved            |                   |                       |                     |                       |                              |                    |                     |       | 0x00             | R/W |
| 0x15 | DEVICE_STATUS            | Reserved            |                   | STAT_DCLKMODE         | STAT_DCLKIO         | STAT_MODE             | STAT_CLKSEL                  | STAT_FUSE_ECC      | STAT_PLL_LOCK       | 0x00  | R                |     |
| 0x16 | ODR_VAL_INT_LSB          | ODR_VAL_INT[7:0]    |                   |                       |                     |                       |                              |                    |                     |       | 0x40             | R/W |
| 0x17 | ODR_VAL_INT_MID          | ODR_VAL_INT[15:8]   |                   |                       |                     |                       |                              |                    |                     |       | 0x00             | R/W |
| 0x18 | ODR_VAL_INT_MSB          | ODR_VAL_INT[23:16]  |                   |                       |                     |                       |                              |                    |                     |       | 0x00             | R/W |
| 0x19 | ODR_VAL_FLT_LSB          | ODR_VAL_FLT[7:0]    |                   |                       |                     |                       |                              |                    |                     |       | 0x72             | R/W |
| 0x1A | ODR_VAL_FLT_MID0         | ODR_VAL_FLT[15:8]   |                   |                       |                     |                       |                              |                    |                     |       | 0xB7             | R/W |
| 0x1B | ODR_VAL_FLT_MID1         | ODR_VAL_FLT[23:16]  |                   |                       |                     |                       |                              |                    |                     |       | 0xCE             | R/W |
| 0x1C | ODR_VAL_FLT_MSB          | ODR_VAL_FLT[31:24]  |                   |                       |                     |                       |                              |                    |                     |       | 0x2B             | R/W |
| 0x1D | CHANNEL_ODR_SELECT       | ODR_RATE_SEL_CH3    | ODR_RATE_SEL_CH2  |                       | ODR_RATE_SEL_CH1    |                       | ODR_RATE_SEL_CH0             |                    |                     | 0x00  | R/W              |     |
| 0x1E | CHAN_DIG_FILTER_SEL      | DIGFILTER_SEL_CH3   | DIGFILTER_SEL_CH2 |                       | DIGFILTER_SEL_CH1   |                       | DIGFILTER_SEL_CH0            |                    |                     | 0x00  | R/W              |     |
| 0x1F | FIR_BW_SEL               | Reserved            |                   |                       |                     | WB_FILTER_SEL_CH3     | WB_FILTER_SEL_CH2            | WB_FILTER_SEL_CH1  | WB_FILTER_SEL_CH0   | 0x00  | R/W              |     |
| 0x20 | GPIO_DIR_CTRL            | GPIO_IO_CONTROL     |                   |                       |                     |                       |                              |                    |                     |       | 0x00             | R/W |
| 0x21 | GPIO_DATA                | GPIO_DATA           |                   |                       |                     |                       |                              |                    |                     |       | 0x00             | R/W |
| 0x22 | ERROR_PIN_SRC_CONTROL    | Reserved            |                   | ERR_PIN_EN_OR_AIN     | ERR_PIN_EN_INTERNAL | ERR_PIN_EN_SPI        | Reserved                     |                    |                     | 0x00  | R/W              |     |
| 0x23 | ERROR_PIN_CONTROL        | Reserved            |                   |                       |                     |                       | ERR_PIN_IN_STATUS            | ERR_PIN_IN_EN      | ERR_PIN_OUT_EN      | 0x00  | R/W              |     |
| 0x24 | VCMBUF_CTRL              | Reserved            | PWRDN_VCMBUF      | VCMBUF_REF_DIV_SEL    |                     |                       |                              |                    | VCMBUF_REF_SEL      | 0x00  | R/W              |     |
| 0x25 | Diagnostic Control       | Reserved            |                   | ERR_OR_AIN_EN         | Reserved            | MCLK_CNT_EN           | ERR_SPI_CRC_EN               | ERR_MM_CRC_EN      | FUSE_CRC_CHECK      | 0x00  | R/W              |     |

| Reg  | Name               | Bit 7             | Bit 6             | Bit 5             | Bit 4            | Bit 3             | Bit 2            | Bit 1             | Bit 0        | Reset | RW   |      |     |
|------|--------------------|-------------------|-------------------|-------------------|------------------|-------------------|------------------|-------------------|--------------|-------|------|------|-----|
| 0x26 | MPC_CONFIG         | MPC_CLKDEL_EN_CH3 |                   | MPC_CLKDEL_EN_CH2 |                  | MPC_CLKDEL_EN_CH1 |                  | MPC_CLKDEL_EN_CH0 |              | 0x00  | R/W  |      |     |
| 0x27 | CH0_GAIN_LSB       | GAIN_CH0[7:0]     |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x28 | CH0_GAIN_MID       | GAIN_CH0[15:8]    |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x29 | CH0_GAIN_MSB       | Reserved          |                   |                   | GAIN_CAL_SEL_CH0 |                   | GAIN_CH0[19:16]  |                   |              |       | 0x00 | R/W  |     |
| 0x2A | CH0_OFFSET_LSB     | OFFSET_CH0[7:0]   |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x2B | CH0_OFFSET_MID     | OFFSET_CH0[15:8]  |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x2C | CH0_OFFSET_MSB     | OFFSET_CAL_EN_CH0 | OFFSET_CH0[22:16] |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x2D | CH1_GAIN_LSB       | GAIN_CH1[7:0]     |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x2E | CH1_GAIN_MID       | GAIN_CH1[15:8]    |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x2F | CH1_GAIN_MSB       | Reserved          |                   |                   | GAIN_CAL_SEL_CH1 |                   | GAIN_CH1[19:16]  |                   |              |       | 0x00 | R/W  |     |
| 0x30 | CH1_OFFSET_LSB     | OFFSET_CH1[7:0]   |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x31 | CH1_OFFSET_MID     | OFFSET_CH1[15:8]  |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x32 | CH1_OFFSET_MSB     | OFFSET_CAL_EN_CH1 | OFFSET_CH1[22:16] |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x33 | CH2_GAIN_LSB       | GAIN_CH2[7:0]     |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x34 | CH2_GAIN_MID       | GAIN_CH2[15:8]    |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x35 | CH2_GAIN_MSB       | Reserved          |                   |                   | GAIN_CAL_SEL_CH2 |                   | GAIN_CH2[19:16]  |                   |              |       | 0x00 | R/W  |     |
| 0x36 | CH2_OFFSET_LSB     | OFFSET_CH2[7:0]   |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x37 | CH2_OFFSET_MID     | OFFSET_CH2[15:8]  |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x38 | CH2_OFFSET_MSB     | OFFSET_CAL_EN_CH2 | OFFSET_CH2[22:16] |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x39 | CH3_GAIN_LSB       | GAIN_CH3[7:0]     |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x3A | CH3_GAIN_MID       | GAIN_CH3[15:8]    |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x3B | CH3_GAIN_MSB       | Reserved          |                   |                   | GAIN_CAL_SEL_CH3 |                   | GAIN_CH3[19:16]  |                   |              |       | 0x00 | R/W  |     |
| 0x3C | CH3_OFFSET_LSB     | OFFSET_CH3[7:0]   |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x3D | CH3_OFFSET_MID     | OFFSET_CH3[15:8]  |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x3E | CH3_OFFSET_MSB     | OFFSET_CAL_EN_CH3 | OFFSET_CH3[22:16] |                   |                  |                   |                  |                   |              |       |      | 0x00 | R/W |
| 0x3F | MCLK_COUNTER       | MCLK_COUNT        |                   |                   |                  |                   |                  |                   |              |       |      | 0x00 | R   |
| 0x40 | DIG_FILTER_OFUF    | Reserved          |                   |                   |                  | ERR_OFUF_CH3      | ERR_OFUF_CH2     | ERR_OFUF_CH1      | ERR_OFUF_CH0 | 0x00  | R    |      |     |
| 0x41 | DIG_FILTER_SETTLED | Reserved          |                   |                   |                  | CH3_SETTLED       | CH2_SETTLED      | CH1_SETTLED       | CH0_SETTLED  | 0x00  | R    |      |     |
| 0x42 | INTERNAL_ERROR     | Reserved          |                   |                   |                  | ERR_DCLK          | ERR_FUSE_CRC     | ERR_ASRC          | ERR_MM_CRC   | 0x00  | R    |      |     |
| 0x47 | SPI Error          | Reserved          |                   |                   |                  | ERR_SPI_CRC       | ERR_SPI_SCLK_CNT | ERR_SPI_WRITE     | ERR_SPI_READ | 0x00  | R    |      |     |
| 0x48 | AIN_OR_ERROR       | Reserved          |                   |                   |                  | ERR_OR_AIN3       | ERR_OR_AIN2      | ERR_OR_AIN1       | ERR_OR_AIN0  | 0x00  | R    |      |     |

<sup>1</sup> N/A means not applicable. The reset value is time stamp dependent and programmed in production.

## REGISTER DETAILS

Address: 0x0, Reset: 0x18, Name: INTERFACE\_CONFIG\_A

Table 39. Bit Descriptions for INTERFACE\_CONFIG\_A

| Bits | Bit Name                     | Settings | Description  | Reset | Access |
|------|------------------------------|----------|--|-------|--------|
| 7    | SOFT_RESET                   | 0<br>1   | Soft Reset of the Device. This bit is cleared on completion of a reset.<br>Default.<br>Initiates a soft reset.   | 0x0   | R/W    |
| 6    | Reserved                     |          | Reserved.  | 0x0   | R      |
| 5    | ADDRESS_ASCENSION_BIT        | 0<br>1   | Register Map Address Ascension/Descend Control. Used in conjunction with streaming mode, address ascension causes sequential register addresses to ascend in order. Disabling causes sequential register addresses to descend in order.<br>Sequential register address in descending order.<br>Sequential register address in ascending order. | 0x0   | R/W    |
| 4    | SDO_ACTIVE_BIT               | 0<br>1   | SDO Control.<br>SDO disabled, exhibit high impedance.<br>SDO enabled.  | 0x1   | R/W    |
| 3    | SDO_ACTIVE_BIT_MIRROR        |          | Mirror Image of SDO_ACTIVE_BIT.  | 0x1   | R      |
| 2    | ADDRESS_ASCENSION_BIT_MIRROR |          | Mirror Image of ADDRESS_ASCENSION_BIT.   | 0x0   | R      |
| 1    | Reserved                     |          | Reserved.  | 0x0   | R      |
| 0    | SOFT_RESET_MIRROR            | 0<br>1   | Mirror Image of SOFT_RESET.<br>Default.<br>Initiates a soft reset.   | 0x0   | R/W    |

Address: 0x1, Reset: 0x80, Name: INTERFACE\_CONFIG\_B

Table 40. Bit Descriptions for INTERFACE\_CONFIG\_B

| Bits  | Bit Name             | Settings | Description   | Reset | Access |
|-------|----------------------|----------|---|-------|--------|
| 7     | SINGLE_INSTR         | 0<br>1   | Single Instruction Mode Control. When set, this bit disables streaming regardless of the state of $\overline{CS}$ . When clear, streaming is enabled.<br>Disable.<br>Enable.  | 0x1   | R/W    |
| 6     | Reserved             |          | Reserved.   | 0x0   | R      |
| 5     | MASTER_SLAVE_RD_CTRL | 0<br>1   | Master Slave Readback Control. Determines the data to read back from the master or slave buffered bits (ODR_VAL_INT_x and ODR_VAL_FLT_x). Set to 1 to read back from master output. Clear this bit to read back from slave output.<br>Readback of the slave flip flop outputs.<br>Readback of the master flip flop outputs. | 0x0   | R/W    |
| [4:2] | Reserved             |          | Reserved.   | 0x0   | R      |
| 1     | DIG_IF_RESET         |          | Digital Interface Reset.  | 0x0   | R/W    |
| 0     | Reserved             |          | Reserved.   | 0x0   | R/W    |

Address: 0x2, Reset: 0xD0, Name: DEVICE\_CONFIG

Table 41. Bit Descriptions for DEVICE\_CONFIG

| Bits  | Bit Name       | Settings | Description   | Reset | Access |
|-------|----------------|----------|---|-------|--------|
| [7:6] | Reserved       |          | Reserved.   | 0x3   | R      |
| 5     | OP_IN_PROGRESS | 0<br>1   | Operation in Progress Indicator. A readback value of 0 indicates that the device is busy.<br>Some operation in progress.<br>No operation in progress. | 0x0   | R      |

| Bits  | Bit Name    | Settings | Description   | Reset | Access |
|-------|-------------|----------|---|-------|--------|
| 4     | NO_CHIP_ERR | 0<br>1   | Error Flag for all of the Enabled Status Errors. This bit is the OR of all the enabled error bits and continues to stay clear as long as any error flag is set.<br>Device has a chip error.<br>No chip error. | 0x1   | R      |
| [3:1] | Reserved    |          | Reserved.   | 0x0   | R      |
| 0     | POWER_MODE  | 0<br>1   | Device Power Mode Control.<br>Low power mode.<br>High performance mode.   | 0x0   | R/W    |

Address: 0x3, Reset: 0x07, Name: CHIP\_TYPE

Table 42. Bit Descriptions for CHIP\_TYPE

| Bits  | Bit Name  | Settings | Description  | Reset | Access |
|-------|-----------|----------|--|-------|--------|
| [7:0] | CHIP_TYPE |          | Code to Indicate the Type of Device. Read 0x07 to confirm for precision ADC. | 0x7   | R      |

Address: 0x4, Reset: 0x00, Name: PRODUCT\_ID\_LSB

Table 43. Bit Descriptions for PRODUCT\_ID\_LSB

| Bits  | Bit Name        | Settings | Description | Reset                       | Access |
|-------|-----------------|----------|-------------|-----------------------------|--------|
| [7:0] | PRODUCT_ID[7:0] |          | Product ID. | Not applicable <sup>1</sup> | R      |

<sup>1</sup> Reset value is time stamp dependent and programmed in production.

Address: 0x5, Reset: 0x00, Name: PRODUCT\_ID\_MSB

Table 44. Bit Descriptions for PRODUCT\_ID\_MSB

| Bits  | Bit Name         | Settings | Description | Reset                       | Access |
|-------|------------------|----------|-------------|-----------------------------|--------|
| [7:0] | PRODUCT_ID[15:8] |          | Product ID. | Not applicable <sup>1</sup> | R      |

<sup>1</sup> Reset value is time stamp dependent and programmed in production.

Address: 0x6, Reset: 0x00, Name: CHIP\_GRADE

Table 45. Bit Descriptions for CHIP\_GRADE

| Bits  | Bit Name       | Settings | Description          | Reset | Access |
|-------|----------------|----------|----------------------|-------|--------|
| [7:4] | PRODUCT_GRADE  |          | Grade of the Device. | 0x0   | R      |
| [3:0] | DEVICE_VERSION |          | Device Version.      | 0x0   | R      |

Address: 0x7, Reset: 0x02, Name: SILICON\_REV

Table 46. Bit Descriptions for SILICON\_REV

| Bits  | Bit Name            | Settings | Description  | Reset | Access |
|-------|---------------------|----------|--|-------|--------|
| [7:0] | SILICON_REVISION_ID |          | Stores the Revision Number of the Current Silicon. | 0x2   | R      |

Address: 0xA, Reset: 0x00, Name: SCRATCH\_PAD

Table 47. Bit Descriptions for SCRATCH\_PAD

| Bits  | Bit Name    | Settings | Description  | Reset | Access |
|-------|-------------|----------|--|-------|--------|
| [7:0] | SCRATCH_PAD |          | Scratch Pad for Checking SPI Read and Write Operation. | 0x0   | R/W    |

Address: 0xB, Reset: 0x02, Name: SPI\_REVISION

Table 48. Bit Descriptions for SPI\_REVISION

| Bits  | Bit Name            | Settings | Description                                       | Reset | Access |
|-------|---------------------|----------|---|-------|--------|
| [7:0] | SPI_REVISION_NUMBER |          | Indicate the Revision Number of the SPI Protocol. | 0x2   | R      |

Address: 0xC, Reset: 0x56, Name: VENDOR\_ID\_LSB

Table 49. Bit Descriptions for VENDOR\_ID\_LSB

| Bits  | Bit Name       | Settings | Description | Reset | Access |
|-------|----------------|----------|-------------|-------|--------|
| [7:0] | VENDOR_ID[7:0] |          | Vendor ID.  | 0x56  | R      |



Address: 0xD, Reset: 0x04, Name: VENDOR\_ID\_MSB

Table 50. Bit Descriptions for VENDOR\_ID\_MSB

| Bits  | Bit Name        | Settings | Description | Reset | Access |
|-------|-----------------|----------|-------------|-------|--------|
| [7:0] | VENDOR_ID[15:8] |          | Vendor ID.  | 0x4   | R      |

Address: 0xE, Reset: 0x00, Name: STREAM\_MODE

Table 51. Bit Descriptions for STREAM\_MODE

| Bits  | Bit Name         | Settings | Description   | Reset | Access |
|-------|------------------|----------|---|-------|--------|
| [7:0] | STREAM_MODE_BITS |          | Defines the Depth of the Loop for User Stream Mode. | 0x0   | R/W    |

Address: 0xF, Reset: 0x00, Name: TRANSFER\_REGISTER

Table 52. Bit Descriptions for TRANSFER\_REGISTER

| Bits  | Bit Name            | Settings | Description  | Reset | Access |
|-------|---------------------|----------|--|-------|--------|
| [7:1] | Reserved            |          | Reserved.  | 0x0   | R      |
| 0     | MASTER_SLAVE_TX_BIT |          | Master Slave Transfer Bit. When this bit is set, data is entered into the master registers transferred to the slave. Upon completion of the transfer, the slave device clears this bit (autoclears), indicating to the SPI master that the transfer was complete and the slave data can be read back if desired by the control program. Prior to a transfer, an attempted readback views the prior data unless Bit 5 of Register 0x1 (MASTER_SLAVE_RD_CTRL) is set. In that case, the master data is accessed. Another method to invoke the transfer is to use the $\overline{CS}$ low to high transition. | 0x0   | R/W    |

Address: 0x10, Reset: 0x00, Name: DEVICE\_CONFIG\_1

Table 53. Bit Descriptions for DEVICE\_CONFIG\_1

| Bits  | Bit Name           | Settings | Description  | Reset | Access |
|-------|--------------------|----------|--|-------|--------|
| [7:4] | Reserved           |          | Reserved, is always zero.  | 0x0   | R/W    |
| 3     | AA_MODE            | 0<br>1   | Sets Inherent Antialiasing Mode.<br>AA1 mode.<br>AA2 mode.   | 0x0   | R/W    |
| 2     | SDO_PIN_SRC_SEL    | 0<br>1   | DEC3/SDO Pin Signal Source Selection. In minimum I/O mode, the user can use the DEC3/SDO pin for both register content and ADC conversion data readback.<br>DEC3/SDO pin acts as SPI serial data output.<br>Signal on DOUT0 is duplicated on DEC3/SDO pin. | 0x0   | R/W    |
| 1     | REFIN_GAIN_CORR_EN | 0<br>1   | Enables Reference Gain Correction.<br>Reference gain correction disabled.<br>Reference gain correction enabled.  | 0x0   | R/W    |
| 0     | XCLKOUT_EN         | 0<br>1   | XCLKOUT Output Enable Control.<br>XCLKOUT disabled.<br>XCLKOUT enabled.  | 0x0   | R/W    |

Address: 0x11, Reset: 0x00, Name: DATA\_PACKET\_CONFIG

Table 54. Bit Descriptions for DATA\_PACKET\_CONFIG

| Bits | Bit Name         | Settings | Description  | Reset | Access |
|------|------------------|----------|--|-------|--------|
| 7    | CRC_POLY_RST_SEL | 0<br>1   | Data Interface CRC Reset Method Selection.<br>The data interface CRC is reset with default seed value at the end of every data frame.<br>The data interface CRC does not reset at the end of each data frame. The CRC value calculated from the proceeding data frame seeds the CRC calculation of the current data frame. | 0x0   | R/W    |
| 6    | Reserved         |          | Reserved   | 0x0   | R      |

| Bits  | Bit Name      | Settings   | Description  | Reset | Access |
|-------|---------------|--|--|-------|--------|
| [5:4] | Frame         | 0<br>1<br>10<br>11   | ADC Conversion Data Output Frame Control.<br>16-bit ADC data only.<br>16-bit ADC data followed by 6-bit CRC.<br>24-bit ADC data only.<br>24-bit ADC data followed by 6-bit CRC.  | 0x0   | R/W    |
| [3:0] | DCLK_FREQ_SEL | 0<br>1<br>10<br>11<br>100<br>101<br>110<br>111<br>1000<br>1001<br>1010<br>1011<br>1100<br>1101<br>1110<br>1111 | Controls DCLK Output Frequency.<br>$f_{DCLK} = 48$ MHz.<br>$f_{DCLK} = 24$ MHz.<br>$f_{DCLK} = 12$ MHz.<br>$f_{DCLK} = 6$ MHz.<br>$f_{DCLK} = 3$ MHz.<br>$f_{DCLK} = 1.5$ MHz.<br>$f_{DCLK} = 750$ kHz.<br>$f_{DCLK} = 375$ kHz.<br>$f_{DCLK} = 187.5$ kHz.<br>$f_{DCLK} = 93.75$ kHz.<br>$f_{DCLK} = 46.875$ kHz.<br>$f_{DCLK} = 23.4375$ kHz.<br>$f_{DCLK} = 11.71875$ kHz.<br>$f_{DCLK} = 5.859$ kHz.<br>$f_{DCLK} = 2.929$ kHz.<br>$f_{DCLK} = 1.464$ kHz. | 0x0   | R/W    |

Address: 0x12, Reset: 0x00, Name: DIGITAL\_INTERFACE\_CONFIG

Table 55. Bit Descriptions for DIGITAL\_INTERFACE\_CONFIG

| Bits  | Bit Name            | Settings   | Description   | Reset | Access |
|-------|---------------------|--|---|-------|--------|
| [7:4] | DAISY_CHAIN_DEV_NUM | 0<br>1<br>10<br>11<br>100<br>101<br>110<br>111<br>1000<br>1001<br>1010<br>1011<br>1100<br>1101<br>1110<br>1111 | Sets the Number of Devices Connected in a Daisy-Chain Configuration. This register is only applicable to a device set to output DCLK to other devices in a daisy-chain configuration. The register value acts as a clock cycle multiplier in DCLK output configuration. For example, setting the daisy-chain device number to two doubles the number of DCLK cycles output per ODR cycle.<br>Only one device is used.<br>2 devices are in daisy-chain configuration.<br>3 devices are in daisy-chain configuration.<br>4 devices are in daisy-chain configuration.<br>5 devices are in daisy-chain configuration.<br>6 devices are in daisy-chain configuration.<br>7 devices are in daisy-chain configuration.<br>8 devices are in daisy-chain configuration.<br>9 devices are in daisy-chain configuration.<br>10 devices are in daisy-chain configuration.<br>11 devices are in daisy-chain configuration.<br>12 devices are in daisy-chain configuration.<br>13 devices are in daisy-chain configuration.<br>14 devices are in daisy-chain configuration.<br>15 devices are in daisy-chain configuration.<br>16 devices are in daisy-chain configuration. | 0x0   | R/W    |

| Bits  | Bit Name | Settings           | Description   | Reset | Access |
|-------|----------|--------------------|---|-------|--------|
| [3:2] | AVG_SEL  | 0<br>1<br>10<br>11 | Multichannel ADC Conversion Data Averaging Control.<br>0 Data from all four channels are averaged and output on DOUT0. DOUT2 acts as daisy-chain input. DOUT1 and DOUT3 are disabled.<br>1 Data from Channel 0 and Channel 1 are averaged and output on DOUT0. DOUT1 is disabled. Channel 2 and Channel 3 are under normal operation.<br>10 Data from Channel 2 and Channel 3 are averaged and output on DOUT2. DOUT3 is disabled. Channel 0 and Channel 1 are under normal operation.<br>11 Data from Channel 0 and Channel 1 are averaged and output on DOUT0. Data from Channel 2 and Channel 3 are averaged and output on DOUT1. DOUT2 and DOUT3 act as daisy-chain inputs. | 0x0   | R/W    |
| [1:0] | Format   | 0<br>1<br>10<br>11 | DOUTx Output Format Configuration.<br>0 Single-channel daisy-chain mode. DOUT0 acts as an output and DOUT2 acts as a daisy-chain input. DOUT1 and DOUT3 are disabled. Data from all four ADC channels are output on DOUT0.<br>1 Dual-channel daisy-chain mode. DOUT0 and DOUT1 act as output and DOUT2 and DOUT3 act as daisy-chain input. Data from Channel 0 and Channel 1 are output on DOUT0. Data from Channel 2 and Channel 3 are output on DOUT1.<br>10 Quad channel parallel output mode. Each ADC channel has a dedicated data output pin.<br>11 Channel data averaging mode, averaging operation is defined by AVG_SEL.   | 0x0   | R/W    |

Address: 0x13, Reset: 0x00, Name: POWER\_DOWN\_CONTROL

Table 56. Bit Descriptions for POWER\_DOWN\_CONTROL

| Bits | Bit Name      | Settings | Description   | Reset | Access |
|------|---------------|----------|---|-------|--------|
| 7    | Reserved      |          | Reserved.   | 0x0   | R      |
| 6    | PWRDN_CH3     | 0<br>1   | Powers Down Analog Input Channel 3.<br>0 Power up.<br>1 Power down.   | 0x0   | R/W    |
| 5    | PWRDN_CH2     | 0<br>1   | Powers Down Analog Input Channel 2.<br>0 Power up.<br>1 Power down.   | 0x0   | R/W    |
| 4    | PWRDN_CH1     | 0<br>1   | Powers Down Analog Input Channel 1.<br>0 Power up.<br>1 Power down.   | 0x0   | R/W    |
| 3    | PWRDN_CH0     | 0<br>1   | Powers Down Analog Input Channel 0.<br>0 Power up.<br>1 Power down.   | 0x0   | R/W    |
| 2    | Reserved      |          | Reserved.   | 0x0   | R      |
| 1    | PWRDN_LDO     | 0<br>1   | Powers Down the Internal Analog and Clock LDO Regulators.<br>0 Internal LDO regulators powered.<br>1 Internal LDO regulators powered down.            | 0x0   | R/W    |
| 0    | SLEEP_MODE_EN | 0<br>1   | All Blocks Except Digital LDO Regulator are Turned Off. On-chip register contents remain the same.<br>0 Sleep mode disabled.<br>1 Sleep mode enabled. | 0x0   | R/W    |

Address: 0x14, Reset: 0x00, Name: RESERVED

Table 57. Bit Descriptions for RESERVED

| Bits  | Bit Name | Settings | Description            | Reset | Access |
|-------|----------|----------|------------------------|-------|--------|
| [7:0] | Reserved |          | Reserved. Always zero. | 0x0   | R/W    |

Address: 0x15, Reset: 0x00, Name: DEVICE\_STATUS

Table 58. Bit Descriptions for DEVICE\_STATUS

| Bits  | Bit Name      | Settings | Description  | Reset | Access |
|-------|---------------|----------|--|-------|--------|
| [7:6] | Reserved      |          | Reserved.  | 0x0   | R      |
| 5     | STAT_DCLKMODE | 0<br>1   | DEC1/DCLKMODE Pin Status Indicates if DCLK is in Free Running or Gated Mode.<br>DCLK is in gated mode. Compatible with SPI interface.<br>DCLK is in free running mode.       | 0x0   | R      |
| 4     | STAT_DCLKIO   | 0<br>1   | DEC0/DCLKIO Pin Status Indicates DCLK Pin Direction.<br>DCLK is input.<br>DCLK is output.  | 0x0   | R      |
| 3     | STAT_MODE     | 0<br>1   | MODE Pin Status Indicates Whether Device is Master or Slave.<br>Slave mode: ODR is input.<br>Master mode: ODR is output.   | 0x0   | R      |
| 2     | STAT_CLKSEL   | 0<br>1   | CLKSEL Pin Status Indicates the Clock Source.<br>CMOS input clock is connected.<br>Crystal input is connected.   | 0x0   | R      |
| 1     | STAT_FUSE_ECC | 0<br>1   | Status Bit that Indicates Application of Fuse Error Correction Code. This bit is cleared on is read.<br>Error code correction not applied.<br>Error code correction applied. | 0x0   | R      |
| 0     | STAT_PLL_LOCK | 0<br>1   | PLL Status in Slave Mode. Indicates if PLL has locked or not. Setting this bit indicates PLL is locked.<br>PLL not locked.<br>PLL locked.                                    | 0x0   | R      |

Address: 0x16, Reset: 0x40, Name: ODR\_VAL\_INT\_LSB

Table 59. Bit Descriptions for ODR\_VAL\_INT\_LSB

| Bits  | Bit Name         | Settings | Description  | Reset | Access |
|-------|------------------|----------|--|-------|--------|
| [7:0] | ODR_VAL_INT[7:0] |          | Integer Portion of Decimation Rate. Decimation rate is the ratio of MCLK to ODR. In master mode, the user can program this register to set the ODR output frequency based on the MCLK frequency. | 0x40  | R/W    |

Address: 0x17, Reset: 0x00, Name: ODR\_VAL\_INT\_MID

Table 60. Bit Descriptions for ODR\_VAL\_INT\_MID

| Bits  | Bit Name          | Settings | Description  | Reset | Access |
|-------|-------------------|----------|--|-------|--------|
| [7:0] | ODR_VAL_INT[15:8] |          | Integer Portion of Decimation Rate. Decimation rate is the ratio of MCLK to ODR. In master mode, the user can program this register to set the ODR output frequency based on the MCLK frequency. | 0x0   | R/W    |

Address: 0x18, Reset: 0x00, Name: ODR\_VAL\_INT\_MSB

Table 61. Bit Descriptions for ODR\_VAL\_INT\_MSB

| Bits  | Bit Name           | Settings | Description  | Reset | Access |
|-------|--------------------|----------|--|-------|--------|
| [7:0] | ODR_VAL_INT[23:16] |          | Integer Portion of Decimation Rate. Decimation rate is the ratio of MCLK to ODR. In master mode, the user can program this register to set the ODR output frequency based on the MCLK frequency. | 0x0   | R/W    |

Address: 0x19, Reset: 0x72, Name: ODR\_VAL\_FLT\_LSB

Table 62. Bit Descriptions for ODR\_VAL\_FLT\_LSB

| Bits  | Bit Name         | Settings | Description   | Reset | Access |
|-------|------------------|----------|---|-------|--------|
| [7:0] | ODR_VAL_FLT[7:0] |          | Fractional Portion of Decimation Rate. Decimation rate is the ratio of MCLK to ODR. In master mode, the user can program this register to set the ODR output frequency based on the MCLK frequency. | 0x72  | R/W    |

Address: 0x1A, Reset: 0xB7, Name: ODR\_VAL\_FLT\_MID0

Table 63. Bit Descriptions for ODR\_VAL\_FLT\_MID0

| Bits  | Bit Name          | Settings | Description   | Reset | Access |
|-------|-------------------|----------|---|-------|--------|
| [7:0] | ODR_VAL_FLT[15:8] |          | Fractional Portion of Decimation Rate. Decimation rate is the ratio of MCLK to ODR. In master mode, the user can program this register to set the ODR output frequency based on the MCLK frequency. | 0xB7  | R/W    |

Address: 0x1B, Reset: 0xCE, Name: ODR\_VAL\_FLT\_MID1

Table 64. Bit Descriptions for ODR\_VAL\_FLT\_MID1

| Bits  | Bit Name           | Settings | Description   | Reset | Access |
|-------|--------------------|----------|---|-------|--------|
| [7:0] | ODR_VAL_FLT[23:16] |          | Fractional Portion of Decimation Rate. Decimation rate is the ratio of MCLK to ODR. In master mode, the user can program this register to set the ODR output frequency based on the MCLK frequency. | 0xCE  | R/W    |

Address: 0x1C, Reset: 0x2B, Name: ODR\_VAL\_FLT\_MSB

Table 65. Bit Descriptions for ODR\_VAL\_FLT\_MSB

| Bits  | Bit Name           | Settings | Description   | Reset | Access |
|-------|--------------------|----------|---|-------|--------|
| [7:0] | ODR_VAL_FLT[31:24] |          | Fractional Portion of Decimation Rate. Decimation rate is the ratio of MCLK to ODR. In master mode, the user can program this register to set the ODR output frequency based on the MCLK frequency. | 0x2B  | R/W    |

Address: 0x1D, Reset: 0x00, Name: CHANNEL\_ODR\_SELECT

Table 66. Bit Descriptions for CHANNEL\_ODR\_SELECT

| Bits  | Bit Name         | Settings           | Description   | Reset | Access |
|-------|------------------|--------------------|---|-------|--------|
| [7:6] | ODR_RATE_SEL_CH3 | 0<br>1<br>10<br>11 | Select Output Data Rate to ODR Frequency Ratio for Channel 3.<br>Output data rate = ODR.<br>Output data rate = ODR/2.<br>Output data rate = ODR/4.<br>Output data rate = ODR/8. | 0x0   | R/W    |
| [5:4] | ODR_RATE_SEL_CH2 | 0<br>1<br>10<br>11 | Select Output Data Rate to ODR Frequency Ratio for Channel 2.<br>Output data rate = ODR.<br>Output data rate = ODR/2.<br>Output data rate = ODR/4.<br>Output data rate = ODR/8. | 0x0   | R/W    |
| [3:2] | ODR_RATE_SEL_CH1 | 0<br>1<br>10<br>11 | Select Output Data Rate to ODR Frequency Ratio for Channel 1.<br>Output data rate = ODR.<br>Output data rate = ODR/2.<br>Output data rate = ODR/4.<br>Output data rate = ODR/8. | 0x0   | R/W    |
| [1:0] | ODR_RATE_SEL_CH0 | 0<br>1<br>10<br>11 | Select Output Data Rate to ODR Frequency Ratio for Channel 0.<br>Output data rate = ODR.<br>Output data rate = ODR/2.<br>Output data rate = ODR/4.<br>Output data rate = ODR/8. | 0x0   | R/W    |

Address: 0x1E, Reset: 0x00, Name: CHAN\_DIG\_FILTER\_SEL

Table 67. Bit Descriptions for CHAN\_DIG\_FILTER\_SEL

| Bits  | Bit Name          | Settings            | Description   | Reset | Access |
|-------|-------------------|---------------------|---|-------|--------|
| [7:6] | DIGFILTER_SEL_CH3 | 0<br>01<br>10<br>11 | Channel 3 Digital Filter Type Selection.<br>Wideband filter.<br>Sinc6 filter.<br>Sinc3 filter.<br>Sinc3 filter with simultaneous 50 Hz and 60 Hz rejection. | 0x0   | R/W    |
| [5:4] | DIGFILTER_SEL_CH2 | 0<br>01             | Channel 2 Digital Filter Type Selection.<br>Wideband filter.<br>Sinc6 filter.   | 0x0   | R/W    |

| Bits  | Bit Name          | Settings | Description   | Reset | Access |
|-------|-------------------|----------|---|-------|--------|
|       |                   | 10       | Sinc3 filter.   |       |        |
|       |                   | 11       | Sinc3 filter with simultaneous 50 Hz and 60 Hz rejection. |       |        |
| [3:2] | DIGFILTER_SEL_CH1 |          | Channel 1 Digital Filter Type Selection.                  | 0x0   | R/W    |
|       |                   | 0        | Wideband filter.  |       |        |
|       |                   | 01       | Sinc6 filter.   |       |        |
|       |                   | 10       | Sinc3 filter.   |       |        |
|       |                   | 11       | Sinc3 filter with simultaneous 50 Hz and 60 Hz rejection. |       |        |
| [1:0] | DIGFILTER_SEL_CH0 |          | Channel 0 Digital Filter Type Selection.                  | 0x0   | R/W    |
|       |                   | 0        | Wideband filter.  |       |        |
|       |                   | 01       | Sinc6 filter.   |       |        |
|       |                   | 10       | Sinc3 filter.   |       |        |
|       |                   | 11       | Sinc3 filter with simultaneous 50 Hz and 60 Hz rejection. |       |        |

Address: 0x1F, Reset: 0x00, Name: FIR\_BW\_SEL

Table 68. Bit Descriptions for FIR\_BW\_SEL

| Bits  | Bit Name          | Settings | Description  | Reset | Access |
|-------|-------------------|----------|--|-------|--------|
| [7:4] | Reserved          |          | Reserved.  | 0x0   | R      |
| 3     | WB_FILTER_SEL_CH3 |          | Channel 3 Wideband Filter Bandwidth Selection.       | 0x0   | R/W    |
|       |                   | 0        | Wideband filter has a bandwidth of 0.433 Hz × ODR.   |       |        |
|       |                   | 1        | Wideband filter has a bandwidth of 0.10825 Hz × ODR. |       |        |
| 2     | WB_FILTER_SEL_CH2 |          | Channel 2 Wideband Filter Bandwidth Selection.       | 0x0   | R/W    |
|       |                   | 0        | Wideband filter has a bandwidth of 0.433 Hz × ODR.   |       |        |
|       |                   | 1        | Wideband filter has a bandwidth of 0.10825 Hz × ODR. |       |        |
| 1     | WB_FILTER_SEL_CH1 |          | Channel 1 Wideband Filter Bandwidth Selection.       | 0x0   | R/W    |
|       |                   | 0        | Wideband filter has a bandwidth of 0.433 Hz × ODR.   |       |        |
|       |                   | 1        | Wideband filter has a bandwidth of 0.10825 Hz × ODR. |       |        |
| 0     | WB_FILTER_SEL_CH0 |          | Channel 0 Wideband Filter Bandwidth Selection.       | 0x0   | R/W    |
|       |                   | 0        | Wideband filter has a bandwidth of 0.433 Hz × ODR.   |       |        |
|       |                   | 1        | Wideband filter has a bandwidth of 0.10825 Hz × ODR. |       |        |

Address: 0x20, Reset: 0x00, Name: GPIO\_DIR\_CTRL

Table 69. Bit Descriptions for GPIO\_DIR\_CTRL

| Bits  | Bit Name        | Settings | Description   | Reset | Access |
|-------|-----------------|----------|---|-------|--------|
| [7:0] | GPIO_IO_CONTROL |          | GPIO I/O Direction Control. Each bit controls the direction of a GPIO pin. A value of 0 sets the GPIO pin as an input. A value of 1 sets the GPIO pin as an output. Bit 0 is associated with GPIO0. | 0x0   | R/W    |

Address: 0x21, Reset: 0x00, Name: GPIO\_DATA

Table 70. Bit Descriptions for GPIO\_DATA

| Bits  | Bit Name  | Settings | Description   | Reset | Access |
|-------|-----------|----------|---|-------|--------|
| [7:0] | GPIO_DATA |          | GPIO Data Value. If a GPIO pin is configured as an input, the corresponding bit is read only and its value reflects the input logic status of the pin. If a GPIO pin is configured as an output, write to the corresponding bit to control the output logic of the pin. Bit 0 is associated with GPIO0. 1 = logic high and 0 = logic low. | 0x0   | R/W    |

Address: 0x22, Reset: 0x00, Name: ERROR\_PIN\_SRC\_CONTROL

Table 71. Bit Descriptions for ERROR\_PIN\_SRC\_CONTROL

| Bits  | Bit Name          | Settings | Description  | Reset | Access |
|-------|-------------------|----------|--|-------|--------|
| [7:6] | Reserved          |          | Reserved.  | 0x0   | R      |
| 5     | ERR_PIN_EN_OR_AIN |          | Enables Error Reporting on GPIO7 for Input Overrange Errors. | 0x0   | R/W    |
|       |                   | 0        | Disables pin toggle for overvoltage error.                   |       |        |
|       |                   | 1        | Enables pin toggle for overvoltage error.                    |       |        |

| Bits  | Bit Name            | Settings | Description   | Reset | Access |
|-------|---------------------|----------|---|-------|--------|
| 4     | ERR_PIN_EN_INTERNAL | 0<br>1   | Enables Error Reporting on GPIO7 for Any Internal Errors. Internal error can be digital overflow or underflow error, memory map CRC error, ASRC error, fuse CRC error, or DCLK counter error. Make sure to enable the corresponding error in the diagnostic control register to enable this reporting.<br>Disables pin toggle for internal errors.<br>Enables pin toggle for internal errors. | 0x0   | R/W    |
| 3     | ERR_PIN_EN_SPI      | 0<br>1   | Enables error reporting on GPIO7 if there are any SPI errors such as read, write, CRC check, and clock counter errors. Make sure to enable SPI CRC error for reporting those errors on the pin.<br>Disables pin toggle for SPI related errors.<br>Enables pin toggle for SPI related errors.  | 0x0   | R/W    |
| [2:0] | Reserved            |          | Reserved.   | 0x0   | R      |

Address: 0x23, Reset: 0x00, Name: ERROR\_PIN\_CONTROL

Table 72. Bit Descriptions for ERROR\_PIN\_CONTROL

| Bits  | Bit Name          | Settings | Description   | Reset | Access |
|-------|-------------------|----------|---|-------|--------|
| [7:3] | Reserved          |          | Reserved.   | 0x0   | R      |
| 2     | ERR_PIN_IN_STATUS |          | This bit is the readback of the latched status of the error input, GPIO6, when it is enabled using the ERR_PIN_IN_EN bit.         | 0x0   | R      |
| 1     | ERR_PIN_IN_EN     |          | Enables GPIO6 as an error input. This bit allows error to be daisy-chained from a digital host and is OR'ed with internal errors. | 0x0   | R/W    |
| 0     | ERR_PIN_OUT_EN    |          | Enables GPIO7 as an error output pin. The source of this error is defined by the ERROR_PIN_SRC_CONTROL register.                  | 0x0   | R/W    |

Address: 0x24, Reset: 0x00, Name: VCMBUF\_CTRL

Table 73. Bit Descriptions for VCMBUF\_CTRL

| Bits  | Bit Name           | Settings  | Description   | Reset | Access |
|-------|--------------------|---|---|-------|--------|
| 7     | Reserved           |   | Reserved.   | 0x0   | R      |
| 6     | PWRDN_VCMBUF       | 0<br>1  | VCM Buffer Power Control.<br>VCM buffer powered on.<br>VCM buffer powered down.   | 0x0   | R/W    |
| [5:1] | VCMBUF_REF_DIV_SEL | 0<br>1<br>10<br>11<br>100<br>101<br>110<br>111<br>1000<br>1001<br>1010<br>1011<br>1100<br>1101<br>1110<br>1111<br>10000<br>10001<br>10010<br>10011<br>11101<br>11110<br>11111 | V <sub>CM</sub> Output Voltage Level Selection when VCMBUF_REF_SEL = 0.<br>V <sub>CM</sub> = V <sub>REF</sub> × 10/20.<br>Reserved.<br>V <sub>CM</sub> = V <sub>REF</sub> × 19/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 18/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 17/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 16/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 15/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 14/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 13/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 12/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 11/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 9/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 8/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 7/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 6/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 5/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 4/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 3/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 2/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 1/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 10/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 10/20.<br>V <sub>CM</sub> = V <sub>REF</sub> × 10/20. | 0x0   | R/W    |

| Bits | Bit Name       | Settings | Description   | Reset | Access |
|------|----------------|----------|---|-------|--------|
| 0    | VCMBUF_REF_SEL | 0<br>1   | VCM Output Source Selection.<br>VCM as a ratio of $V_{REF}$ . The VCM output level is $V_{REF}$ divided by the ratio set with VCMBUF_REF_DIV_SEL.<br>$V_{CM}$ is fixed to $AVDD5/2$ . | 0x0   | R/W    |

Address: 0x25, Reset: 0x00, Name: Diagnostic Control

Table 74. Bit Descriptions for Diagnostic Control

| Bits  | Bit Name       | Settings | Description   | Reset | Access |
|-------|----------------|----------|---|-------|--------|
| [7:6] | Reserved       |          | Reserved.   | 0x0   | R      |
| 5     | ERR_OR_AIN_EN  | 0<br>1   | Enables Overrange Monitor on all Enabled Analog Input Channels.<br>Input overvoltage monitor is disabled.<br>Input overvoltage monitor is enabled.  | 0x0   | R/W    |
| 4     | Reserved       |          | Reserved  | 0x0   | R      |
| 3     | MCLK_CNT_EN    | 0<br>1   | Enables Master Clock Counter. Starts the MCLK counter, which monitors the external clock being used by the ADC.<br>Disables MCLK counter.<br>Enables MCLK counter.  | 0x0   | R/W    |
| 2     | ERR_SPI_CRC_EN | 0<br>1   | Enables CRC Check on SPI Read and Write Operations. The ERR_SPI_CRC bit in the SPI error register is set if the CRC check fails. In addition, an 8-bit CRC word is appended to all SPI read operations.<br>SPI CRC disabled.<br>SPI CRC enabled.  | 0x0   | R/W    |
| 1     | ERR_MM_CRC_EN  | 0<br>1   | Enables Memory Map CRC Calculation. CRC calculation is performed on the memory map each time the registers are written to. Following this write, periodic CRC checks are performed on the on-chip registers. If the register contents have changed, the ERR_MM_CRC bit is set.<br>Disables memory map CRC check.<br>Enables memory map CRC check. | 0x0   | R/W    |
| 0     | FUSE_CRC_CHECK | 0<br>1   | Initiates a CRC Calculation on the Fuse Contents. If the fuse contents have changed, the ERR_FUSE_CRC bit is set. This bit is cleared on completion of the check.<br>CRC calculation disabled.<br>CRC calculation enabled.  | 0x0   | R/W    |

Address: 0x26, Reset: 0x00, Name: MPC\_CONFIG

Table 75. Bit Descriptions for MPC\_CONFIG

| Bits  | Bit Name          | Settings             | Description   | Reset | Access |
|-------|-------------------|----------------------|---|-------|--------|
| [7:6] | MPC_CLKDEL_EN_CH3 | 00<br>01<br>10<br>11 | Magnitude and Phase Matching Calibration Clock Delay Enable for Channel 3.<br>Magnitude and phase clock delay: 0 clock delays.<br>Magnitude and phase clock delay: 1 clock delay.<br>Magnitude and phase clock delay: 2 clock delays.<br>Magnitude and phase clock delay: 0 clock delays. | 0x0   | R/W    |
| [5:4] | MPC_CLKDEL_EN_CH2 | 00<br>01<br>10<br>11 | Magnitude and Phase Matching Calibration Clock Delay Enable for Channel 2.<br>Magnitude and phase clock delay: 0 clock delays.<br>Magnitude and phase clock delay: 1 clock delay.<br>Magnitude and phase clock delay: 2 clock delays.<br>Magnitude and phase clock delay: 0 clock delays. | 0x0   | R/W    |
| [3:2] | MPC_CLKDEL_EN_CH1 | 00<br>01<br>10<br>11 | Magnitude and Phase Matching Calibration Clock Delay Enable for Channel 1.<br>Magnitude and phase clock delay: 0 clock delays.<br>Magnitude and phase clock delay: 1 clock delay.<br>Magnitude and phase clock delay: 2 clock delays.<br>Magnitude and phase clock delay: 0 clock delay.  | 0x0   | R/W    |
| [1:0] | MPC_CLKDEL_EN_CH0 | 00<br>01             | Magnitude and Phase Matching Calibration Clock Delay Enable for Channel 0.<br>Magnitude and phase clock delay: 0 clock delays.<br>Magnitude and phase clock delay: 1 clock delay.   | 0x0   | R/W    |



| Bits | Bit Name | Settings | Description                                      | Reset | Access |
|------|----------|----------|--|-------|--------|
|      |          | 10       | Magnitude and phase clock delay: 2 clock delays. |       |        |
|      |          | 11       | Magnitude and phase clock delay: 0 clock delay.  |       |        |

Address: 0x27, Reset: 0x00, Name: CH0\_GAIN\_LSB

Table 76. Bit Descriptions for CH0\_GAIN\_LSB

| Bits  | Bit Name      | Settings | Description                       | Reset | Access |
|-------|---------------|----------|-----------------------------------|-------|--------|
| [7:0] | GAIN_CH0[7:0] |          | Channel 0 Gain Calibration Value. | 0x0   | R/W    |

Address: 0x28, Reset: 0x00, Name: CH0\_GAIN\_MID

Table 77. Bit Descriptions for CH0\_GAIN\_MID

| Bits  | Bit Name       | Settings | Description                       | Reset | Access |
|-------|----------------|----------|-----------------------------------|-------|--------|
| [7:0] | GAIN_CH0[15:8] |          | Channel 0 Gain Calibration Value. | 0x0   | R/W    |

Address: 0x29, Reset: 0x00, Name: CH0\_GAIN\_MSB

Table 78. Bit Descriptions for CH0\_GAIN\_MSB

| Bits  | Bit Name         | Settings | Description                            | Reset | Access |
|-------|------------------|----------|--|-------|--------|
| [7:5] | Reserved         |          | Reserved.                              | 0x0   | R      |
| 4     | GAIN_CAL_SEL_CH0 |          | Enables Gain Calibration on Channel 0. | 0x0   | R/W    |
| [3:0] | GAIN_CH0[19:16]  |          | Channel 0 Gain Calibration Value.      | 0x0   | R/W    |

Address: 0x2A, Reset: 0x00, Name: CH0\_OFFSET\_LSB

Table 79. Bit Descriptions for CH0\_OFFSET\_LSB

| Bits  | Bit Name        | Settings | Description                         | Reset | Access |
|-------|-----------------|----------|-------------------------------------|-------|--------|
| [7:0] | OFFSET_CH0[7:0] |          | Channel 0 Offset Calibration Value. | 0x0   | R/W    |

Address: 0x2B, Reset: 0x00, Name: CH0\_OFFSET\_MID

Table 80. Bit Descriptions for CH0\_OFFSET\_MID

| Bits  | Bit Name         | Settings | Description                         | Reset | Access |
|-------|------------------|----------|-------------------------------------|-------|--------|
| [7:0] | OFFSET_CH0[15:8] |          | Channel 0 Offset Calibration Value. | 0x0   | R/W    |

Address: 0x2C, Reset: 0x00, Name: CH0\_OFFSET\_MSB

Table 81. Bit Descriptions for CH0\_OFFSET\_MSB

| Bits  | Bit Name          | Settings | Description                              | Reset | Access |
|-------|-------------------|----------|--|-------|--------|
| 7     | OFFSET_CAL_EN_CH0 |          | Enables Offset Calibration on Channel 0. | 0x0   | R/W    |
| [6:0] | OFFSET_CH0[22:16] |          | Channel 0 Offset Calibration Value.      | 0x0   | R/W    |

Address: 0x2D, Reset: 0x00, Name: CH1\_GAIN\_LSB

Table 82. Bit Descriptions for CH1\_GAIN\_LSB

| Bits  | Bit Name      | Settings | Description                       | Reset | Access |
|-------|---------------|----------|-----------------------------------|-------|--------|
| [7:0] | GAIN_CH1[7:0] |          | Channel 1 Gain Calibration Value. | 0x0   | R/W    |

Address: 0x2E, Reset: 0x00, Name: CH1\_GAIN\_MID

Table 83. Bit Descriptions for CH1\_GAIN\_MID

| Bits  | Bit Name       | Settings | Description                       | Reset | Access |
|-------|----------------|----------|-----------------------------------|-------|--------|
| [7:0] | GAIN_CH1[15:8] |          | Channel 1 Gain Calibration Value. | 0x0   | R/W    |

Address: 0x2F, Reset: 0x00, Name: CH1\_GAIN\_MSB

Table 84. Bit Descriptions for CH1\_GAIN\_MSB

| Bits  | Bit Name         | Settings | Description                            | Reset | Access |
|-------|------------------|----------|--|-------|--------|
| [7:5] | Reserved         |          | Reserved.                              | 0x0   | R      |
| 4     | GAIN_CAL_SEL_CH1 |          | Enables Gain Calibration on Channel 1. | 0x0   | R/W    |
| [3:0] | GAIN_CH1[19:16]  |          | Channel 1 Gain Calibration Value.      | 0x0   | R/W    |

Address: 0x30, Reset: 0x00, Name: CH1\_OFFSET\_LSB

Table 85. Bit Descriptions for CH1\_OFFSET\_LSB

| Bits  | Bit Name        | Settings | Description                         | Reset | Access |
|-------|-----------------|----------|-------------------------------------|-------|--------|
| [7:0] | OFFSET_CH1[7:0] |          | Channel 1 Offset Calibration Value. | 0x0   | R/W    |

Address: 0x31, Reset: 0x00, Name: CH1\_OFFSET\_MID

Table 86. Bit Descriptions for CH1\_OFFSET\_MID

| Bits  | Bit Name         | Settings | Description                         | Reset | Access |
|-------|------------------|----------|-------------------------------------|-------|--------|
| [7:0] | OFFSET_CH1[15:8] |          | Channel 1 Offset Calibration Value. | 0x0   | R/W    |

Address: 0x32, Reset: 0x00, Name: CH1\_OFFSET\_MSB

Table 87. Bit Descriptions for CH1\_OFFSET\_MSB

| Bits  | Bit Name          | Settings | Description                              | Reset | Access |
|-------|-------------------|----------|--|-------|--------|
| 7     | OFFSET_CAL_EN_CH1 |          | Enables Offset Calibration on Channel 1. | 0x0   | R/W    |
| [6:0] | OFFSET_CH1[22:16] |          | Channel 1 Offset Calibration Value.      | 0x0   | R/W    |

Address: 0x33, Reset: 0x00, Name: CH2\_GAIN\_LSB

Table 88. Bit Descriptions for CH2\_GAIN\_LSB

| Bits  | Bit Name      | Settings | Description                       | Reset | Access |
|-------|---------------|----------|-----------------------------------|-------|--------|
| [7:0] | GAIN_CH2[7:0] |          | Channel 2 Gain Calibration Value. | 0x0   | R/W    |

Address: 0x34, Reset: 0x00, Name: CH2\_GAIN\_MID

Table 89. Bit Descriptions for CH2\_GAIN\_MID

| Bits  | Bit Name       | Settings | Description                       | Reset | Access |
|-------|----------------|----------|-----------------------------------|-------|--------|
| [7:0] | GAIN_CH2[15:8] |          | Channel 2 Gain Calibration Value. | 0x0   | R/W    |

Address: 0x35, Reset: 0x00, Name: CH2\_GAIN\_MSB

Table 90. Bit Descriptions for CH2\_GAIN\_MSB

| Bits  | Bit Name         | Settings | Description                            | Reset | Access |
|-------|------------------|----------|--|-------|--------|
| [7:5] | Reserved         |          | Reserved.                              | 0x0   | R      |
| 4     | GAIN_CAL_SEL_CH2 |          | Enables Gain Calibration on Channel 2. | 0x0   | R/W    |
| [3:0] | GAIN_CH2[19:16]  |          | Channel 2 Gain Calibration Value.      | 0x0   | R/W    |

Address: 0x36, Reset: 0x00, Name: CH2\_OFFSET\_LSB

Table 91. Bit Descriptions for CH2\_OFFSET\_LSB

| Bits  | Bit Name        | Settings | Description                         | Reset | Access |
|-------|-----------------|----------|-------------------------------------|-------|--------|
| [7:0] | OFFSET_CH2[7:0] |          | Channel 2 Offset Calibration Value. | 0x0   | R/W    |

Address: 0x37, Reset: 0x00, Name: CH2\_OFFSET\_MID

Table 92. Bit Descriptions for CH2\_OFFSET\_MID

| Bits  | Bit Name         | Settings | Description                         | Reset | Access |
|-------|------------------|----------|-------------------------------------|-------|--------|
| [7:0] | OFFSET_CH2[15:8] |          | Channel 2 Offset Calibration Value. | 0x0   | R/W    |

Address: 0x38, Reset: 0x00, Name: CH2\_OFFSET\_MSB

Table 93. Bit Descriptions for CH2\_OFFSET\_MSB

| Bits  | Bit Name          | Settings | Description                              | Reset | Access |
|-------|-------------------|----------|--|-------|--------|
| 7     | OFFSET_CAL_EN_CH2 |          | Enables Offset Calibration on Channel 2. | 0x0   | R/W    |
| [6:0] | OFFSET_CH2[22:16] |          | Channel 2 Offset Calibration Value.      | 0x0   | R/W    |

Address: 0x39, Reset: 0x00, Name: CH3\_GAIN\_LSB

Table 94. Bit Descriptions for CH3\_GAIN\_LSB

| Bits  | Bit Name      | Settings | Description                       | Reset | Access |
|-------|---------------|----------|-----------------------------------|-------|--------|
| [7:0] | GAIN_CH3[7:0] |          | Channel 3 Gain Calibration Value. | 0x0   | R/W    |

Address: 0x3A, Reset: 0x00, Name: CH3\_GAIN\_MID

Table 95. Bit Descriptions for CH3\_GAIN\_MID

| Bits  | Bit Name       | Settings | Description                       | Reset | Access |
|-------|----------------|----------|-----------------------------------|-------|--------|
| [7:0] | GAIN_CH3[15:8] |          | Channel 3 Gain Calibration Value. | 0x0   | R/W    |

Address: 0x3B, Reset: 0x00, Name: CH3\_GAIN\_MSB

Table 96. Bit Descriptions for CH3\_GAIN\_MSB

| Bits  | Bit Name         | Settings | Description                            | Reset | Access |
|-------|------------------|----------|--|-------|--------|
| [7:5] | Reserved         |          | Reserved.                              | 0x0   | R      |
| 4     | GAIN_CAL_SEL_CH3 |          | Enables Gain Calibration on Channel 3. | 0x0   | R/W    |
| [3:0] | GAIN_CH3[19:16]  |          | Channel 3 Gain Calibration Value.      | 0x0   | R/W    |

Address: 0x3C, Reset: 0x00, Name: CH3\_OFFSET\_LSB

Table 97. Bit Descriptions for CH3\_OFFSET\_LSB

| Bits  | Bit Name        | Settings | Description                         | Reset | Access |
|-------|-----------------|----------|-------------------------------------|-------|--------|
| [7:0] | OFFSET_CH3[7:0] |          | Channel 3 Offset Calibration Value. | 0x0   | R/W    |

Address: 0x3D, Reset: 0x00, Name: CH3\_OFFSET\_MID

Table 98. Bit Descriptions for CH3\_OFFSET\_MID

| Bits  | Bit Name         | Settings | Description                         | Reset | Access |
|-------|------------------|----------|-------------------------------------|-------|--------|
| [7:0] | OFFSET_CH3[15:8] |          | Channel 3 Offset Calibration Value. | 0x0   | R/W    |

Address: 0x3E, Reset: 0x00, Name: CH3\_OFFSET\_MSB

Table 99. Bit Descriptions for CH3\_OFFSET\_MSB

| Bits  | Bit Name          | Settings | Description                              | Reset | Access |
|-------|-------------------|----------|--|-------|--------|
| 7     | OFFSET_CAL_EN_CH3 |          | Enables Offset Calibration on Channel 3. | 0x0   | R/W    |
| [6:0] | OFFSET_CH3[22:16] |          | Channel 3 Offset Calibration Value.      | 0x0   | R/W    |

Address: 0x3F, Reset: 0x00, Name: MCLK\_COUNTER

Table 100. Bit Descriptions for MCLK\_COUNTER

| Bits  | Bit Name   | Settings | Description   | Reset | Access |
|-------|------------|----------|---|-------|--------|
| [7:0] | MCLK_COUNT |          | 8-Bit Counter that Increments Once Every 12,000 MCLK Cycles. The counter output is read back, which enables the user to determine the frequency of the external clock. The MCLK counter starts when MCLK_CNT_EN is set, and ends when it reaches 255 MCLK cycles. | 0x0   | R      |

Address: 0x40, Reset: 0x00, Name: DIG\_FILTER\_OFUF

Table 101. Bit Descriptions for DIG\_FILTER\_OFUF

| Bits  | Bit Name     | Settings | Description                     | Reset | Access |
|-------|--------------|----------|---------------------------------|-------|--------|
| [7:4] | Reserved     |          | Reserved.                       | 0x0   | R      |
| 3     | ERR_OFUF_CH3 | 0        | No overflow or underflow error. | 0x0   | R      |
|       |              | 1        | Overflow or underflow error.    |       |        |
| 2     | ERR_OFUF_CH2 | 0        | No overflow or underflow error. | 0x0   | R      |
|       |              | 1        | Overflow or underflow error.    |       |        |
| 1     | ERR_OFUF_CH1 | 0        | No overflow or underflow error. | 0x0   | R      |
|       |              | 1        | Overflow or underflow error.    |       |        |
| 0     | ERR_OFUF_CH0 | 0        | No overflow or underflow error. | 0x0   | R      |
|       |              | 1        | Overflow or underflow error.    |       |        |

Address: 0x41, Reset: 0x00, Name: DIG\_FILTER\_SETTLED

Table 102. Bit Descriptions for DIG\_FILTER\_SETTLED

| Bits  | Bit Name    | Settings | Description   | Reset | Access |
|-------|-------------|----------|---|-------|--------|
| [7:4] | Reserved    |          | Reserved.   | 0x0   | R      |
| 3     | CH3_SETTLED | 0<br>1   | Channel 3 Digital Filter Status.<br>Digital filter not settled.<br>Digital filter is settled. | 0x0   | R      |
| 2     | CH2_SETTLED | 0<br>1   | Channel 2 Digital Filter Status.<br>Digital filter not settled.<br>Digital filter is settled. | 0x0   | R      |
| 1     | CH1_SETTLED | 0<br>1   | Channel 1 Digital Filter Status.<br>Digital filter not settled.<br>Digital filter is settled. | 0x0   | R      |
| 0     | CH0_SETTLED | 0<br>1   | Channel 0 Digital Filter Status.<br>Digital filter not settled.<br>Digital filter is settled. | 0x0   | R      |

Address: 0x42, Reset: 0x00, Name: INTERNAL\_ERROR

Table 103. Bit Descriptions for INTERNAL\_ERROR

| Bits  | Bit Name     | Settings | Description   | Reset | Access |
|-------|--------------|----------|---|-------|--------|
| [7:4] | Reserved     |          | Reserved.   | 0x0   | R      |
| 3     | ERR_DCLK     | 0<br>1   | DCLK Error Flag Indicates that the DCLK Programmed or Provided is Low to Clock Out the Complete Frame.<br>No DCLK error.<br>DCLK error.   | 0x0   | R      |
| 2     | ERR_FUSE_CRC | 0<br>1   | Fuse Error Flag Indicates a CRC Error in Fuse Contents. When enabled, a CRC calculation is performed on the fuse contents. If the contents have changed, this bit is set.<br>No fuse CRC error.<br>Fuse CRC error.  | 0x0   | R      |
| 1     | ERR_ASRC     | 0<br>1   | ASRC Error Flag Indicates if ODR is Out of Range of the Filter Selected.<br>No ASRC error.<br>ASRC error.   | 0x0   | R      |
| 0     | ERR_MM_CRC   | 0<br>1   | Memory Map Error Flag Indicates CRC Error in On-Chip Register Contents. When enabled, a CRC calculation is performed on the memory map each time the registers are written to. Following this calculation, periodic CRC checks are performed on the on-chip registers. If the register contents have changed, an error is flagged.<br>No memory map error.<br>Memory map error. | 0x0   | R      |

Address: 0x47, Reset: 0x00, Name: SPI Error

Table 104. Bit Descriptions for SPI Error

| Bits  | Bit Name         | Settings | Description  | Reset | Access |
|-------|------------------|----------|--|-------|--------|
| [7:4] | Reserved         |          | Reserved.  | 0x0   | R      |
| 3     | ERR_SPI_CRC      | 0<br>1   | SPI CRC Error Flag Indicates CRC Error During SPI Communications. This error reporting is enabled using the ERR_SPI_CRC_EN bit in the diagnostic control register.<br>No CRC error.<br>CRC error detected. | 0x0   | R      |
| 2     | ERR_SPI_SCLK_CNT | 0<br>1   | SCLK counter error flag indicates that the number of SCLK cycles during SPI communication is not a multiple of eight.<br>No error.<br>SCLK counter error detected.   | 0x0   | R      |
| 1     | ERR_SPI_WRITE    | 0<br>1   | SPI Write Error Flag Indicates Error During SPI Write Operation.<br>No error.<br>SPI write error.  | 0x0   | R      |

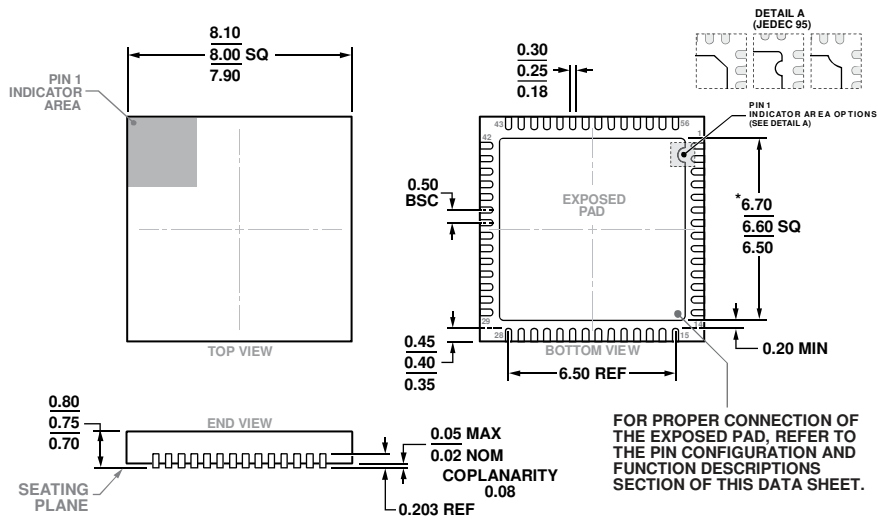
| Bits | Bit Name     | Settings | Description   | Reset | Access |
|------|--------------|----------|---|-------|--------|
| 0    | ERR_SPI_READ | 0<br>1   | SPI Read Error Flag Indicates Error During SPI Read Operation.<br>No error.<br>Read error detected. | 0x0   | R      |

Address: 0x48, Reset: 0x00, Name: AIN\_OR\_ERROR

Table 105. Bit Descriptions for AIN\_OR\_ERROR

| Bits  | Bit Name    | Settings | Description  | Reset | Access |
|-------|-------------|----------|--|-------|--------|
| [7:4] | Reserved    |          | Reserved.  | 0x0   | R      |
| 3     | ERR_OR_AIN3 | 0<br>1   | Input Overvoltage Flag on Channel 3. When enabled, this bit detects the input voltage exceeding the absolute value of $V_{REF}$ .<br>No overvoltage input detected.<br>Overvoltage input detected. | 0x0   | R      |
| 2     | ERR_OR_AIN2 | 0<br>1   | Input Overvoltage Flag on Channel 2. When enabled, this bit detects the input voltage exceeding the absolute value of $V_{REF}$ .<br>No overvoltage input detected.<br>Overvoltage input detected. | 0x0   | R      |
| 1     | ERR_OR_AIN1 | 0<br>1   | Input Overvoltage Flag on Channel 1. When enabled, this bit detects the input voltage exceeding the absolute value of $V_{REF}$ .<br>No overvoltage input detected.<br>Overvoltage input detected. | 0x0   | R      |
| 0     | ERR_OR_AIN0 | 0<br>1   | Input Overvoltage Flag on Channel 0. When enabled, this bit detects the input voltage exceeding the absolute value of $V_{REF}$ .<br>No overvoltage input detected.<br>Overvoltage input detected. | 0x0   | R      |

OUTLINE DIMENSIONS



\*COMPLIANT TO JEDEC STANDARDS MO-220-WLLD-5 WITH EXCEPTION TO EXPOSED PAD DIMENSION

Figure 127. 56-Lead Lead Frame Chip Scale Package [LFCSP]  
8 mm x 8 mm Body and 0.75 mm Package Height  
(CP-56-9)  
Dimensions shown in millimeters

ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                           | Package Option |
|--------------------|-------------------|---|----------------|
| AD7134BCPZ         | 0°C to 85°C       | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-9        |
| AD7134BCPZ-RL7     | 0°C to 85°C       | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-9        |
| EVAL-AD7134FMCZ    |                   | Evaluation Board                              |                |
| EVAL-SDP-CH1Z      |                   | Controller Board                              |                |

<sup>1</sup> Z = RoHS Compliant Part.