HMC941A

v04.0818

0.5 dB LSB GaAs MMIC 5-BIT DIGITAL ATTENUATOR, 0.1 - 30 GHz

Typical Applications

The HMC941A is ideal for:

- Fiber Optics & Broadband Telecom
- Microwave Radio & VSAT
- Military Radios, Radar & ECM
- Space Applications

Features

0.5 dB LSB Steps to 15.5 dB

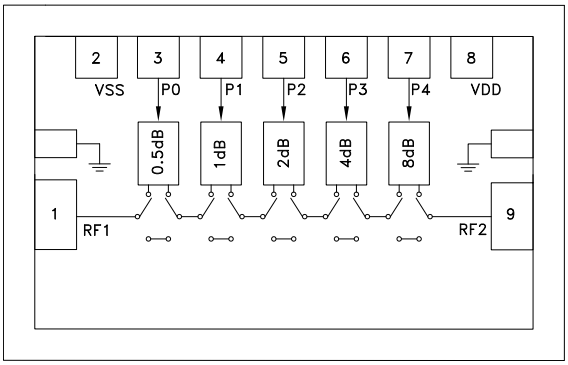
Single Positive Control Line Per Bit

±0.5 dB Typical Bit Error

High Input IP3: +45 dBm

Die Size: 2.29 mm x 0.96 mm x 0.1 mm

Functional Diagram



General Description

The HMC941A die is a broadband 5-bit GaAs IC digital attenuator MMIC chip. Covering 0.1 to 30 GHz, the insertion loss is less than 4 dB typical. The attenuator bit values are 0.5 (LSB), 1, 2, 4, 8, for a total attenuation of 15.5 dB. Attenuation accuracy is excellent at less than ± 0.5 dB typical step error with an IIP3 of +45 dBm. Five control voltage inputs, toggled between +5V and 0V, are used to select each attenuation state.

Electrical Specifications, T_A = +25° C, With Vdd = +5V, Vss = -5V & VCTL = 0/ +5V

Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Insertion Loss	0.1 - 18.0 GHz 18.0 - 30.0 GHz		3.1 4.2	4.3 5.1	dB dB
Attenuation Range	0.1 - 30.0 GHz		15.5		dB
Return Loss (RF1 & RF2, All Atten. States)	0.1 - 30.0 GHz		12		dB
Attenuation Accuracy: (Referenced to Insertion Loss) 0.5 - 7.5 dB States 8 - 15.5 dB States	 0.1 - 30.0 GHz 0.1 - 30.0 GHz	 ± (0.3 + 4% of Atten. Setting)Max ± (0.3 + 5% of Atten. Setting) Max			 dB dB
Input Power for 0.1 dB Compression	0.1 - 0.5 GHz 0.5 - 30.0 GHz		22 26		dBm dBm
Input Third Order Intercept Point (Two-Tone Input Power= +8 dBm Each Tone)	0.1 - 0.5 GHz 0.5 - 30.0 GHz		45 43		dBm dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON/tOFF (50% CTL to 10/90% RF)	0.1 - 30.0 GHz		 35 50		 ns ns
Idd	0.1 - 30.0 GHz	3	5	7	mA
Iss	0.1 - 30.0 GHz	-4	-6	-8	mA

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

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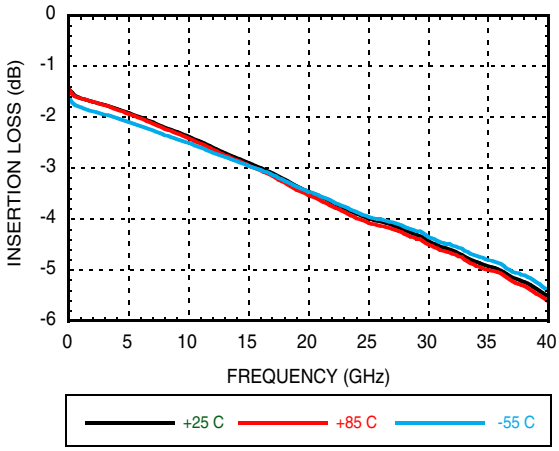
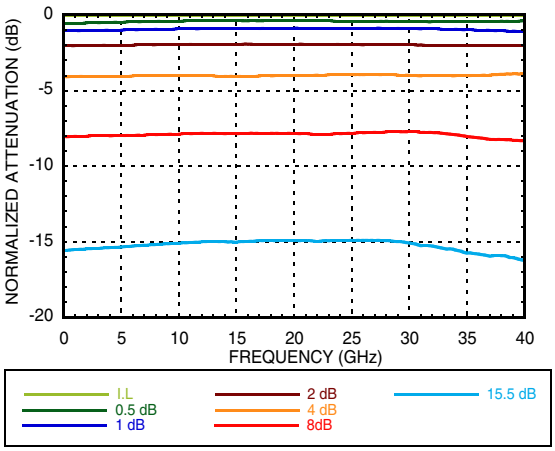
Insertion Loss vs. Temperature



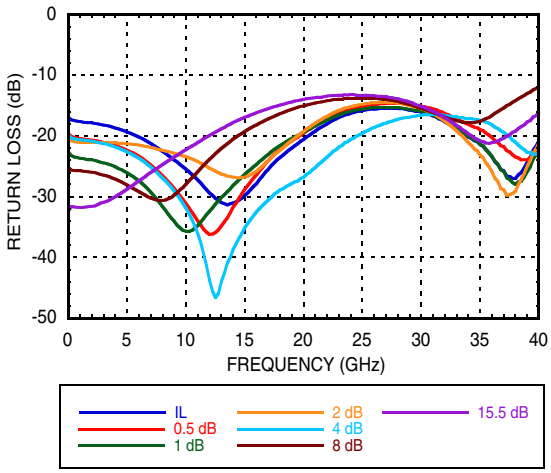
Normalized Attenuation

(Only Major States are Shown)



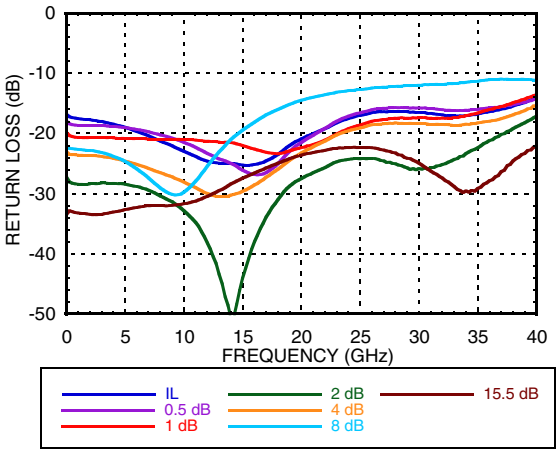
Input Return Loss

(Only Major States are Shown)

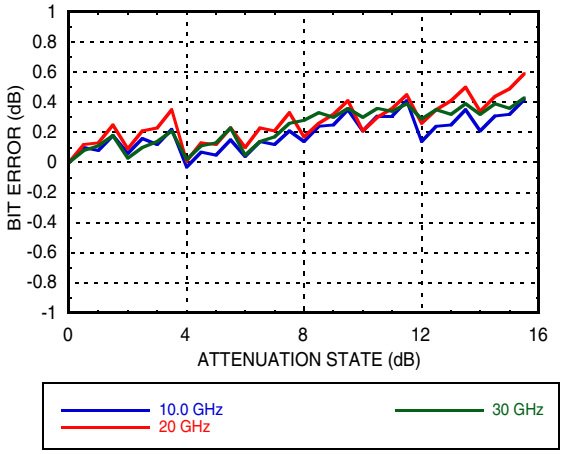


Output Return Loss

(Only Major States are Shown)

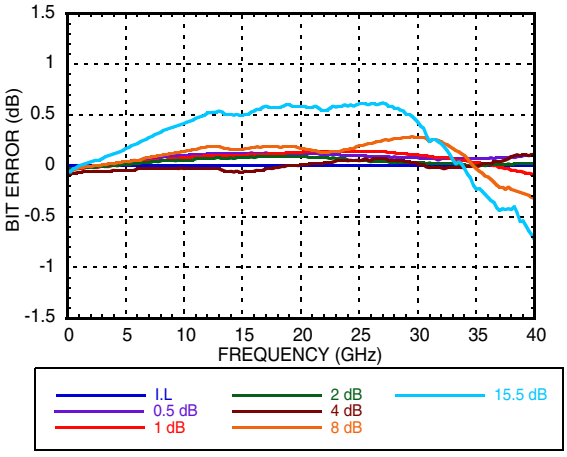


Bit Error vs. Attenuation State



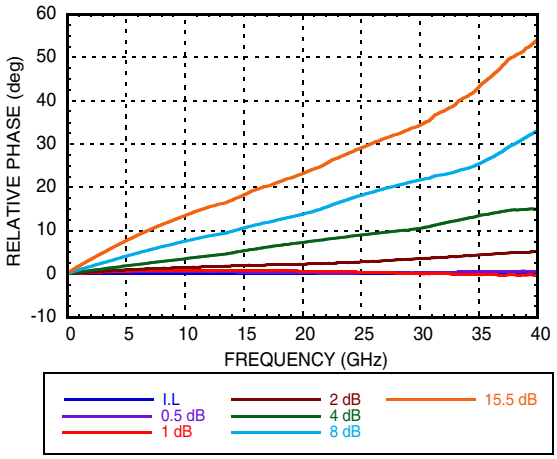
Bit Error vs. Frequency

(Only Major States are Shown)

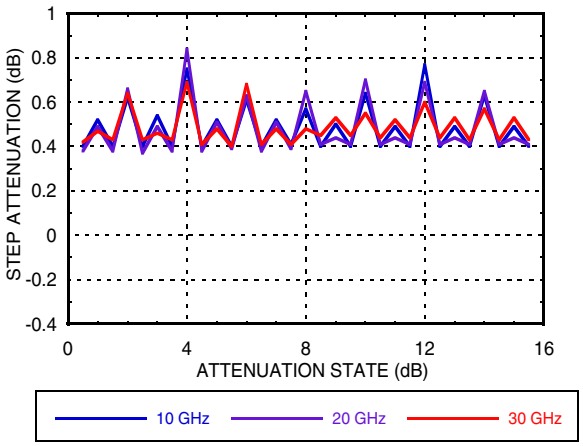


Relative Phase vs. Frequency

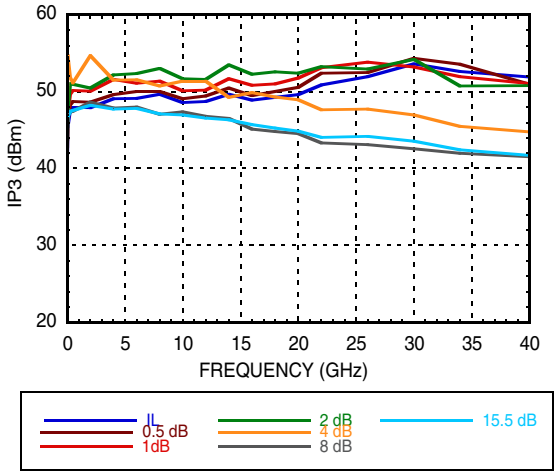
(Only Major States are Shown)



Step Attenuation vs. Attenuation State

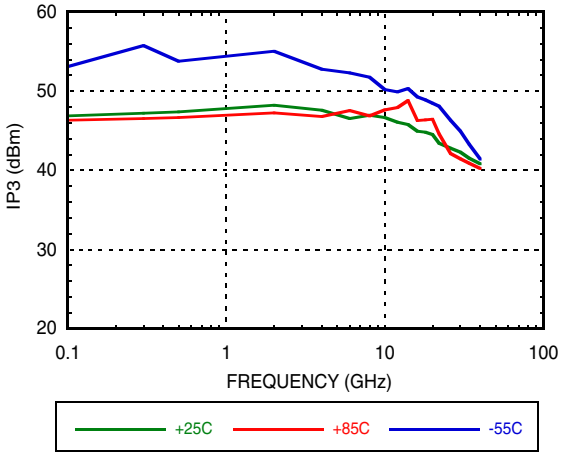


Input IP3 Over Major Attenuation States

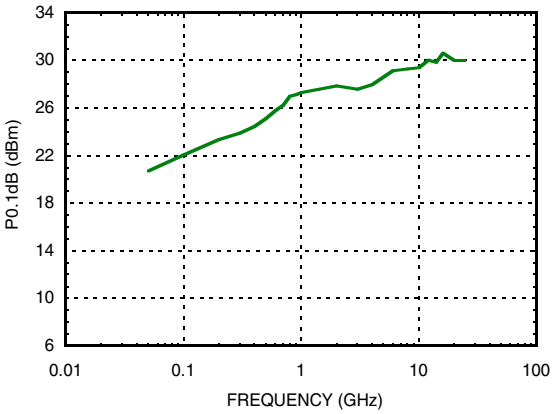


Input IP3 vs. Temperature

(Minimum Attenuation State)



Input Power for 0.1 dB Compression



Truth Table

Control Voltage Input					Attenuation State RF1 - RF2
P4 8 dB	P3 4 dB	P2 2 dB	P1 1 dB	P0 0.5 dB	
High	High	High	High	High	Reference I.L.
High	High	High	High	Low	0.5 dB
High	High	High	Low	High	1 dB
High	High	Low	High	High	2 dB
High	Low	High	High	High	4 dB
Low	High	High	High	High	8 dB
Low	Low	Low	Low	Low	15.5 dB

Any Combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.

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Absolute Maximum Ratings

RF Input Power (0.5 to 30 GHz)	+27 dBm
Control Voltage (P0 to P4)	Vdd + 0.5V
Vdd	+7 Vdc
Vss	-7 Vdc
Channel Temperature	150 °C
Continuous Pdiss (T=85°C) (derate 6.97 mW/°C above 85°C)	0.453 W
Thermal Resistance (channel to die bottom)	143.5 °C/W
Storage Temperature	-65 to + 150 °C
Operating Temperature	-55 to +85 °C
ESD Sensitivity (HBM)	Class 1A

Bias Voltages & Currents

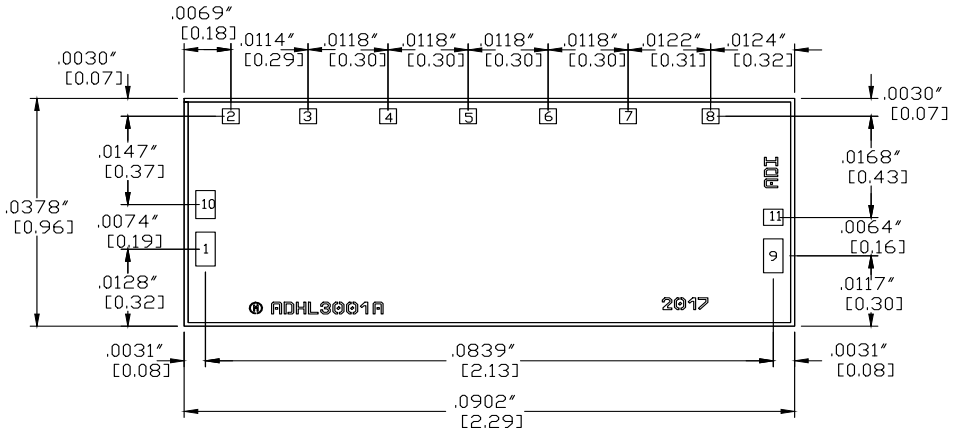
Vdd	+5V @ 5 mA (Typ)
Vss	-5V @ 6 mA (Typ)

Control Voltage

State	Bias Condition
Low	0 to 0.8V @ 1 µA (Typ)
High	2 to 5V @ 1 µA (Typ)

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



PAD	DESCRIPTION	PAD SIZE
1	RF1	0.0056"[0.14] X 0.0029"[0.07]
2	VSS	0.0025"[0.06] X 0.0025"[0.06]
3,4,5,6,7	P0,P1,P2,P3,P4	0.0025"[0.06] X 0.0025"[0.06]
8	VDD	0.0025"[0.06] X 0.0025"[0.06]
9	RF2	0.0056"[0.14] X 0.0029"[0.07]
10	GND	0.0046"[0.12] X 0.0029"[0.07]
11	GND	0.0029"[0.07] X 0.0029"[0.07]

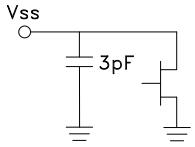
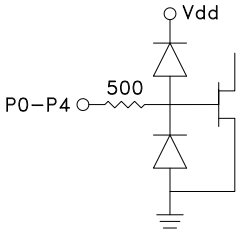
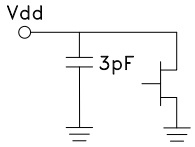
1. ALL DIMENSIONS ARE IN INCHES [MILLIMETERS]
2. TYPICAL BOND PAD SPACING IS 0.0118" CENTER TO CENTER EXCEPT AS NOTED.
3. BACKSIDE METALIZATION: GOLD
4. BACKSIDE METAL IS GROUND
5. BOND PAD METALIZATION: GOLD

Die Packaging Information [1]

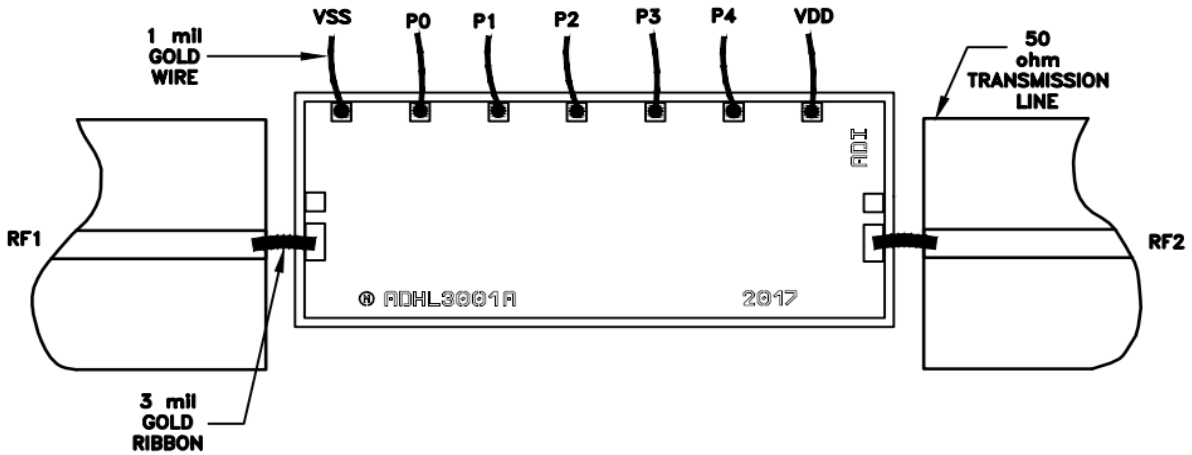
Standard	Alternate
WP-9 (Waffle Pack)	[2]

[1] Refer to the "Packaging Information" section for die packaging dimensions.
[2] For alternate packaging information contact Analog Devices Inc.

Pad Descriptions

Pad Number	Function	Description	Interface Schematic
10,11	GND	Die bottom must be connected to RF ground.	
1, 9	RF1, RF2	This pad is DC coupled and matched to 50 Ohm. Blocking capacitors are required if RF line potential is not equal to 0V.	
2	Vss	Negative Bias -5V	
3 - 7	P0 - P4	See truth table and control voltage table.	
8	Vdd	Positive Bias +5V	

Assembly Diagram



Mounting & Bonding Techniques for Millimeterwave GaAs MMICs

The die should be attached directly to the ground plane eutectically or with conductive epoxy (see HMC general Handling, Mounting, Bonding Note).

50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a 0.150mm (6 mil) thick molybdenum heat spreader (moly-tab) which is then attached to the ground plane (Figure 2).

Microstrip substrates should brought as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076mm to 0.152 mm (3 to 6 mils).

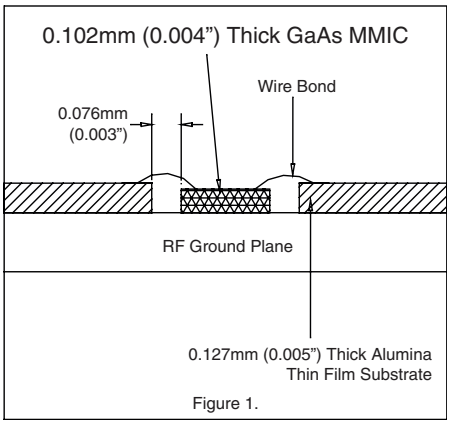


Figure 1.

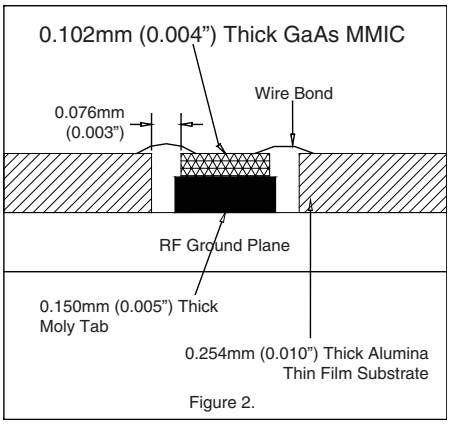


Figure 2.

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

Eutectic Die Attach: A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31mm (12 mils).