32Mx8, 16Mx16, 8Mx32
256Mb Synchronous DRAM

FEBRUARY 2015

FEATURES

- Fully synchronous; all signals referenced to a positive clock edge
- Internal bank for hiding row access and pre-charge
- Programmable CAS latency: 2, 3
- Programmable Burst Length: 1, 2, 4, 8, and Full Page
- Programmable Burst Sequence:
  – Sequential and Interleave
- Auto Refresh (CBR)

OPTIONS

- Configurations:
  – 32M x 8
  – 16M x 16
  – 8M x 32
- Power Supply
  IS42VSxxx – V_{DD}/V_{DDQ} = 1.8V
- Packages:
  x8 –TSOP II (54)
  x16 –TSOP II (54)
  x32 – TSOP II (86)
- Temperature Range:
  Industrial (–40 ºC to 85 ºC)

DESCRIPTION

ISSI's 256Mb Synchronous DRAM achieves high-speed data transfer using pipeline architecture. All input and output signals refer to the rising edge of the clock input. Both write and read accesses to the SDRAM are burst oriented. The 256Mb Synchronous DRAM is designed to minimize power consumption making it ideal for low-power applications.

KEY TIMING PARAMETERS

Parameter	-75	-10	Unit
CLK Cycle Time			
$\overline{CAS}$ Latency = 3	7.5	10	ns
$\overline{CAS}$ Latency = 2	9.6	12	ns
CLK Frequency			
$\overline{CAS}$ Latency = 3	133	100	Mhz
$\overline{CAS}$ Latency = 2	104	83	Mhz
Access Time from CLK			
$\overline{CAS}$ Latency = 3	5.4	8	ns
$\overline{CAS}$ Latency = 2	8	10	ns

ADDRESSING TABLE

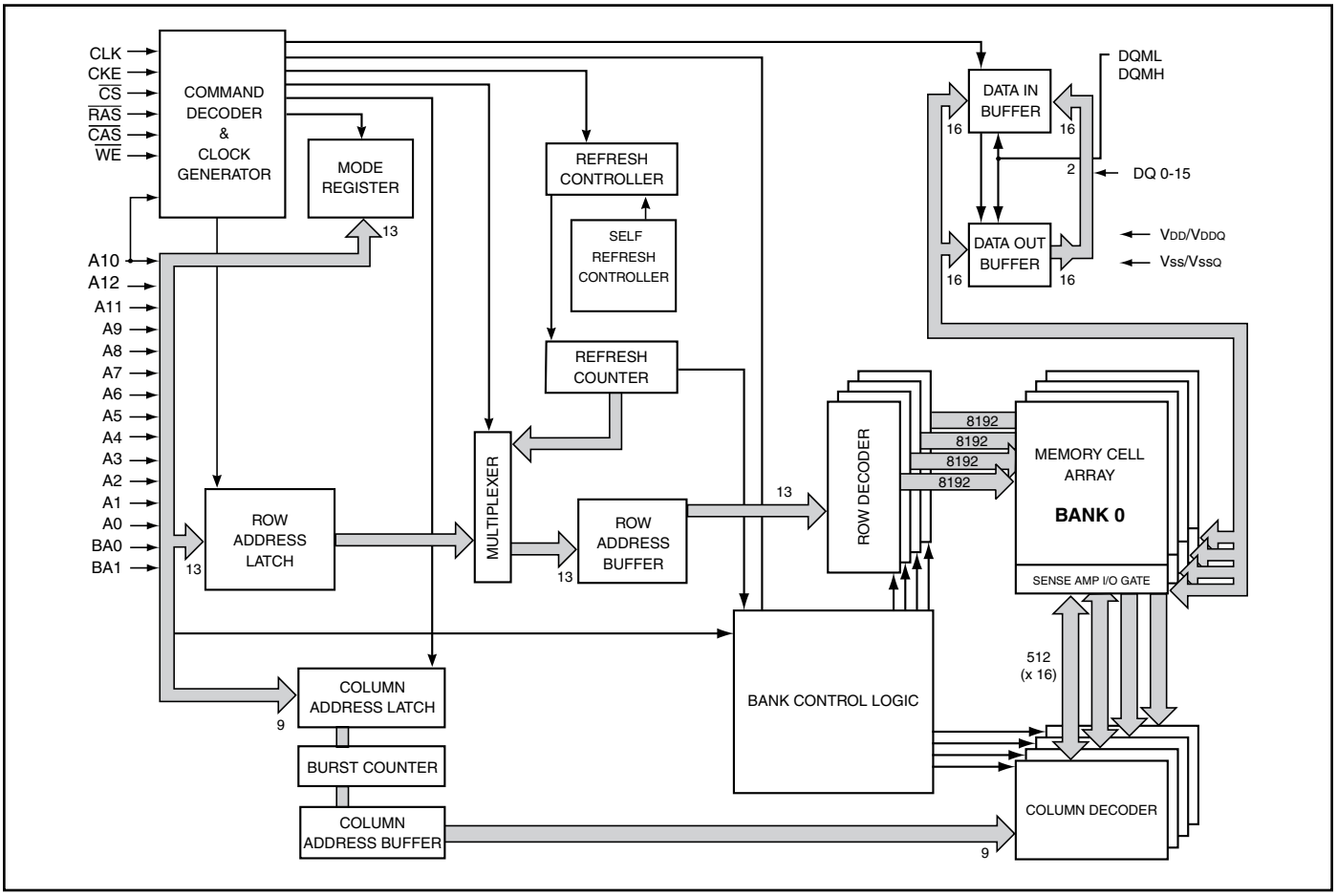
Parameter	32M x 8	16M x 16	8M x 32
Configuration	8M x 8 x 4 banks	4M x 16 x 4 banks	2M x 32 x 4 banks
Refresh Count	8K/64ms	8K/64ms	4K/64ms
Row Addressing	A0-A12	A0-A12	A0-A11
Column Addressing	A0-A9	A0-A8	A0-A8
Bank Addressing	BA0, BA1	BA0, BA1	BA0, BA1
Precharge Addressing	A10	A10	A10

General Description

ISSI's 256Mb SDRAM is a high speed CMOS, dynamic random-access memory designed to operate in 1.8V V_{DD}/V_{DDQ} memory systems containing 268,435,456 bits. Internally configured as a quad-bank DRAM with a synchronous interface. The 256Mb SDRAM includes an AUTO REFRESH MODE, and a power-saving, power-down mode. All signals are registered on the positive edge of the clock signal, CLK. All inputs and outputs are LVCMOS (VDD = 1.8V) compatible. The 256Mb SDRAM has the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time and the capability to randomly change column addresses on each clock cycle during burst access.

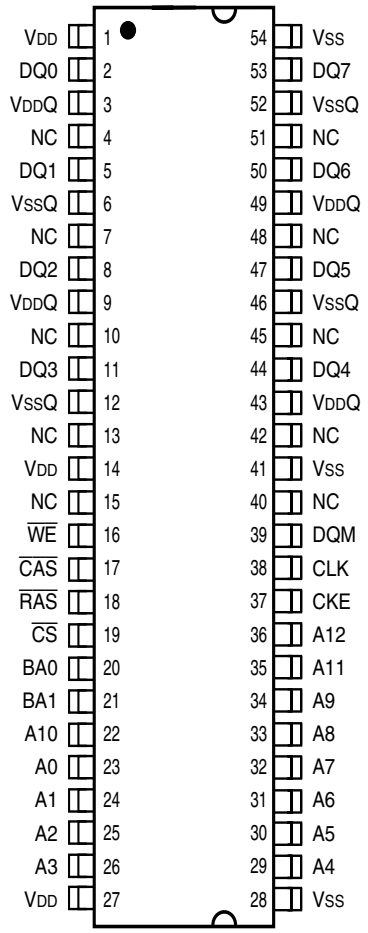
A self-timed row precharge initiated at the end of the burst sequence is available with the AUTO PRECHARGE function enabled. Precharge one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation. SDRAM read and write accesses are burst oriented starting at a selected location and continuing for a programmed number of locations in a programmed sequence. The registration of an Active command begins accesses, followed by a Read or Write command. The ACTIVE command in conjunction with address bits registered are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 (x8 and x16) and A0-A11 (x32) select the row). The READ or WRITE commands in conjunction with address bits registered are used to select the starting column location for the burst access. Programmable READ or WRITE burst lengths consist of 1, 2, 4 and 8 locations, or full page, with a burst terminate option.

FUNCTIONAL BLOCK DIAGRAM (FOR 16Mx16 BANKS SHOWN)



PIN CONFIGURATIONS

54 pin TSOP – Type II for x8



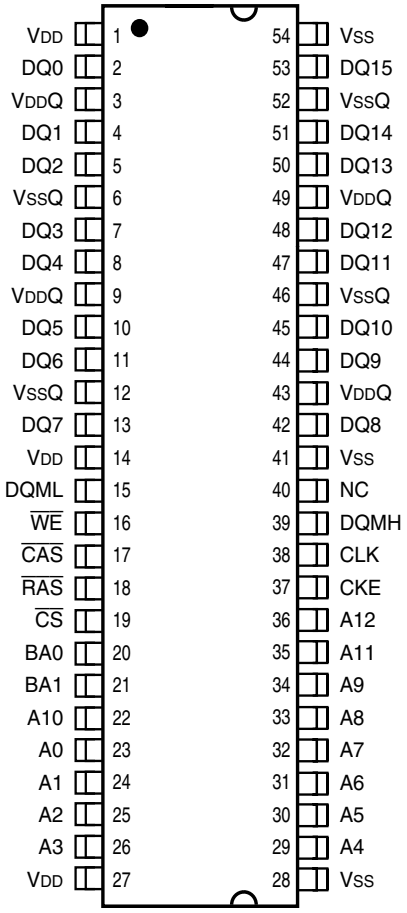
PIN DESCRIPTIONS

32M x 8	Pin Name
A0–A12	Row Address Input
A0–A9	Column Address Input
BA0, BA1	Bank Select Address
DQ0–DQ7	Data Input/Output
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command

32M x 8	Pin Name
$\overline{CAS}$	Column Address Strobe Command
$\overline{WE}$	Write Enable
DQM	Data Input/Output Mask
VDD	Power
VSS	Ground
VDDQ	Power Supply for I/O Pin
VSSQ	Ground for I/O Pin
NC	No Connection

PIN CONFIGURATIONS

54 pin TSOP – Type II for x16



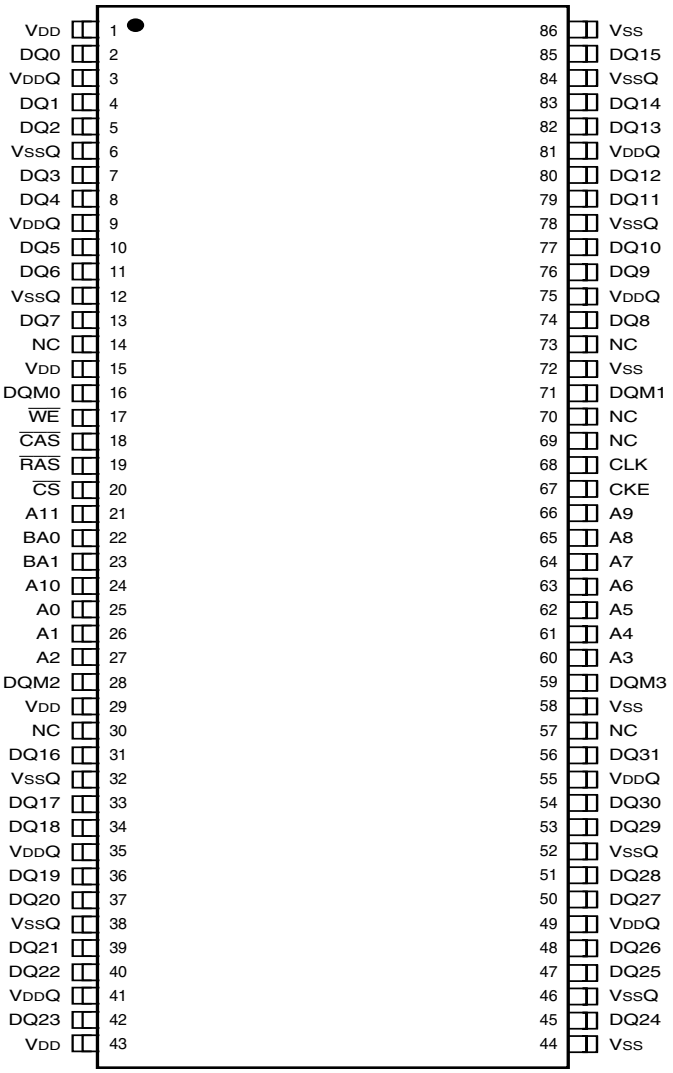
PIN DESCRIPTIONS

16M x16	Pin Name
A0–A12	Row Address Input
A0–A8	Column Address Input
BA0, BA1	Bank Select Address
DQ0–DQ15	Data Input/Output
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

16M x16	Pin Name
$\overline{WE}$	Write Enable
DQML / DQMH	Data Input/Output Mask
VDD	Power
VSS	Ground
VDDQ	Power Supply for I/O Pin
VSSQ	Ground for I/O Pin
NC	No Connection

PIN CONFIGURATIONS

86 pin TSOP – Type II for x32



PIN DESCRIPTIONS

8M x32	Pin Name
A0–A11	Row Address Input
A0–A8	Column Address Input
BA0, BA1	Bank Select Address
DQ0–DQ31	Data Input/Output
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

8M x32	Pin Name
$\overline{WE}$	Write Enable
DQM0 - DQM3	Data Input/Output Mask
VDD	Power
VSS	Ground
VDDQ	Power Supply for I/O Pin
VSSQ	Ground for I/O Pin
NC	No Connection

1.8V (VS) SDRAM Functionality

ISSI's 256Mb 42VS Series SDRAM IS42VS83200J, IS42VS16160J, and IS42VS32800J, are pin compatible and have similar functionality with ISSI's standard 3.3V SDRAMs, but offer lower operating voltages and lower current. For detailed descriptions of pin functions, command truth tables, functional truth tables, device operation as well as timing diagrams please refer to datasheets related to IS42S83200J, IS42S16160J, or IS42S32800J, listed at www.issi.com

REGISTER DEFINITION

Mode Register (MR)

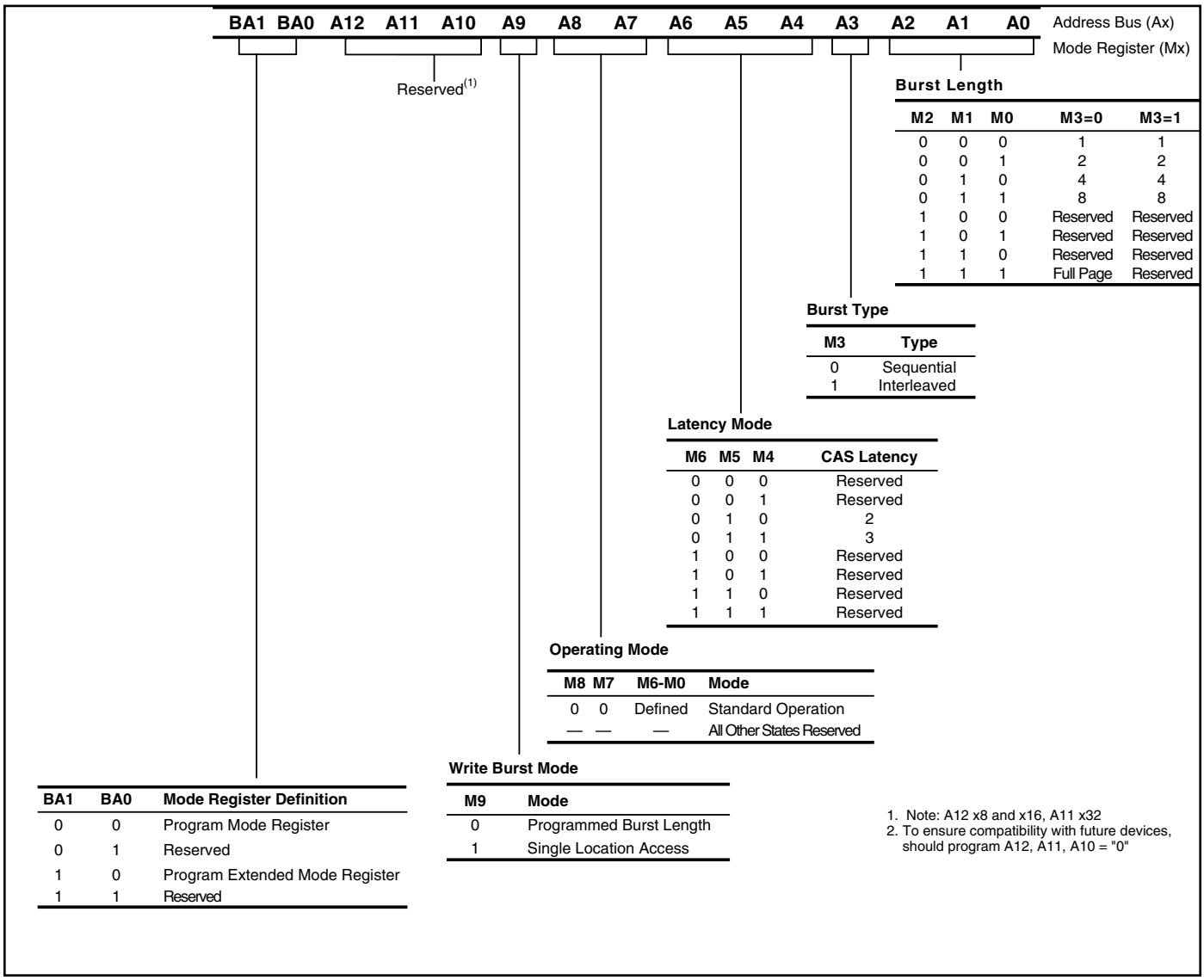
There is a mode register in the SDRAM. The Mode Register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of burst length, a burst type, CAS Latency, operating mode, and a write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

The MR is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure MODE REGISTER DEFINITION. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0 - M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4 - M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the WRITE burst mode, and M10, M11, and M12 are reserved for future use.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

MODE REGISTER DEFINITION



Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in MODE REGISTER DEFINITION. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4 or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A8 (x32), A1-A8 (x16) or A1-A9 (x8) when the burst length is set to two; by A2-A8 (x32), A2-A8 (x16) or A2-A9 (x8) when the burst length is set to four; and by A3-A8 (x32), A3-A8 (x16) or A3-A9 (x8) when the burst length is set to eight. The remaining (least significant) address bit(s) are used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in BURST DEFINITION table.

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
			A 0		
2			0	0-1	0-1
			1	1-0	1-0
		A 1	A 0		
		0	0	0-1-2-3	0-1-2-3
4		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
	A 2	A 1	A 0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
8	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A8 (x16, x32) n = A0-A9 (x8) (location 0-y)			Cn + 3, Cn + 4... …Cn - 1, Cn…	Cn, Cn + 1, Cn + 2 Not Supported

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge n + m. The DQs will start driving as a result of the clock edge one cycle earlier (n + m - 1), and provided that the relevant access times are met, the data will be valid by clock edge n + m. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in CAS Latency diagrams.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

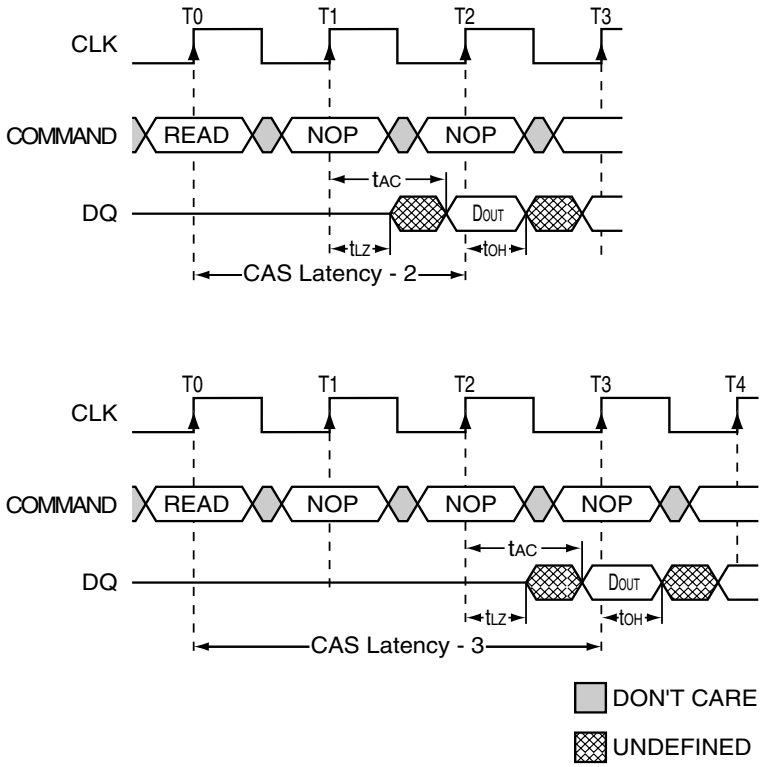
The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

CAS LATENCY



Note: A12 x8 and x16, A11 x32

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters	Rating	Unit
$V_{DD\ MAX}$	Maximum Supply Voltage	–0.35 to +2.8	V
$V_{DDQ\ MAX}$	Maximum Supply Voltage for Output Buffer	–0.35 to +2.8	V
V_{IN}	Input Voltage	–0.35 to V_{DDQ} + 0.5	V
V_{OUT}	Output Voltage	–0.35 to V_{DDQ} + 0.5	V
$P_{D\ MAX}$	Allowable Power Dissipation	1	W
I_{CS}	Output Shorted Current	50	mA
T_{OPR}	Operating Temperature	–40 to +85	°C
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are referenced to Vss.

CAPACITANCE CHARACTERISTICS - x8, x16

Symbol	Parameters	Min.	Max.	Unit
$C_{IN}1$	Input Capacitance: CLK	2.5	3.5	pF
$C_{IN}2$	Input Capacitance: All Other Input Pins	2.5	3.8	pF
$C_{I/O}$	Data Input/Output Capacitance: I/Os	4.0	6.0	pF

CAPACITANCE CHARACTERISTICS - x32

Symbol	Parameters	Min.	Max.	Unit
$C_{IN}1$	Input Capacitance: CLK	2.5	3.5	pF
$C_{IN}2$	Input Capacitance: All Other Input Pins	2.5	3.8	pF
$C_{I/O}$	Data Input/Output Capacitance: I/Os	4.0	6.5	pF

DC RECOMMENDED OPERATING CONDITIONS
IS42VSxxx - 1.8V Operation

Symbol	Parameters	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	1.7	1.8	1.95	V
V_{DDQ}	I/O Supply Voltage	1.7	1.8	1.95	V
V_{IH}(1)	Input High Voltage	0.8xV_{DDQ}	–	V_{DDQ}+0.3	V
V_{IL}(2)	Input Low Voltage	-0.3	–	0.8	V
I_{IL}	Input Leakage Current (0V ≤ V_{IN} ≤ V_{DD})	-1	–	+1	µA
I_{OL}	Output Leakage Current (Output disabled, 0V ≤ V_{OUT} ≤ V_{DD})	-1.5	–	+1.5	µA
V_{OH}	Output High Voltage Current (I_{OH} = -100µA)	0.9xV_{DDQ}	–	–	V
V_{OL}	Output Low Voltage Current (I_{OL} = 100µA)	–	–	0.2	V

Notes:
1. V_{IH} (overshoot): V_{IH} (max) = V_{DDQ} +1.2V (pulse width < 3ns).
2. V_{IL} (undershoot): V_{IH} (min) = -1.2V (pulse width < 3ns).
3. All voltages are referenced to Vss.

DC ELECTRICAL CHARACTERISTICS VDD = 1.8V

Symbol	Parameter	Test Condition	–75	–10	Unit
$I_{DD}1$ (1)	Operating Current	One Bank Active, CL = 3, BL = 2, tCLK = tCLK(min), tRC = tRC(min)	70	55	mA
$I_{DD}2P$ (3)	Precharge Standby Current (In Power-Down Mode)	CKE ≤ V_{IL} (max), tCK = 15ns $\overline{CS}$ ≥ V_{DD} - 0.2V	3	3	mA
$I_{DD}2PS$ (3)	Precharge Standby Current With Clock Stop (In Power-Down Mode)	CKE ≤ V_{IL} (max), CLK ≤ V_{IL} (max) $\overline{CS}$ ≥ V_{DD} - 0.2V	3	3	mA
$I_{DD}2N$ (2)	Precharge Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (min) tCK = 15 ns	22	22	mA
$I_{DD}2NS$	Precharge Standby Current With Clock Stop (In Non-Power Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (min) All Inputs Stable	10	10	mA
$I_{DD}3P$ (2)	Active Standby Current (In Power-Down Mode)	CKE ≤ V_{IL} (max), $\overline{CS}$ ≥ V_{DD} - 0.2V tCK = 15 ns, All Banks Active	7	7	mA
$I_{DD}3PS$	Active Standby Current With Clock Stop (In Power-Down Mode)	CKE ≤ V_{IL} (max), CLK ≤ V_{IL} (max) $\overline{CS}$ ≥ V_{DD} - 0.2V, All Banks Active	7	7	mA
$I_{DD}3N$ (2)	Active Standby Current (In Non Power-Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (min) tCK = 15 ns, All Banks Active	30	30	mA
$I_{DD}3NS$	Active Standby Current With Clock Stop (In Non Power-Down Mode)	$\overline{CS}$ ≥ V_{DD} - 0.2V, CKE ≥ V_{IH} (min) All Inputs Stable, All Banks Active	15	15	mA
$I_{DD}4$	Operating Current	All Banks Active, BL = Full, CL = 3 tCK = tCK(min)	100	75	mA
$I_{DD}5$	Auto-Refresh Current	tRC = tRC(min), tCLK = tCLK(min)	110	80	mA
$I_{DD}6$	Self-Refresh Current	CKE ≤ 0.2V	3	3	mA

Notes:
1. I_{DD} (max) is specified at the output open condition.
2. Input signals are changed one time during 30ns.
3. Tested after 500ms delay

AC ELECTRICAL CHARACTERISTICS (1, 2, 3)

			-75		-10		
Symbol	**Parameter**		**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
tCK3	Clock Cycle Time	CAS Latency = 3	7.5	–	10	–	ns
tCK2		CAS Latency = 2	9.6	–	12	–	ns
tAC3	Access Time From CLK	CAS Latency = 3	–	5.4	–	8	ns
tAC2		CAS Latency = 2	–	8	–	10	ns
tCHI	CLK HIGH Level Width		2.5	–	2.5	–	ns
tCL	CLK LOW Level Width		2.5	–	2.5	–	ns
tOH3	Output Data Hold Time	CAS Latency = 3	2.7	–	2.7	–	ns
tOH2		CAS Latency = 2	2.7	–	2.7	–	ns
tLZ	Output LOW Impedance Time		0	–	0	–	ns
tHZ3	Output HIGH Impedance Time	CAS Latency = 3	2.7	5.4	2.7	8	ns
tHZ2		CAS Latency = 2	2.7	8	2.7	10	
tDS	Input Data Setup Time (2)		1.5	–	1.5	–	ns
tDH	Input Data Hold Time (2)		1.0	–	1.0	–	ns
tAS	Address Setup Time (2)		1.5	–	1.5	–	ns
tAH	Address Hold Time (2)		1.0	–	1.0	–	ns
tCKS	CKE Setup Time (2)		1.5	–	1.5	–	ns
tCKH	CKE Hold Time (2)		1.0	–	1.0	–	ns
tCS	Command Setup Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)(2)		1.5	–	1.5	–	ns
tCH	Command Hold Time (($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)(2)		1.0	–	1.0	–	ns
tRC	Command Period (REF to REF / ACT to ACT)		75	–	96	–	ns
tRAS	Command Period (ACT to PRE)		48	100K	60	100K	ns
tRP	Command Period (PRE to ACT)		19	–	24	–	ns
tRCD	Active Command to Read/ Write Command Delay Time		19	–	24	–	ns
tRRD	Command Period (ACT [0] to ACT [1])		15	–	20	–	ns
tDPL	Input Data to Precharge Command Delay Time		15	–	20	–	ns
tDAL	Input Data to Active/Refresh Command Delay Time (During Auto-Precharge)		37	–	48	–	ns
tMRD	Mode Register Program Time		15	–	20	–	ns
tDDE	Power Down Exit Setup Time		7.5	–	10	–	ns
tXSR	Exit Self-Refresh to Active Time		75	–	100	–	ns
tT	Transition Time		0.3	1.2	0.3	1.2	ns
tREF	Refresh Cycle Time	8K times (x8/x16)	–	64	–	64	ms
		4K times (x32)	–	64	–	64	ms

Notes:
1. The power-on sequence must be executed before starting memory operation.
2. Measured with tT = 1 ns. If clock rising time is longer than 1ns, (tT/2 - 0.5) ns should be added to the parameter.
3. The reference level is 0.9V when measuring input signal timing. Rise and fall times are measured between V_{IH}(min.) and V_{IL} (max).

OPERATING FREQUENCY / LATENCY RELATIONSHIPS

SYMBOL	PARAMETER	-75	-10	UNITS
—	Clock Cycle Time	7.5	10	ns
—	Operating Frequency	133	100	MHz
t_{CAC}	$\overline{CAS}$ Latency	3	3	cycle
t_{RCD}	Active Command To Read/Write Command Delay Time	3	3	cycle
t_{RAC}	$\overline{RAS}$ Latency (t_{RCD} + t_{CAC}) $\overline{CAS}$ Latency = 3	6	6	cycle
t_{RC}	Command Period (REF to REF / ACT to ACT)	10	10	cycle
t_{RAS}	Command Period (ACT to PRE)	7	7	cycle
t_{RP}	Command Period (PRE to ACT)	3	3	cycle
t_{RRD}	Command Period (ACT[0] to ACT [1])	2	2	cycle
t_{CCD}	Column Command Delay Time (READ, READA, WRIT, WRITA)	1	1	cycle
t_{DPL}	Input Data To Precharge Command Delay Time	2	2	cycle
t_{DAL}	Input Data To Active/Refresh Command Delay Time (During Auto-Precharge)	5	5	cycle
t_{RBD}	Burst Stop Command To Output in HIGH-Z Delay Time (Write) $\overline{CAS}$ Latency = 3	3	3	cycle
t_{WBD}	Burst Stop Command To Input in Invalid Delay Time (Write)	0	0	cycle
t_{RQL}	Precharge Command To Output in HIGH-Z Delay Time (Read) $\overline{CAS}$ Latency = 3	3	3	cycle
t_{WDL}	Precharge Command To Input in Invalid Delay Time (Write)	0	0	cycle
t_{PQL}	Last Output To Auto-Precharge Start Time (Read) $\overline{CAS}$ Latency = 3	-2	-2	cycle
t_{QMD}	DQM To Output Delay Time (Read)	2	2	cycle
t_{DMD}	DQM To Input Delay Time (Write)	0	0	cycle
t_{MRD}	Mode Register Set To Command Delay Time	2	2	cycle

Note: Clock cycle values follow the timing values from AC Electrical Characteristics.

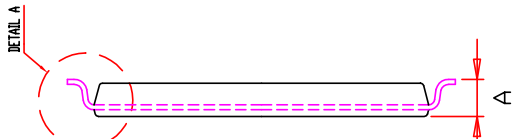
Ordering Information – V_{DD} = 1.8V

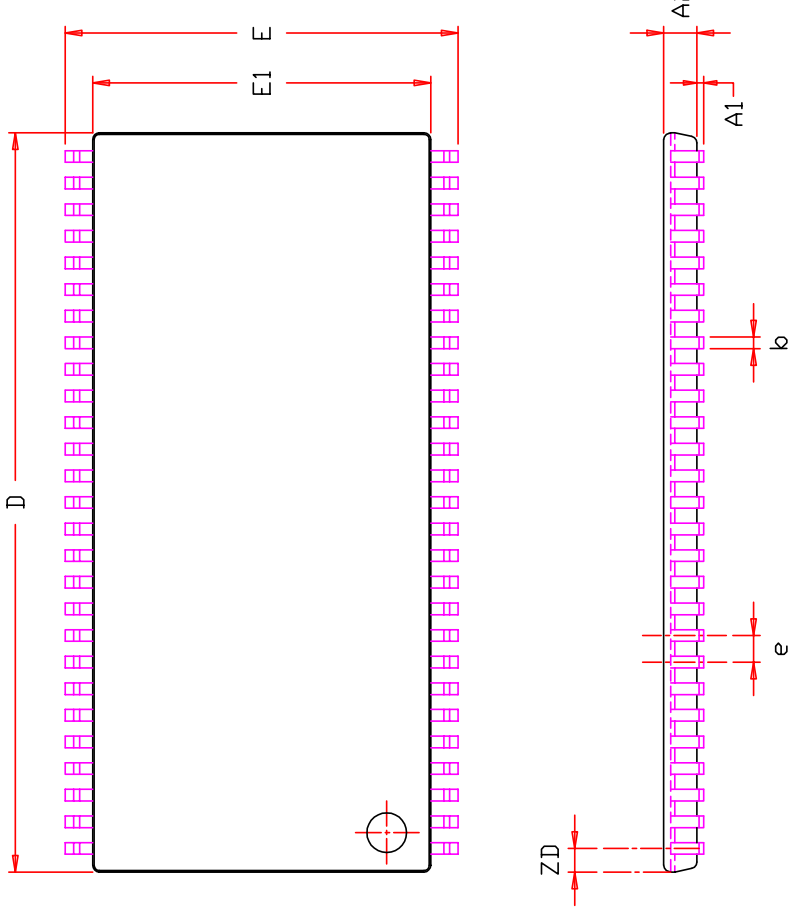
Industrial Range: (–40°C to 85°C)

Configuration	Frequency (MHz)	Speed (ns)	Order Part No.	Package
32Mx8	133	7.5	IS42VS83200J-75TLI	54-pin TSOP II, Lead-free
16Mx16	133	7.5	IS42VS16160J-75TLI	54-pin TSOP II, Lead-free
8Mx32	100	10	IS42VS32800J-10TLI	86-pin TSOP II, Lead-free

Note: Contact ISSI for leaded parts support.

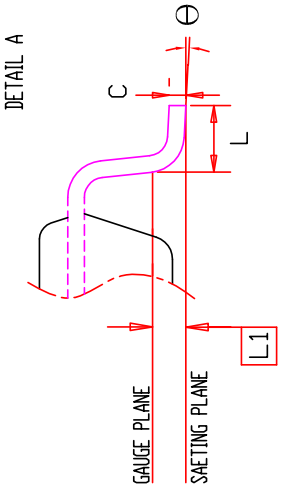
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012	—	0.018
C	0.12	—	0.21	0.005	—	0.008
D	22.02	22.22	22.42	0.867	0.875	0.883
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BSC.			0.010 BSC.		
ZD	0.71 REF.			0.028 REF.		
θ	0	—	8°	0	—	8°



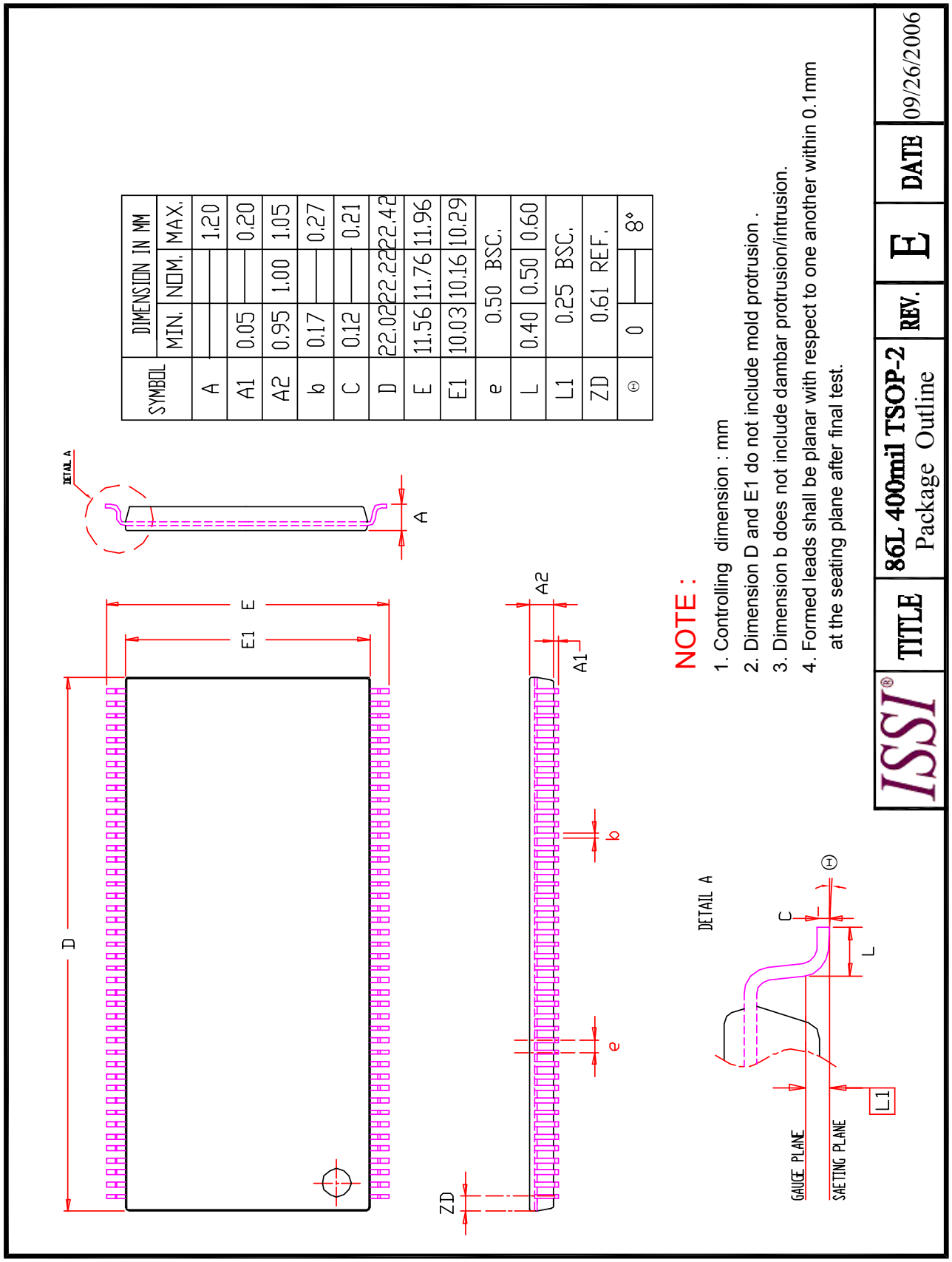


NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.



	TITLE	REV.	DATE
ISSI	54L 400mil TSOP-2 Package Outline	F	03/24/2009


SYMBOL
DIMENSION IN MM
MIN.
NOM.
MAX.
A — — 1.20
A1 0.05 — 0.20
A2 0.95 1.00 1.05
b 0.17 — 0.27
C 0.12 — 0.21
D 22.02 22.22 22.42
E 11.56 11.76 11.96
E1 10.03 10.16 10.29
e 0.50 BSC.
L 0.40 0.50 0.60
L1 0.25 BSC.
ZD 0.61 REF.
θ 0 — 8°
NOTE :
1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
ISSI
TITLE
86L 400mil TSOP-2 Package Outline
REV.
E
DATE
09/26/2006
DETAIL A
GAUGE PLANE
SEATING PLANE
L1
D
E
E1
A
A2
A1
b
e
ZD
C
L
θ