ANALOG DEVICES

Ethernet/Gigabit Ethernet Clock Generator

Data Sheet **AD9574**

FEATURES

Redundant input reference clock capability
Reference monitoring function
Fully integrated VCO/PLL core
Jitter (rms)
- **0.234 ps rms jitter (10 kHz to 10 MHz) at 156.25 MHz**
- **0.243 ps rms jitter (12 kHz to 20 MHz) at 156.25 MHz**

Input frequency: 19.44 MHz or 25 MHz
Preset frequency translations
- **Using a 19.44 MHz input reference**
  - **19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz**
- **Using a 25 MHz input reference**
  - **25 MHz, 33.33 MHz, 50 MHz, 66.67 MHz, 80 MHz, 100 MHz, 125 MHz, 133.3 MHz, 156.25 MHz, 160 MHz, 312.5 MHz**

Output drive formats: HSTL, LVDS, HCSL, and 1.8 V and 3.3 V CMOS
Integrated loop filter (requires a single external capacitor)
2 copies of reference clock output
Device configuration via strapping pins (PPRx)
Space-saving 7 mm × 7 mm 48-lead LFCSP
3.3 V operation

APPLICATIONS

Ethernet line cards, switches, and routers
SATA and PCI express
Low jitter, low phase noise clock generation

FUNCTIONAL BLOCK DIAGRAM

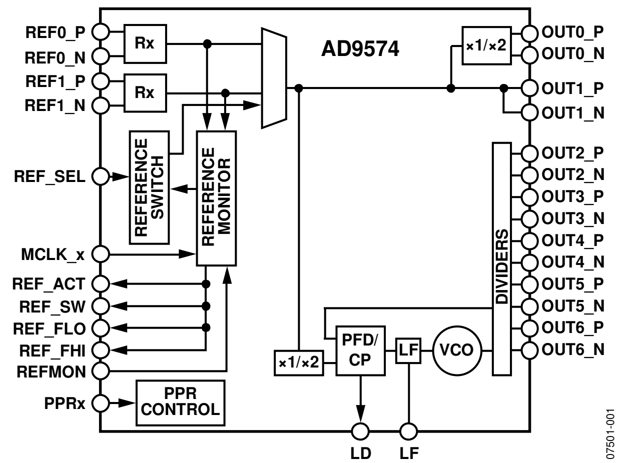

Figure 1.

GENERAL DESCRIPTION

The AD9574 provides a multiple output clock generator function comprising a dedicated phase-locked loop (PLL) core optimized for Ethernet and gigabit Ethernet line card applications. The integer-N PLL design is based on the Analog Devices, Inc., proven portfolio of high performance, low jitter frequency synthesizers to maximize network performance. The AD9574 also benefits other applications requiring low phase noise and jitter performance.

Configuring the AD9574 for a particular application requires only the connection of external pull-up or pull-down resistors to the appropriate pin program reader pins (PPRx). These pins provide control of the internal dividers for establishing the desired frequency translations, clock output functionality, and input reference functionality. Connecting an external 19.44 MHz or 25 MHz oscillator to one or both of the REF0_P/REF0_N or REF1_P/REF1_N reference inputs results in a set of output frequencies prescribed by the PPRx pins. Connecting a stable clock source (8 kHz/10 MHz/19.44 MHz/25 MHz/38.88 MHz) to the monitor clock input enables the optional monitor circuit providing quality of service (QoS) status for REF0 or REF1.

The PLL section consists of a low noise phase frequency detector (PFD), a precision charge pump (CP), a partially integrated loop filter (LF), a low phase noise voltage controlled oscillator (VCO), and feedback and output dividers. The divider values depend on the PPRx pins. The integrated loop filter requires only a single external capacitor connected to the LF pin.

The AD9574 is packaged in a 48-lead 7 mm × 7 mm LFCSP, requiring only a single 3.3 V supply. The operating temperature range is −40°C to +85°C.

Note that throughout this data sheet, OUT0 to OUT6, REF0, and REF1 refer to the respective channels, which consist of the differential pins, OUT0_P/OUT0_N to OUT6_P/OUT6_N, REF0_P/REF0_N, and REF1_P/REF1_N, respectively.

Rev. B Document Feedback

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9/2014—Revision 0: Initial Version

SPECIFICATIONS

OUT0 CHANNEL ABSOLUTE CLOCK JITTER

Typical values applicable under the conditions of V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HIGH SPEED TRANSCEIVER LOGIC (HSTL) INTEGRATED JITTER					Jitter integration bandwidth = 12 kHz to 5 MHz
19.44 MHz Output		0.196		ps rms	
25 MHz Output		0.179		ps rms	
38.88 MHz Output		1.943		ps rms	
50 MHz Output		1.523		ps rms	
3.3 V CMOS INTEGRATED JITTER					Jitter integration bandwidth = 12 kHz to 5 MHz
19.44 MHz Output		0.204		ps rms	
25 MHz Output		0.178		ps rms	
38.88 MHz Output		1.969		ps rms	
50 MHz Output		1.446		ps rms	

OUT1 CHANNEL ABSOLUTE CLOCK JITTER

Typical values applicable under the conditions of V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL INTEGRATED JITTER					Jitter integration bandwidth = 12 kHz to 5 MHz
19.44 MHz Output		0.175		ps rms	
25 MHz Output		0.153		ps rms	
3.3 V CMOS INTEGRATED JITTER					Jitter integration bandwidth = 12 kHz to 5 MHz
19.44 MHz Output		0.184		ps rms	
25 MHz Output		0.160		ps rms	

OUT2 AND OUT3 CHANNELS ABSOLUTE CLOCK JITTER

Typical values applicable under the conditions of V_S = 3.3 V, T_A = 25°C, unless otherwise noted. Frequency multiplier (×2) at PLL input enabled.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL INTEGRATED JITTER					
Jitter Integration Bandwidth = 10 kHz to 10 MHz					
155.52 MHz Output		0.244		ps rms	
156.25 MHz Output		0.234		ps rms	
160 MHz Output		1.290		ps rms	Frequency multiplier (×2) at PLL input bypassed
Jitter Integration Bandwidth = 12 kHz to 20 MHz					
155.52 MHz Output		0.470		ps rms	
156.25 MHz Output		0.243		ps rms	
160 MHz Output		1.329		ps rms	Frequency multiplier (×2) at PLL input bypassed
Jitter Integration Bandwidth = 1.875 MHz to 20 MHz					
155.52 MHz Output		0.409		ps rms	
156.25 MHz Output		0.100		ps rms	
160 MHz Output		1.257		ps rms	Frequency multiplier (×2) at PLL input bypassed

OUT4 AND OUT5 CHANNELS ABSOLUTE CLOCK JITTER

Typical values applicable under the conditions of V_S = 3.3 V, T_A = 25°C. Frequency multiplier (×2) at PLL input enabled unless otherwise indicated.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL INTEGRATED JITTER					Input = crystal oscillator
Jitter Integration Bandwidth = 10 kHz to 10 MHz					
38.88 MHz Output		0.251		ps rms	
77.76 MHz Output		0.245		ps rms	
80 MHz Output		1.267		ps rms	Frequency multiplier (×2) at PLL input bypassed
100 MHz Output		0.240		ps rms	
125 MHz Output		0.228		ps rms	
160 MHz Output		1.277		ps rms	Frequency multiplier (×2) at PLL input bypassed
312.5 MHz Output		0.234		ps rms	
Jitter Integration Bandwidth = 12 kHz to 20 MHz					
77.76 MHz Output		0.488		ps rms	
80 MHz Output		1.314		ps rms	Frequency multiplier (×2) at PLL input bypassed
100 MHz Output		0.252		ps rms	
125 MHz Output		0.233		ps rms	
160 MHz Output		1.321		ps rms	Frequency multiplier (×2) at PLL input bypassed
312.5 MHz Output		0.236		ps rms	
Jitter Integration Bandwidth = 50 kHz to 80 MHz					
312.5 MHz Output		0.389		ps rms	
Jitter Integration Bandwidth = 1.875 MHz to 20 MHz					
77.76 MHz Output		0.430		ps rms	
80 MHz Output		1.242		ps rms	Frequency multiplier (×2) at PLL input bypassed
100 MHz Output		0.115		ps rms	
125 MHz Output		0.089		ps rms	
160 MHz Output		1.248		ps rms	Frequency multiplier (×2) at PLL input bypassed
312.5 MHz Output		0.072		ps rms	
HIGH SPEED CURRENT SINKING LOGIC (HCSL) INTEGRATED JITTER					Input = crystal oscillator
Jitter Integration Bandwidth = 10 kHz to 10 MHz					
100 MHz Output		0.238		ps rms	
125 MHz Output		0.226		ps rms	
312.5 MHz Output		0.240		ps rms	
Jitter Integration Bandwidth = 12 kHz to 20 MHz					
100 MHz Output		0.255		ps rms	
125 MHz Output		0.233		ps rms	
312.5 MHz Output		0.243		ps rms	
Jitter Integration Bandwidth = 50 kHz to 80 MHz					
312.5 MHz Output		0.445		ps rms	
Jitter Integration Bandwidth = 1.875 MHz to 20 MHz					
100 MHz Output		0.131		ps rms	
125 MHz Output		0.098		ps rms	
312.5 MHz Output		0.082		ps rms	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) INTEGRATED JITTER					Input = crystal oscillator
Jitter Integration Bandwidth = 10 kHz to 10 MHz					
38.88 MHz Output		0.396		ps rms	
77.76 MHz Output		0.270		ps rms	
80 MHz Output		1.304		ps rms	Frequency multiplier (×2) at PLL input bypassed
100 MHz Output		0.247		ps rms	
125 MHz Output		0.234		ps rms	
160 MHz Output		1.314		ps rms	Frequency multiplier (×2) at PLL input bypassed
312.5 MHz Output		0.246		ps rms	
Jitter Integration Bandwidth = 12 kHz to 20 MHz					
77.76 MHz Output		0.529		ps rms	
80 MHz Output		1.360		ps rms	Frequency multiplier (×2) at PLL input bypassed
100 MHz Output		0.267		ps rms	
125 MHz Output		0.243		ps rms	
160 MHz Output		1.357		ps rms	Frequency multiplier (×2) at PLL input bypassed
312.5 MHz Output		0.249		ps rms	
Jitter Integration Bandwidth = 50 kHz to 80 MHz					
312.5 MHz Output		0.473		ps rms	
Jitter Integration Bandwidth = 1.875 MHz to 20 MHz					
77.76 MHz Output		0.474		ps rms	
80 MHz Output		1.289		ps rms	Frequency multiplier (×2) at PLL input bypassed
100 MHz Output		0.149		ps rms	
125 MHz Output		0.109		ps rms	
160 MHz Output		1.284		ps rms	Frequency multiplier (×2) at PLL input bypassed
312.5 MHz Output		0.082		ps rms	

OUT6 CHANNEL ABSOLUTE CLOCK JITTER

Typical values applicable under the conditions of V_S = 3.3 V, T_A = 25°C, unless otherwise noted. Frequency multiplier (×2) at PLL input enabled. Cycle to cycle jitter magnitude varies with respect to the clock edge (rising or falling). Table 5 entries indicate jitter for the worst edge (rising or falling). The better edge typically offers a factor of 2 improvement over the tabulated jitter.

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS CYCLE TO CYCLE JITTER					1000 cycles
66.6 MHz Output		210		ps p-p	
133.3 MHz Output		353		ps p-p	
1.8 V CMOS CYCLE TO CYCLE JITTER					1000 cycles
66.6 MHz Output		234		ps p-p	
133.3 MHz Output		363		ps p-p	
3.3 V CMOS CYCLE TO CYCLE JITTER					1000 cycles
33.3 MHz Output		28		ps p-p	
66.6 MHz Output		207		ps p-p	
133.3 MHz Output		360		ps p-p	

CLOCK OUTPUTS (OUT0_x TO OUT6_x)—STATIC

Typical is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL (OUT0_x TO OUT5_x ONLY)					100 Ω termination (differential)
Differential Output Voltage Swing	745	955	1235	mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage	745	950	1010	mV	Output driver static
HCSL (OUT4_x AND OUT5_x ONLY)					50 Ω from each output pin to GND
Differential Output Voltage Swing	570	700	830	mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage	295	360	430	mV	Output driver static
LVDS (OUT4_x TO OUT6_x ONLY)					100 Ω termination (differential)
Differential Output Voltage (V_{OD})	247	350	454	mV	Magnitude of voltage across pins; output driver static
Delta V_{OD}			50	mV	
Output Offset Voltage (V_{OS})	1.125	1.25	1.375	V	
Delta V_{OS}			50	mV	
Short-Circuit Current (I_{SA}, I_{SB})		14	24	mA	Output shorted to GND
1.8 V CMOS (OUT6_x ONLY)					
Output High Voltage (V_{OH})	1.7			V	I_{LOAD} = 1 mA
Output Low Voltage (V_{OL})			0.1	V	I_{LOAD} = 1 mA
3.3 V CMOS (OUT0_x, OUT1_x, AND OUT6_x ONLY)					
Output High Voltage (V_{OH})	V_{DD}[1] − 0.5			V	I_{LOAD} = 10 mA
Output Low Voltage (V_{OL})			0.5	V	I_{LOAD} = 10 mA

[1] V_{DD} is the supply of all VDD_x pins.

CLOCK OUTPUTS (OUT0_x TO OUT6_x)—DYNAMIC

Typical is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation. Rise and fall time measurement thresholds are 20% and 80% of the nominal low and high amplitude of the waveform.

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL (OUT1_x TO OUT5_x ONLY)					100 Ω termination (differential)
OUT0_x and OUT1_x					Measured differentially
Output Rise Time, t_{RL}	161	195	232	ps	
Output Fall Time, t_{FL}	164	193	226	ps	
OUT2_x to OUT5_x					Measured differentially
Output Rise Time, t_{RP}	114	144	175	ps	
Output Fall Time, t_{FP}	111	143	177	ps	
Duty Cycle					
OUT0_x and OUT1_x	45		55	%	Assumes 50% reference input duty cycle; duty cycle specification does not apply to OUT0_x for 38.88 MHz and 50 MHz operation
OUT2_x to OUT5_x	45		55	%	
HCSL (OUT4_x AND OUT5_x ONLY)					50 Ω from each output pin to GND
Output Rise Time, t_{RL}	195	206	221	ps	Measured differentially
Output Fall Time, t_{FL}	188	211	238	ps	Measured differentially
Duty Cycle	45		55	%	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS (OUT4_x TO OUT6_x ONLY)					100 Ω termination (differential)
OUT4_x, OUT5_x					
Output Rise Time, t_{RL}	151	193	238	ps	Measured differentially
Output Fall Time, t_{FL}	152	195	242	ps	Measured differentially
OUT6_x					
Output Rise Time, t_{RL}	221	242	273	ps	Measured differentially
Output Fall Time, t_{FL}	224	241	270	ps	Measured differentially
Duty Cycle					
OUT4_x, OUT5_x	45		55	%	
OUT6_x	45		55	%	
1.8 V CMOS (OUT6_x ONLY)					C_{LOAD} = 10 pF
Output Rise Time, t_{RC}		1.2	1.7	ns	
Output Fall Time, t_{FC}		1.2	1.8	ns	
Duty Cycle	45		55	%	
3.3 V CMOS (OUT0_x, OUT1_x, AND OUT6_x ONLY)					C_{LOAD} = 10 pF
Output Rise Time, t_{RC}		0.5	1.0	ns	
Output Fall Time, t_{FC}		0.6	1.1	ns	
Duty Cycle					
OUT0_x	45		55	%	Not applicable for 38.88 MHz and 50 MHz operation
OUT1_x	45		55	%	
OUT6_x	45		55	%	

MONITOR CLOCK INPUTS (MCLK_x)—STATIC

Typical is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL INPUT MODE					
Common-Mode Internally Generated Bias Voltage		1.192		V	
Common-Mode Voltage Tolerance	0.6		1.5	V	The acceptable common-mode range for a 200 mV p-p dc-coupled input signal
Differential Input Capacitance		2		pF	
Differential Input Resistance		5		kΩ	
SINGLE-ENDED INPUT CMOS MODE					
Hysteresis		230		mV	
Input Resistance		1		MΩ	
Input Capacitance		2		pF	
Input High Voltage	2			V	
Input Low Voltage			1.2	V	

MONITOR CLOCK INPUTS (MCLK_x)—DYNAMIC

Typical is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL INPUT MODE					
Input Sensitivity	100			mV p-p	
Minimum Input Slew Rate	50			V/µs	Ensures proper device function when using a sinusoidal source
Duty Cycle	40		60	%	
SINGLE-ENDED INPUT CMOS MODE					
Duty Cycle	40		60	%	

REFERENCE INPUTS (REF0_x AND REF1_x)—STATIC

Typical is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL INPUT MODE					
Common-Mode Internally Generated Bias Voltage		1.218		V	
Common-Mode Voltage Tolerance	0.650		1.8	V	The acceptable common-mode range for a 200 mV p-p dc-coupled input signal
Differential Input Capacitance		2		pF	
Differential Input Resistance		4.3		kΩ	
SINGLE-ENDED INPUT CMOS MODE					
Hysteresis		220		mV	
Input Resistance		1		MΩ	
Input Capacitance		2		pF	
Input High Voltage	2			V	
Input Low Voltage			1.2	V	

REFERENCE INPUTS (REF0_x AND REF1_x)—DYNAMIC

Typical is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL INPUT MODE					
Input Sensitivity	200			mV p-p	
Minimum Input Slew Rate	100			V/µs	Minimum limit imposed for jitter performance (when using a sinusoidal source, for example)
Duty Cycle					
PLL ×2 Multiplier Bypass	40		60	%	
PLL ×2 Multiplier Active	40		60	%	
OUT0 ×2 Multiplier Active	40		60	%	
SINGLE-ENDED INPUT CMOS MODE					
Duty Cycle					
PLL ×2 Multiplier Bypass	40		60	%	
PLL ×2 Multiplier Active	40		60	%	
OUT0 ×2 Multiplier Active	40		60	%	Ensures OUT0_x duty cycle limits with OUT0 ×2 multiplier enabled

REFERENCE SWITCHOVER OUTPUT DISTURBANCE

Typical is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INSTANTANEOUS FREQUENCY (dθ/dt) DISTURBANCE DUE TO REFERENCE SWITCHOVER		250	500	ppm pk	Applies only to PLL outputs; 1 ppm frequency offset between the REF0 and REF1 channels
INSTANTANEOUS PHASE DISTURBANCE DUE TO REFERENCE SWITCHOVER		220		ps	Applies to OUT0 and OUT1 with OUT0 ×2 multiplier bypassed

CONTROL PINS

Typical is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					
REF_SEL Pin					Internal 30 kΩ pull-down resistor
Logic 1 Voltage (V_{IH})	2.0			V	
Logic 0 Voltage (V_{IL})			0.8	V	
Logic 1 Current (I_{IH})			150	µA	$V_{IH} = V_{DD}$
Logic 0 Current (I_{IL})			150	µA	V_{IL} = GND
$\overline{\text{RESET}}$ Pin					Internal 30 kΩ pull-up resistor
Logic 1 Voltage (V_{IH})	2.0			V	
Logic 0 Voltage (V_{IL})			0.8	V	
Logic 1 Current (I_{IH})			350	µA	$V_{IH} = V_{DD}$
Logic 0 Current (I_{IL})			350	µA	V_{IL} = GND
REFMON Pin					Do not float this pin or toggle it during device operation; connect to a static Logic 0 or Logic 1
Logic 1 Voltage (V_{IH})	V_{DD} – 0.5			V	
Logic 0 Voltage (V_{IL})			0.5	V	
Logic 1 Current (I_{IH})			150	µA	$V_{IH} = V_{DD}$
Logic 0 Current (I_{IL})			150	µA	V_{IL} = GND
PPR0 to PPR6 Pins					Maximum resistor tolerance = 10%
PPRx State 0		820		Ω	Pull-down to GND
PPRx State 1		1800		Ω	Pull-down to GND
PPRx State 2		3900		Ω	Pull-down to GND
PPRx State 3		8200		Ω	Pull-down to GND
PPRx State 4		820		Ω	Pull-up to V_{DD}
PPRx State 5		1800		Ω	Pull-up to V_{DD}
PPRx State 6		3900		Ω	Pull-up to V_{DD}
PPRx State 7		8200		Ω	Pull-up to V_{DD}

STATUS PINS

Typical is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					I_{LOAD} = 1 mA (source or sink)
LD Pin					
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
REF_ACT Pin					
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
REF_SW Pin					
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
REF_FHI Pin					Internal 30 kΩ pull-down resistor
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
REF_FLO Pin					Internal 30 kΩ pull-down resistor
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	

POWER SUPPLY AND DISSIPATION

Typical is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY VOLTAGE	2.97	3.3	3.63	V	
POWER DISSIPATION					
Typical Configuration	466	569	654	mW	PPR0 State 0 (REF0_x: 25 MHz, 3.3 V CMOS buffer; REF1_x: no connection) PPR1 State 0 (PLL input ×2: off; OUT2: 156.25 MHz, HSTL; OUT3: 156.25 MHz, HSTL) PPR2 State 7 (OUT0: 25 MHz, HSTL, ×2 off; OUT1: disabled) PPR3 State 0 (OUT4: 100 MHz, HSTL; OUT5: 125 MHz, HSTL) PPR4 State 5 (OUT6: 66.67 MHz, 3.3 V CMOS) PPR5 State 0 (reference monitor threshold: not applicable (25 ppm)) PPR6 State 0 (MCLK_x: no connection (19.44 MHz differential)) REFMON: GND
All Blocks Running	579	698	803	mW	PPR0 State 4 (REF0_x: 25 MHz, differential; REF1_x: 25 MHz, differential) PPR1 State 0 (PLL input ×2: off; OUT2: 156.25 MHz, HSTL; OUT3: 156.25 MHz, HSTL) PPR2 State 2 (OUT0: 50 MHz, 3.3 V CMOS, ×2 on; OUT1: 25 MHz, 3.3 V CMOS) PPR3 State 2 (OUT4: 100 MHz, HCSL; OUT5: 125 MHz, HSTL) PPR4 State 1 (OUT6: 133.33 MHz, 3.3 V CMOS) PPR5 State 6 (reference monitor threshold: 100 ppm) PPR6 State 4 (MCLK_x: 38.88 MHz, differential) REFMON: V_{DD}

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Minimal Power Configuration	346	422	486	mW	PPR0 State 0 (REF0_x: 19.44 MHz, 3.3 V CMOS buffer; REF1_x: 19.44 MHz, 3.3 V CMOS buffer)
					PPR1 State 4 (PLL input ×2: off, OUT2: 155.52 MHz, HSTL; OUT3: 155.52 MHz, HSTL)
					PPR2 State 4 (OUT0: disabled; OUT1: disabled)
					PPR3 State 7 (OUT4: disabled; OUT5: disabled)
					PPR4 State 0 (OUT6: disabled)
					PPR5 State 0 (reference monitor threshold: not applicable (25 ppm)
					PPR6 State 1 (MCLK_x: no connection (19.44 MHz, 3.3 V CMOS buffer))
					REFMON: GND
Incremental Power Dissipation					Typical configuration; values show the change in power due to the indicated operation
Input Reference On/Off					Applies to one reference clock input
Single-Ended	0.23	0.30	0.36	mW	
Differential	20.5	25.1	30.0	mW	
Output Driver On/Off					
LVDS (at 312.5 MHz)	18.1	22.5	27.2	mW	
HSTL (at 156.25 MHz)	30.6	36.6	42.5	mW	
1.8 V CMOS (at 66 MHz)	13.7	16.2	19.2	mW	A single 1.8 V CMOS output with an 10 pF load
3.3 V CMOS (at 25 MHz)	9.5	12.2	15.2	mW	A single 3.3 V CMOS output with an 10 pF load
Other Blocks On/Off					
OUT0 ×2 On/Off	3.1	4.0	5.4	mW	
POWER SUPPLY CURRENT (I_{SUPPLY})					Total supply current for VDD_x pins[1] in aggregate
Typical Configuration	157	172	180	mA	For power dissipation with typical configuration settings
All Blocks Running Configuration	195	212	221	mA	For power dissipation with all blocks running configuration settings
Minimal Power Configuration	117	128	134	mA	For power dissipation with minimal power configuration settings

[1] VDD_x pins include VDD_REF0, VDD_REF1, VDD_OUT01, VDD_PLL, VDD_VCO, VDD_RFDIV, VDD_OUT6, VDD_OUT4, VDD_OUT5, VDD_OUT23, and VDD_MCLK.

TIMING SPECIFICATIONS

Typical is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation. The indicated times assume the voltage applied to all 3.3 V power supply pins is within specification and stable.

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MONITOR CLOCK INPUT TO REF_FHI/REF_FLO TIME					Elapsed time from the first rising edge of the monitor clock input signal to the valid reference status as indicated by the REF_FHI and REF_FLO pins (the active reference must be stable)
f_{MCLK} = 8 kHz			4200	ms	
f_{MCLK} = 10 MHz			3400	ms	
f_{MCLK} = 19.44 MHz			1800	ms	
f_{MCLK} = 25 MHz			1400	ms	
f_{MCLK} = 38.88 MHz			870	ms	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT READY TIME					
OUT0 to OUT1		0.2		ms	Typical start-up time of the external crystal oscillator dominates the output ready time of the OUT0 and OUT1 channels
OUT2 to OUT6					Time interval from $\overline{\text{RESET}}$ pin = Logic 1 to LD pin = Logic 1 (PLL lock detection)
PPR1 State 0		5.0		ms	
PPR1 State 1		2.8		ms	
PPR1 State 2		5.0		ms	
PPR1 State 3		2.8		ms	
PPR1 State 4		6.4		ms	
PPR1 State 5		3.6		ms	
PPR1 State 6		22.3		ms	
PPR1 State 7		11.5		ms	

TIMING DIAGRAMS

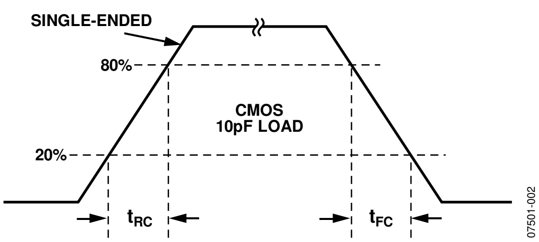


Figure 2. CMOS Timing, Single-Ended, 10 pF Load

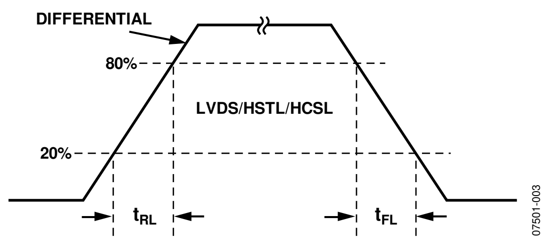


Figure 3. LVDS, HSTL, HCSL Timing, Differential

ABSOLUTE MAXIMUM RATINGS

Table 17.

Parameter	Rating
VDD_x to GND	−0.3 V to +3.6 V
Junction Temperature[1]	150°C
Storage Temperature Range	−65°C to +150°C

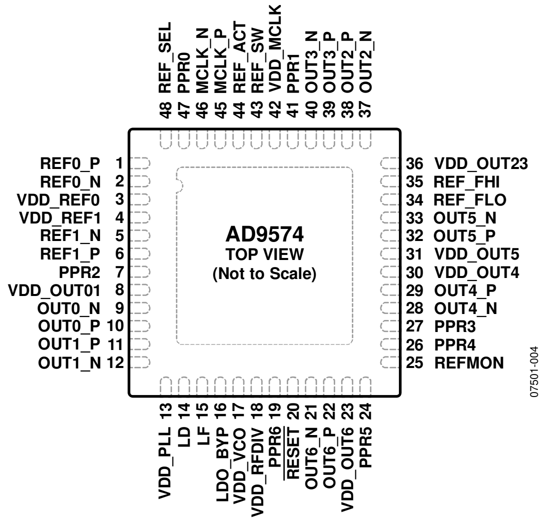
[1] See the Thermal Performance section for details on junction temperature.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED DIE PAD MUST BE CONNECTED TO THE POWER SUPPLY COMMON (GND).

Figure 4. Pin Configuration

Table 18. Pin Function Descriptions

Pin No.	Mnemonic	Input/Output	Pin Type	Description
1	REF0_P	Input	Configurable clock input	Reference Clock Input 0, Positive. Configurable via PPR0 (Pin 47).
2	REF0_N	Input	Configurable clock input	Reference Clock Input 0, Negative. Configurable via PPR0 (Pin 47).
3	VDD_REF0	Input	Power	3.3 V Input Supply for Reference Clock Input 0 (REF0_x). This pin supplies the single-ended input receiver and internal low dropout (LDO) regulator for the differential receiver.
4	VDD_REF1	Input	Power	3.3 V Input Supply for Reference Clock Input 1 (REF1_x). This pin supplies the single-ended input receiver and internal LDO regulator for the differential receiver.
5	REF1_N	Input	Configurable clock input	Reference Clock Input 1, Negative. Configurable via PPR0 (Pin 47).
6	REF1_P	Input	Configurable clock input	Reference Clock Input 1, Positive. Configurable via PPR0 (Pin 47).
7	PPR2	Input	Control	Pin Program Reader 2. Connect a resistor to this pin to configure the OUT0 and OUT1 channels (see the PPR2—OUT0 and OUT1 Configuration section for more information).
8	VDD_OUT01	Input	Power	3.3 V Supply. 3.3 V input for the CMOS drivers of OUT0_x and OUT1_x and the source for an internal 1.8 V LDO regulator for the differential drivers of OUT0_x and OUT1_x.
9	OUT0_N	Output	Configurable clock output	Clock Output 0, Negative. Configurable via PPR2 (Pin 7).
10	OUT0_P	Output	Configurable clock output	Clock Output 0, Positive. Configurable via PPR2 (Pin 7).
11	OUT1_P	Output	Configurable clock output	Clock Output 1, Positive. Configurable via PPR2 (Pin 7).
12	OUT1_N	Output	Configurable clock output	Clock Output 1, Negative. Configurable via PPR2 (Pin 7).
13	VDD_PLL	Input	Power	3.3 V Input to the Internal LDO Regulator for the PLL.
14	LD	Output	3.3 V CMOS	PLL Lock Detector Status. Logic 0 = unlocked; Logic 1 = locked.
15	LF	Input/Output	Analog	Loop Filter. Connect a capacitor or series RC network (see Table 32) from this pin to LDO_BYP (Pin 16).
16	LDO_BYP	Output	Analog	LDO Bypass. Connect a 470 nF capacitor from this pin to GND.

Pin No.	Mnemonic	Input/Output	Pin Type	Description
17	VDD_VCO	Input	Power	3.3 V Supply. 3.3 V input to the internal LDO regulator for the VCO.
18	VDD_RFDIV	Input	Power	3.3 V Supply. 3.3 V input to the internal LDO regulator for the VCO RF dividers.
19	PPR6	Input	Control	Pin Program Reader 6. Connect a resistor to this pin to configure the MCLK_x input (see the PPR6—Monitor Clock (MCLK_x) Input Configuration section for more information).
20	$\overline{\text{RESET}}$	Input	3.3 V CMOS	Reset. Logic 0 (GND) initializes the device to its default state (see the PPRx Pins section for details). This pin has an internal 30 kΩ pull-up resistor.
21	OUT6_N	Output	Configurable clock output	Clock Output 6, Negative. Configurable via PPR4 (Pin 26).
22	OUT6_P	Output	Configurable clock output	Clock Output 6, Positive. Configurable via PPR4 (Pin 26).
23	VDD_OUT6	Input	Power	3.3 V Supply. 3.3 V input for the CMOS drivers of OUT6_x and the source for an internal 1.8 V LDO regulator for the 1.8 V CMOS drivers and differential drivers of OUT6_x.
24	PPR5	Input	Control	Pin Program Reader 5. Connect a resistor to this pin to configure the reference clock frequency error threshold (see the PPR5—Reference Monitor Threshold section for more information).
25	REFMON	Input	Control	Reference Frequency Monitor Enable/Disable. Do not float this pin or toggle it during device operation. Connect it to a static Logic 0 or Logic 1.
26	PPR4	Input	Control	Pin Program Reader 4. Connect a resistor to this pin to configure the OUT6 channel (see the PPR4—OUT6 Configuration section for more information).
27	PPR3	Input	Control	Pin Program Reader 3. Connect a resistor to this pin to configure the OUT4 and OUT5 channels (see the PPR3—OUT4 and OUT5 Configuration section for more information).
28	OUT4_N	Output	Configurable clock output	Clock Output 4, Negative. Configurable via PPR3 (Pin 27).
29	OUT4_P	Output	Configurable clock output	Clock Output 4, Positive. Configurable via PPR3 (Pin 27).
30	VDD_OUT4	Input	Power	3.3 V Supply. 3.3 V input for an internal 1.8 V LDO regulator for the differential drivers of OUT4_x.
31	VDD_OUT5	Input	Power	3.3 V Supply. 3.3 V input for an internal 1.8 V LDO regulator for the differential drivers of OUT5_x.
32	OUT5_P	Output	Configurable clock output	Clock Output 5, Positive. Configurable via PPR3 (Pin 27).
33	OUT5_N	Output	Configurable clock output	Clock Output 5, Negative. Configurable via PPR3 (Pin 27).
34	REF_FLO	Output	3.3 V CMOS	Low Reference Frequency Status Indicator. A Logic 1 indicates that the reference frequency is below the lower threshold limit (see the Reference Monitor section for details). This pin is an open-drain output with an internal 30 kΩ pull-down resistor.
35	REF_FHI	Output	3.3 V CMOS	High Reference Frequency Status Indicator. A Logic 1 indicates that the reference frequency is above the upper threshold limit (see the Reference Monitor section for details). This pin is an open-drain output with an internal 30 kΩ pull-down resistor.
36	VDD_OUT23	Input	Power	3.3 V Supply. 3.3 V input for an internal 1.8 V LDO regulator for the differential drivers of OUT2_x and OUT3_x.
37	OUT2_N	Output	Configurable clock output	Clock Output 2, Negative (HSTL). Configurable via PPR2 (Pin 7).
38	OUT2_P	Output	Configurable clock output	Clock Output 2, Positive (HSTL). Configurable via PPR2 (Pin 7).
39	OUT3_P	Output	Configurable clock output	Clock Output 3, Positive (HSTL). Configurable via PPR2 (Pin 7).
40	OUT3_N	Output	Configurable clock output	Clock Output 3, Negative (HSTL). Configurable via PPR2 (Pin 7).
41	PPR1	Input	Control	Pin Program Reader 1. Connect a resistor to this pin to select a predefined frequency translation configuration (see the PPR1—Frequency Translation Settings section for more information).
42	VDD_MCLK	Input	Power	3.3 V Supply. 3.3 V input for Reference Monitor Clock 0 (MCLK_x). This pin supplies the single-ended input receiver and internal LDO regulator for the differential receiver.

Pin No.	Mnemonic	Input/Output	Pin Type	Description
43	REF_SW	Output	3.3 V CMOS	Reference Switchover Status Indicator. This pin indicates when the device is in the process of switching references (see the Reference Monitor section for more information).
44	REF_ACT	Output	3.3 V CMOS	Reference Active Status Indicator. This pin indicates whether REF0 or REF1 is the active reference (see the Reference Monitor section for more information).
45	MCLK_P	Input	Configurable monitor clock input	Reference Monitor Clock Normal Input. Configurable via PPR6 (Pin 18).
46	MCLK_N	Input	Configurable monitor clock input	Reference Monitor Clock Complementary Input. Configurable via PPR6 (Pin 18).
47	PPR0	Input	Control	Pin Program Reader 0. Connect a resistor to this pin to configure the reference clock inputs (see the PPR0—Reference Clock Input Configuration section for more information).
48	REF_SEL	Input	3.3 V CMOS	Reference Clock Select. The pin selects Input Reference Clock 0 or Input Reference Clock 1 as the internal reference clock source (Logic 0 or Logic 1, respectively). This pin has an internal 30 kΩ pull-down resistor.
	EP	Input	GND	Exposed Pad. The exposed die pad must be connected to the power supply common (GND).

TYPICAL PERFORMANCE CHARACTERISTICS

PHASE NOISE AND VOLTAGE WAVEFORMS

V_{DD} = nominal, T_A = 25°C. The only enabled output channels are those indicated in the figure captions. The phase noise plots (see Figure 5 to Figure 9) show the Taitien XO A0145-L-006-3 phase noise normalized to the output frequency. The voltage waveform plots (see Figure 10 to Figure 16) embody ac coupling to the measurement instrument.

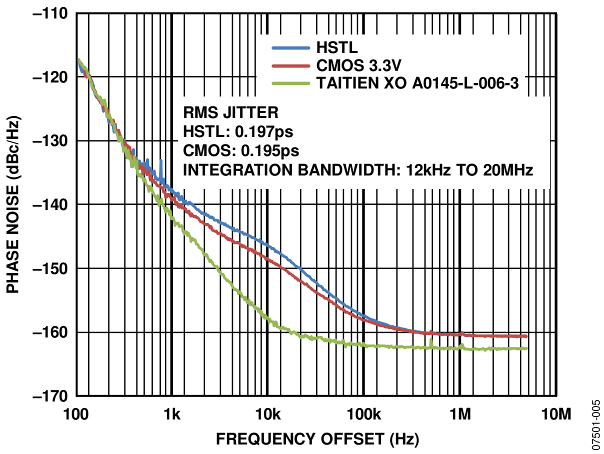


Figure 5. Phase Noise (OUT0)—f_{OUT0} = 25 MHz

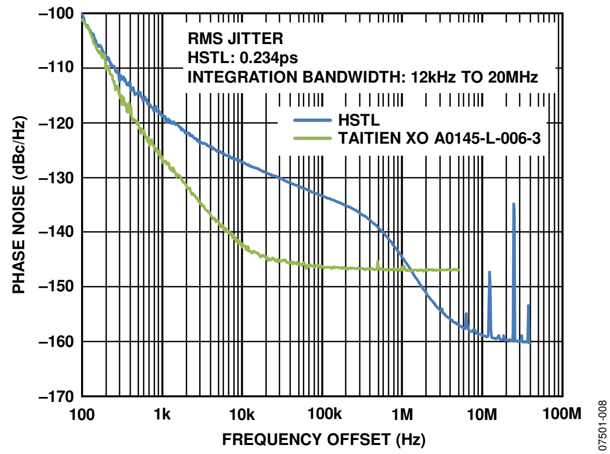


Figure 8. Phase Noise (OUT2)—f_{OUT2} = 156.25 MHz

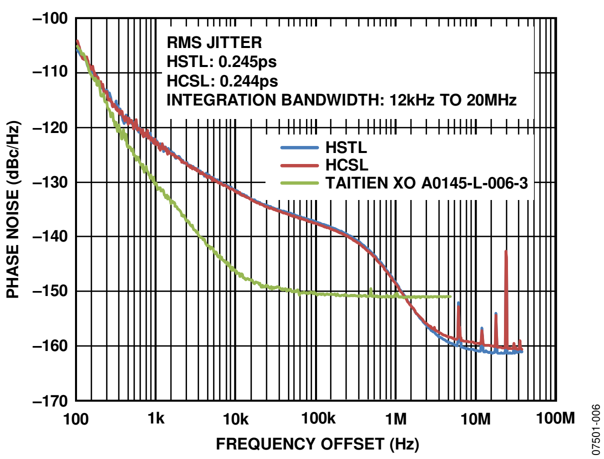


Figure 6. Phase Noise (OUT4)—f_{OUT4} = 100 MHz, f_{OUT5} = 125 MHz

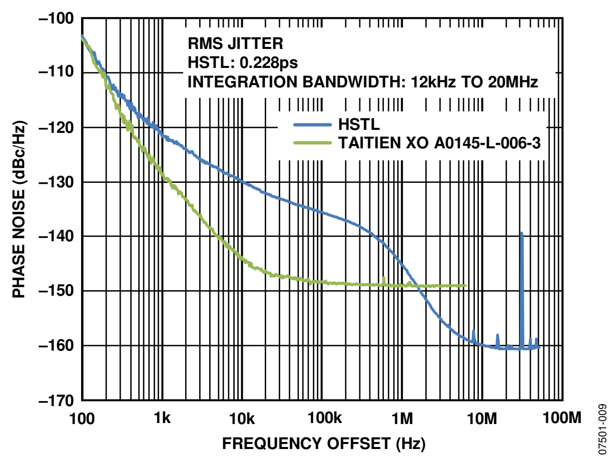


Figure 9. Phase Noise (OUT5)—f_{OUT4} = 100 MHz, f_{OUT5} = 125 MHz

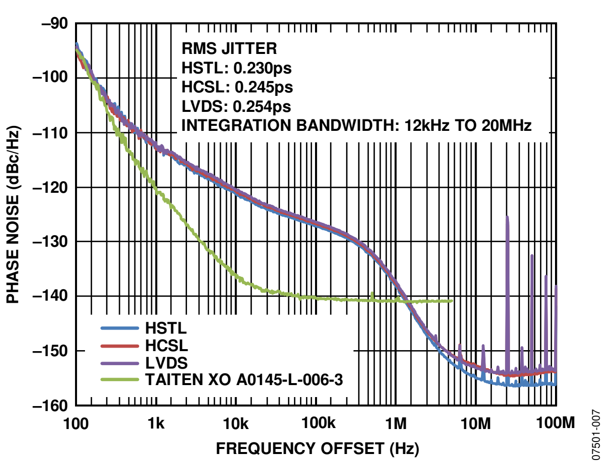


Figure 7. Phase Noise (OUT4)—f_{OUT4} = 312.5 MHz

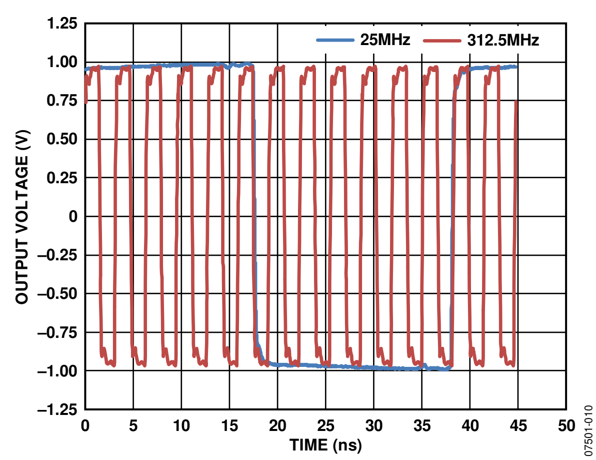


Figure 10. Output Waveform, HSTL (25 MHz, 312.5 MHz)

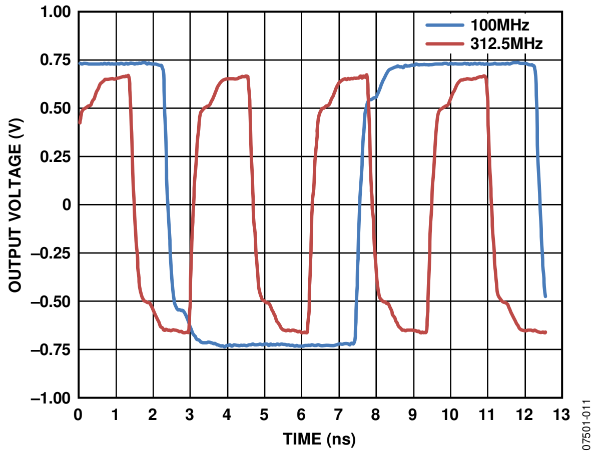


Figure 11. Output Waveform, HCSL (100 MHz, 312.5 MHz)

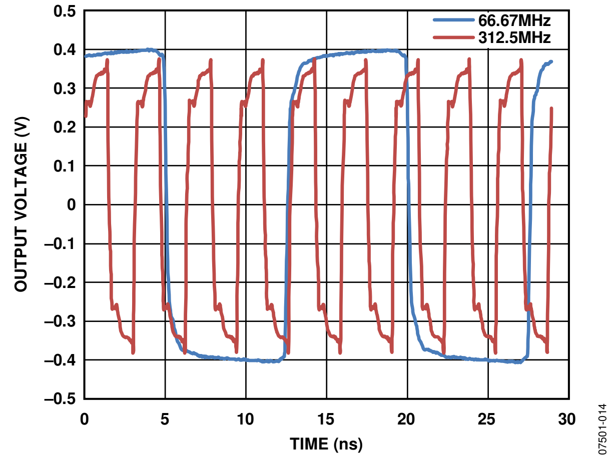


Figure 14. Output Waveform, LVDS (66.67 MHz, 312.5 MHz)

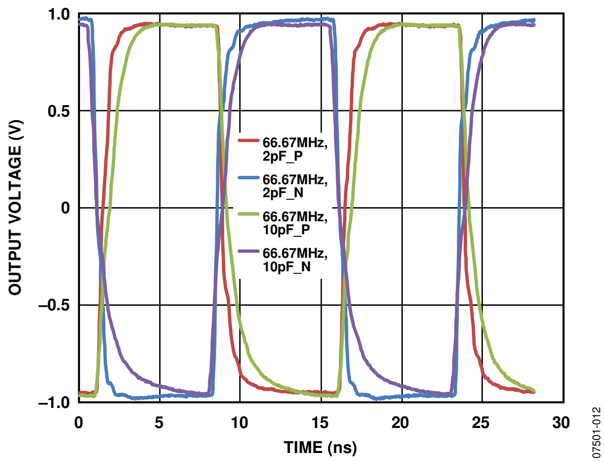


Figure 12. Output Waveform, 1.8 V CMOS (66.67 MHz)

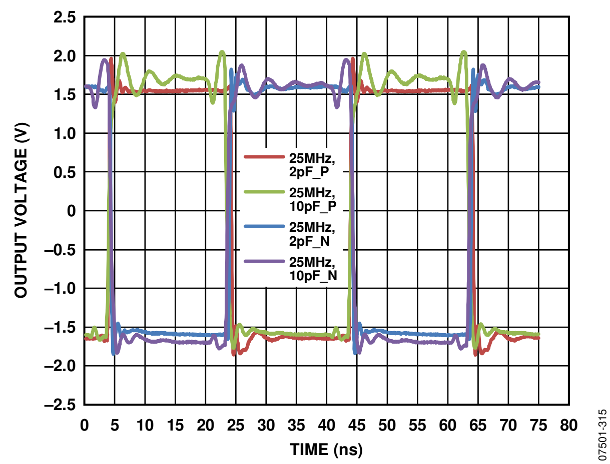


Figure 15. Output Waveform, 3.3 V CMOS (25 MHz)

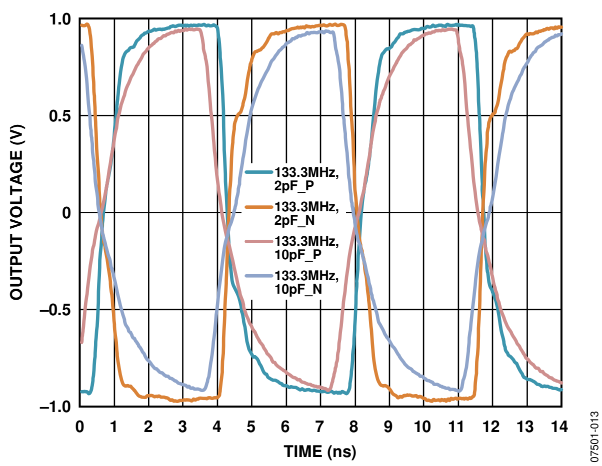


Figure 13. Output Waveform, 1.8 V CMOS (133.3 MHz)

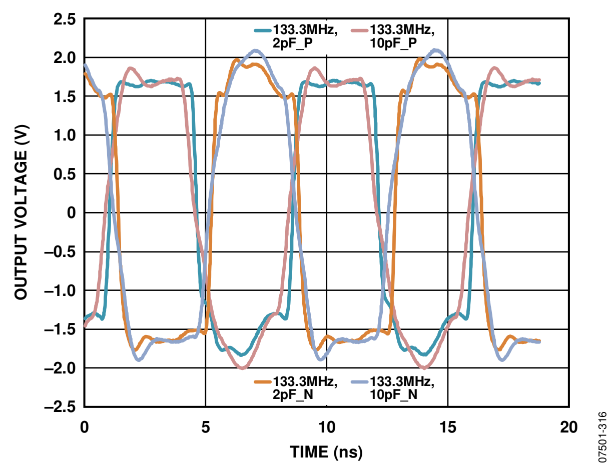


Figure 16. Output Waveform, 3.3 V CMOS (133.3 MHz)

REFERENCE SWITCHING FREQUENCY AND PHASE DISTURBANCE

V_{DD} = nominal, T_A = 25°C. The only enabled output channels are those indicated in the figure captions. The reference switchover phase disturbance plots (see Figure 18 and Figure 19) each show a collection of output phase variations due to approximately 250 reference switching events between two references with a frequency offset of approximately 2 ppm. Each reference switch event (initiated by toggling the REF_SEL pin) occurs at a random phase offset between the two references. The plots demonstrate the tightly controlled phase disturbance at the output as a result of the reference switching logic seeking the optimal moment to switch references.

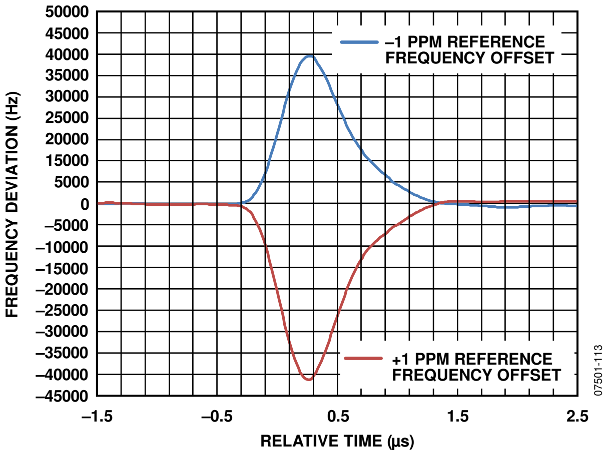


Figure 17. Reference Switchover Frequency Disturbance for OUT2 at 156.25 MHz (PPR0 = 0, PPR1 = 1, PPR2 = 2, PPR3 = 0, PPR4 = 0, PPR5 = 0, PPR6 = 2)

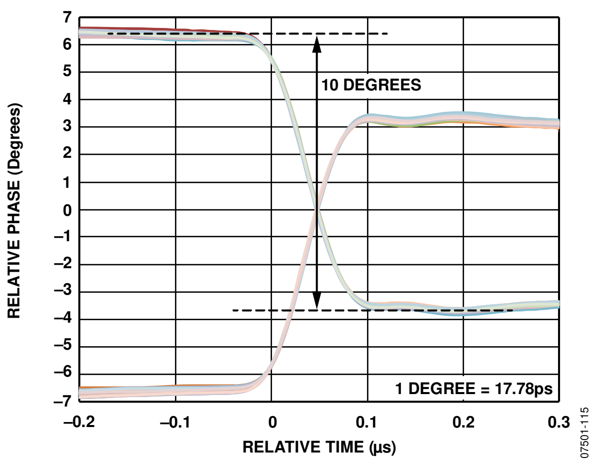


Figure 18. Reference Switchover Phase Disturbance for OUT3 at 156.25 MHz (PPR0 = 0, PPR1 = 1, PPR2 = 3, PPR3 = 2, PPR4 = 1, PPR5 = 7, PPR6 = 7)

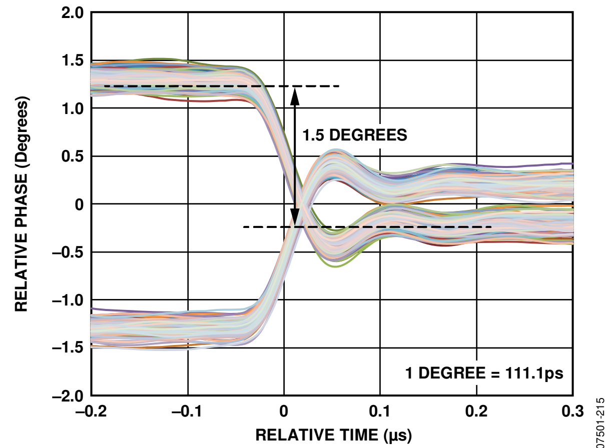


Figure 19. Reference Switchover Phase Disturbance for OUT0 at 25 MHz with Output ×2 Multiplier Bypassed (PPR0 = 0, PPR1 = 1, PPR2 = 3, PPR3 = 2, PPR4 = 1, PPR5 = 7, PPR6 = 7)

TERMINOLOGY

Phase Jitter

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as Gaussian (normal) in distribution.

This phase jitter leads to the energy of the sine wave spreading out in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in dB) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

Phase Noise

When the total power contained within some interval of offset frequencies (for example, 12 kHz to 20 MHz) is integrated, it is called the integrated phase noise over that frequency offset interval, and it can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on error rate performance by increasing eye closure at the transmitter output and reducing the jitter tolerance/sensitivity of the receiver.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings is seen to vary. In a square wave, the time jitter is seen as a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in units of seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Additive Phase Noise

Additive phase noise is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise.

Additive Time Jitter

Additive time jitter is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

THEORY OF OPERATION

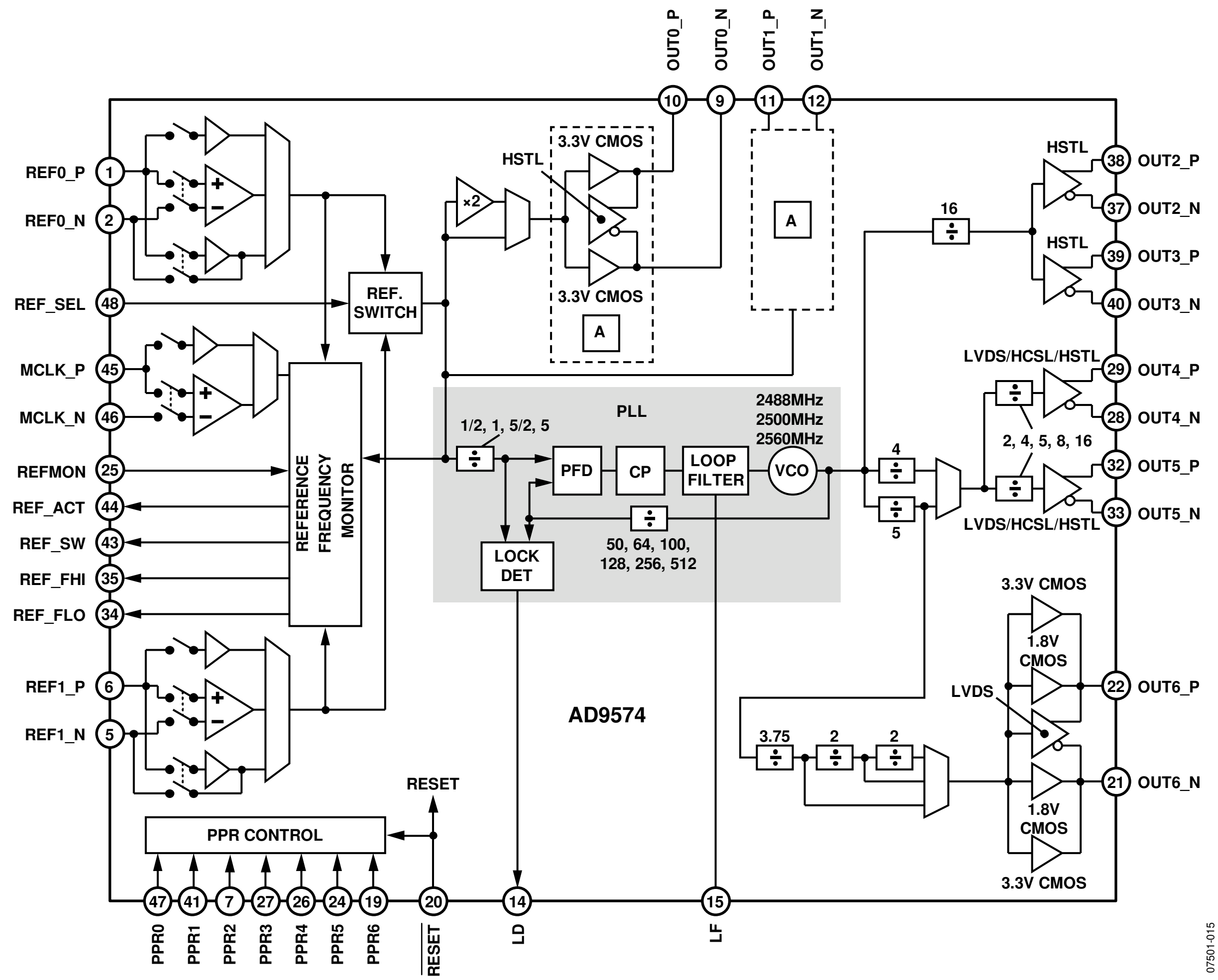


Figure 20. Detailed Block Diagram

OVERVIEW

Figure 20 shows a block diagram of the AD9574. The AD9574 accepts a 19.44 MHz or 25 MHz reference clock at the REF0_x and/or REF1_x inputs. It also accepts a 0.008 MHz, 10 MHz, 19.44 MHz, 25 MHz, or 38.88 MHz monitor input clock at the MCLK_x input. The monitor input clock serves as a stable frequency reference for the internal reference frequency monitor of the device. The input clock receivers provide differential or single-ended input configurations.

The AD9574 provides up to seven output channel clocks (OUT0 to OUT6). The OUT0 and OUT1 channels provide a replica of the REF0 or REF1 channel frequency with a frequency doubling option for OUT0. The OUT2 through OUT6 channels provide various output frequencies by means of an integrated PLL and divider chains. The output clock drivers provide for a variety of modes including LVDS, HSTL, HCSL, 1.8 V CMOS, and 3.3 V CMOS, although not all modes are available at every output.

The integrated PLL provides the necessary frequency translations. The divider block at the input to the PLL consists of a ×2 multiplier, a divide-by-5, and a multiplexer configured to provide the four possible divide values (1/2, 1, 5/2, or 5), as shown in Figure 20.

PPRx PINS

The AD9574 makes use of seven PPRx pins to configure the device. Internal circuitry scans the PPRx pins for the presence of resistor terminations and configures the device accordingly. A PPRx pin scan occurs automatically as part of the power-on reset sequence (see the Power-On Reset (POR) section) or following assertion of the RESET pin.

Each PPRx pin controls a specific function or functional block within the device (see Table 19). The configuration of a functional block depends on the scanned state of the corresponding PPRx pin. The scan of a PPRx pin identifies one of eight possible states based on an external pull-up or pull-down resistor (maximum 10% tolerance) per Table 20.

Table 19. PPRx Pin Function Assignments

Mnemonic	Pin No.	Function Assignment
PPR0	47	Reference input configuration
PPR1	41	Frequency translation settings
PPR2	7	OUT0 and OUT1 channel configuration
PPR3	27	OUT4 and OUT5 channel configuration
PPR4	26	OUT6 channel configuration
PPR5	24	Reference clock frequency monitor error threshold
PPR6	19	Monitor clock (MCLK_x) input configuration

Device programming consists of connecting the appropriate value programming resistors to the PPRx pins and terminating the resistors to V_{DD} or GND (per Table 20). For example, Figure 21 shows how to program PPR0 to State 3.

Table 20. PPRx State

PPRx State	Resistance	Terminus
0	820 Ω	GND
1	1.8 kΩ	GND
2	3.9 kΩ	GND
3	8.2 kΩ	GND
4	820 Ω	V_{DD}
5	1.8 kΩ	V_{DD}
6	3.9 kΩ	V_{DD}
7	8.2 kΩ	V_{DD}

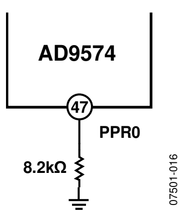


Figure 21. PPRx Programming Resistor Example

For details regarding the device configuration based on the scanned PPRx states, see the description of each PPRx pin in the following sections.

PPR0—Reference Clock Input Configuration

The PPR0 pin controls the configuration of the reference clock inputs (REF0_x and REF1_x). The selected PPR0 state applies to both references (REF0_x and REF1_x). Table 21 associates each PPR0 state with a particular reference input configuration.

Table 21. PPR0—Reference Input Options

PPR0 State	Reference Clock Input Configuration
0	Single-ended 3.3 V CMOS buffer
1	Not applicable
2	Not applicable
3	Not applicable
4	Differential
5	Not applicable
6	Not applicable
7	Not applicable

PPR1—Frequency Translation Settings

The PPR1 pin allows the user to select from a predefined set of frequency translation groups per Table 22 (with all frequency entries in MHz). The frequency translations apply to the OUT4 and OUT5 channels with respect to the reference frequency (f_{REF}) at the REF0_x or REF1_x inputs. This also establishes the frequency at the OUT2 and OUT3 channels, as shown in Table 22. Note that the frequency translation associated with each PPRx state relies on one of three possible VCO frequencies shown in Table 22. The ×2 column in Table 22 indicates the status of the ×2 multiplier associated with the divider at the input to the PLL (as explained in the Overview section). The PLL bandwidth column indicates the −3 dB closed-loop bandwidth of the PLL.

The frequency group for a given PPR1 state defines a pair of OUT4 and OUT5 frequencies. The frequency pair associated with a PPR1 state may apply to the OUT4 or OUT5 channel in any combination. For example, although PPR1 State 0 defines both 100 MHz and 125 MHz output frequencies, OUT4 and OUT5 may be any pairing of the two frequencies: 100 MHz at both output channels, 100 MHz on OUT4 and 125 MHz at OUT5, 125 MHz at OUT4 and 100 MHz at OUT5, or 125 MHz at both output channels. The specific OUT4 and OUT5 frequency assignments depend on the state of PPR3 (see Table 24). See the Output Clocks section for details for the specific frequency translations on a per output basis.

Table 22. PPR1—Frequency Translation Options

PPR1 State	f_{REF} (MHz)	OUT4/OUT5 Frequency (MHz)	×2	PLL Bandwidth (MHz)	f_{VCO}	OUT2/OUT3 Frequency (MHz)
0	25	100, 125	Bypass	0.7	2500	156.25
1	25	100,125	Active	0.6	2500	156.25
2	25	125, 312.5	Bypass	0.7	2500	156.25
3	25	125, 312.5	Active	0.6	2500	156.25
4	19.44	38.88, 77.76	Bypass	0.6	2488	155.52
5	19.44	38.88, 77.76	Active	0.6	2488	155.52
6	25	80, 160	Bypass	0.3	2560	160
7	25	80, 160	Active	0.6	2560	160

PPR2—OUT0 and OUT1 Configuration

The PPR2 pin allows the user to select from a predefined set of configurations for the OUT0 and OUT1 channels per Table 23. The output configuration includes the type of output driver and a frequency scale factor that indicates whether the output frequency is the same or twice the input reference frequency. See the Output Drivers section for details regarding output driver types.

PPR3—OUT4 and OUT5 Configuration

The PPR3 pin allows the user to select from a predefined set of configurations for the OUT4 and OUT5 channels per Table 24. The output configuration includes the frequency (in MHz) and type of output driver assignment (see the Output Drivers section for details regarding output driver types). Note that the state of PPR1 (frequency translation options) determines the frequency pair available for assignment to the OUT4 and OUT5 channels.

Table 23. PPR2—OUT0/OUT1 Options

	OUT0		OUT1	
PPR2 State	**Driver**	**Scale**	**Driver**	**Scale**
0	HSTL	1	HSTL	1
1	HSTL	2	HSTL	1
2	3.3 V CMOS	2	3.3 V CMOS	1
3	3.3 V CMOS	1	3.3 V CMOS	1
4	Disabled	Not applicable	Disabled	Not applicable
5	3.3 V CMOS	1	Disabled	Not applicable
6	HSTL	2	Disabled	Not applicable
7	HSTL	1	Disabled	Not applicable

Table 24. PPR3—OUT4/OUT5 Options

PPR State		OUT4		OUT5	
PPR1	**PPR3**	**Driver**	**f_{OUT4} (MHz)**	**Driver**	**f_{OUT5} (MHz)**
0 or 1	0	HSTL	100	HSTL	125
	1	HCSL	100	HCSL	100
	2	HCSL	100	HSTL	125
	3	LVDS	125	LVDS	125
	4	HSTL	125	HSTL	125
	5	LVDS	100	HCSL	100
	6	HSTL	100	HSTL	100
	7	Disabled	Not applicable	Disabled	Not applicable
2 or 3	0	HSTL	312.5	HSTL	312.5
	1	LVDS	312.5	LVDS	312.5
	2	HCSL	312.5	HCSL	312.5
	3	HSTL	312.5	HSTL	125
	4	LVDS	312.5	LVDS	125
	5	HCSL	312.5	HCSL	125
	6	LVDS	312.5	HSTL	125
	7	HCSL	125	HCSL	125
4 or 5	0	HSTL	38.88	HSTL	77.76
	1	LVDS	38.88	LVDS	77.76
	2	LVDS	38.88	LVDS	38.88
	3	HSTL	38.88	HSTL	38.88
	4	HSTL	77.76	HSTL	77.76
	5	LVDS	77.76	LVDS	77.76
	6	Disabled	Not applicable	HSTL	38.88
	7	Disabled	Not applicable	Disabled	Not applicable
6 or 7	0	HSTL	80	HSTL	80
	1	LVDS	80	HSTL	80
	2	LVDS	80	LVDS	160
	3	Disabled	Not applicable	HSTL	80
	4	LVDS	80	LVDS	80
	5	HSTL	80	HSTL	160
	6	Disabled	Not applicable	HSTL	160
	7	Disabled	Not applicable	Disabled	Not applicable

PPR4—OUT6 Configuration

The PPR4 pin allows the user to select from a predefined set of configurations for the OUT6 channel per Table 25. The output configuration includes the frequency (MHz) and type of output driver assignment (see the Output Drivers section for details regarding output driver types). Note that the PPR4 assignments share a dependency with the state of PPR1 (frequency translation options) in that the OUT6 channel is disabled for PPR1 State 2 through State 7.

Table 25. PPR4—OUT6 Options

PPR State		OUT6	
PPR1	**PPR4**	**Driver**	**f_{OUT6} (MHz)**
0 or 1	0	Disabled	Not applicable
	1	3.3 V CMOS	133.3
	2	1.8 V CMOS	133.3
	3	LVDS	133.3
	4	LVDS	66.67
	5	3.3 V CMOS	66.67
	6	1.8 V CMOS	66.67
	7	3.3 V CMOS	33.33
2 to 7	0 to 7	Disabled	Not applicable

PPR5—Reference Monitor Threshold

The PPR5 pin controls the range of the frequency error threshold associated with the reference frequency monitor (see the Reference Monitor section) per Table 26. The threshold has units of parts per million (ppm) relative to the nominal input reference frequency (19.44 MHz or 25 MHz).

Table 26. PPR5—Reference Monitor Threshold Options

PPR5 State	Threshold (ppm)
0	±25
1	±25
2	±10
3	±10
4	±50
5	±50
6	±100
7	±100

PPR6—Monitor Clock (MCLK_x) Input Configuration

The PPR6 pin controls the configuration of the MCLK_x inputs, which includes a combination of both frequency (MHz) and input type (see the Monitor Clock Input section for details regarding MCLK_x input types). Table 27 associates each PPR6 state with a particular MCLK_x input configuration.

Table 27. PPR6—MCLK_x Input Options

PPR6 State	f_{MCLK} (MHz)	MCLK_x Input Configuration
0	19.44	Differential
1	19.44	Single-ended 3.3 V CMOS buffer
2	0.008	Single-ended 3.3 V CMOS buffer
3	0.008	Differential
4	38.88	Differential
5	25	Differential
6	10	Single-ended 3.3 V CMOS buffer
7	10	Differential

Dependency of PPR3 and PPR4 on PPR1

PPR1 defines the input reference frequency, configures the internal PLL to yield certain OUT2 and OUT3 frequencies and establishes the state of the ×2 multiplier at the input of the PLL (bypass/active). PPR3 and PPR4 affect the frequency and output driver of the OUT4, OUT5, and OUT6 channels, but with a dependency on the state of PPR1, as summarized in Table 28.

With regard to Table 28, the user may select any PPR3 state and any PPR4 state for a given PPR1 state (that is, PPR3 and PPR4 are completely independent of one another).

Table 28. PPR1, PPR3, and PPR4 Dependencies[1]

PPR1 State	f_{REF} (MHz)	PLL ×2	OUT2/OUT3 Frequency (MHz)	PPR3 State	OUT4 Frequency (MHz)	OUT4 Driver	OUT5 Frequency (MHz)	OUT5 Driver	PPR4 State	OUT6 Frequency (MHz)	OUT6 Driver
0	25	Bypass	156.25	0	100	HSTL	125	HSTL	0	N/A	Disabled
1	25	Active	156.25	1	100	HCSL	100	HCSL	1	133.3	3.3 V CMOS
				2	100	HCSL	125	HSTL	2	133.3	1.8 V CMOS
				3	125	LVDS	125	LVDS	3	133.3	LVDS
				4	125	HSTL	125	HSTL	4	66.67	LVDS
				5	100	LVDS	100	HCSL	5	66.67	3.3 V CMOS
				6	100	HSTL	100	HSTL	6	66.67	1.8 V CMOS
				7	N/A	Disabled	N/A	Disabled	7	33.33	3.3 V CMOS
2	25	Bypass	156.25	0	312.5	HSTL	312.5	HSTL	0	N/A	Disabled
3	25	Active	156.25	1	312.5	LVDS	312.5	LVDS	1	N/A	Disabled
				2	312.5	HCSL	312.5	HCSL	2	N/A	Disabled
				3	312.5	HSTL	125	HSTL	3	N/A	Disabled
				4	312.5	LVDS	125	LVDS	4	N/A	Disabled
				5	312.5	HCSL	125	HCSL	5	N/A	Disabled
				6	312.5	LVDS	125	HSTL	6	N/A	Disabled
				7	125	HCSL	125	HCSL	7	N/A	Disabled
4	19.44	Bypass	155.52	0	38.88	HSTL	77.76	HSTL	0	N/A	Disabled
5	19.44	Active	155.52	1	38.88	LVDS	77.76	LVDS	1	N/A	Disabled
				2	38.88	LVDS	38.88	LVDS	2	N/A	Disabled
				3	38.88	HSTL	38.88	HSTL	3	N/A	Disabled
				4	77.76	HSTL	77.76	HSTL	4	N/A	Disabled
				5	77.76	LVDS	77.76	LVDS	5	N/A	Disabled
				6	N/A	Disabled	38.88	HSTL	6	N/A	Disabled
				7	N/A	Disabled	N/A	Disabled	7	N/A	Disabled
6	25	Bypass	160	0	80	HSTL	80	HSTL	0	N/A	Disabled
7	25	Active	160	1	80	LVDS	80	HSTL	1	N/A	Disabled
				2	80	LVDS	160	LVDS	2	N/A	Disabled
				3	N/A	Disabled	80	HSTL	3	N/A	Disabled
				4	80	LVDS	80	LVDS	4	N/A	Disabled
				5	80	HSTL	160	HSTL	5	N/A	Disabled
				6	N/A	Disabled	160	HSTL	6	N/A	Disabled
				7	N/A	Disabled	N/A	Disabled	7	N/A	Disabled

[1] N/A means not applicable.

POWER-ON RESET (POR)

Applying power to the AD9574 causes an internal power-on reset (POR) event. A POR event allows the device to initialize to a known state at power-up by initiating a scan of the PPRx pins (see the PPRx Pins section).

In general, the AD9574 follows an orderly power-on sequence beginning with the POR circuit detecting a valid 3.3 V supply. This activates the internal LDO regulators. Detection of valid LDO voltages by the POR circuit triggers a PPRx scan sequence, which results in the configuration of the input reference receivers.

Assuming the presence of the active reference, the reference signal appears at the input to the PLL and at the OUT0 and OUT1 channels. With a reference signal applied to the input of the PLL, the VCO calibration sequence initiates. Assuming a valid input reference signal, the PLL eventually locks to the reference signal as indicated by assertion of the LD pin. This lock enables the prescale dividers at the output of the VCO, which starts the output drivers toggling (that is, those output drivers enabled per the PPRx settings).

To ensure maximum operational robustness, the power-on initialization sequence shown in Figure 22 is recommended. The power supply initialization loop assumes the user can monitor the V_{DD} supply voltages applied to the device. The chip level reset loop assumes the user can monitor the state of the lock detect pin (LD, Pin 14) and assert the $\overline{\text{RESET}}$ pin (Pin 20) under software control. The variables RST_COUNT, time, and PLL_TO denote quantities maintained in the power-on initialization software routine of the user.

The $\overline{\text{RESET}}$ count (RST_COUNT) represents an integer counter implemented in the software to track the number of times the $\overline{\text{RESET}}$ pin is asserted under software control. Time is a variable implemented in the software to track elapsed time. The PLL timeout (PLL_TO) variable is implemented in the software to indicate the maximum amount of time allowed for the PLL to lock following an assertion of the $\overline{\text{RESET}}$ pin. Note that the value of PLL_TO depends on the selected PPR state. See Table 16 in the Timing Specifications section to determine the appropriate value for the PLL_TO variable.

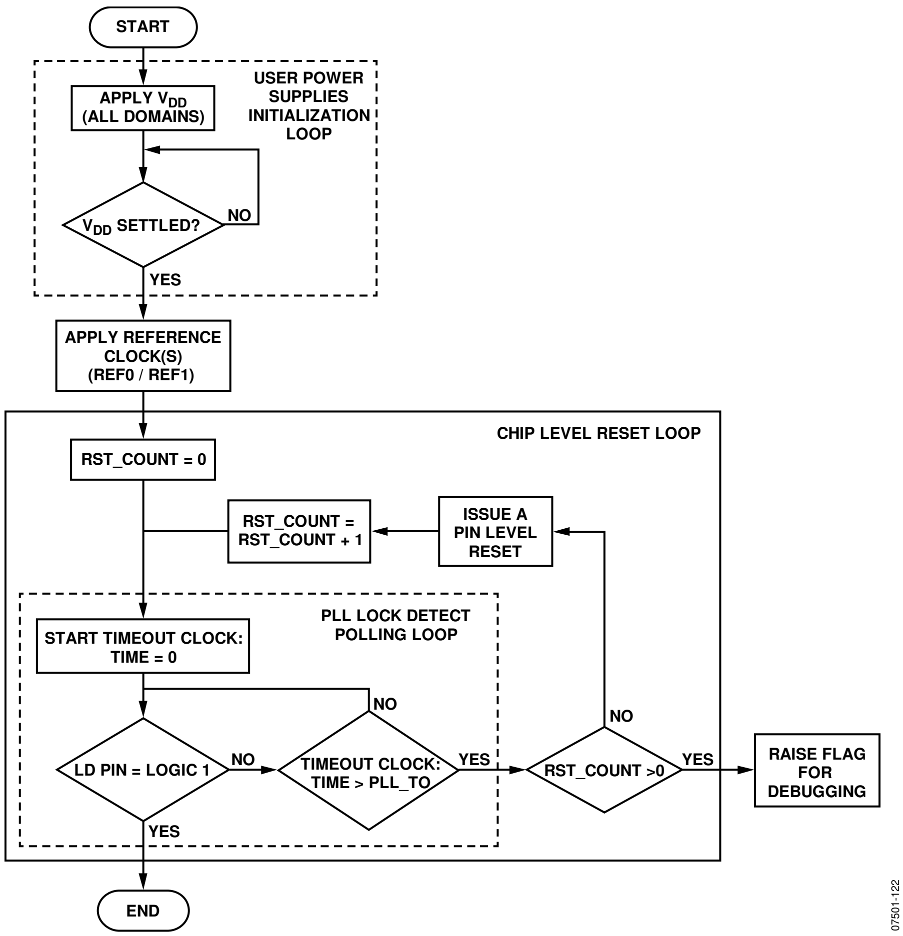


Figure 22. Recommended Power-On Initialization Sequence

REFERENCE CLOCK INPUTS

The REF0 and REF1 input channels provide for two operating modes based on the scanned state of PPR0. Note that the resulting mode applies to both the REF0 and REF1 channels. That is, independent input mode selection is not an option.

In single-ended 3.3 V CMOS buffer mode, the user may connect a 3.3 V clock source directly to the positive reference input pin (REF0_P, for example). Note that in single-ended mode, it is best to connect a 0.1 nF capacitor from the negative input pin (REF0_N, for example) to GND.

In differential mode, the user may connect a differential clock driver to the two reference input pins (REF0_P and REF0_N, for example). Note that differential operation requires ac coupling, that is, a series connected 0.1 nF capacitor from each output of an external differential clock driver to the corresponding reference input pin. This mode also supports a single-ended 1.8 V CMOS clock source by connecting the source to either of the reference input pins (REF0_P or REF0_N, for example). Connect the unused input pin to GND via a 0.1 nF capacitor.

MONITOR CLOCK INPUT

The MCLK_x pins are the monitor clock inputs and are intended to accept a stable frequency reference source. The MCLK_x pins are configurable as either single-ended 3.3 V CMOS or differential. The monitor clock accepts a fixed frequency of 0.008 MHz, 10 MHz, 19.44 MHz, 25 MHz, or 38.88 MHz. Note that the monitor clock input frequency and receiver configuration depend on the scanned state of PPR6 (see the PPR6—Monitor Clock (MCLK_x) Input Configuration section for details).

A stable monitor clock frequency source supports the operation of the reference monitor (see the Reference Monitor section). Because the reference monitor relies on the precision and stability of the monitor clock input signal, the user must ensure the frequency accuracy of the monitor clock source.

REFERENCE SWITCHING

The AD9574 provides for manual reference switching capability. Although the on-board reference monitor provides the user with information regarding the status of the input references, the device does not provide for automatic reference switchover as a result of status changes. Rather, the REF_SEL pin provides the user with manual reference switchover control. A Logic 0 on the REF_SEL pin informs the internal reference switching logic to make REF0 the active reference, whereas a Logic 1 makes REF1 the active reference.

The switch to a new active reference does not occur instantaneously with a corresponding change of state on the REF_SEL pin. Instead, the reference switching logic notes the request for a reference switch and waits for the opportune moment to make the physical switch. This functionality ensures a minimal frequency disturbance on the output clocks associated with the integrated PLL (the OUT2 through OUT6 channels).

The reference switching logic provides information about which reference channel (REF0 or REF1) is the currently active reference via the REF_ACT output pin. The REF_ACT pin is Logic 0 when REF0 is the active reference and Logic 1 when REF1 is the active reference. Furthermore, the reference switching logic indicates when the device is in the process of performing a reference switchover via the REF_SW pin (that is, REF_SW is Logic 1 when a reference switch is in progress). The REF_SW pin assumes a Logic 1 state when REF_SEL changes states and returns to a Logic 0 state when the device completes the reference switchover process. See the Reference Switching section for additional information.

Changing the state of the REF_SEL pin triggers the internal state machine to perform the reference switching process. Confirm (via the REF_ACT pin) that the device has switched to the desired reference before a subsequent change of the REF_SEL pin. Changing the state of the REF_SEL pin before the internal state machine completes the reference switching process may cause undesired results.

Because the reference switching logic waits for an optimal switchover point rather than switching immediately, there is the rare possibility that either or both references happen to fail (resulting in a loss of reference (LOR) fault condition) just after the user requests a reference switchover (via the REF_SEL pin), but before the switching logic identifies the optimal switchover point. In such an instance, the LOR condition associated with either reference causes the internal state machine to stall and the device fails to switch references, thereby retaining the currently active reference. If the currently active reference fails, the device loses lock, thereby necessitating a device reset. If the requested reference fails, the device retains the currently active reference, but switches to the requested reference if it becomes available. Note that as long as a reference remains in an LOR condition, the state machine remains stalled. Only a device reset makes the state machine disregard the initial request to switch references.

The REF_SEL pin determines which reference is the active reference any time device power is cycled or the user asserts the $\overline{\text{RESET}}$ pin.

REFERENCE MONITOR

An on-board reference frequency monitor provides the user with a means to validate the frequency accuracy of the active reference channel (REF0 or REF1) in real time. The REFMON pin enables or disables the reference monitoring function (Logic 1 or Logic 0, respectively).

Apply a static and valid Logic 0 or Logic 1 level to the REFMON pin. Do not allow the REFMON pin to float. Do not toggle the REFMON pin during device operation.

When enabled, the reference monitor continuously tests the frequency of the active reference by comparing it to the frequency of the MCLK_x signal. The result of this comparison appears on the REF_FHI and REF_FLO pins per Table 29.

The above or below frequency decision threshold of the monitor is 10 ppm, 25 ppm, 50 ppm, or 100 ppm per the scanned value of PPR5 (see the PPR5—Reference Monitor Threshold section).

Following a power-up or $\overline{\text{RESET}}$, the reference monitor indicates an indeterminate (see Table 29) condition until enough time elapses to make a valid decision (see the monitor clock input to REF_FHI/REF_FLO time parameter in Table 16). The monitoring process begins when the following two conditions are met: the REFMON pin is Logic 1 and a valid signal is present at the MCLK_x pins. Within the time specified by the monitor clock input to REF_FHI/REF_FLO time parameter (per Table 16), the reference monitor indicates the results on the reference monitor status pins, REF_FHI/REF_FLO (per Table 29).

The REF_FHI and REF_FLO pins are open-drain with internal pull-down resistors allowing wire-OR'ed operation. That is, both pins can be connected together to yield a single in tolerance or out of tolerance indication. With a wire-OR'ed connection, however, it is not possible to discern whether the reference frequency is above or below the tolerance threshold.

Table 29. Reference Frequency Monitor Status

REF_FHI	REF_FLO	Active Reference Status
0	0	Frequency within tolerance threshold
0	1	Frequency below tolerance threshold
1	0	Frequency above tolerance threshold
1	1	Indeterminate or fault condition

In addition to its frequency monitoring function, the reference monitor also checks for the presence of a clock signal at the REF0_x, REF1_x, and MCLK_x inputs. The absence of a clock signal results in an internal LOR indication for that particular clock input. Note that LOR indication occurs when the input frequency is below approximately 1 MHz.

The one exception is for f_{MCLK} = 8 kHz, for which an LOR indication occurs if f_{MCLK} is below approximately 6.1 kHz. An LOR condition may cause the REF_FHI and REF_FLO pins to indicate an indeterminate state (a Logic 1 on both the REF_FHI and REF_FLO pins). See the Reference Switching section for details regarding LOR conditions that occur during a reference switching operation.

PLL

The PLL consists of six functional elements.

- Frequency prescaler
- PFD
- Charge pump
- Loop filter
- VCO
- Feedback divider

The AD9574 automatically configures the six functional elements based on the prevailing PPRx settings.

The prescaler is shown functionally as a programmable divider in Figure 20. It actually consists of a ×2 frequency multiplier, a divide-by-5 block, and multiplexers to yield the necessary frequency divide ratios per Table 30.

Table 30. PLL Frequency Prescaler

×2	÷5	Frequency Division
Active	Bypassed	1/2 (same as multiply by 2)
Bypassed	Bypassed	1
Active	Active	5/2
Bypassed	Active	5

Table 31. REF_FHI and REF_FLO Status[1]

REFMON	MCLK_x	REF_SEL	REF_SW[2]	REF0_x	REF1_x	REF_Fx[3]
0	Not applicable	0	0	LOR	Not applicable	11
0	Not applicable	0	0	OK	Not applicable	00
0	Not applicable	1	0	Not applicable	LOR	11
0	Not applicable	1	0	Not applicable	OK	00
0	Not applicable	Not applicable	1	LOR	Not applicable	11
0	Not applicable	Not applicable	1	Not applicable	LOR	11
0	Not applicable	Not applicable	1	OK	OK	00
1	LOR	Not applicable	Not applicable	Not applicable	Not applicable	11
1	OK	0	0	LOR	Not applicable	11
1	OK	0	0	OK	Not applicable	00, 01, or 10
1	OK	1	0	Not applicable	LOR	11
1	OK	1	0	Not applicable	OK	00, 01, or 10
1	OK	Not applicable	1	LOR	Not applicable	11
1	OK	Not applicable	1	Not applicable	LOR	11
1	OK	Not applicable	1	OK	OK	00, 01, or 10

[1] OK means the signal is present.
[2] For REF_SW = 1, LOR means a transition to a LOR condition while the device is in the process of a reference switchover.
[3] REF_Fx refers to the combined state of the REF_FHI and REF_FLO pins per Table 29.

The PFD, charge pump, and loop filter work together to tune the VCO output frequency according to the phase difference of the clock edges at the input to the PFD. The closed-loop configuration gradually causes the phase difference at the PFD input to settle near zero and the VCO output frequency to settle to a value of N times the PFD input frequency (N is the feedback divider value). Based on the PPRx pin settings, the AD9574 automatically selects the value of N and the prescaler value to yield one of three VCO frequencies (2488 MHz, 2500 MHz, or 2560 MHz) per Table 22.

The loop filter consists of a partially integrated third-order RC network with an external network connected between the LF and LDO_BYP pins. The external network consists of a 1 nF or 2 nF capacitor or a series connected 2 nF capacitor, C, and 4.75 kΩ resistor, R (see Table 32). The loop filter components, charge pump current, feedback divider, and VCO gain define the bandwidth of the PLL according to Table 22. The device automatically adjusts the internal components per the PPRx settings to maintain an approximately constant loop bandwidth.

Table 32. External Loop Filter Components

PPR1 State	External Components
0	C = 1 nF
1	C = 2 nF
2	C = 1 nF
3	C = 2 nF
4	C = 1 nF
5	C = 2 nF
6	C = 2 nF in series with R = 4.75 kΩ
7	C = 2 nF in series with R = 4.75 kΩ

Figure 23 is a diagram of the loop filter portion of the PLL.

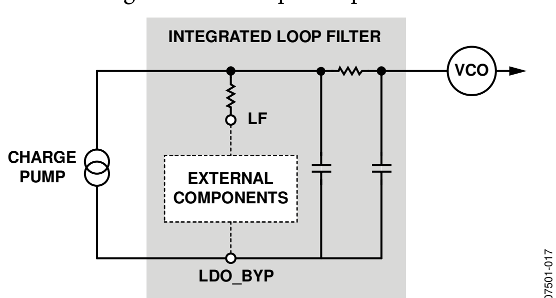


Figure 23. PLL Loop Filter Detail

The AD9574 also provides a digital lock detect output signal at the LD pin, which indicates (active high) when the device considers the PFD input phase differential to have stabilized near zero.

The OUT2 through OUT6 channels are static (outputs do not toggle) while the PLL is unlocked (that is, while the LD pin is Logic 0).

OUTPUT DRIVERS

The output channels of the AD9574 offer the flexibility of a variety of drive formats, including HSTL, HCSL, LVDS, and CMOS. Each channel offers a subset of these formats (see Table 33).

Table 33. Output Drive Formats

Output Channel	Format				
				CMOS	
	HSTL	HCSL	LVDS	3.3 V	1.8 V
0	Yes	No	No	Yes	No
1	Yes	No	No	Yes	No
2	Yes	No	No	No	No
3	Yes	No	No	No	No
4	Yes	Yes	Yes	No	No
5	Yes	Yes	Yes	No	No
6	No	No	Yes	Yes	Yes

OUTPUT CLOCKS

The seven output clock channels (OUT0 through OUT6) provide two different frequency translation functions. OUT0 and OUT1 offer a replica of the reference frequency (with a frequency doubling option for OUT0), whereas OUT2 through OUT6 offer rational frequency translations by means of an integrated integer-N PLL. Table 34 shows a summary of the available frequencies for each output channel (in units of MHz). The indicated reference to output frequency translations depends on the results of a PPRx scan (see the PPRx Pins section for details).

Table 34. Output Frequencies

	Output (MHz)						
f_{REF}	0	1	2	3	4	5	6
25	25 50	25	156.25	156.25	100 125 312.5 80 160	100 125 312.5 80 160	33.33 66.67 133.3
19.44	19.44	19.44	155.52	155.52	38.88 77.76	38.88 77.76	N/A[1]

[1] N/A means not applicable.

APPLICATIONS INFORMATION

DUAL OSCILLATOR REFERENCE INPUT APPLICATION

Figure 24 depicts a typical application diagram using two crystal oscillators (XOs) as the reference inputs. A stable oscillator source supplies the MCLK_x inputs and serves as the timing reference for the on-board reference monitoring function. A field-programmable gate array (FPGA) handles the control interface for monitoring the status of the references and the PLL (lock detector) and for switching between references as required. The FPGA also controls the on/off state of the reference oscillators, which provides for shutting down a faulty reference or for keeping a redundant reference turned off until needed. The general configuration of the AD9574 is set via a group of resistors that establish the desired PPRx states. Although Figure 24 shows XOs with differential outputs, single-ended XOs can be substituted by connecting the XO output to the REFx_P pin and a 0.1 nF capacitor from the REFx_N pin to GND.

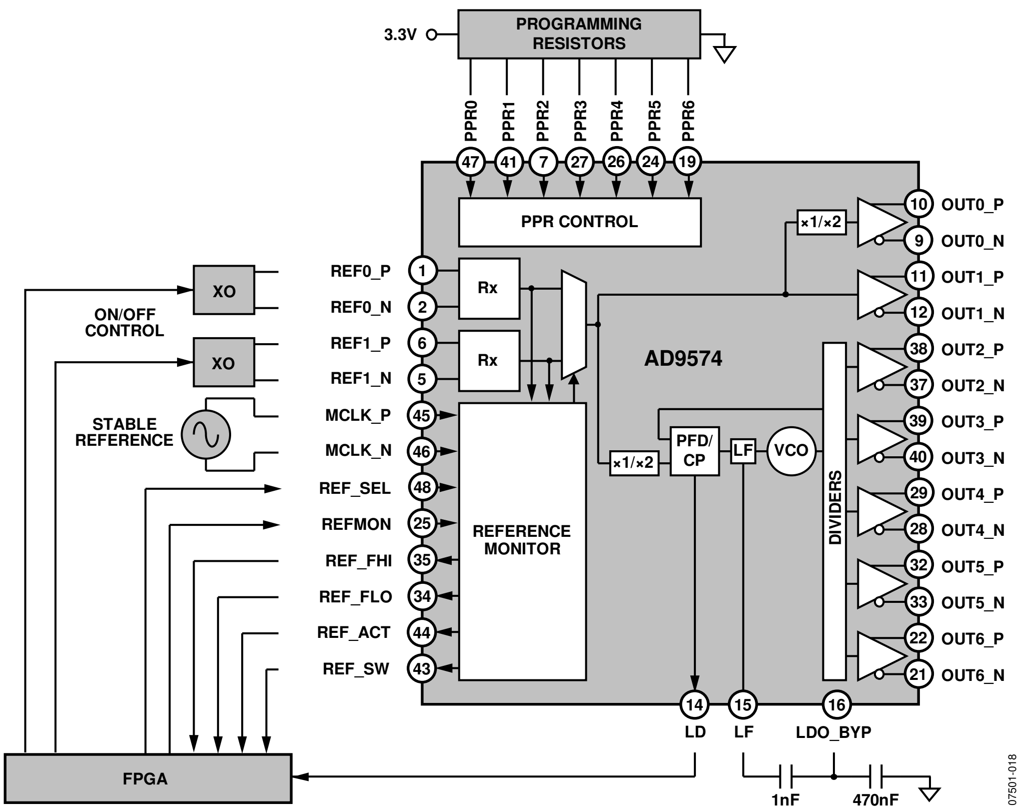


Figure 24. Dual Oscillator Reference Input Application Diagram

SIMPLE, SINGLE OSCILLATOR REFERENCE INPUT APPLICATION

Figure 27 depicts a simple application using a single crystal oscillator as the reference input with minimal reference monitoring functionality. The wire-OR'ed REF_FHI and REF_FLO connection in conjunction with REF_MON tied to GND (REF_MON = 0; see Table 31) yields a LOR function indicating only that REF0 is present (or not); that is, there is no specific indication of high or low frequency status. The LOR and LD signals can notify a controller (not shown) of a reference failure or an unlocked PLL condition. The general configuration of the AD9574 is set via a group of resistors that establish the desired PPRx states. Although Figure 27 shows an XO with differential outputs, a single-ended XO can be substituted by connecting the XO output to the REF0_P pin and a 0.1 nF capacitor from the REF0_N pin to GND.

INTERFACING TO CMOS CLOCK OUTPUTS

Apply the following general guidelines when using the single-ended 1.8 V or 3.3 V CMOS clock output drivers.

Design point-to-point nets such that a driver has only one receiver on the net, if possible. This allows simple termination schemes and minimizes ringing due to possible mismatched impedances on the net. Series termination at the source is generally required to provide transmission line matching and/or to reduce current transients at the driver.

The value of the series termination depends on the board design and timing requirements (typically 10 Ω to 100 Ω). CMOS outputs are limited in terms of the capacitive load or trace length that they can drive. Typically, trace lengths less than 6 inches are recommended to preserve signal rise/fall times and signal integrity.

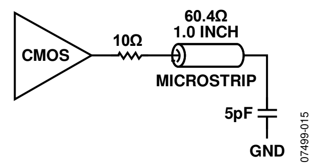


Figure 25. Series Termination of CMOS Output

Termination at the far end of the printed circuit board (PCB) trace is a second option. The CMOS outputs of the AD9574 do not supply enough current to provide a full voltage swing with a low impedance resistive, far end termination, as shown in Figure 26. Ensure that the impedance of the far end termination network matches the PCB trace impedance and provides the desired switching point. The reduced signal swing may still meet receiver input requirements in some applications. This can be useful when driving long trace lengths on less critical nets.

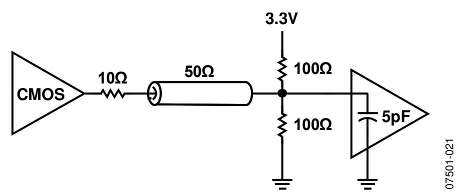


Figure 26. CMOS Output with Far End Termination

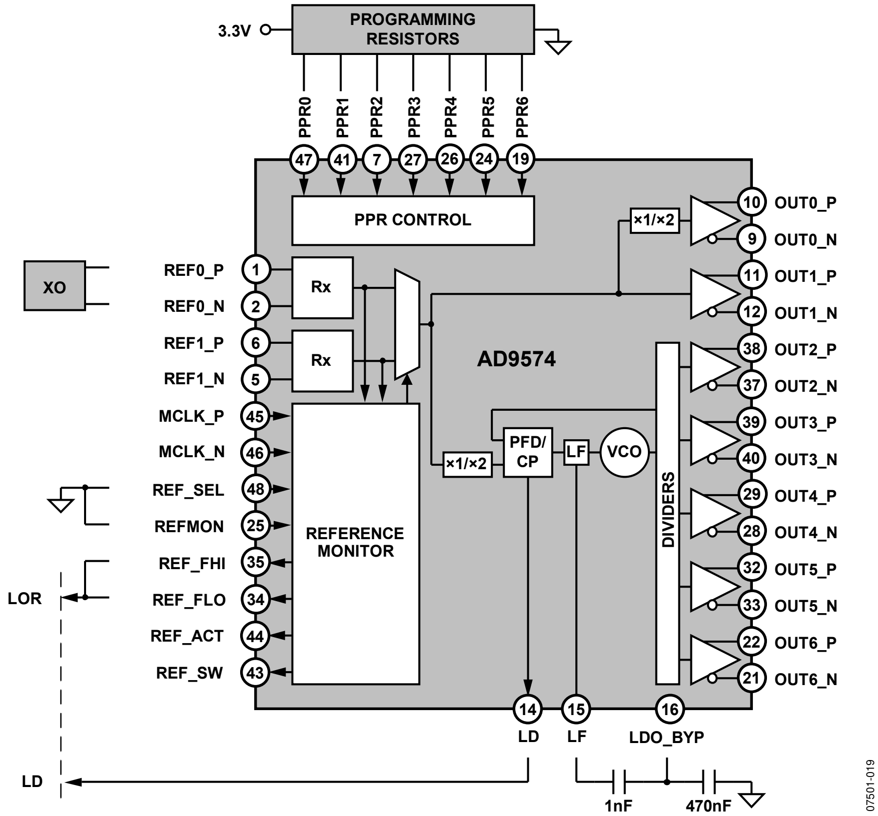


Figure 27. Single Oscillator Reference Input Application Diagram

INTERFACING TO LVDS AND HSTL CLOCK OUTPUTS

LVDS and HSTL both employ a differential output driver. The recommended termination circuit for LVDS and HSTL drivers appears in Figure 28.

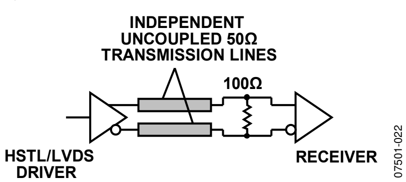


Figure 28. LVDS or HSTL Output Termination

See the AN-586 Application Note for more information about LVDS.

INTERFACING TO HCSL CLOCK OUTPUTS

HCSL uses a differential open-drain architecture. The open-drain architecture necessitates the use of an external termination resistor. Figure 29 shows the typical method for interfacing to HCSL drivers.

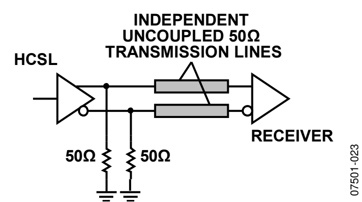


Figure 29. HCSL Output Termination

In some cases, the fast switching capability of HCSL drivers results in overshoot and ringing. The alternative HCSL interface shown in Figure 30 can mitigate this problem via a small series resistor, typically in the 10 Ω to 30 Ω range.

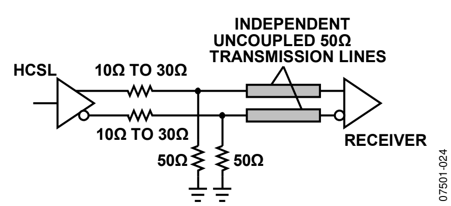


Figure 30. Alternate HCSL Output Termination

POWER SUPPLY

The AD9574 requires a power supply of 3.3 V ± 10%. The Specifications section gives the performance expected from the AD9574 with the power supply voltage within this range. The absolute maximum range of −0.3 V to +3.6 V, with respect to GND, must never be exceeded on the VDD_x pins.

Follow good engineering practice in the layout of power supply traces and the ground plane of the PCB. Bypass the power supply on the PCB with adequate capacitance (>10 μF). Bypass the AD9574 with adequate capacitors (0.1 μF) at all power pins as close as possible to the device. The layout of the AD9574 evaluation board is a good example of how to route power supply traces and where to place bypass capacitors.

The exposed metal pad on the AD9574 package is an electrical connection, as well as a thermal enhancement. For the device to function properly, the pad must be properly attached to ground (GND). The PCB acts as a heat sink for the AD9574; therefore, this GND connection provides a good thermal path to a larger heat dissipation area, such as a ground plane on the PCB.

POWER AND GROUNDING CONSIDERATIONS AND POWER SUPPLY REJECTION

Many applications seek high speed and performance under less than ideal operating conditions. In these application circuits, the implementation and construction of the PCB is as important as the circuit design. Proper RF techniques must be used for device selection, placement, and routing, as well as for power supply bypassing and grounding to ensure optimum performance.

THERMAL PERFORMANCE

Table 35. Thermal Parameters for the 48-Lead, 7 mm × 7 mm LFCSP

Symbol	Thermal Characteristic Using a JEDEC 51-7 Plus JEDEC 51-5 2S2P Test Board[8]	Value[9]	Unit
θ_{JA}	Junction to ambient thermal resistance, 0.0 m/sec airflow per JEDEC JESD51-2 (still air)	32.6	°C/W
θ_{JB}	Junction to board thermal resistance, 0.0 m/sec airflow per JEDEC JESD51-8 (still air)	18.7	°C/W
θ_{JC}	Junction to case thermal resistance (die-to-heat sink) per MIL-Standard 883, Method 1012.1	3.5	°C/W
Ψ_{JT}	Junction to top of package characterization parameter, 0 m/sec airflow per JEDEC JESD51-2 (still air)	0.3	°C/W
Ψ_{JT}	Junction to top of package characterization parameter, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air)	0.4	°C/W
Ψ_{JT}	Junction to top of package characterization parameter, 2.5 m/sec airflow per JEDEC JESD51-6 (moving air)	0.6	°C/W

[8] The exposed pad on the bottom of the package must be soldered to ground to achieve the specified thermal performance.
[9] Results are from simulations. The PCB is a JEDEC multilayer type. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

The AD9574 is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, an airflow source can be used. Use the following equation to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured by the customer at the top center of the package.
Ψ_{JT} is the value as indicated in Table 35.
PD is the power dissipation (see Table 15).

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation

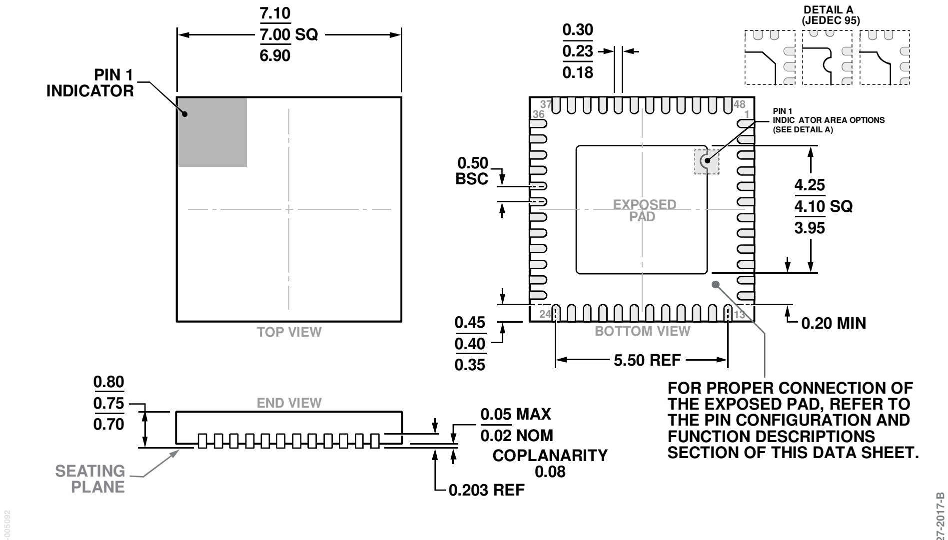
$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD-4.

Figure 31. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9574BCPZ	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-5
AD9574BCPZ-REEL7	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-5
AD9574/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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