

# HEF4073B

Triple 3-input AND gate

Rev. 4 — 6 October 2017

Product data sheet

## 1 General description

The HEF4073B is a triple 3-input AND gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity to output impedance variations.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

## 2 Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

## 3 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
HEF4073BT	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

## 4 Functional diagram

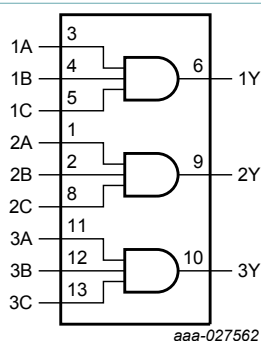


Figure 1. Functional diagram

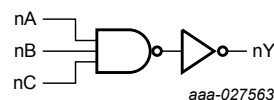
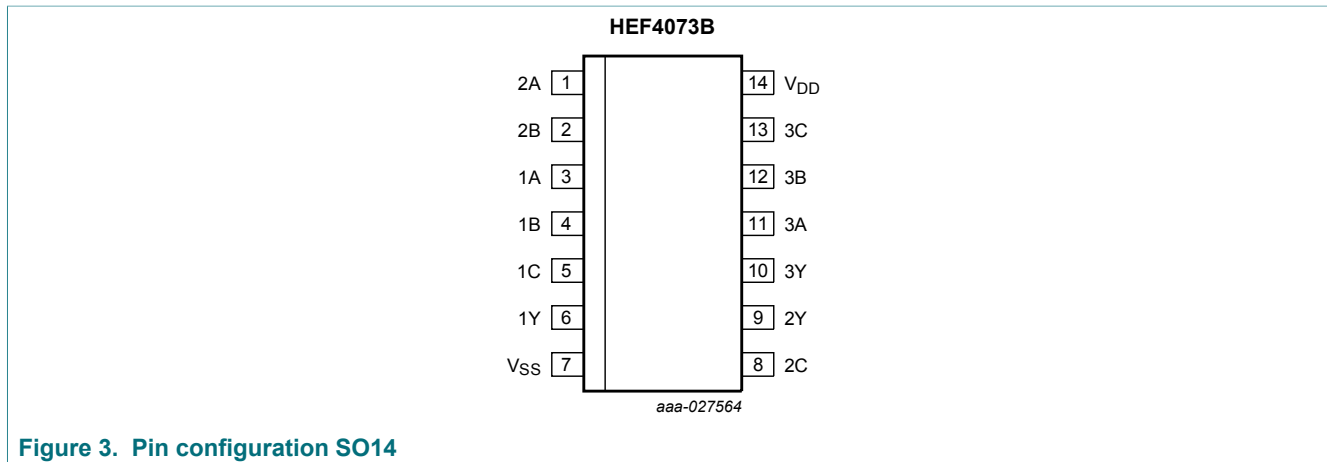


Figure 2. Logic diagram (one gate)

## 5 Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A	3, 1, 11	data input
1B, 2B, 3B	4, 2, 12	data input
1C, 2C, 3C	5, 8, 13	data input
1Y, 2Y, 3Y	6, 9, 10	data output
V <sub>SS</sub>	7	ground (0 V)
V <sub>DD</sub>	14	supply voltage

## 6 Functional description

Table 3. Function selection <sup>[1]</sup>

Input			Output
nA	nB	nC	nY
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

[1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care

## 7 Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0$  V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V	-	$\pm 10$	mA
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to + 85 °C [1]	-	500	mW
$P$	power dissipation	per output	-	100	mW

[1] For SO14 packages: above  $T_{amb} = 70$  °C,  $P_{tot}$  derates linearly with 8 mW/K.

## 8 Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		3	15	V
$V_I$	input voltage		0	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5$ V	-	3.75	ns/V
		$V_{DD} = 10$ V	-	0.5	ns/V
		$V_{DD} = 15$ V	-	0.08	ns/V

## 9 Static characteristics

**Table 6. Static characteristics**
 $V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	all valid input combinations; $I_O = 0\text{ A}$	5 V	-	1.0	-	1.0	-	7.5	$\mu\text{A}$
			10 V	-	2.0	-	2.0	-	15.0	$\mu\text{A}$
			15 V	-	4.0	-	4.0	-	30.0	$\mu\text{A}$
$C_I$	input capacitance			-	-	-	7.5	-	-	pF

## 10 Dynamic characteristics

**Table 7. Dynamic characteristics**
 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; for test circuit see [Figure 5](#).

Symbol	Parameter	Conditions	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	nA, nB, nC to nY; see <a href="#">Figure 4</a>					
		$V_{DD} = 5\text{ V}$	$23 + 0.55 \times C_L$	-	55	110	ns
		$V_{DD} = 10\text{ V}$	$14 + 0.23 \times C_L$	-	25	50	ns
		$V_{DD} = 15\text{ V}$	$12 + 0.16 \times C_L$	-	20	40	ns
$t_{PLH}$	LOW to HIGH propagation delay	nA, nB, nC to nY; see <a href="#">Figure 4</a>					
		$V_{DD} = 5\text{ V}$	$13 + 0.55 \times C_L$	-	45	90	ns
		$V_{DD} = 10\text{ V}$	$9 + 0.23 \times C_L$	-	20	40	ns
		$V_{DD} = 15\text{ V}$	$7 + 0.16 \times C_L$	-	15	30	ns
$t_t$	output transition time	nY; see <a href="#">Figure 4</a>	<sup>[2]</sup> $10 + 1.0 \times C_L$	-	60	120	ns
			$9 + 0.42 \times C_L$	-	30	60	ns
			$6 + 0.28 \times C_L$	-	20	40	ns

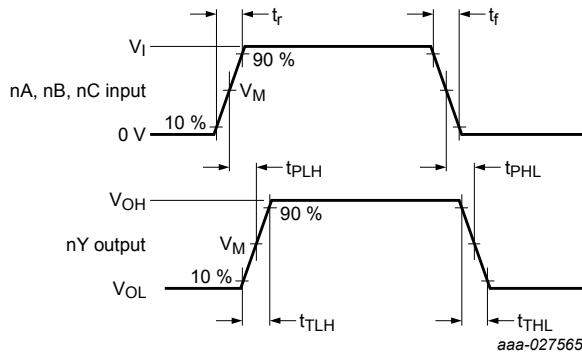
[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula ( $C_L$  in pF).

[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

**Table 8. Dynamic power dissipation**
 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ ( $\mu\text{W}$ )	$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz; $C_L$ = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; $V_{DD}$ = supply voltage in V.
		10 V	$P_D = 2700 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ ( $\mu\text{W}$ )	
		15 V	$P_D = 8400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ ( $\mu\text{W}$ )	

10.1 Waveforms and test circuit



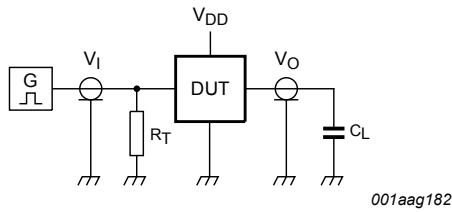
Measurement points are given in [Table 9](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Figure 4. Input to output propagation delay and output transition times

Table 9. Measurement points

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).

Definitions for test circuit:

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Figure 5. Test circuit for measuring switching times

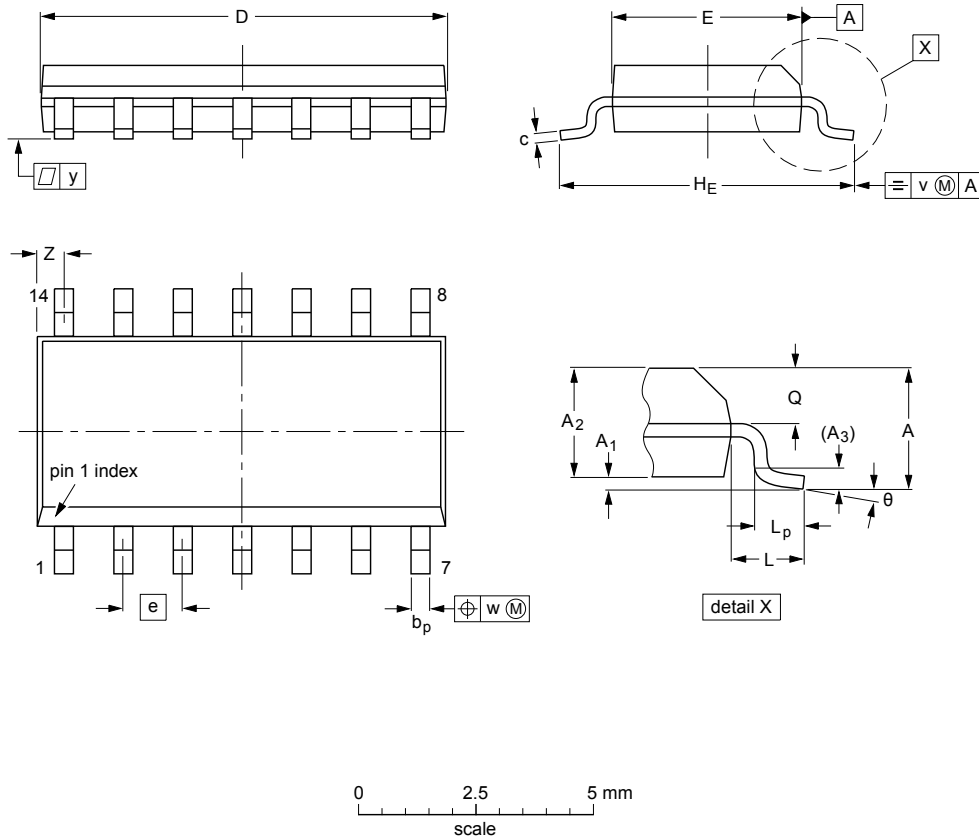
Table 10. Test data

Supply voltage	Input	Load
$V_{DD}$	$V_I$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	$\leq 20$ ns
		50 pF

11 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT108-1	076E06	MS-012			99-12-27 03-02-19

Figure 6. Package outline SOT108-1 (SO14)

## 12 Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test

## 13 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4073B v.4	20171006	Product data sheet	-	HEF4073B_CNV v.3
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Type numbers HEF4073BP and HEF4073BD removed.</li></ul>			
HEF4073B_CNV v.3	19950101	Product specification	-	-



## 14 Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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