User's Guide
SBVU014–August 2009

TPS73x01DRBEVM-518

This user's guide describes the characteristics, operation, and use of the TPS73x01DRBEVM-518 evaluation module. This document includes setup instructions, a schematic diagram, thermal guidelines, a bill of materials (BOM), and printed circuit board (PCB) layout drawings.

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1 Overview

This document describes the characteristics, operation, and use of the TPS73x01DRBEVM-518 evaluation module (EVM). This EVM demonstrates the capabilities and features of Texas Instruments' TPS73201DRB, TPS73601DRB, and TPS73701DRB low-dropout (LDO) linear regulators. These regulators, each available in a 3-mm × 3-mm SON package, are capable of 250-mA, 400-mA, and 1-A output currents, respectively. The TPS73x01DRBEVM-518 module helps designers evaluate the operation and performance of the TPS73201, TPS73601, and TPS73701 LDO devices in a variety of configurations. The output voltage from the LDO device can be selected by a jumper to obtain 1.8 V, 2.5 V, 2.8 V, 3.0 V or 3.3 V. Table 1 summarizes the LDOs that are suitable for use with this EVM.

Table 1. Device Summary

Device	Package Size	Description
TPS73201DRB	3-mm × 3-mm SON	Cap-Free, NMOS, 250-mA Low Dropout Regulator with Reverse Current Protection
TPS73601DRB	3-mm × 3-mm SON	Cap-Free, NMOS, 400-mA Low Dropout Regulator with Reverse Current Protection
TPS73701DRB	3-mm × 3-mm SON	1-A Low Dropout Regulator with Reverse Current Protection

1.1 Related Documentation from Texas Instruments

The following related documents are available through the Texas Instruments web site at http://www.ti.com.

Table 2. Related Documentation

Part Number	Literature Number
TPS73201	SBVS037
TPS73601	SBVS038
TPS73701	SBVS067

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS73x01DRBEVM-518.

2.1 Input/Output Connector Descriptions

2.1.1 J1: VIN

This connector is the positive input supply voltage. The leads to the input supply should be twisted and kept as short as possible to minimize electromagnetic interference (EMI) transmission. Additional bulk capacitance should be added between J1 and J2 if the supply leads are greater than 6 inches (15,24 cm). An additional 47-µF or greater capacitor improves the transient response of the TPS73x01DRB and helps to reduce ringing on the input when long supply wires are used. The TPS73x01DRBEVM-518 has a footprint (C4) on the EVM available for this purpose.

2.1.2 J3: VOUT

This jumper is the positive connection from the output. Connect this pin to the positive input of the load.

2.1.3 J2: GND

This jumper is the return connection for the input power supply of the regulator.

2.1.4 J4: GND

This point is the return connection for the output.

2.1.5 JP1: ENABLE

This jumper is used to enable or disable the output of the TPS73x01DRB. Placing a shorting jumper between pins 1 and 2 (*ON* position) enables the TPS73x01DRB. Placing the shorting jumper between pins 2 and 3 (*OFF* position) disables the TPS73x01DRB.

2.1.6 JP2: V_{OUT} Selection

This jumper sets the desired output voltage from the TPS73x01DRB. Placing a shorting jumper between the appropriate pins gives the corresponding outputs.

WARNING

1. The Jumper JP2 should only be changed from one place to another when the power is off.
2. The user should not touch the jumper JP2 while the power is applied to the EVM since the output voltage may change due to the noise pick-up in the feedback path.

3 Operation

This section provides information about the operation of the TPS73x01DRBEVM.

3.1 Configuration and Initial Operation

Connect the positive input power supply to J1. Connect the input power return (ground) to J2. The TPS73x01DRB has an absolute maximum input voltage of 6.0 V. The recommended maximum operating voltage is 5.5 V. The actual highest input voltage may be less than 5.5 V as a result of thermal conditions. See the *Thermal Considerations* section of this manual to determine the highest input voltage for maintaining a safe junction temperature.

Connect the desired load between J3 (positive lead) and J4 (negative or return lead). Configure jumper JP2 for the desired output voltage.

4 Thermal Guidelines

This section presents guidelines for the thermal management of the TPS73x01DRBEVM-518 board.

4.1 Thermal Considerations

Thermal management is a key design component of any power converter, and is especially important when power dissipation in the LDO is high. To better help you design the TPS73x01DRB family into your applications, the following formula should be used to approximate the maximum power dissipation (P_{DMax}) at a particular ambient temperature:

$$T_J = T_A + P_D \times \theta_{JA} \quad (1)$$

where:

- T_J is the junction temperature
- T_A is the ambient temperature
- P_D is the power dissipation in the IC
- θ_{JA} is the thermal resistance from junction to ambient

All temperatures are in degrees Celsius.

The measured thermal resistance from junction to ambient for the TPS73x01EVM has a typical value of 40°C/W. The recommended maximum operating junction temperature specified in the product data sheet for the TPS73x01 family is +125°C. With these two pieces of information, the maximum power dissipation can be found by using Equation (1).

Example 1. Sample Calculation

What is the maximum input voltage that can be applied to a TPS73701DRB with a 1.8-V output voltage if the ambient temperature is +85°C and the full 1 A of load current is required?

Given:

T_J = +125°C, T_A = +85°C, θ_{JA} = 40°C/W

Using Equation 1, we substitute in the given values above and find that the maximum power dissipation for the part is P_D = 1 W.

125°C = 85°C + P_D(40°W/C)

This result means that the total power dissipation of the TPS73701DRB must be less than 1 W. Now the input voltage can be calculated.

$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} = (V_{IN} – 1.8\ V) \times 1\ A = 1\ W$

So the maximum input voltage would need to be 2.8 V or less in order to maintain a safe junction temperature.

Similar analysis can be performed to determine the maximum input voltage at room temperature (+25°C) or +85°C to provide full output current while maintaining the junction temperature at or below +125°C. The answer depends on the desired output voltage, as Table 3 shows.

Table 3. Maximum Input Voltage

Output Voltage V_{OUT}	TPS73701DRB		TPS73601DRB		TPS73201DRB	
	Ambient Temperature		Ambient Temperature		Ambient Temperature	
	+25°C	+85°C	+25°C (1)	+85°C	+25°C (1)	+85°C (1)
1.8 V	4.3 V	2.8 V	5.5 V	4.3 V	5.5 V	5.5 V
2.5 V	5.0 V	3.5 V	5.5 V	5.0 V	5.5 V	5.5 V
2.8 V	5.3 V	3.8 V	5.5 V	5.3 V	5.5 V	5.5 V
3.0 V	5.5 V	4.0 V	5.5 V	5.5 V	5.5 V	5.5 V
3.3 V	5.5 V(1)	4.3 V	5.5 V	5.5 V(1)	5.5 V	5.5 V

(1) Limited by recommended operating maximum temperature, not thermal resistance.

5 Board Layout, Schematic, and Parts List

This section provides the TPS73x01DRBEVM-518 board layout and illustrations. It also provides the TPS73x01DRBEVM-518 schematic and bill of materials.

5.1 PCB Layout

Figure 1 through Figure 4 show the layout for the TPS73x01DRBEVM-518 PCB.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing TPS73x01DRBEVM-518 PCBs.

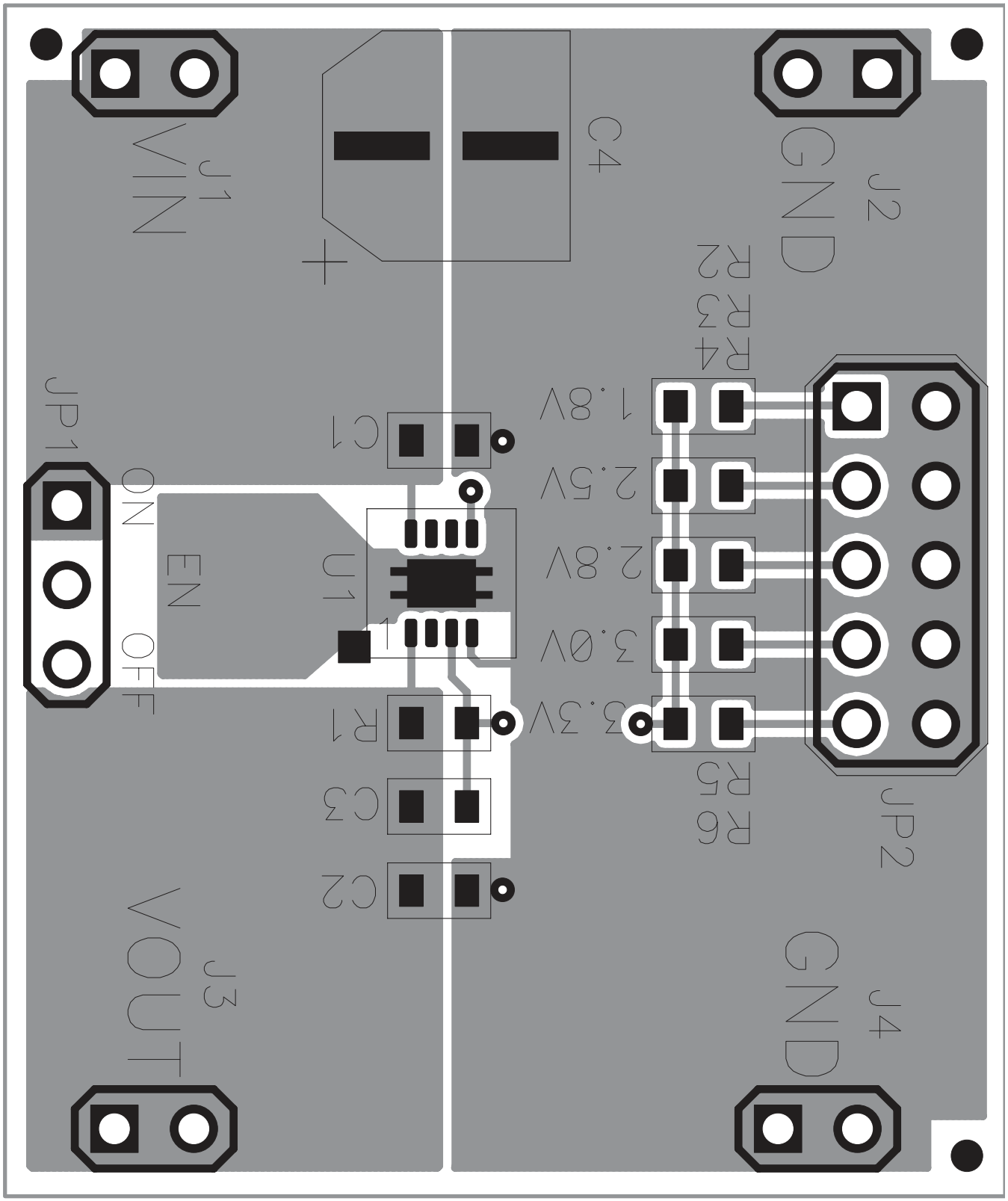

Figure 1. Assembly Layer

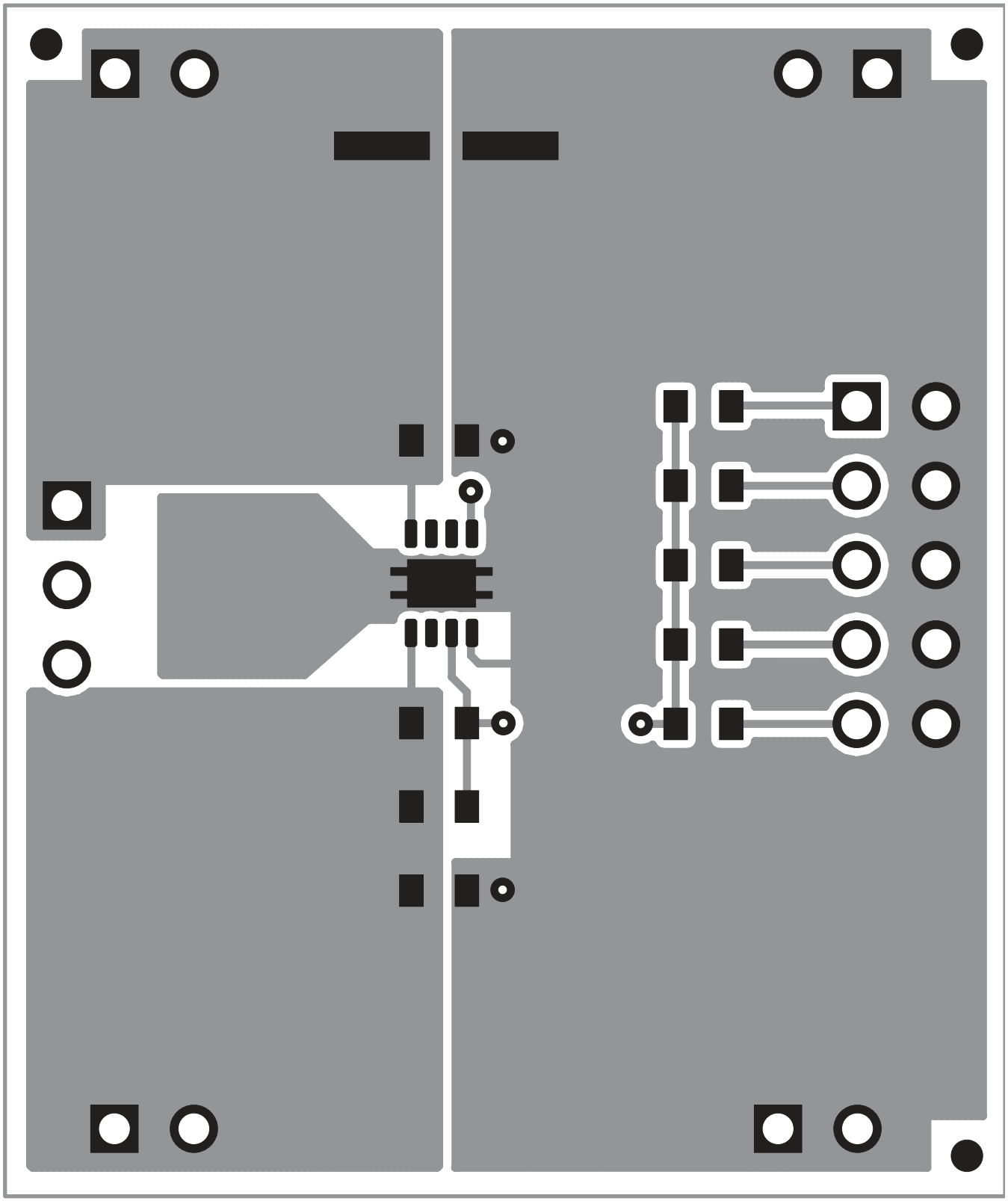

Figure 2. Top Layer Routing

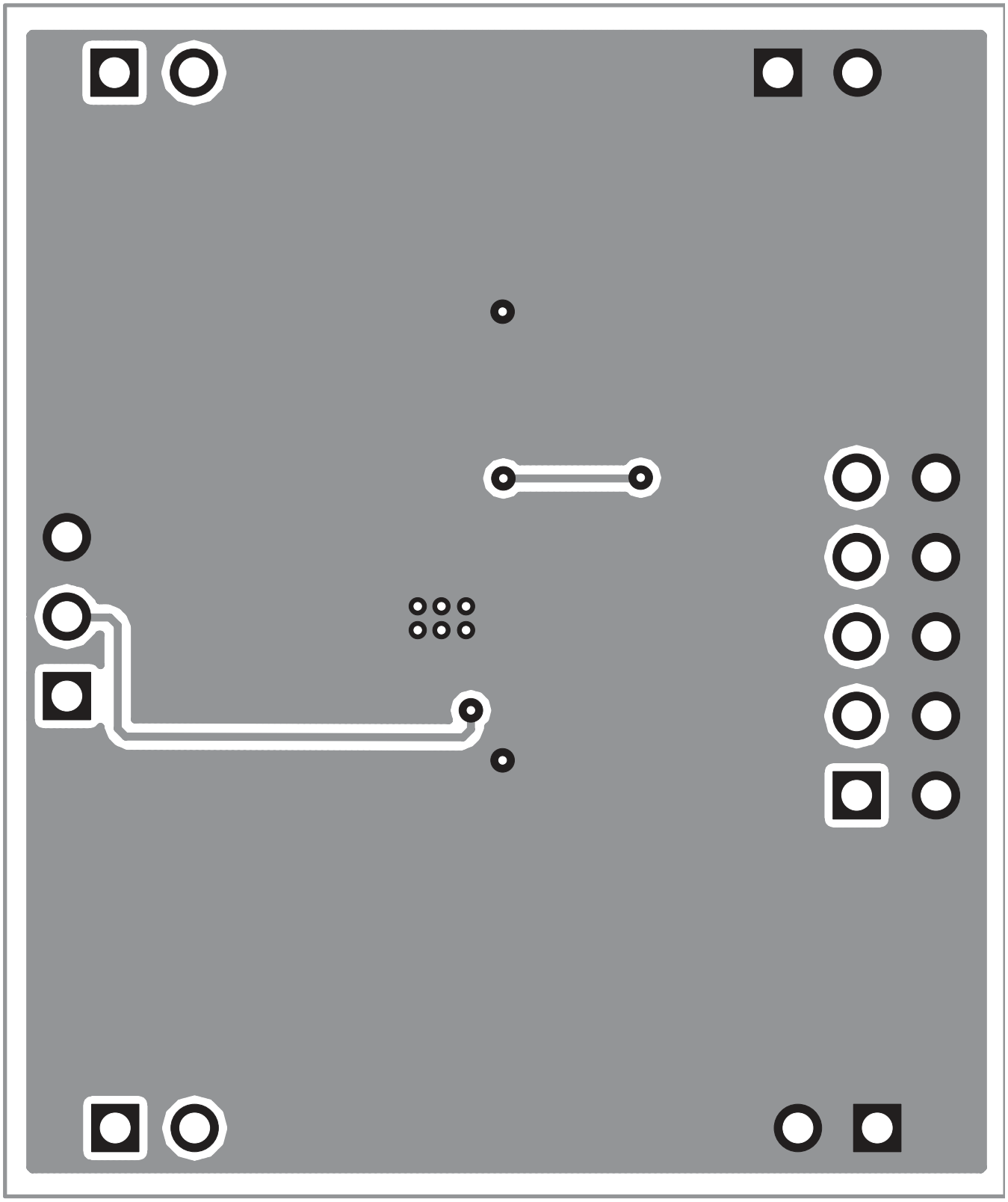

Figure 3. Bottom Layer Assembly

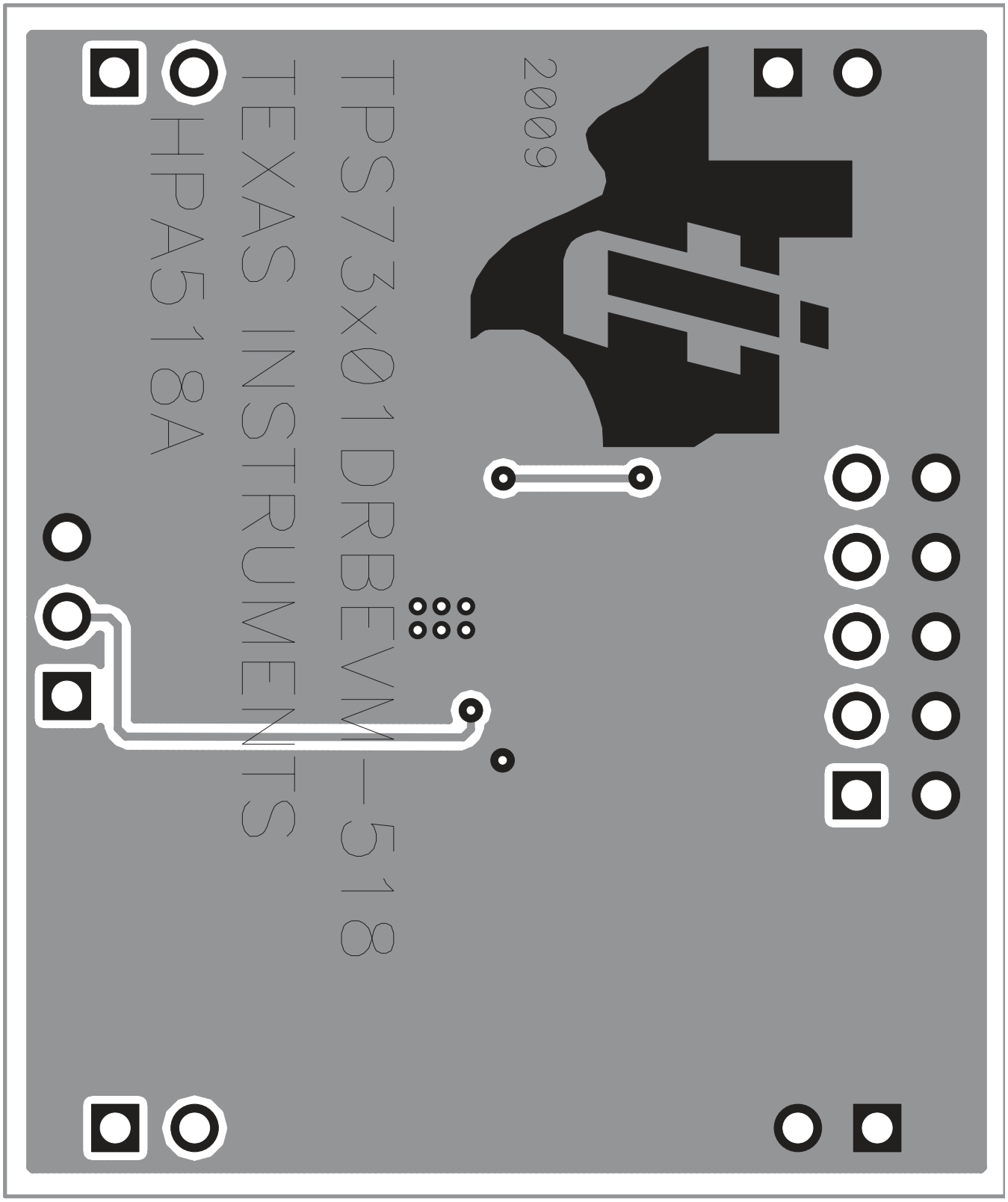

Figure 4. Bottom Layer Routing

5.2 Schematic and BOM

Figure 5 illustrates the TPS73x01DRBEVM-518 schematic. Table 4 lists the bill of materials for this EVM.

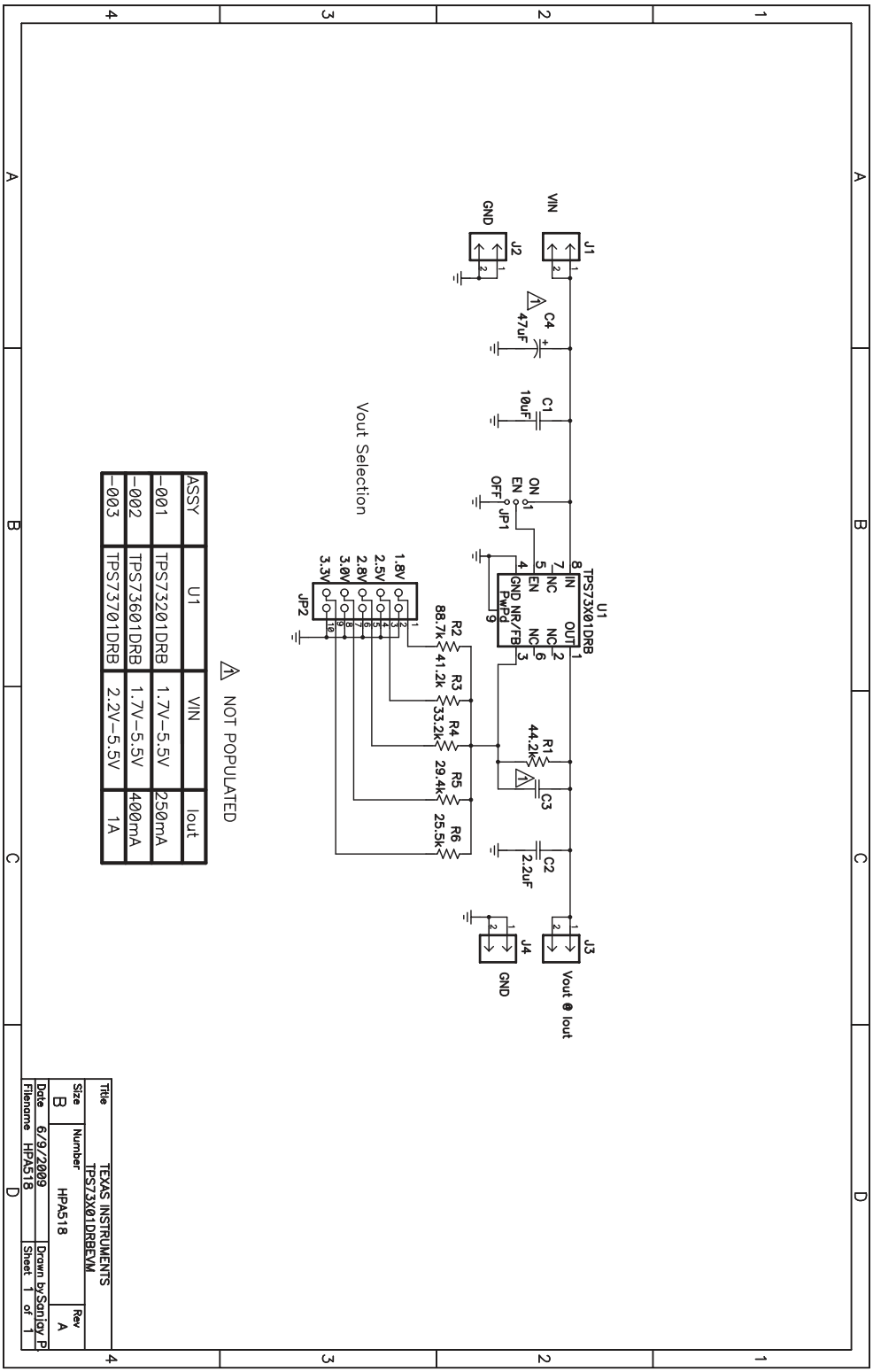

Figure 5. TPS73x01DRBEVM-518 Schematic

Table 4. TPS73x01DRBEVM-518 Bill of Materials(1) (2) (3)

-01	-02	-03	Ref Des (4)	Value	Description	Size	Part Number	Mfr
1	1	1	C1	10 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0603	Std	Std
1	1	1	C2	2.2 µF	Capacitor, ceramic, 10 V, X5R, 10%	0603	Std	Std
0	0	0	C3	—	Capacitor, ceramic, 16 V, X5R, 10%	0603	Std	Std
0	0	0	C4	47 µF	Capacitor, aluminum, 16 V, ±20%	0.260 × 0.307 inch	EEEVFK1C470P	Panasonic
4	4	4	J1, J2, J3, J4	PEC02SAAN	Header, male 2-pin, 100-mil spacing	0.100 inch × 2	PEC02SAAN	Sullins
1	1	1	JP1	PEC03SAAN	Header, 3-pin, 100-mil spacing	0.100 inch × 3	PEC03SAAN	Sullins
1	1	1	JP2	PEC05DAAN	Header, male 2x5-pin, 100-mil spacing	0.100 inch × 5 × 2	PEC05DAAN	Sullins
1	1	1	R1	44.2 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	1	1	R2	88.7 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	1	1	R3	41.2 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	1	1	R4	33.2 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	1	1	R5	29.4 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	1	1	R6	25.5 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	0	0	U1	TPS73201DRB	IC, Cap-free, NMOS, 250-mA LDO regulator with reverse current Protection	QFN-8	TPS73201DRB	Texas Instruments
0	1	0	U1	TPS73601DRB	IC, Cap-free, NMOS, 400-mA LDO regulator with reverse current Protection	QFN-8	TPS73601DRB	Texas Instruments
0	0	1	U1	TPS73701DRB	IC, 1-A LDO regulator with reverse current protection	QFN-8	TPS73701DRB	Texas Instruments
2	2	2	—	—	Shunt, 100-mil black	0.1	929950-00	3M
1	1	1	N/A	—	PCB, FR-4, 2-layer, SMOBC, 1.620 -in × 1.500 in × .062 in	—	HPA518**	Any

(1) These assemblies are ESD sensitive. ESD precautions must be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of no-clean flux is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
(4) Components can be substituted with equivalent manufacturer components except where indicated with **.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 1.7 V to 5.5 V and the output voltage range of 1.2 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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