

**Features**

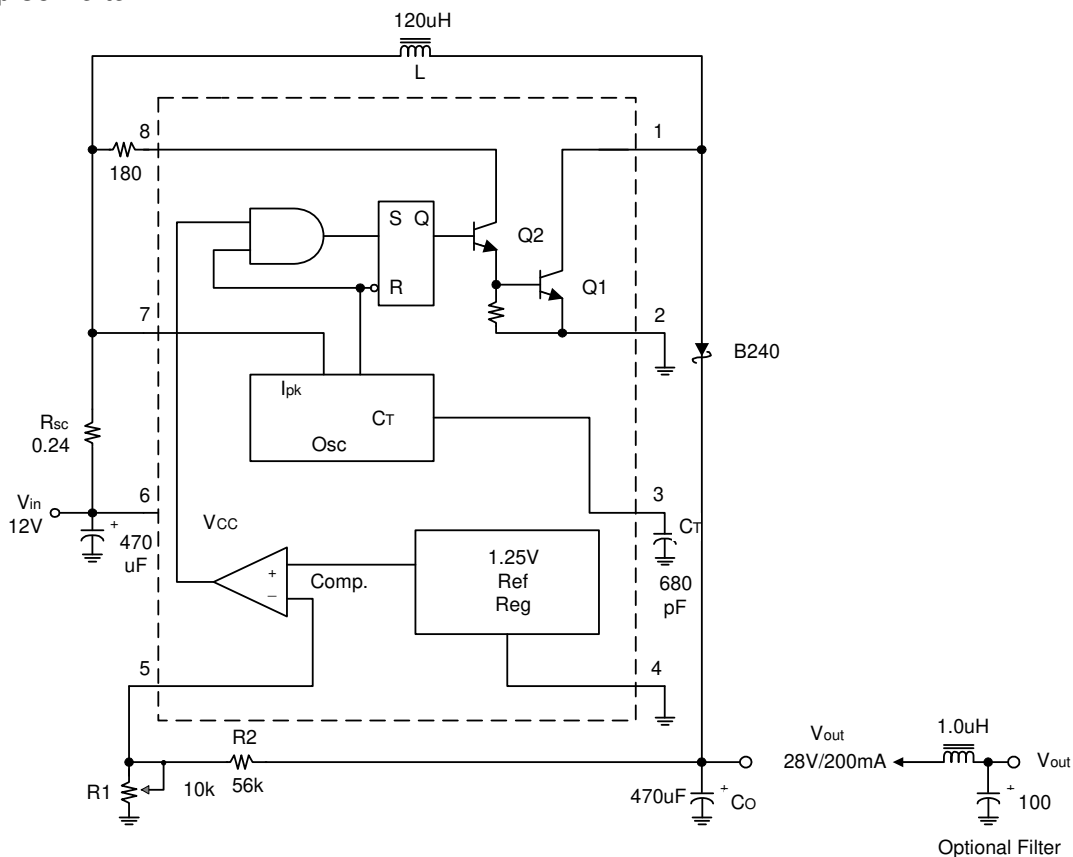
- Operation from 3.0V to 40V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.6A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference
- Lead Free packages: SOP-8L and PDIP-8L (Note 1)
- SOP-8L: Available in "Green" Molding Compound (No Br, Sb)
- Lead Free Finish/RoHS Compliant (Note 2)

**Description**

The AP34063 Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series is specifically designed for incorporating in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

**Application Circuit**

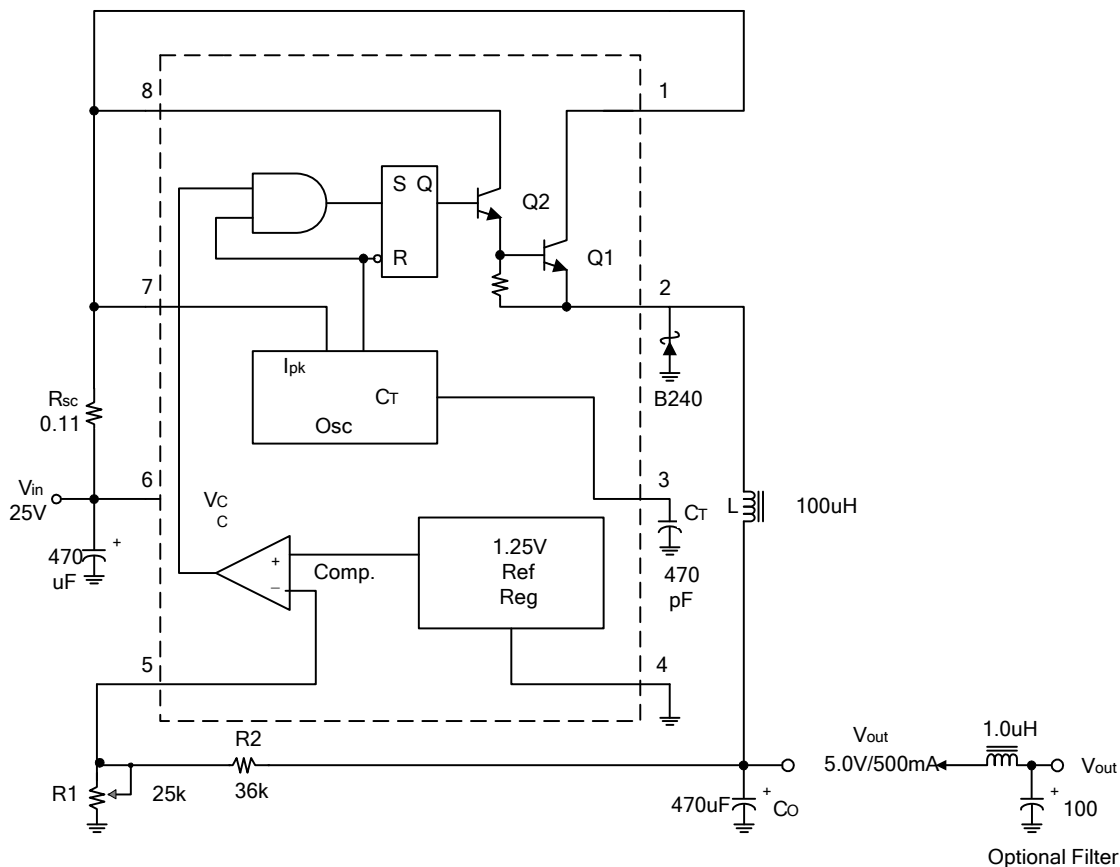
**(1) Step-Up Converter**



Test	Conditions	Results
Line Regulation	$V_{in} = 9V \text{ to } 12V, I_o = 200mA$	$20mV = \pm 0.035\%$
Load Regulation	$V_{in} = 12V, I_o = 50mA \text{ to } 200mA$	$15mV = \pm 0.035\%$
Output Ripple	$V_{in} = 12V, I_o = 200mA$	$500mV_{PP}$
Efficiency	$V_{in} = 12V, I_o = 200mA$	80%

**Application Circuit (Continued)**

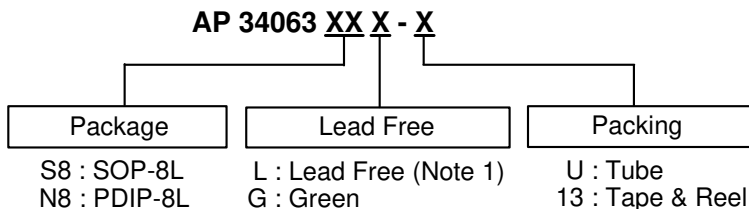
**(2) Step-Down Converter**



Test	Conditions	Results
Line Regulation	$V_{in} = 12V \text{ to } 24V, I_o = 500mA$	$20mV = \pm 0.2\%$
Load Regulation	$V_{in} = 24V, I_o = 50mA \text{ to } 500mA$	$5mV = \pm 0.05\%$
Output Ripple	$V_{in} = 24V, I_o = 500mA$	$160mV_{PP}$
Efficiency	$V_{in} = 24V, I_o = 500mA$	82%



### Ordering Information



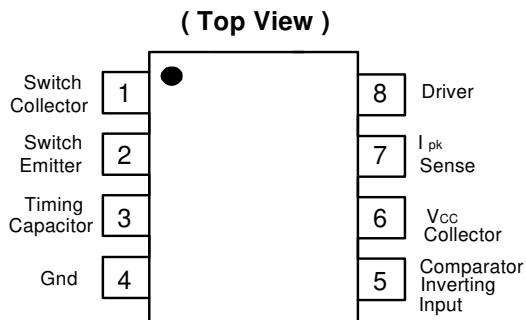
Device	Package Code	Packaging (Note 3)	Tube		13" Tape and Reel	
			Quantity	Part Number Suffix	Quantity	Part Number Suffix
AP34063S8L-13	S8	SOP-8L	NA	NA	2500/Tape & Reel	-13
AP34063S8G-13	S8	SOP-8L	NA	NA	2500/Tape & Reel	-13
AP34063N8L-U	N8	PDIP-8L	60	- U	NA	NA



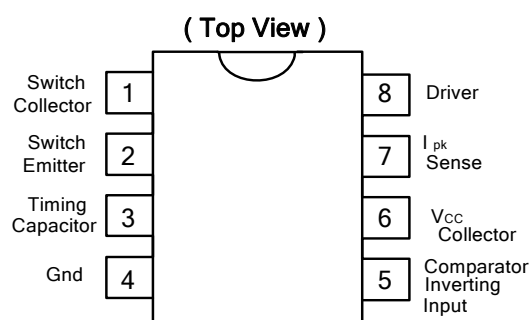
- Notes:
1. PDIP-8L is available in "Lead Free" product only.
  2. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at [http://www.diodes.com/products/lead\\_free.html](http://www.diodes.com/products/lead_free.html).
  3. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

### Pin Assignment

(1) SOP-8L



(2) PDIP-8L



## Maximum Ratings

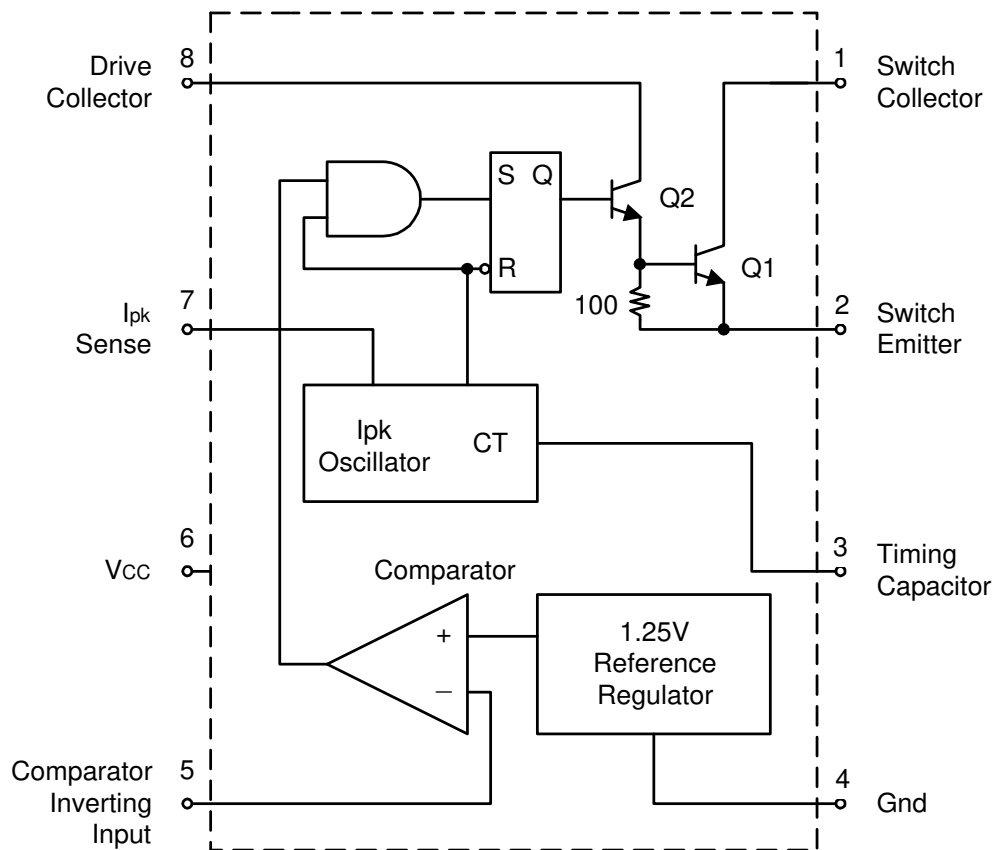
Symbol	Parameter	Value	Unit	
$V_{CC}$	Power Supply Voltage	40	V	
$V_{IR}$	Comparator Input Voltage Range	-0.3 ~ +40	V	
$V_C$ (switch)	Switch Collector Voltage	40	V	
$V_E$ (switch)	Switch Emitter Voltage ( $V_{Pin 1} = 40V$ )	40	V	
$V_{CE}$ (switch)	Switch Collector to Emitter Voltage	40	V	
$V_C$ (driver)	Driver Collector Voltage	40	V	
$I_C$ (driver)	Driver Collector Current	100	mA	
$I_{SW}$	Switch Current	1.6	A	
$P_D$	Power Dissipation and Thermal Characteristics	SOP: $T_A = 25^\circ C$	600	mW
		PDIP: $T_A = 25^\circ C$	1.25	W
		Thermal Resistance	160	$^\circ C/W$
$\theta_{JA}$				
$T_{MJ}$	Maximum Junction Temperature	+150	$^\circ C$	
$T_{OP}$	Operating Junction Temperature Range	0 ~ +105	$^\circ C$	
$T_{stg}$	Storage Temperature Range	-65 ~ +150	$^\circ C$	

Notes: 4. Maximum package power dissipation limits must be observed.  
5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

## Electrical Characteristics ( $V_{CC} = 5.0V$ , unless otherwise specified)

Symbol	Characteristics	Min	Typ.	Max	Unit
<b>OSCILLATOR</b>					
$f_{osc}$	Frequency ( $V_{Pin 5} = 0V$ , $C_T = 1.0nF$ , $T_A = 25^\circ C$ )	24	33	42	kHz
$I_{chg}$	Charge Current ( $V_{CC} = 5.0V$ to $40V$ , $T_A = 25^\circ C$ )	24	30	42	$\mu A$
$I_{dischg}$	Discharge Current ( $V_{CC} = 5.0V$ to $40V$ , $T_A = 25^\circ C$ )	140	200	260	$\mu A$
$I_{dischg} / I_{chg}$	Discharge to Charge Current Ratio (Pin 7 to $V_{CC}$ , $T_A = 25^\circ C$ )	5.2	6.5	7.5	-
$V_{ipk}$ (sense)	Current Limit Sense Voltage ( $I_{chg} = I_{dischg}$ , $T_A = 25^\circ C$ )	300	400	450	mV
<b>OUTPUT SWITCH (Note 3)</b>					
$V_{CE}$ (sat)	Saturation Voltage, Darlington Connection ( $I_{SW} = 1.0A$ , Pins 1,8 connected)	-	1.0	1.3	V
$V_{CE}$ (sat)	Saturation Voltage, Darlington Connection ( $I_{SW} = 1.0A$ , $I_D = 50mA$ , Forced $\beta \approx 20$ )	-	0.45	0.7	V
$h_{FE}$	DC Current Gain ( $I_{SW} = 1.0A$ , $V_{CE} = 5.0V$ , $T_A = 25^\circ C$ )	50	75	-	-
$I_C$ (off)	Collector Off-State Current ( $V_{CE} = 40V$ )	-	0.01	100	$\mu A$
<b>COMPARATOR</b>					
$V_{th}$	Threshold Voltage	-	-	-	V
-	$T_A = 25^\circ C$	1.225	1.25	1.275	-
-	$T_A = 0^\circ C \sim 70^\circ C$	1.21	-	1.29	-
$Reg_{line}$	Threshold Voltage Line Regulation ( $V_{CC} = 3.0V$ to $40V$ )	-	1.4	6.0	mV
<b>TOTAL DEVICE</b>					
$I_{CC}$	Supply Current ( $V_{CC} = 5.0V$ to $40V$ , $C_T = 1.0nF$ , Pin 7 = $V_{CC}$ , $V_{Pin 5} > V_{th}$ Pin 2 = Gnd, remaining pins open)	-	-	3.5	mA

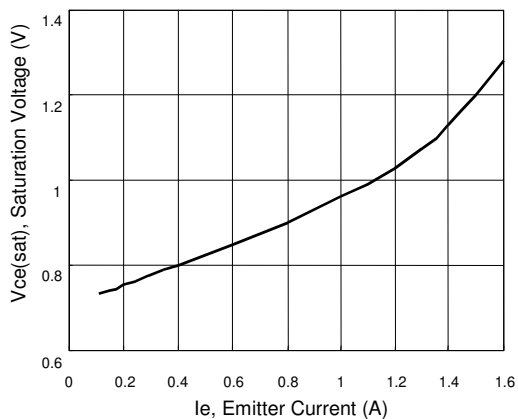
**Representative Schematic Diagram**



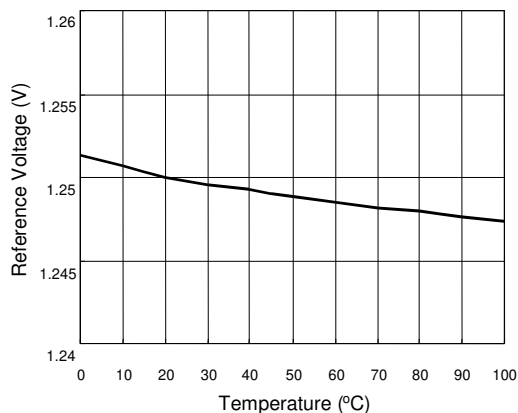
(Bottom View)

**Typical Performance Characteristics**

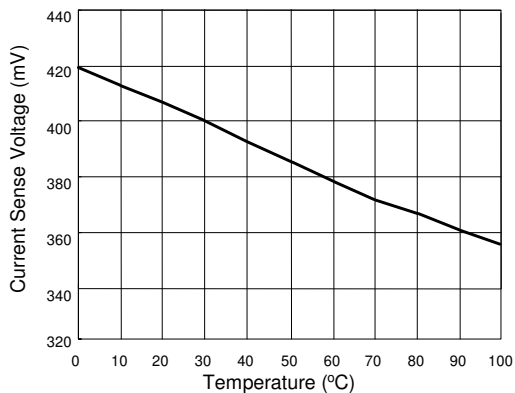
**Figure 1. Vce(sat) versus Ie**



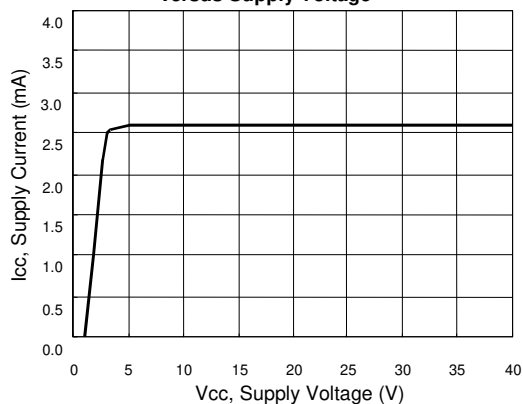
**Figure 2. Reference Voltage versus Temp.**



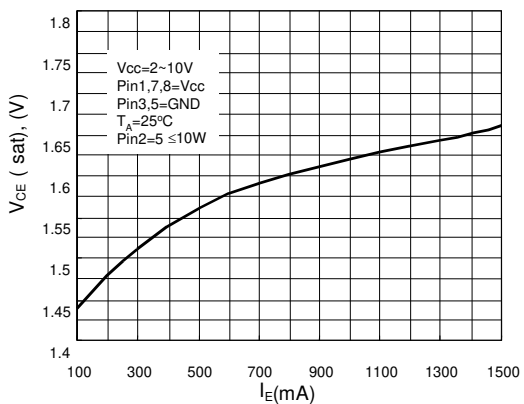
**Figure 3. Current Limit Sense Voltage versus Temperature**



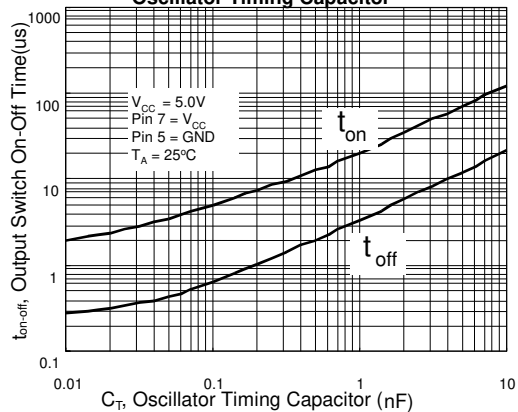
**Figure 4. Standby Supply Current versus Supply Voltage**



**Figure 5. Emitter Follower Configuration Output Saturation Voltage vs. Emitter Current**



**Figure 6. Output Switch On-Off Time versus Oscillator Timing Capacitor**



**Design Formula Table**

Calculation	Step-Up			Step-Down			Voltage-Inverting		
$t_{on} / t_{off}$	$V_{out} + V_F - V_{in (min)}$			$V_{out} + V_F$			$ V_{out}  + V_F$		
	$V_{in (min)} - V_{sat}$			$V_{in(min)} - V_{sat} - V_{out}$			$V_{in} - V_{sat}$		
$(t_{on} + t_{off})$	$1/f$			$1/f$			$1/f$		
$t_{off}$	$t_{on} + t_{off}$			$t_{on} + t_{off}$			$t_{on} + t_{off}$		
	$t_{on}$	+1		$t_{on}$	+1		$t_{on}$	+1	
$t_{off}$	$t_{off}$			$t_{off}$					
$t_{on}$	$(t_{on} + t_{off}) - t_{off}$			$(t_{on} + t_{off}) - t_{off}$			$(t_{on} + t_{off}) - t_{off}$		
$C_T$	$4.0 \times 10^{-5} t_{on}$			$4.0 \times 10^{-5} t_{on}$			$4.0 \times 10^{-5} t_{on}$		
$I_{pk} (switch)$	$2I_{out (max)} (t_{on} / t_{off} + 1)$			$2I_{out (max)}$			$2I_{out (max)} (t_{on} / t_{off} + 1)$		
$R_{sc}$	$0.3 / I_{pk} (switch)$			$0.3 / I_{pk} (switch)$			$0.3 / I_{pk} (switch)$		
$L (min)$	$(V_{in (min)} - V_{sat})$	$t_{on (max)}$		$(V_{in (min)} - V_{sat} - V_{out})$	$t_{on (max)}$		$(V_{in (min)} - V_{sat})$	$t_{on (max)}$	
	$I_{pk} (switch)$			$I_{pk} (switch)$			$I_{pk} (switch)$		
$C_O$	9	$I_{out} t_{on}$		$I_{pk} (switch) (t_{off} + t_{on})$			$I_{out} t_{on}$		
		$V_{ripple (pp)}$		$8V_{ripple (pp)}$			$V_{ripple (pp)}$		

$V_{sat}$  = Saturation voltage of the output switch.

$V_F$  = Forward voltage drop of the output rectifier.

**The following power supply characteristics must be chosen:**

$V_{in}$  - Nominal input voltage.

$V_{out}$  - Desired output voltage,  $|V_{out}| = 1.25 (1+R2/R1)$

$I_{out}$  - Desired output current.

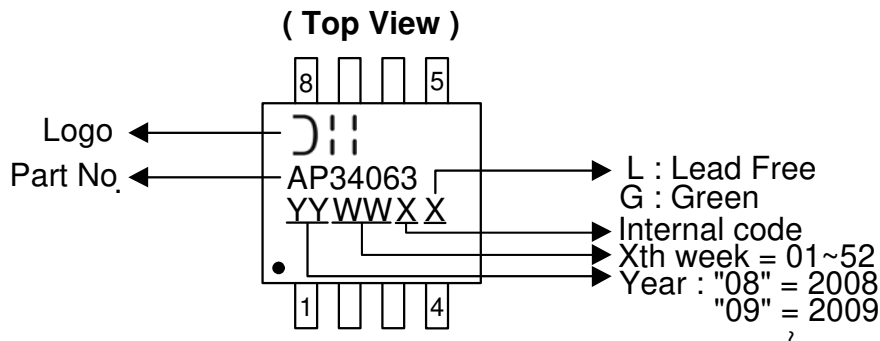
$f_{min}$  - Minimum desired output switching frequency at the selected values of  $V_{in}$  and  $I_o$ .

$V_{ripple(pp)}$  - Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

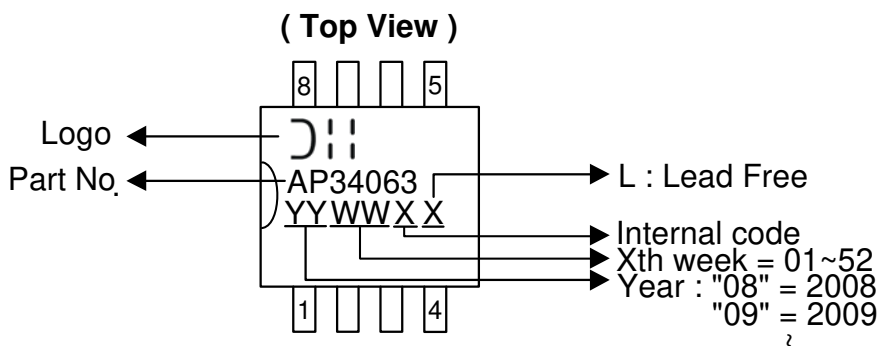


**Marking Information**

(1) SOP-8L

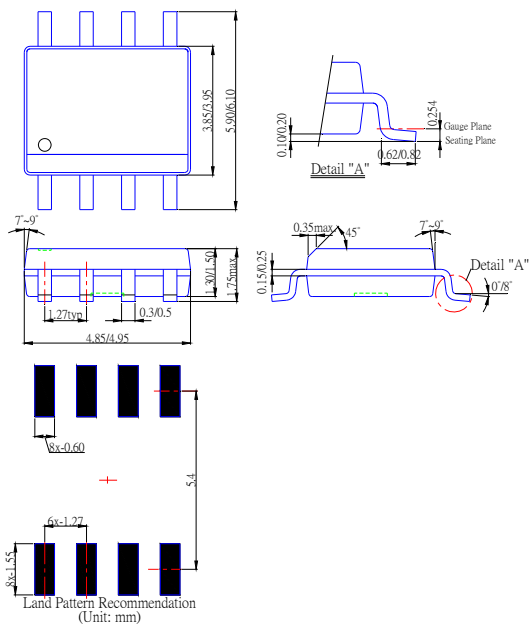


(2) PDIP-8L

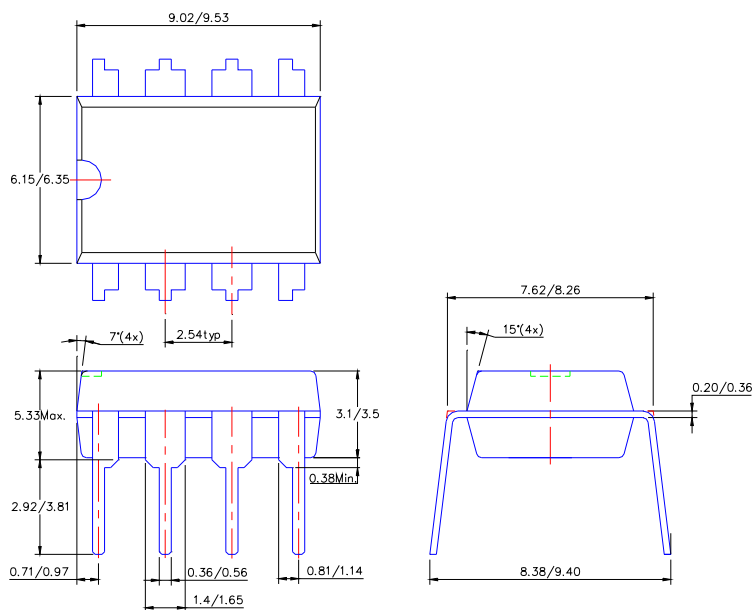


**Package Information (All Dimensions in mm)**

**(1) SOP-8L**



**(2) PDIP-8L**



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