MC10H606, MC100H606

Registered Hex TTL to PECL Translator

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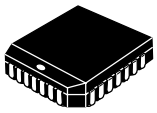
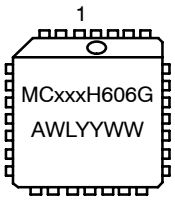


PLCC−28
FN SUFFIX
CASE 776

MARKING DIAGRAM*



xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Description

The MC10/100H606 is a 6−bit, registered, single supply TTL to PECL translator. The device features differential PECL outputs as well as a choice between either a differential PECL clock input or a TTL clock input. The asynchronous master reset control is a PECL level input.

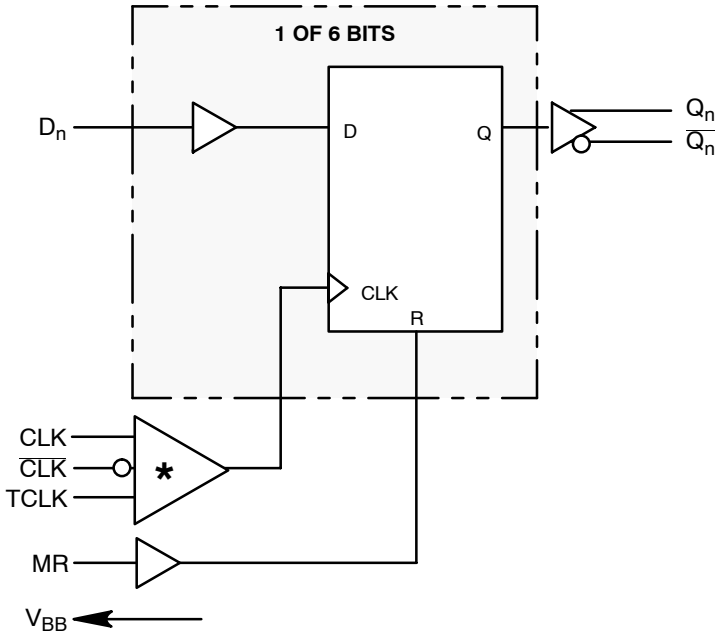
With its differential PECL outputs and TTL inputs the H606 device is ideally suited for the transmit function of a HPPI bus type board−to−board interface application. The on chip registers simplify the task of synchronizing the data between the two boards.

The device is available in either ECL standard: the MECL 10H™ device is compatible with MECL 10KH logic levels, with a V_{CC} of +5.0 V while the 100H device is compatible with 100K logic levels, with a V_{CC} of +5.0 V.

Features

- Differential 50 Ω ECL Outputs
- Choice Between Differential PECL or TTL Clock Input
- Single Power Supply
- Multiple Power and Ground Pins to Minimize Noise
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



* 1. When using PECL inputs, TCLK must be tied to ground (0 V).
2. When using only one PECL input, the unused PECL input must be tied to V_{BB}, and TCLK must be tied to ground (0 V).
3. When using TCLK, both PECL inputs must be tied to ground (0 V).

Figure 1. Logic Diagram

Table 1. TRUTH TABLE

Dn	MR	TCLK/CLK	Qn+1
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

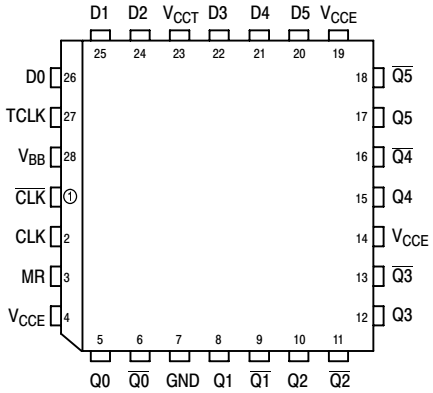


Figure 2. Pinout: PLCC−28
(Top View)

Table 2. PIN NAMES

PIN	FUNCTION
D0 – D5	TTL Data Inputs
CLK, $\overline{CLK}$	Differential PECL Clock Input
TCLK	TTL Clock Input
MR	PECL Master Reset Input
Q0 – Q5	True PECL Outputs
$\overline{Q0}$ – $\overline{Q5}$	Inverted PECL Outputs
V_{CCE}	PECL V_{CC} (+5.0 V)
V_{CCT}	TTL V_{CC} (+5.0 V)
GND	TTL/PECL Ground

Table 3. 10H PECL DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0 V ±5%)

			T_A = 0°C		T_A = 25°C		T_A = 85°C		
Symbol	**Characteristic**	**Condition**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
I_{INH}	Input HIGH Current			255		175		175	μA
I_{INL}	Input LOW Current			0.5		0.5		0.5	μA
V_{IH}	Input HIGH Voltage (Note 4)	V_{CCT} = 5.0 V	3830	4160	3870	4190	3930	4280	mV
V_{IL}	Input LOW Voltage (Note 4)	V_{CCT} = 5.0 V	3050	3520	3050	3520	3050	3555	mV
V_{OH}	Output HIGH Voltage (Note 4)	V_{CCT} = 5.0 V	3980	4160	4020	4190	4080	4270	mV
V_{OL}	Output LOW Voltage (Note 4)	V_{CCT} = 5.0 V	3050	3370	3050	3370	3050	3400	mV
V_{BB}	Reference Voltage (Note 4)	V_{CCT} = 5.0 V	3600	3710	3630	3730	3670	3790	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. PECL V_{IL}, V_{IH}, V_{OL}, V_{OH} V_{BB} are given for V_{CCT} = V_{CCE} = 5.0 V and will vary 1:1 with the power supply.

Table 4. 100H PECL DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0 V ±5%)

			T_A = 0°C		T_A = 25°C		T_A = 85°C		
Symbol	**Characteristic**	**Condition**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
I_{INH}	Input HIGH Current			255		175		175	μA
I_{INL}	Input LOW Current			0.5		0.5		0.5	μA
V_{IH}	Input HIGH Voltage (Note 5)	V_{CCT} = 5.0 V	3835	4120	3835	4120	3835	4120	mV
V_{IL}	Input LOW Voltage (Note 5)	V_{CCT} = 5.0 V	3190	3525	3190	3525	3190	3525	mV
V_{OH}	Output HIGH Voltage (Note 5)	V_{CCT} = 5.0 V	3975	4120	3975	4120	3975	4120	mV
V_{OL}	Output LOW Voltage (Note 5)	V_{CCT} = 5.0 V	3190	3380	3190	3380	3190	3380	mV
V_{BB}	Output Bias Voltage (Note 5)	V_{CCT} = 5.0 V	3600	3720	3600	3720	3600	3720	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. PECL V_{IL}, V_{IH}, V_{OL}, V_{OH} V_{BB} are given for V_{CCT} = V_{CCE} = 5.0 V and will vary 1:1 with the power supply.

Table 5. DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0 V ±5%)

			T_A = 0°C			T_A = + 25°C			T_A = + 85°C			
Symbol	**Characteristic**	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{CCL}	Supply Current	Outputs LOW		18	30		18	30		18	30	mA
I_{CCH}	Supply Current	Outputs HIGH		13	25		13	25		13	25	mA
I_{GND}	Supply Current			75	90		75	90		75	95	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. TTL DC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0 V ±5%)

Symbol	Characteristic	Condition	T_A = 0°C		T_A = 25°C		T_A = 85°C		Unit
			Min	Max	Min	Max	Min	Max	
V_{IH}	Input HIGH Voltage		2.0		2.0		2.0		V
V_{IL}	Input LOW Voltage			0.8		0.8		0.8	V
V_{IK}	Input Clamp Voltage	I_{IN} = −18 mA		−1.2		−1.2		−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V V_{IN} = 7.0 V		20 100		20 100		20 100	V
I_{IL}	Input LOW Current	V_{IN} = 0.5 V		−0.6		−0.6		−0.6	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 7. AC CHARACTERISTICS (V_{CCT} = V_{CCE} = 5.0 V ±5%)

Symbol	Characteristic	Condition	T_A = 0°C			T_A = + 25°C			T_A = + 85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PD}	Propagation Delay TCLK++	50 Ω to V_{CC}−2.0 V	1.75		3.75	1.75	3.00	3.75	1.75		3.75	ns
t_{PD}	Propagation Delay TCLK+−	50 Ω to V_{CC}−2.0 V	1.75		3.75	1.75	3.00	3.75	1.75		3.75	ns
t_{PD}	Propagation Delay CLK++	50 Ω to V_{CC}−2.0 V	1.50		3.50	1.50	2.50	3.50	1.50		3.50	ns
t_{PD}	Propagation Delay CLK+−	50 Ω to V_{CC}−2.0 V	1.50		3.50	1.50	2.50	3.50	1.50		3.50	ns
t_{PD}	Propagation Delay MR+−	50 Ω to V_{CC}−2.0 V	1.50		3.50	1.50	2.50	3.50	1.75		3.75	ns
t_{SKEW}	Device Skew Part−to−Part Within Device	50 Ω to V_{CC}−2.0 V			2.0 0.5		1.0 0.3	2.0 0.5			2.0 0.5	ns
t_S	Setup Time	50 Ω to V_{CC}−2.0 V	1.5	0.5		1.5	0.5		1.5	0.5		ns
t_H	Hold Time	50 Ω to V_{CC}−2.0 V	1.5	0.5		1.5	0.5		1.5	0.5		ns
t_{PW}	Minimum Pulse Width CLK	50 Ω to V_{CC}−2.0 V	1.5			1.5	1.0		1.5			ns
t_{PW}	Minimum Pulse Width MR	50 Ω to V_{CC}−2.0 V	1.5			1.5			1.5			ns
t_r	Rise Time	50 Ω to V_{CC}−2.0 V			2.0		1.0	2.0			2.0	ns
t_f	Fall Time	50 Ω to V_{CC}−2.0 V			2.0		1.0	2.0			2.0	ns
$t_{RES/REC}$	Reset/Recovery Time	50 Ω to V_{CC}−2.0 V	2.5	2.0		2.5	2.0		2.5	2.0		ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

ORDERING INFORMATION

Device	Package	Shipping†
MC10H606FN	PLCC−28	37 Units / Rail
MC10H606FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC10H606FNR2	PLCC−28	500 / Tape & Reel
MC10H606FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel
MC100H606FN	PLCC−28	37 Units / Rail
MC100H606FNG	PLCC−28 (Pb−Free)	37 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

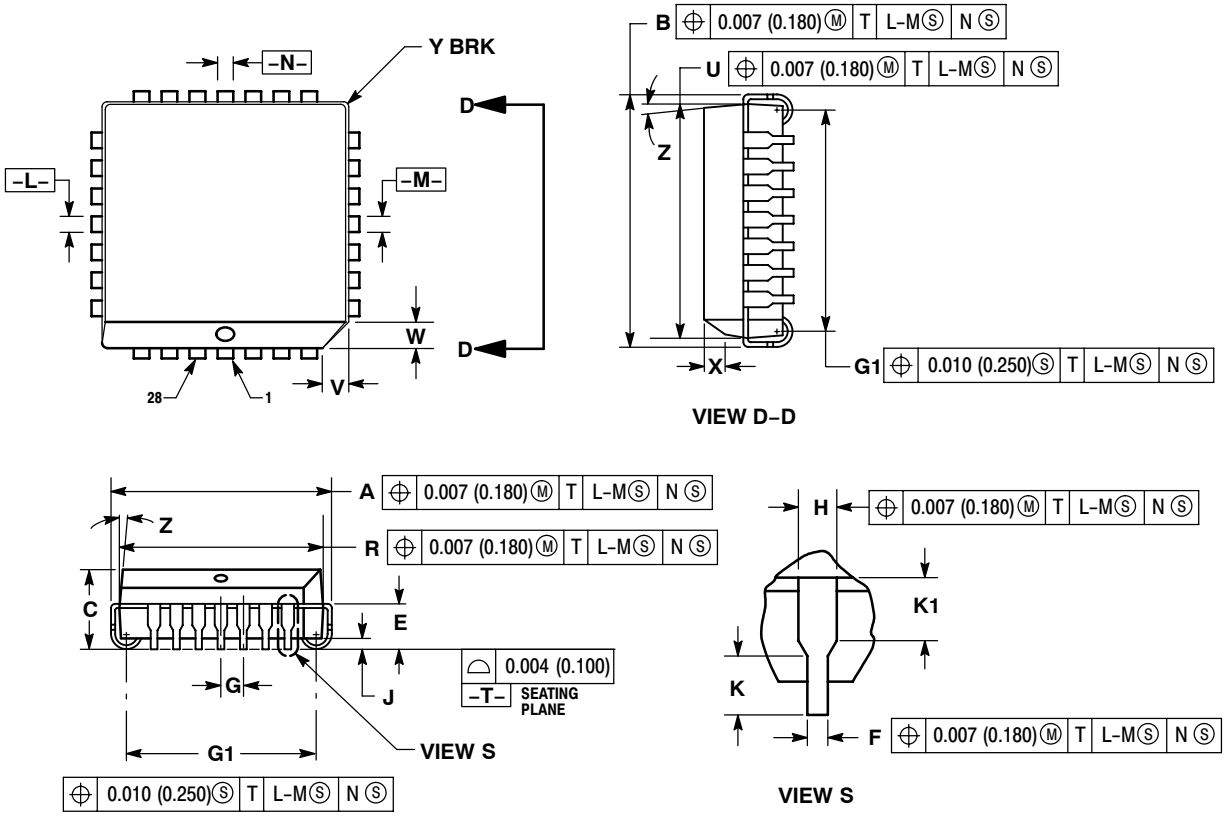
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

PLCC−28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776−02
ISSUE E



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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MECL 10 H is a trademark of Motorola, Inc.

PUBLICATION ORDERING INFORMATION

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