OptiMOS®3 M-Series Power-MOSFET

Features

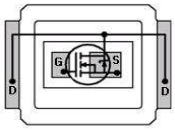
- Pb-free plating; RoHS compliant
- Dual sided cooling
- Low profile (<0.7 mm)
- 100% avalanche tested
- Qualified for consumer level application
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Optimized for high switching frequency DC/DC converter
- Low parasitic inductance
- Compatible with DirectFET® package SQ footprint and outline [1)]

Product Summary

V_{DS}	30	V
$R_{DS(on),max}$	4.5	mΩ
I_D	63	A

MG-WDSON-2

Type	Package	Outline	Marking
BSF045N03MQ3 G	MG-WDSON-2	SQ	0503



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	63	A
		V_{GS}=10 V, T_C=100 °C	40	
		V_{GS}=10 V, T_A=25 °C, R_{thJA}=58 K/W[2)]	18	
Pulsed drain current[3)]	$I_{D,pulse}$	T_C=25 °C	252	
Avalanche current, single pulse[4)]	I_{AS}	T_C=25 °C	35	
Avalanche energy, single pulse	E_{AS}	I_D=35 A, R_{GS}=25 Ω	30	mJ
Gate source voltage	V_{GS}		±20	V

[1)] DirectFET® is a trademark of International Rectfier Corporation
BSF045N03MQ3 G uses DirectFET® technology licensed from International Rectifier Corporation

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	T_C=25 °C	28	W
		T_A=25 °C, R_{thJA}=58 K/W[2)]	2.2	
Operating and storage temperature	T_j, T_{stg}		-40 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}	bottom	-	1.0		K/W
		top	-	-	4.5	
Device on PCB	R_{thJA}	6 cm^2 cooling area[2)]	-	-	58	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 µA	1	-	2.2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=20 A	-	4.7	5.9	mΩ
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=20 A	-	3.8	4.5	
Gate resistance	R_G		-	1.3	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=30 A	38	76	-	S

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3)] See figure 3 for more detailed information

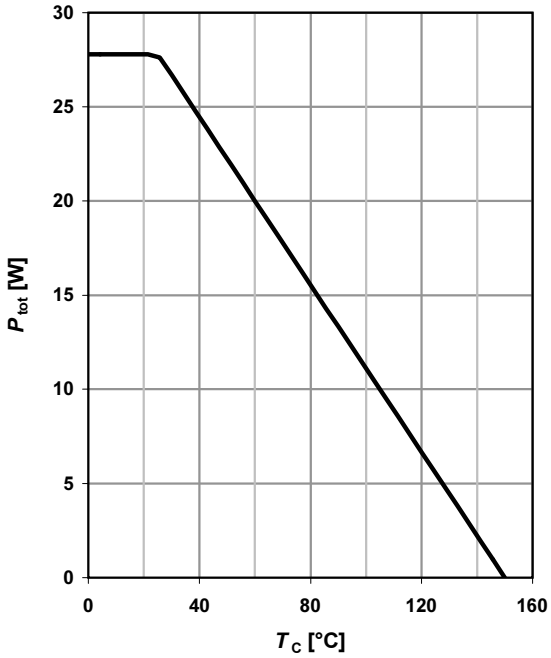
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	2600	-	pF
Output capacitance	C_{oss}		-	790	-	
Reverse transfer capacitance	C_{rss}		-	54	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω	-	5.8	-	ns
Rise time	t_r		-	4.0	-	
Turn-off delay time	$t_{d(off)}$		-	25	-	
Fall time	t_f		-	3.2	-	
Gate Charge Characteristics[5]						
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_D=20 A, V_{GS}=0 to 4.5 V	-	7.3	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	4.2	-	
Gate to drain charge	Q_{gd}		-	3.6	-	
Switching charge	Q_{sw}		-	6.8	-	
Gate charge total	Q_g		-	16	-	
Gate plateau voltage	$V_{plateau}$		-	2.8	-	V
Gate charge total	Q_g	V_{DD}=15 V, I_D=20 A, V_{GS}=0 to 10 V	-	34	-	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V	-	14.3	-	
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	21	-	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	25	A
Diode pulse current	$I_{S,pulse}$		-	-	252	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=20 A, T_j=25 °C	-	0.83		V
Reverse recovery charge	Q_{rr}	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs	-	-	16	nC

[4] See figure 13 for more detailed information

[5] See figure 16 for gate charge parameter definition

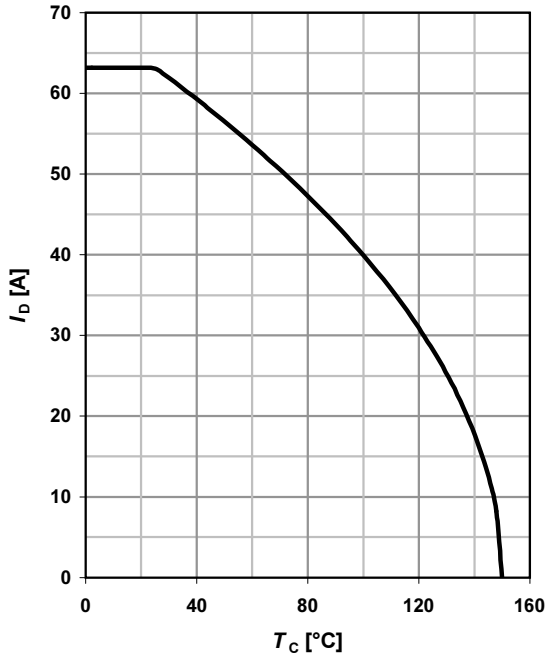
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

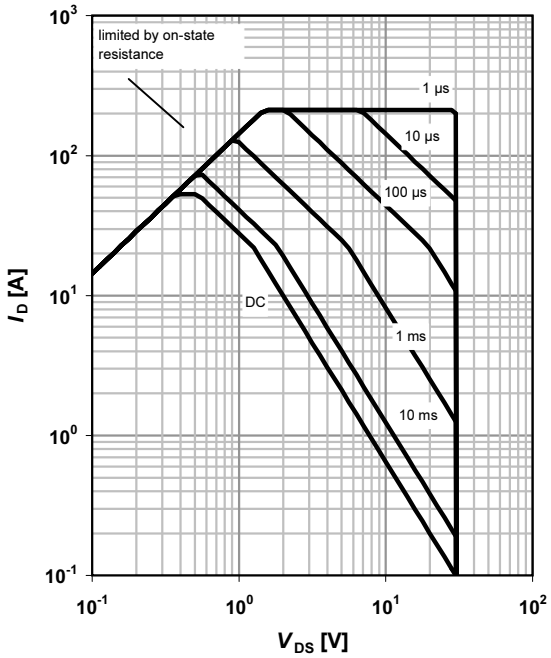
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; T_C=25 °C; D=0

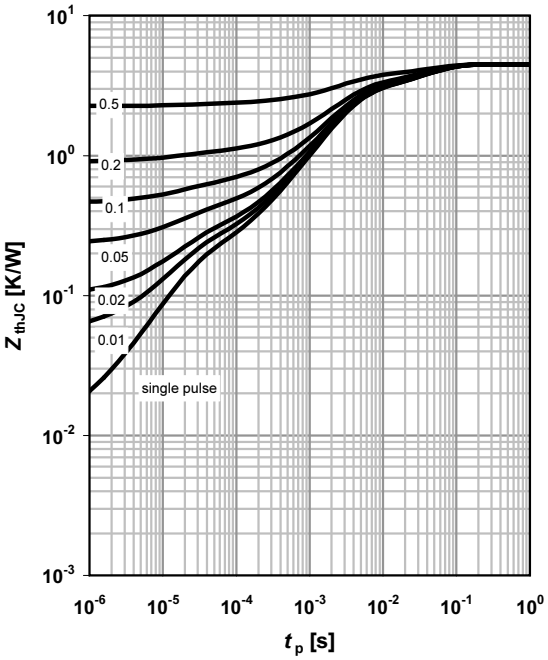
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

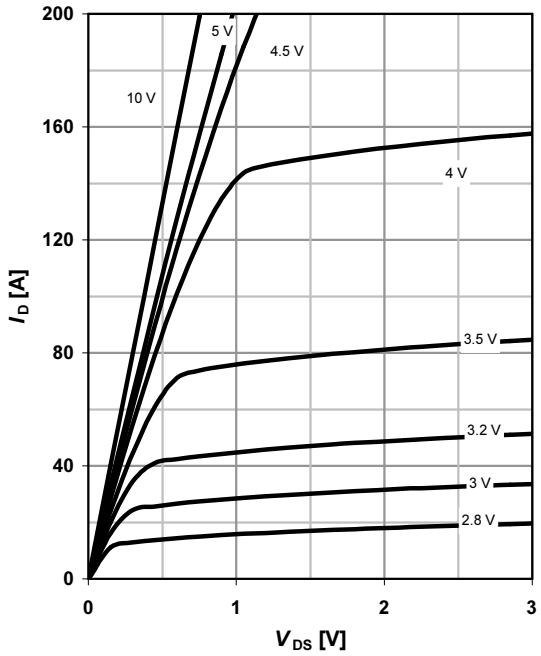
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

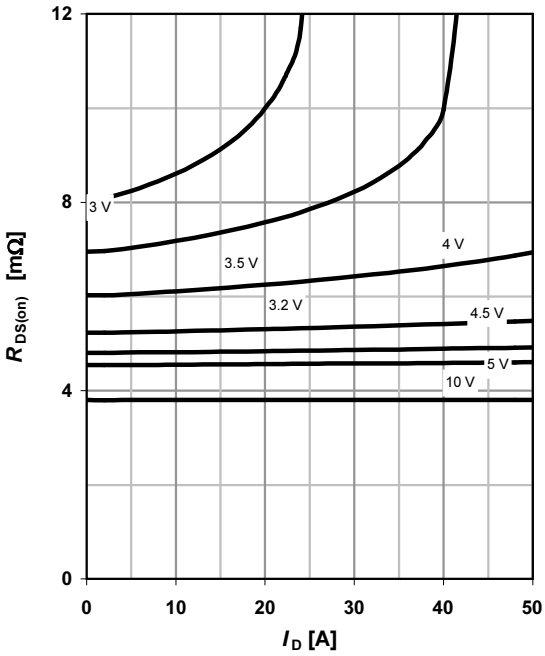
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

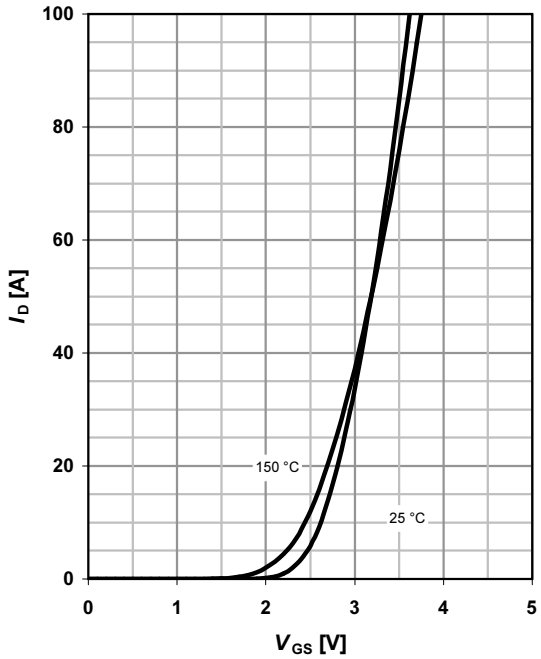
parameter: V_{GS}



7 Typ. transfer characteristics

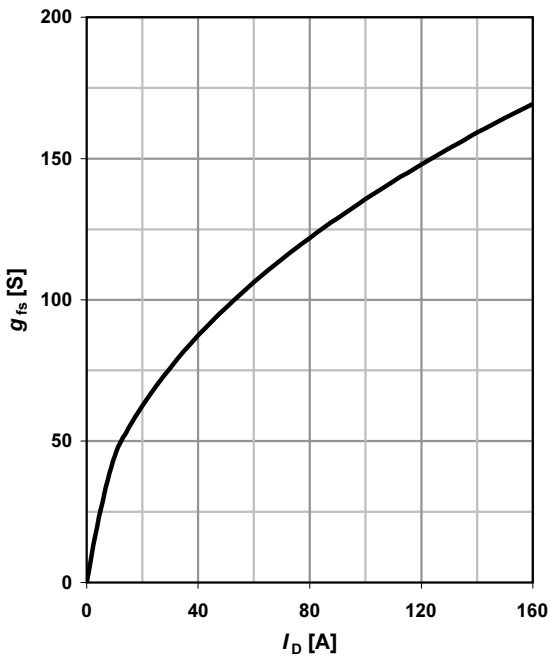
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



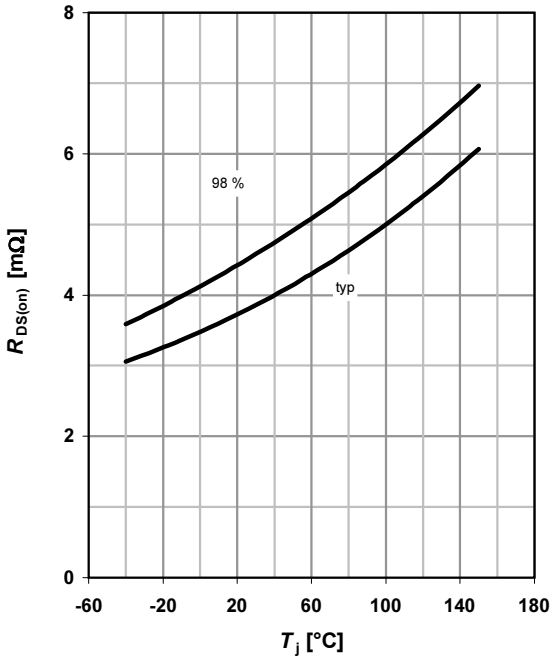
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



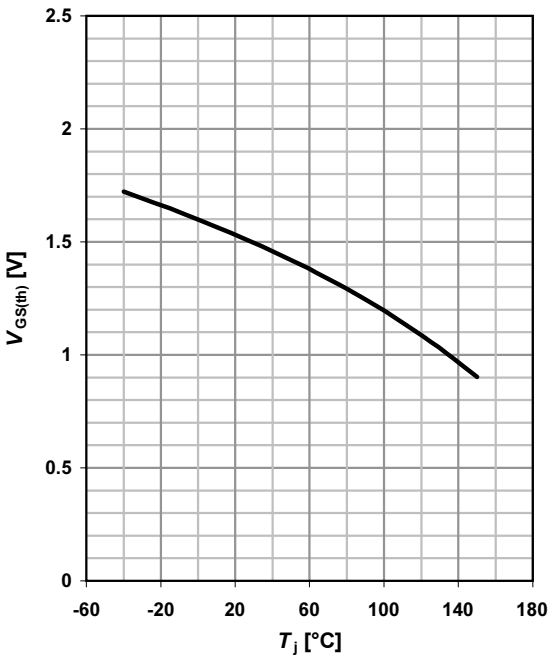
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=20 A; V_{GS}=10 V



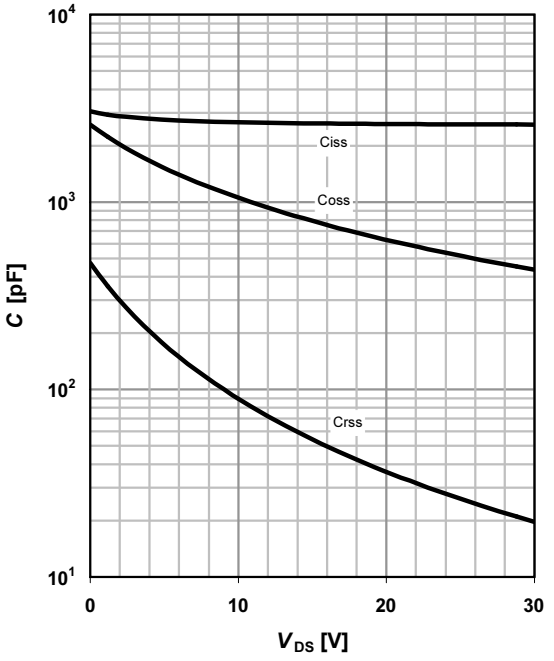
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA



11 Typ. capacitances

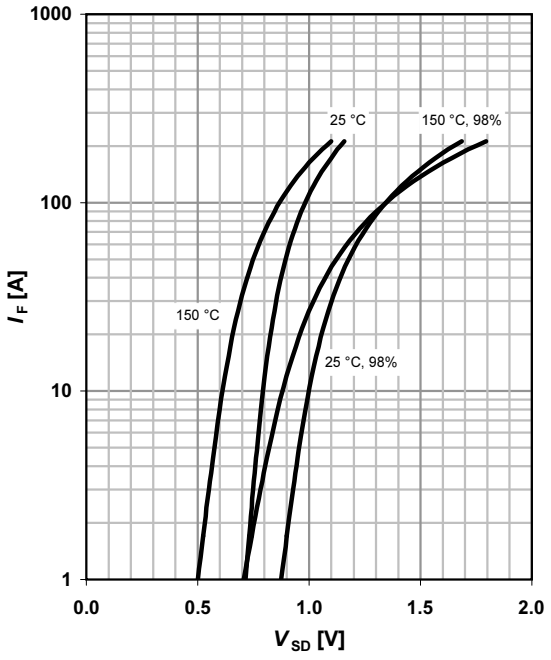
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

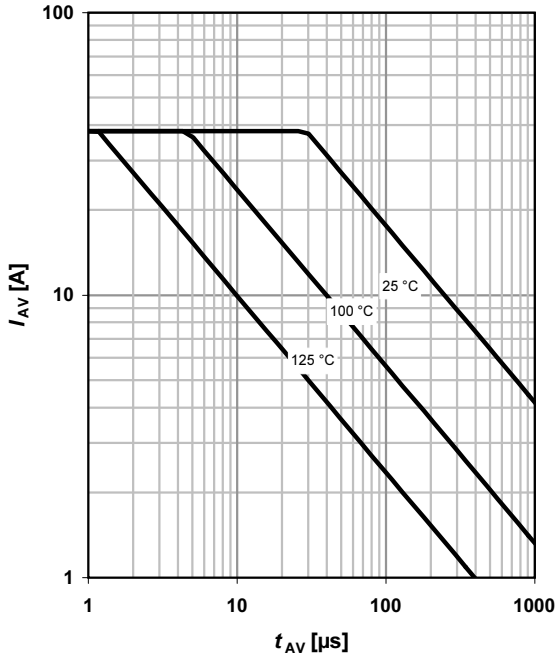
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

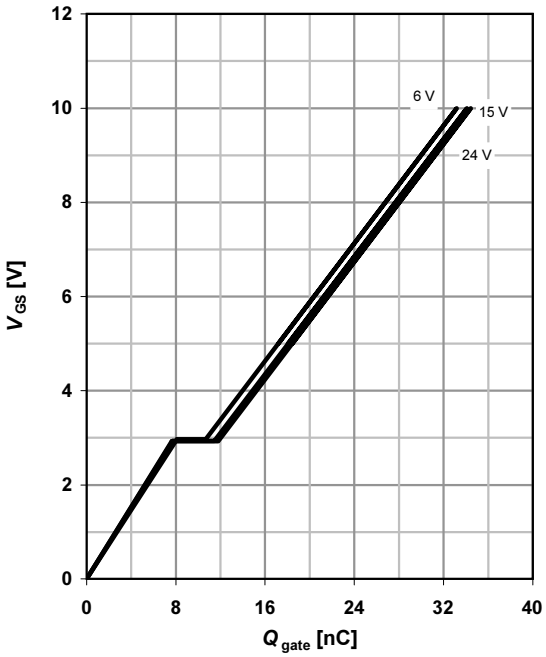
parameter: $T_{j(start)}$



14 Typ. gate charge

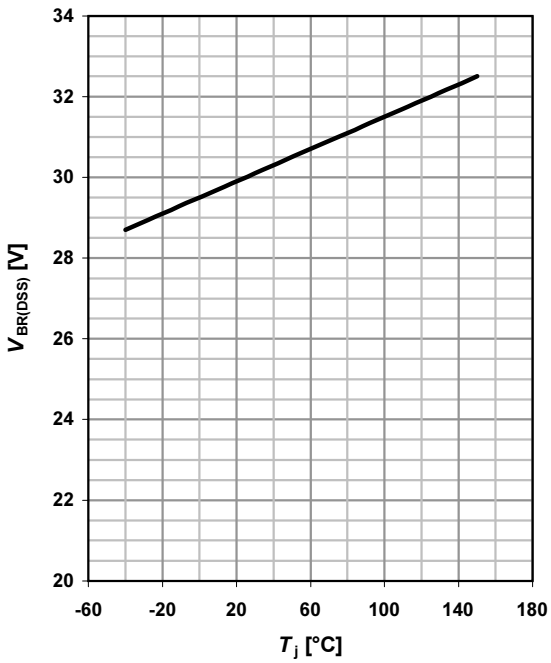
V_{GS}=f(Q_{gate}); I_D=20 A pulsed

parameter: V_{DD}

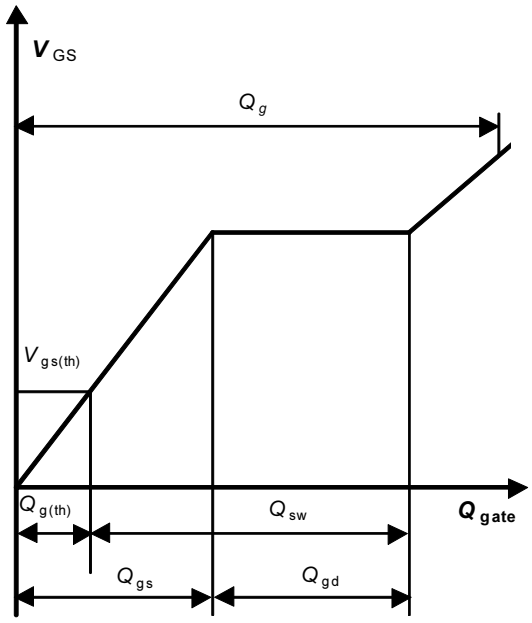


15 Drain-source breakdown voltage

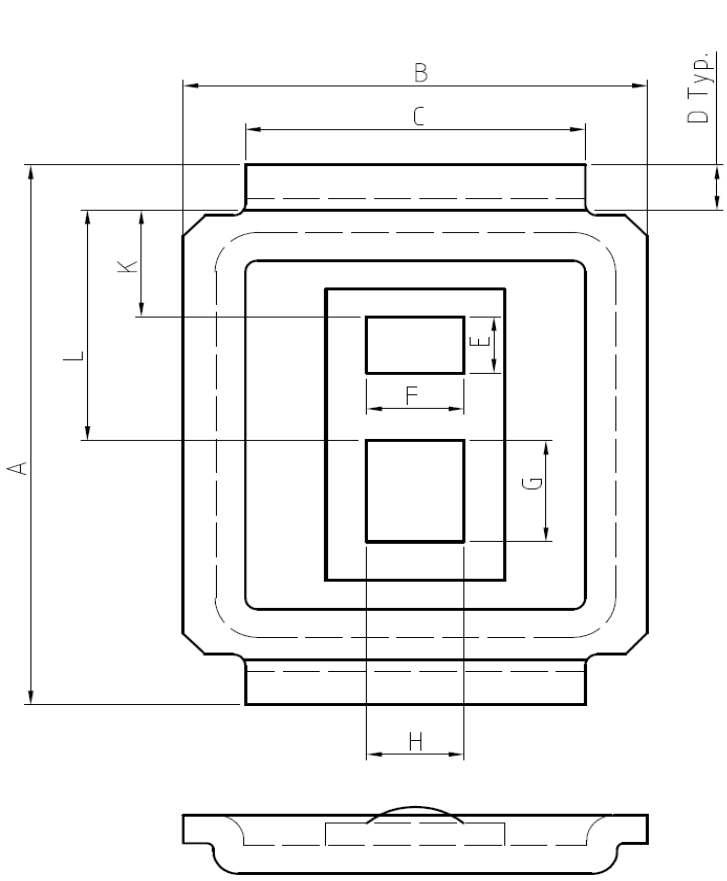
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



16 Gate charge waveforms



Package Outline **MG-WDSON-2**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.75	4.85	0.187	0.191
B	3.70	3.95	0.146	0.156
C	2.75	2.85	0.108	0.112
D	0.35	0.45	0.014	0.018
E	0.48	0.52	0.019	0.020
F	0.78	0.82	0.031	0.032
G	0.88	0.92	0.035	0.036
H	0.78	0.82	0.031	0.032
K	0.93	0.97	0.037	0.038
L	2.00	2.10	0.079	0.083
M	0.62	0.68	0.024	0.027
R	0.02	0.08	0.001	0.003
P	0.08	0.17	0.003	0.007

DOCUMENT NO.
Z8B00134584

SCALE
0 5 5
7.5mm

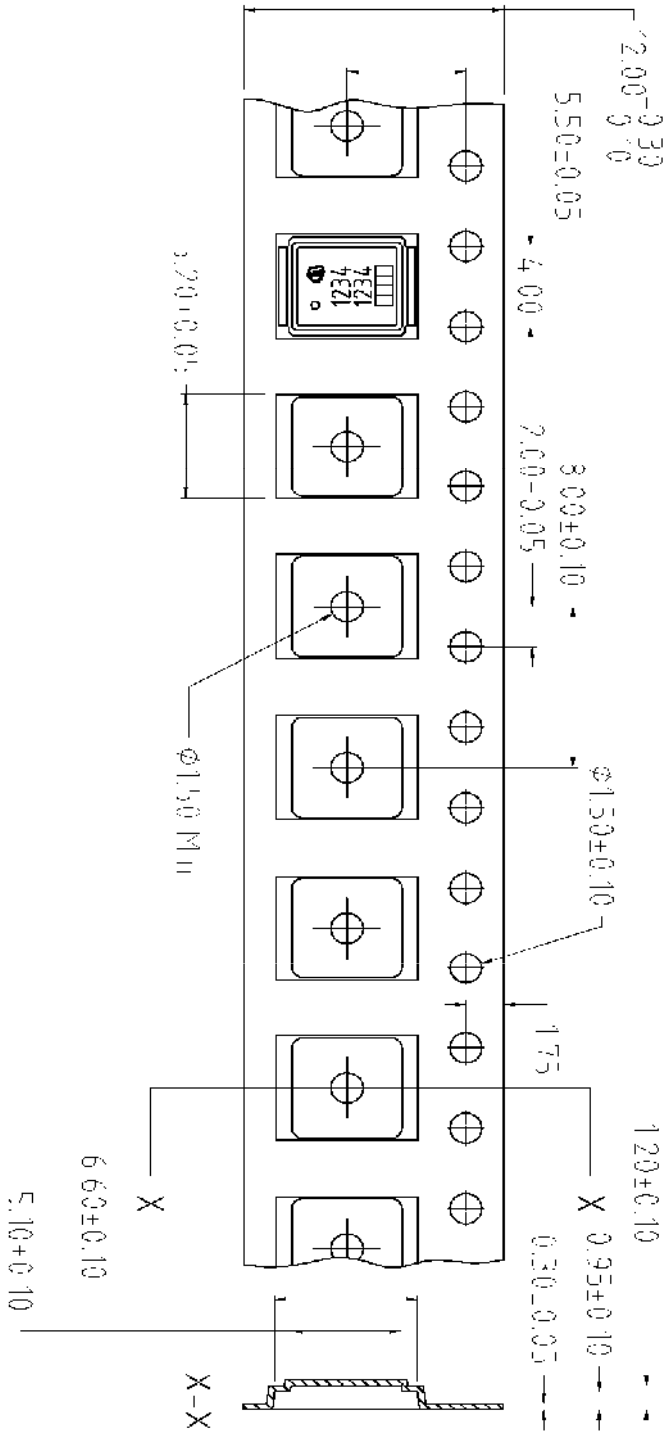
EUROPEAN PROJECTION

ISSUE DATE
18-10-2007

REVISION
01

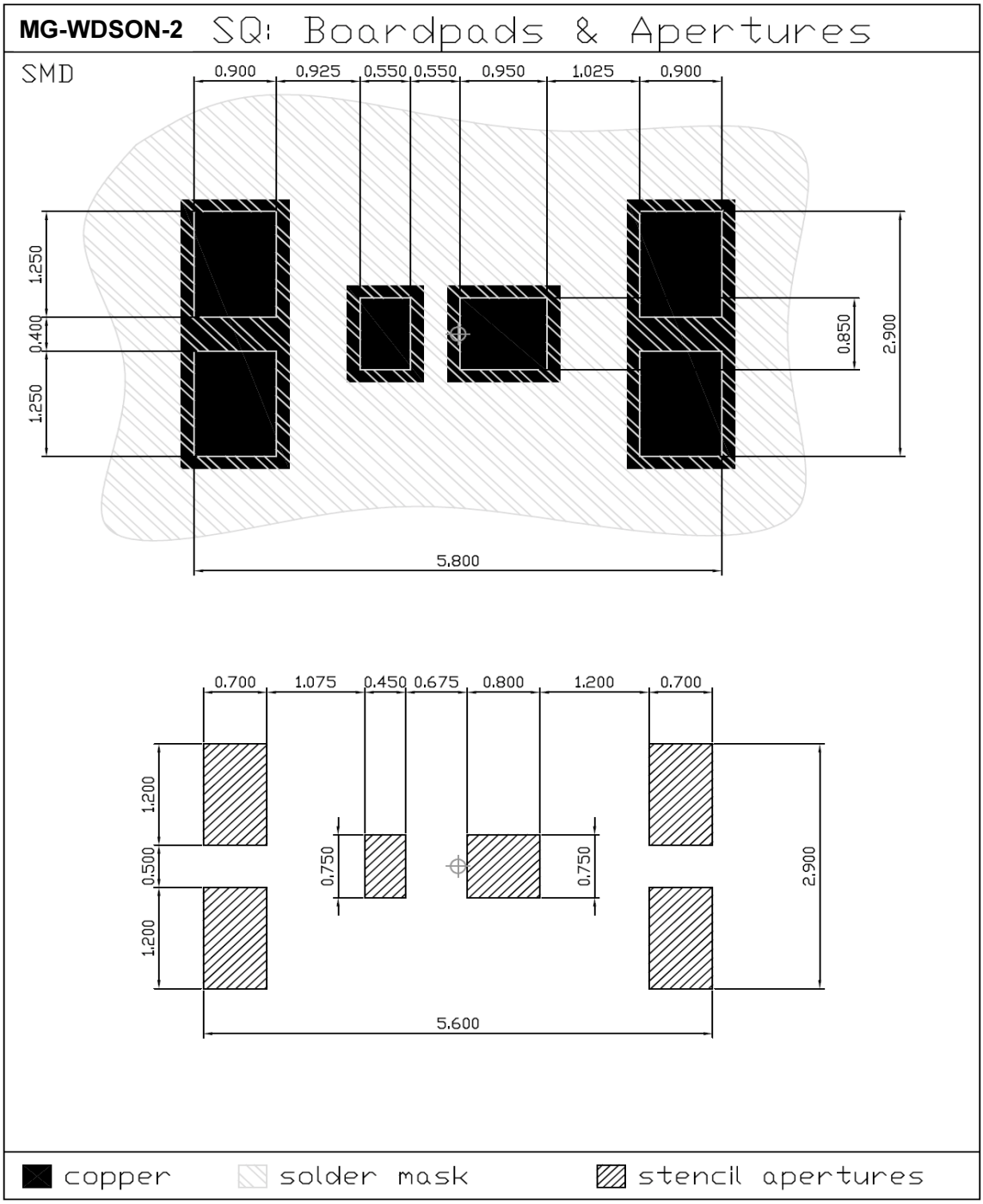
Package Outline **MG-WDSON-2**

PG-TDSON-8: Tape



Dimensions in mm

MG-WDSON-2 SQ: Boardpads & Apertures



Dimensions in mm

Raccomended stencil thikness 150 µm

Published by

Infineon Technologies AG
81726 Munich, Germany

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