

August 1991

Features

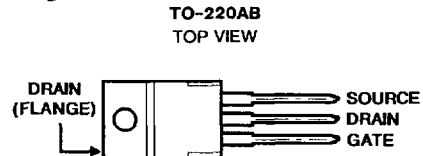
- 1.7A and 2.0A, 350V - 400V
- $r_{DS(on)} = 3.6\Omega$ and 5.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRF710, IRF711, IRF712, and IRF713 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF710R, IRF711R, IRF712R and IRF713R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

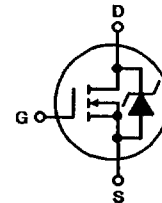
The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	IRF710 IRF710R	IRF711 IRF711R	IRF712 IRF712R	IRF713 IRF713R	UNITS
Drain-Source Voltage (1)	V_{DS} 400	350	400	350	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR} 400	350	400	350	V
Continuous Drain Current					
$T_C = +25^\circ\text{C}$	I_D 2	2	1.7	1.7	A
$T_C = +100^\circ\text{C}$	I_D 1.2	1.2	1.1	1.1	A
Pulsed Drain Current (3)	I_{DM} 5	5	4.3	4.3	A
Gate-Source Voltage	V_{GS} ± 20	± 20	± 20	± 20	V
Maximum Power Dissipation					
$T_C = +25^\circ\text{C}$	P_D 36	36	36	36	W
Linear Derating Factor	0.29	0.29	0.29	0.29	W/ $^\circ\text{C}$
Inductive Current, Clamped	I_{LM} 6.0	6.0	5.0	5.0	A
(See Figure 14, $L = 100\mu\text{H}$)					
Single Pulse Avalanche Energy Rating (4)	E_{AS}^* 120	120	120	120	mJ
Operating and Storage Junction	T_J, T_{STG} -55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Temperature Range					
Maximum Lead Temperature for Soldering	T_L 300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)					

NOTES:

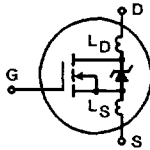
1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$.
2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. $V_{DD} = 50\text{V}$, starting $T_J = +25^\circ\text{C}$, $L = 53\text{mH}$, $R_{GS} = 25\Omega$, $I_{PEAK} = 2\text{A}$. See Figure 15.

*R Suffix Types Only

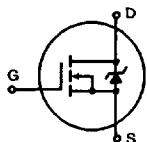
IRF710, IRF711, IRF712, IRF713 IRF710R, IRF711R, IRF712R, IRF713R

Electrical Characteristics $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
Drain-Source Breakdown Voltage IRF710/712, IRF710R/712R IRF711/713, IRF711R/713R	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	400	-	-	V	
			350	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	-	4.0	V	
Gate-Source Leakage Forward	I_{GSS}	$V_{GS} = 20V$	-	-	500	nA	
Gate-Source Leakage Reverse	I_{GSS}	$V_{GS} = -20V$	-	-	-500	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Max Rating}, V_{GS} = 0V$ $V_{DS} = \text{Max Rating} \times 0.8, V_{GS} = 0V,$ $T_J = +125^\circ\text{C}$	-	-	250	μA	
			-	-	1000	μA	
On-State Drain Current (Note 2) IRF710/711, IRF710R/711R IRF712/713, IRF712R/713R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times R_{DS(ON)} \text{ Max}, V_{GS} = 10V$	2.0	-	-	A	
			1.7	-	-	A	
Static Drain-Source On-State Resistance (Note 2) IRF710/711, IRF710R/711R IRF712/713, IRF712R/713R	$r_{DS(ON)}$	$V_{GS} = 10V, I_D = 1.1A$	-	3.3	3.6	Ω	
			-	3.6	5.0	Ω	
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V, I_D = 1.1A$	1.0	1.5	-	S(\bar{U})	
Input Capacitance	C_{ISS}	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$ See Figure 10	-	135	-	pF	
Output Capacitance	C_{OSS}		-	35	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	8.0	-	pF	
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 50V, I_D \approx 5.6A, R_G = 24\Omega$ See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	8.0	12	ns	
Rise Time	t_r		-	10	15	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	21	32	ns	
Fall Time	t_f		-	11	17	ns	
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	$V_{GS} = 10V, I_D = 2.0A, V_{DS} = 0.8V \text{ Max}$ Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	7.0	12	nC	
Gate-Source Charge	Q_{gs}		-	1.2	-	nC	
Gate-Drain ("Miller") Charge	Q_{gd}		-	4.0	-	nC	
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die		-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from pack- age to center of die		-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH	
Junction-to-Case	$R_{\theta JC}$		-	-	3.5	$^\circ\text{C/W}$	
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	$^\circ\text{C/W}$	
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	$^\circ\text{C/W}$	

4
N-CHANNEL
POWER MOSFETs

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.		-	-	2.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}			-	-	5.0	A
Diode Forward Voltage (Note 2)	V_{SD}	$T_J = +25^\circ\text{C}, I_S = 2.0A, V_{GS} = 0V$		-	-	1.6	V
Reverse Recovery Time	t_{rr}	$T_J = +25^\circ\text{C}, I_F = 2.0A, di_F/dt = 100A/\mu s$		110	-	520	ns
Reverse Recovered Charge	Q_{RR}	$T_J = +25^\circ\text{C}, I_F = 2.0A, di_F/dt = 100A/\mu s$		0.40	-	1.4	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.		-	-	-	-

NOTES: 1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$

2. Pulse Test: Pulse width $\leq 300\mu s$,
Duty Cycle $\leq 2\%$

3. Repetitive Rating: Pulse width limited by max.
junction temperature. See Transient Thermal
Impedance Curve (Figure 5)

4. $V_{DD} = 50V$, Start $T_J = +25^\circ\text{C}$, $L = 53mH$,
 $R_{GS} = 25\Omega$, $I_{PEAK} = 2A$ (See Figure 15)

Performance Curves

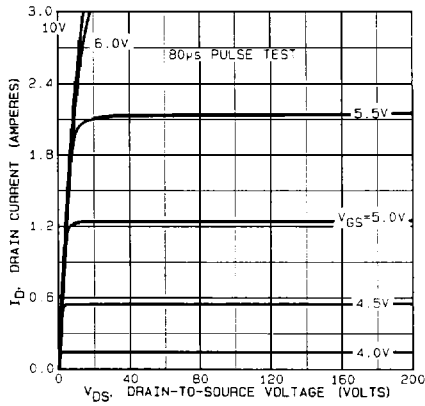


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

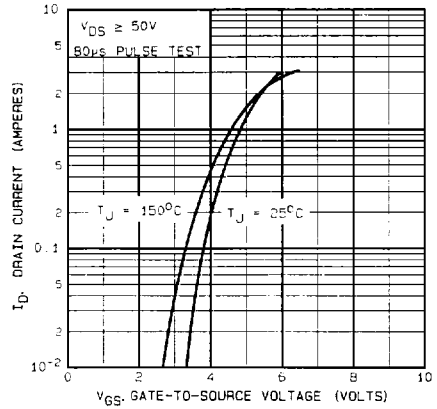


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

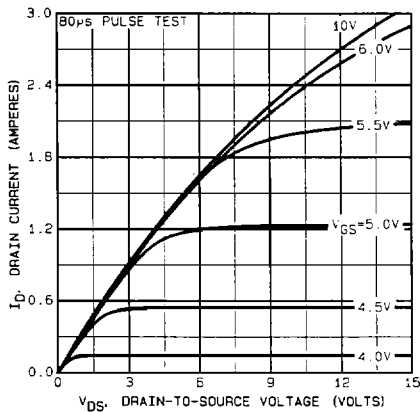


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

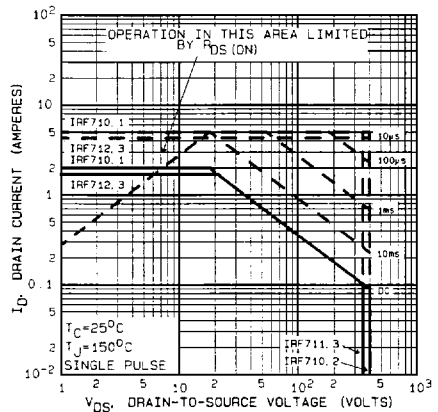


FIGURE 4. MAXIMUM SAFE OPERATING AREA

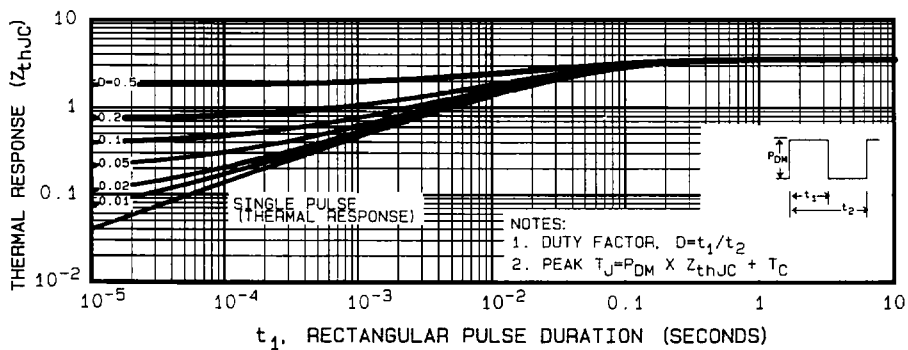


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

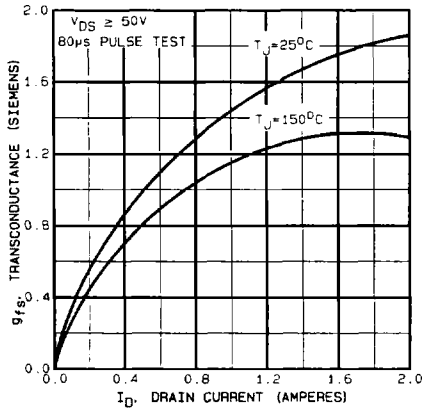


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

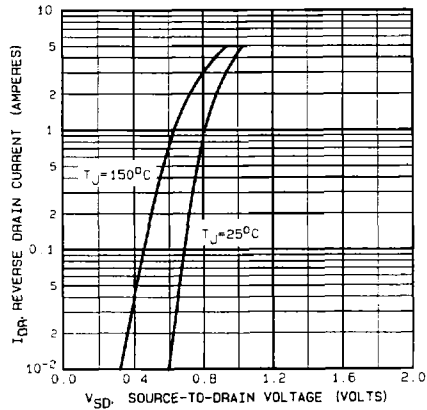


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

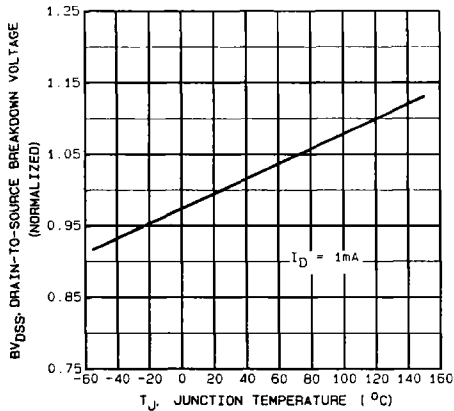


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

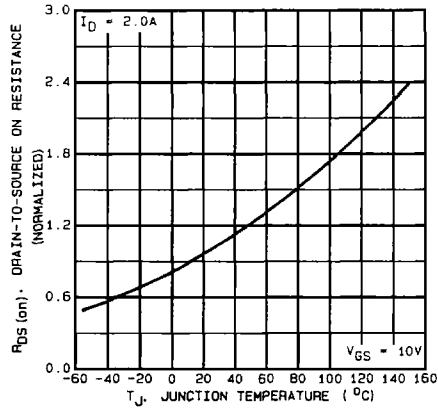


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

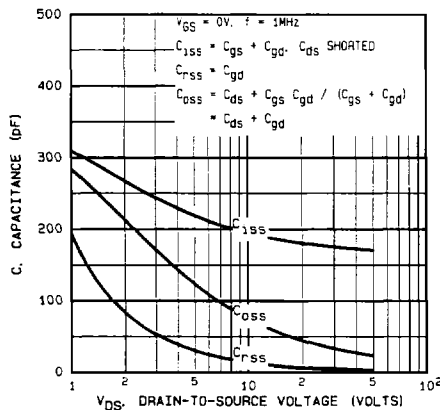


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

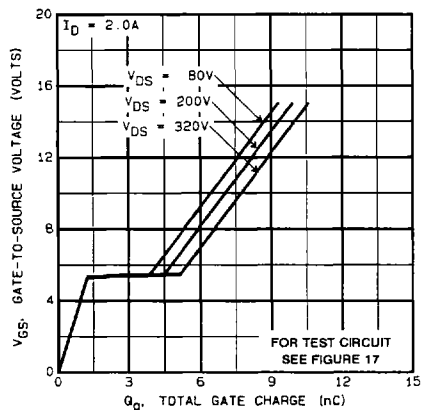


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

4
N-CHANNEL
POWER MOSFETS

Performance Curves (Continued)

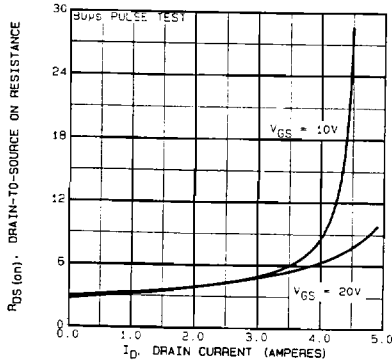


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

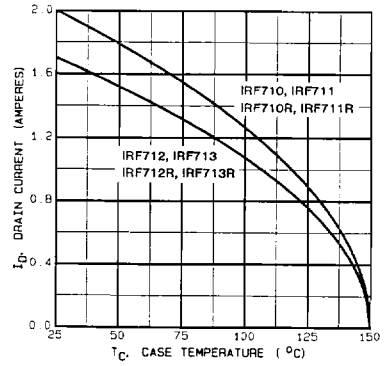


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

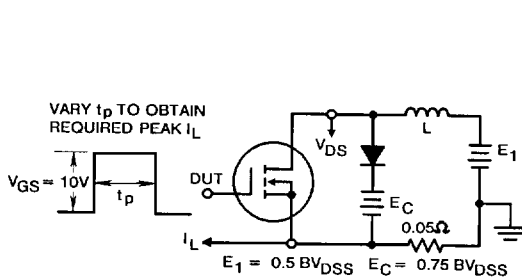


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

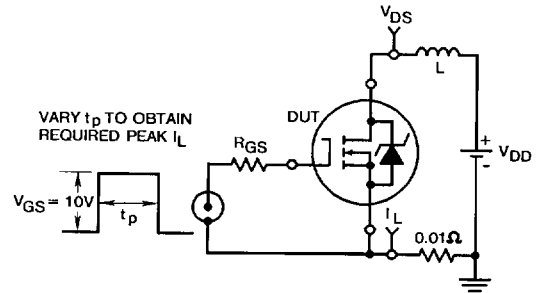


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

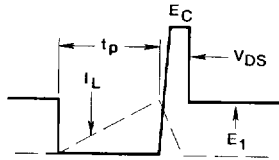


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

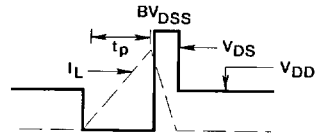


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

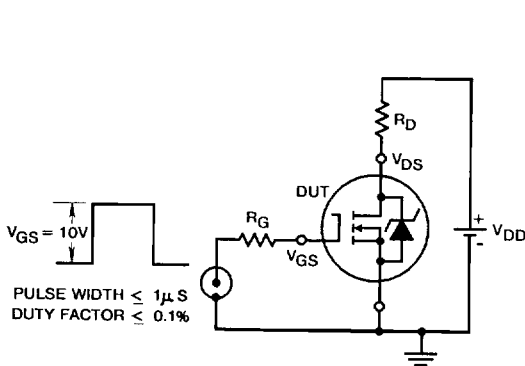


FIGURE 16. SWITCHING TIME TEST CIRCUIT

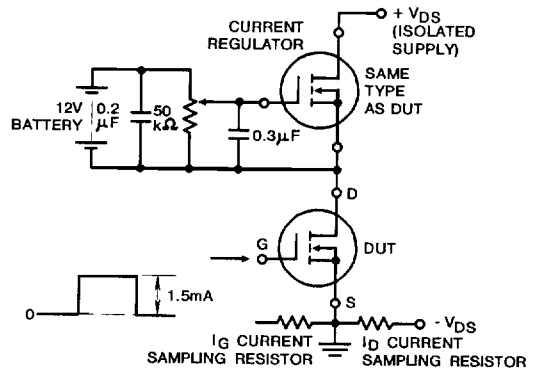


FIGURE 17. GATE CHARGE TEST CIRCUIT