

BUK9M24-40E

N-channel 40 V, 24 m Ω logic level MOSFET in LFPAK33 19 September 2016

Product data sheet

1. **General description**

Logic level N-channel MOSFET in an LFPAK33 (Power33) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. **Features and benefits**

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with V_{GS(th)} rating of greater than 0.5 V at 175 °C

Applications 3.

- 12 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	40	V	
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	30	Α	
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	44	W	
Static charac	Static characteristics							
R _{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ °C}; Fig. 11$		-	20	24	mΩ	
Dynamic characteristics								
Q_{GD}	gate-drain charge	I _D = 10 A; V _{DS} = 32 V; V _{GS} = 5 V; T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>		-	3.3	-	nC	



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline		(Graphic symbol
1	S	Source				D I
2	S	Source				
3	S	Source				G T T
4	G	Gate				mbb076 S
mb	D	Mounting base; connected to drain	LI	FPAK33 (SOT1210)		

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
BUK9M24-40E	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 8 leads	SOT1210			

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9M24-40E	92440E

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	40	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 k Ω		-	40	V
V_{GS}	gate-source voltage	DC; T _j ≤ 175 °C		-10	10	V
		Pulsed; T _j ≤ 175 °C	[1][2]	-15	15	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	44	W
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 2</u>		-	30	Α
		V _{GS} = 5 V; T _{mb} = 100 °C; <u>Fig. 2</u>		-	21.4	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; Fig. 3		-	121	Α

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Symbol	Parameter	Conditions		Min	Max	Unit
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drai	n diode		'			
I _S	source current	T _{mb} = 25 °C		-	30	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 ^{\circ}C$		-	121	Α
Avalanche r	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 30 A; $V_{sup} \le$ 40 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[3][4]	-	12.6	mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm.
- [2] Significantly longer life times are achieved by lowering T_i and or V_{GS}
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.

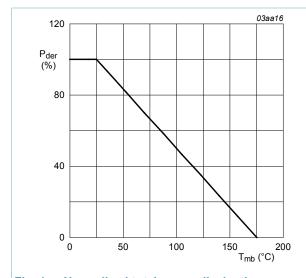
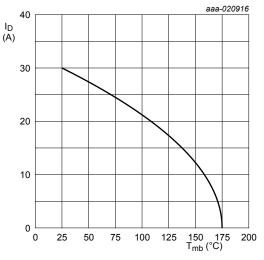


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$



 $V_{GS} \ge 5 \text{ V}$

Fig. 2. Continuous drain current as a function of mounting base temperature

$$I_D = 30 \times \sqrt{\frac{175^{\circ}C - T_{mb}}{150^{\circ}C}} \text{ for } T_{mb} \ge 25^{\circ}C$$

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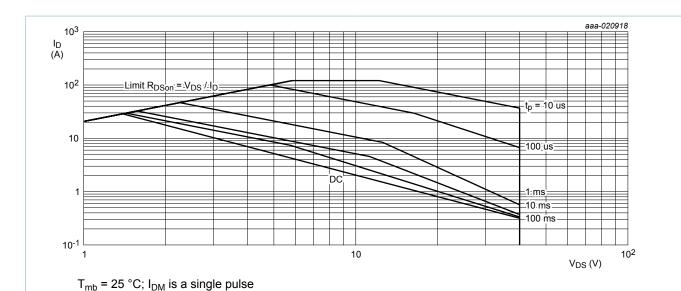
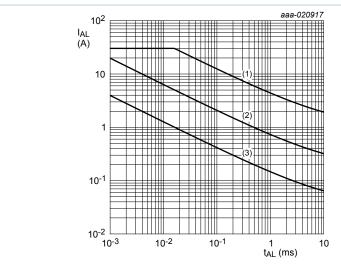


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j \text{ (init)}}$ = 25 °C; (2) $T_{j \text{ (init)}}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

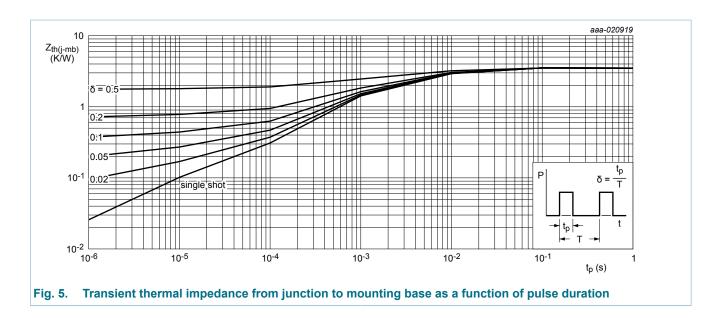
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	2.77	3.4	K/W

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
$V_{(BR)DSS}$	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^{\circ}C$	40	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 10	-	-	2.45	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 10	0.5	-	-	V
I _{DSS} drain leakage cu	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C	-	0.01	1	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 11$	-	20	24	mΩ
	resistance	V_{GS} = 10 V; I_{D} = 10 A; T_{j} = 25 °C; Fig. 11	-	16	20	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 175 °C;$ Fig. 12	-	-	50	mΩ
Dynamic ch	naracteristics					
Q _{G(tot)}	total gate charge	I _D = 10 A; V _{DS} = 32 V; V _{GS} = 5 V;	-	7.7	-	nC
Q _{GS}	gate-source charge	T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	1.7	-	nC

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Q_{GD}	gate-drain charge		-	3.3	-	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz;	-	600	798	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>	-	97	117	pF
C _{rss}	reverse transfer capacitance		-	62	85	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 3 \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 5 \Omega; T_j = 25 \text{ °C}$	-	6.3	-	ns
t _r	rise time		-	9.5	-	ns
t _{d(off)}	turn-off delay time		-	12.1	-	ns
t _f	fall time		-	7.8	-	ns
Source-dra	ain diode					
V_{SD}	source-drain voltage	$I_S = 10 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 ^{\circ}\text{C}$; Fig. 16	-	0.86	1.2	V
t _{rr}	reverse recovery time	$I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	13.4	-	ns
Qr	recovered charge	$V_{DS} = 25 \text{ V}; T_j = 25 \text{ °C}$	-	6.1	-	nC

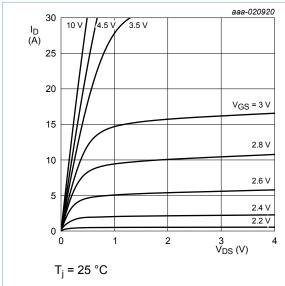


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

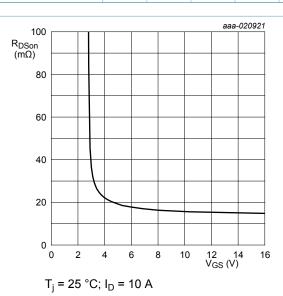


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

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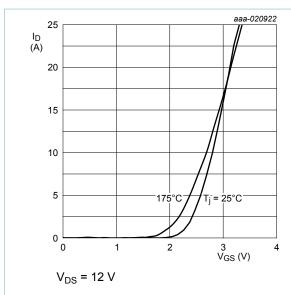


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

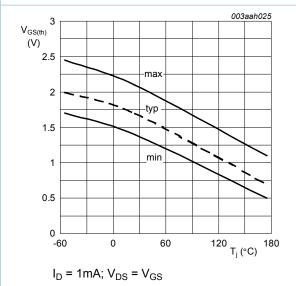


Fig. 10. Gate-source threshold voltage as a function of junction temperature

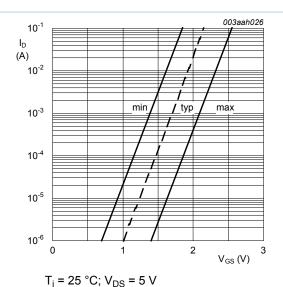


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

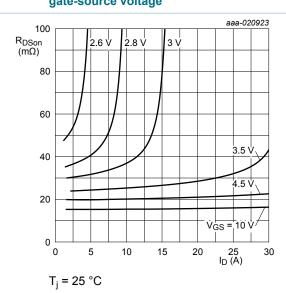


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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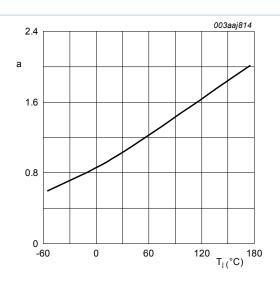


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

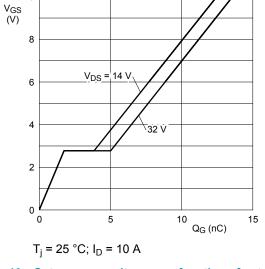


Fig. 13. Gate-source voltage as a function of gate charge; typical values

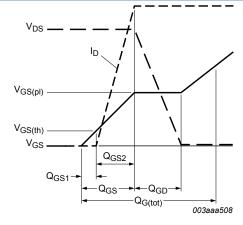
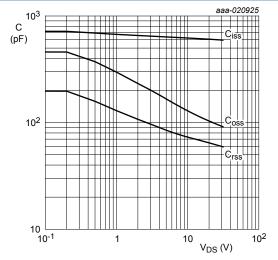


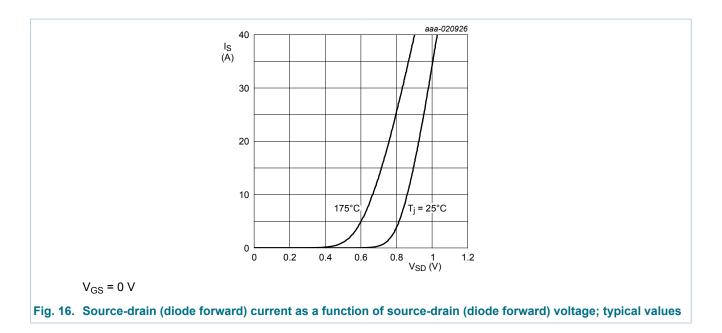
Fig. 14. Gate charge waveform definitions



 $V_{GS} = 0 V$; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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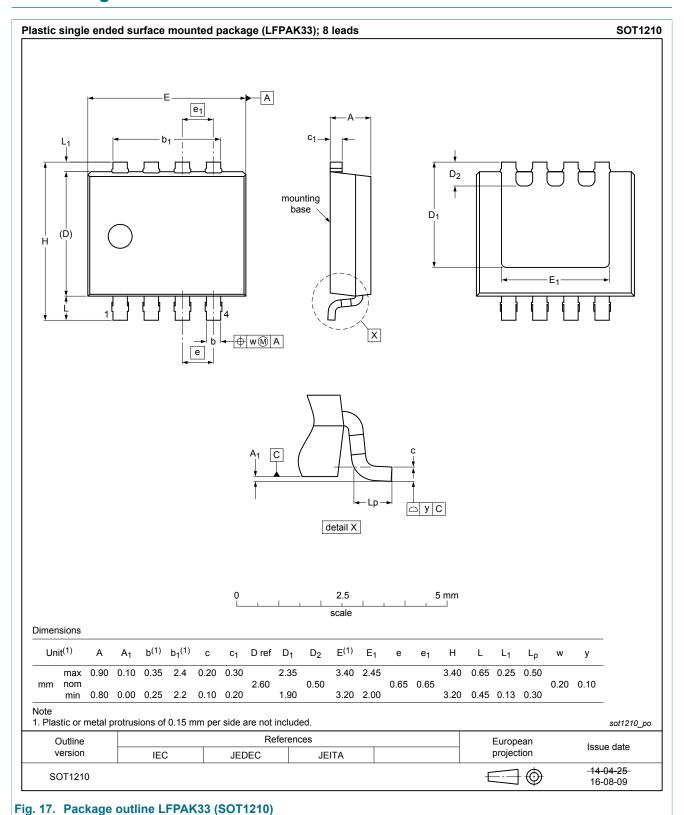


11. Application information

For guidance on how to use and understand this datasheet, please refer to application note AN11158 "Understanding power MOSFET datasheet parameters".

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12. Package outline



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13. Legal information

13.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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