

HA-2539

600MHz, Very High Slew Rate Operational Amplifier

FN2896
 Rev 5.00
 May 2003

The Intersil HA-2539 represents the ultimate in high slew rate, wideband, monolithic operational amplifiers. It has been designed and constructed with the Intersil High Frequency Bipolar Dielectric Isolation process and features dynamic parameters never before available from a truly differential device.

With a 600V/μs slew rate and a 600MHz gain bandwidth product, the HA-2539 is ideally suited for use in video and RF amplifier designs, in closed loop gains of 10 or greater. Full ±10V swing coupled with outstanding AC parameters and complemented by high open loop gain makes the devices useful in high speed data acquisition systems.

For further design assistance please refer to Application Note AN541 (Using the HA-2539 Very High Slew Rate Wideband Operational Amplifiers) and Application Note AN556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers).

For military grade product information, the HA-2539/883 data sheet is available upon request.

Part Number Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA3-2539-5	0 to 75	14 Ld PDIP	E14.3

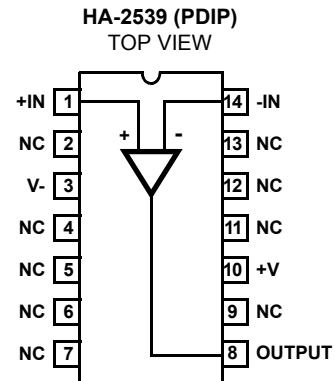
Features

- Very High Slew Rate 600V/μs
- Open Loop Gain 15kV/V
- Wide Gain-Bandwidth ($A_V \geq 10$) 600MHz
- Power Bandwidth 9.5MHz
- Low Offset Voltage 8mV
- Input Voltage Noise $6nV/\sqrt{Hz}$
- Output Voltage Swing ±10V
- Monolithic Bipolar Dielectric Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

Pinout



NOTE: No-Connection (NC) leads may be tied to a ground plane for better isolation and heat dissipation.

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals	35V
Differential Input Voltage	6V
Peak Output Current	50mA
Continuous Output Current	33mA _{RMS}

Operating Conditions

Temperature Range	
HA-2539-5	0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	95	N/A
Maximum Internal Quiescent Power Dissipation (Note 1)		
Maximum Junction Temperature (Plastic Package)		
Maximum Storage Temperature Range		
Maximum Lead Temperature (Soldering 10s)		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below 150°C for the plastic package. By using Application Note AN556 on Safe Operating Area equations, along with the thermal resistances, proper load conditions can be determined. Heat sinking is recommended above 75°C.
- θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications $V_{SUPPLY} = \pm 15V$, $R_L = 1kW$, $C_L < 10pF$, Unless Otherwise Specified

PARAMETER	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	25	-	8	15	mV
	Full	-	13	20	mV
Average Offset Voltage Drift	Full	-	20	-	$\mu V/^\circ C$
Bias Current	25	-	5	20	μA
	Full	-	-	25	μA
Offset Current	25	-	1	6	μA
	Full	-	-	8	μA
Input Resistance	25	-	10	-	k Ω
Input Capacitance	25	-	1	-	pF
Common Mode Range	Full	± 10.0	-	-	V
Input Current Noise (f = 1kHz, $R_{SOURCE} = 0\Omega$)	25	-	6	-	pA/ \sqrt{Hz}
Input Voltage Noise (f = 1kHz, $R_{SOURCE} = 0\Omega$)	25	-	6	-	nV/ \sqrt{Hz}
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Note 3)	25	10	15	-	kV/V
	Full	5	-	--	kV/V
Common Mode Rejection Ratio (Note 4)	Full	60	72	-	dB
Minimum Stable Gain	25	10	-	-	V/V
Gain Bandwidth (Notes 5, 6)	25	-	600	-	MHz

Electrical Specifications $V_{\text{SUPPLY}} = \pm 15\text{V}$, $R_L = 1\text{k}\Omega$, $C_L < 10\text{pF}$, Unless Otherwise Specified (Continued)

PARAMETER	TEMP. (°C)	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Notes 3, 10)	Full	± 10.0	-	-	V
Output Current (Note 3)	25	± 10	± 20	-	mA
Output Resistance	25	-	30	-	Ω
Full Power Bandwidth (Notes 3, 7)	25	8.7	9.5	-	MHz
TRANSIENT RESPONSE (Note 8)					
Rise Time	25	-	7	-	ns
Overshoot	25	-	15	-	%
Slew Rate	25	550	600	-	V/ μs
Settling Time: 10V Step to 0.1%	25	-	180	-	ns
POWER REQUIREMENTS					
Supply Current	Full	-	20	25	mA
Power Supply Rejection Ratio (Note 9)	Full	60	70	-	dB

NOTES:

3. $R_L = 1\text{k}\Omega$, $V_O = \pm 10\text{V}$.
4. $V_{\text{CM}} = \pm 10.0\text{V}$.
5. $V_O = 90\text{mV}$.
6. $A_V = 10$.
7. Full Power Bandwidth guaranteed based on slew rate measurement using: $\text{FPBW} = \frac{\text{Slew Rate}}{2\pi V_{\text{PEAK}}}$.
8. Refer to Test Circuits section of data sheet.
9. $V_{\text{SUPPLY}} = +5\text{V}$, -15V and $+15\text{V}$, -5V .
10. Guaranteed range for output voltage is $\pm 10\text{V}$. Functional operation outside of this range is not guaranteed.

Test Circuits and Waveforms

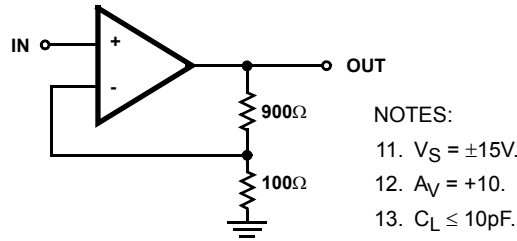
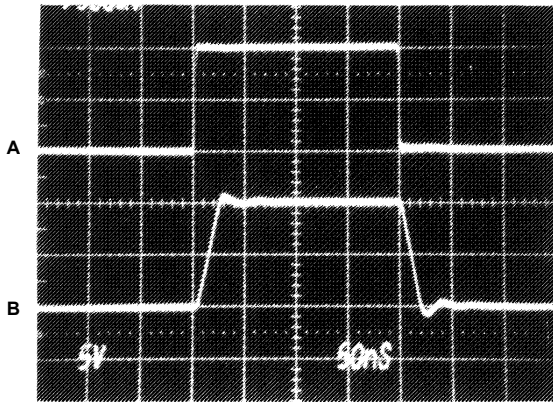
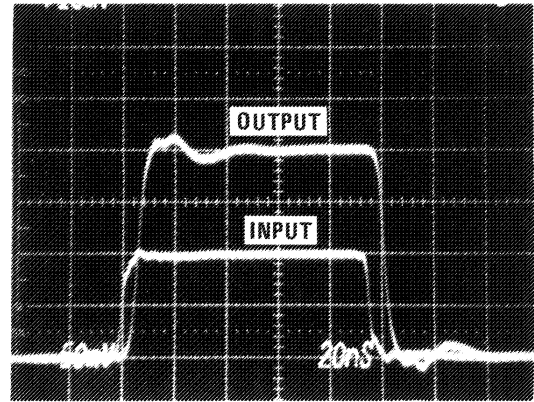


FIGURE 1. TEST CIRCUIT



Vertical Scale: A = 0.5V/Div., B = 5.0V/Div.
Horizontal Scale: 50ns/Div.

FIGURE 2. LARGE SIGNAL RESPONSE



Vertical Scale: Input = 10mV/Div., Output = 50mV/Div.
Horizontal Scale: 20ns/Div.

FIGURE 3. SMALL SIGNAL RESPONSE

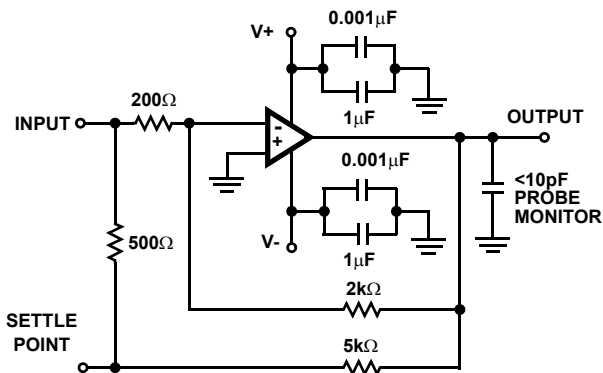
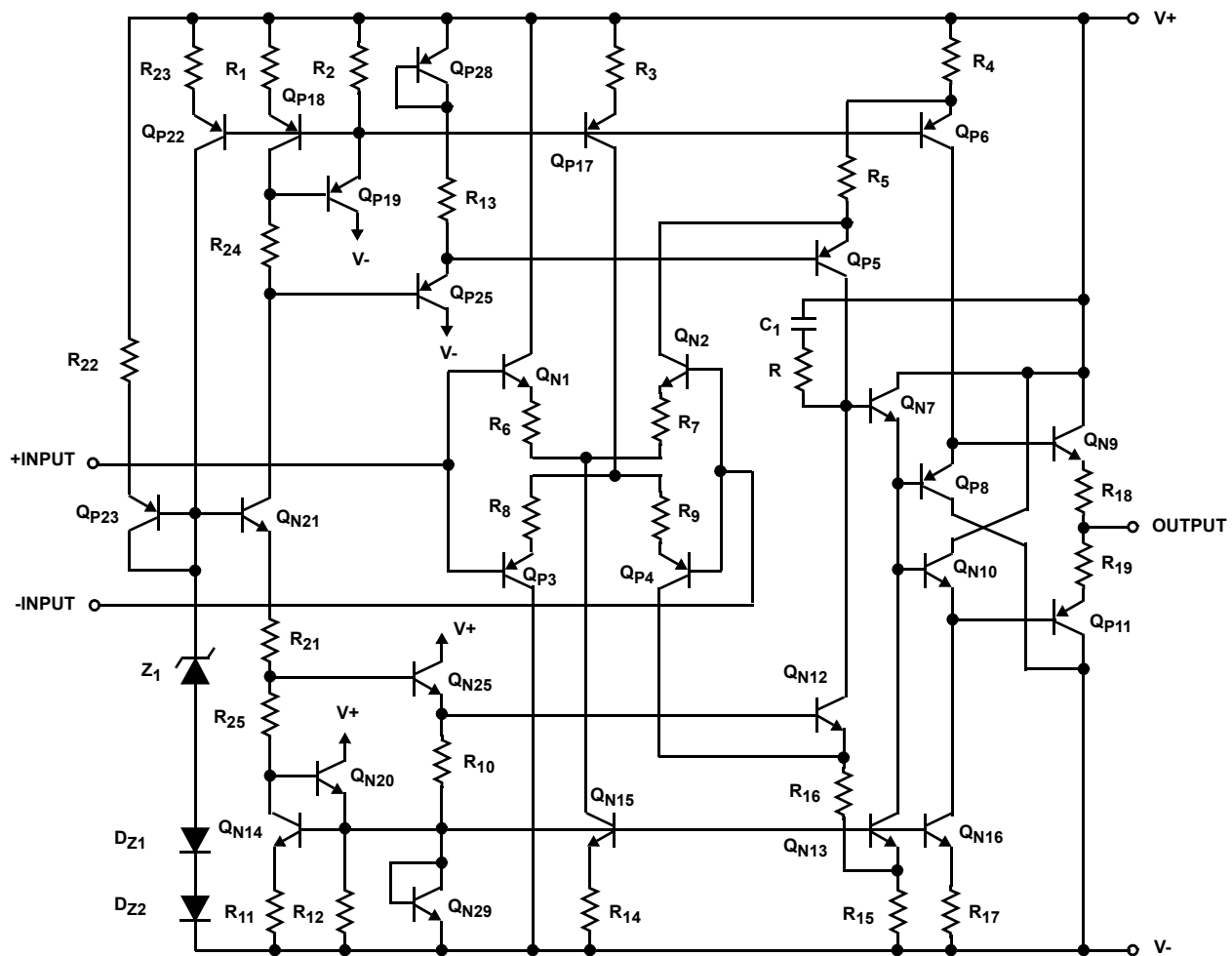


FIGURE 4. SETTLING TIME CIRCUIT

- NOTES:
14. $A_V = -10$.
 15. Load Capacitance should be less than 10pF.
 16. It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
 17. SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

Schematic Diagram



Typical Applications

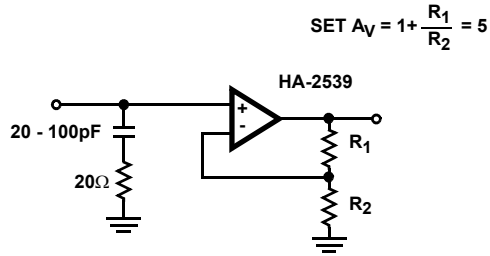


FIGURE 5. FREQUENCY COMPENSATION BY OVERDAMPING

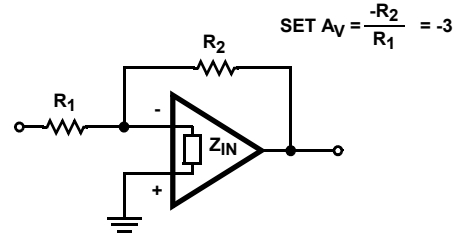


FIGURE 6. STABILIZATION USING Z_{IN}

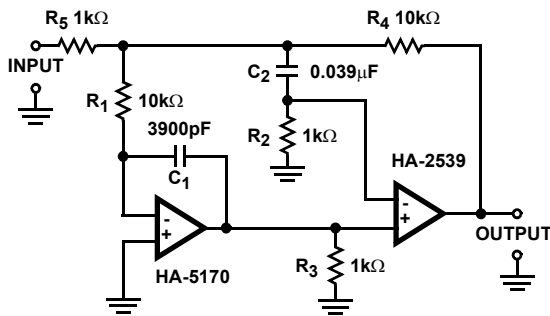


FIGURE 7. REDUCING DC ERRORS; COMPOSITE AMPLIFIER

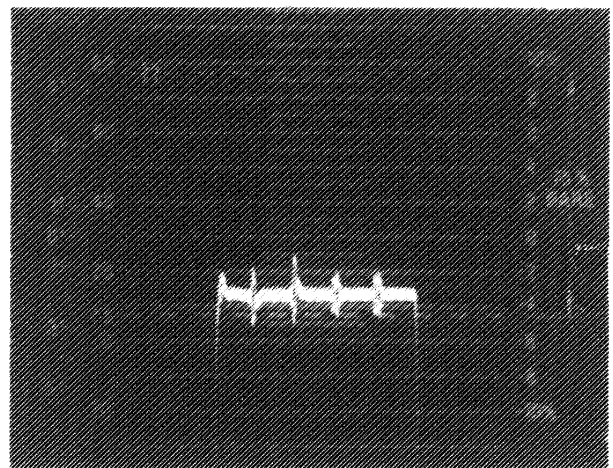


FIGURE 8. DIFFERENTIAL GAIN ERROR (3%) HA-2539 20dB VIDEO GAIN BLOCK

Typical Performance Curves

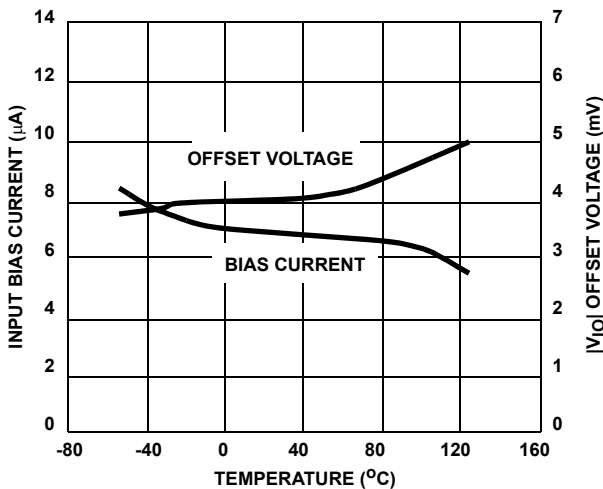


FIGURE 9. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

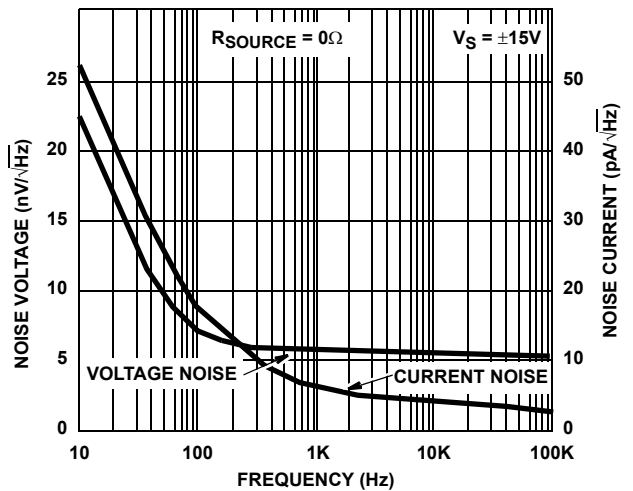


FIGURE 10. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

Typical Performance Curves (Continued)

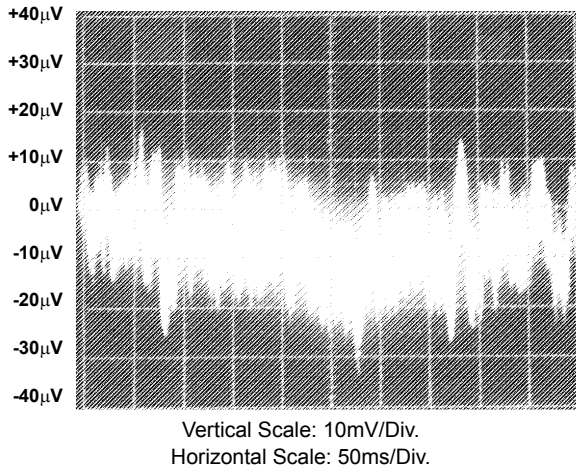


FIGURE 11. BROADBAND NOISE (0.1Hz TO 1MHz)

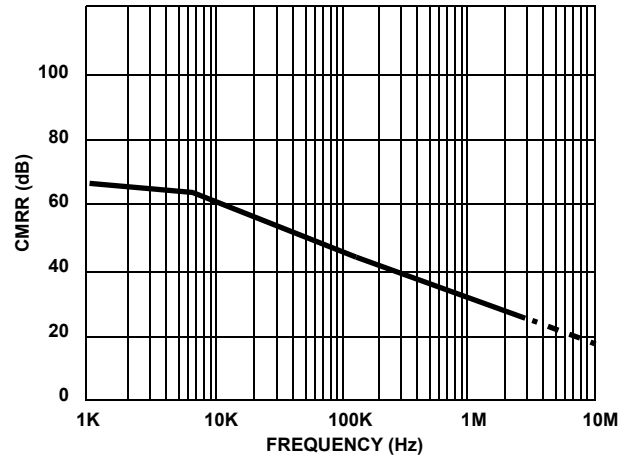


FIGURE 12. COMMON MODE REJECTION RATIO vs FREQUENCY

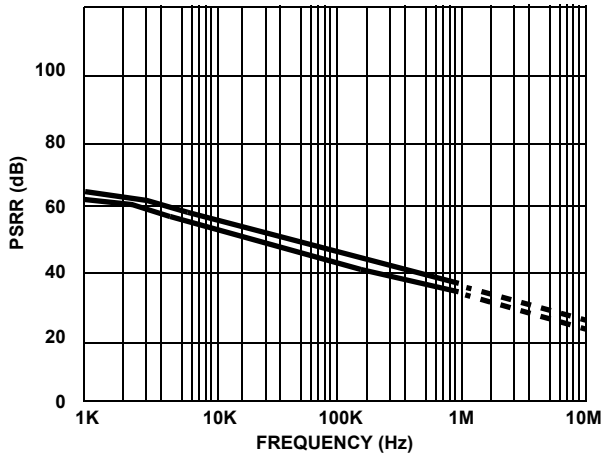


FIGURE 13. POWER SUPPLY REJECTION RATIO vs FREQUENCY

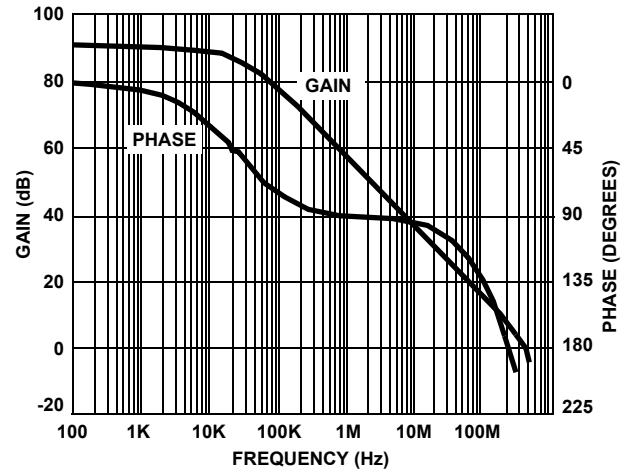


FIGURE 14. OPEN LOOP GAIN/PHASE vs FREQUENCY

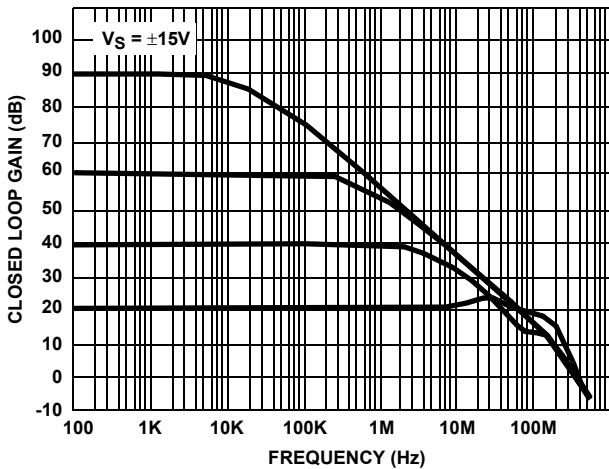


FIGURE 15. CLOSED LOOP FREQUENCY RESPONSE

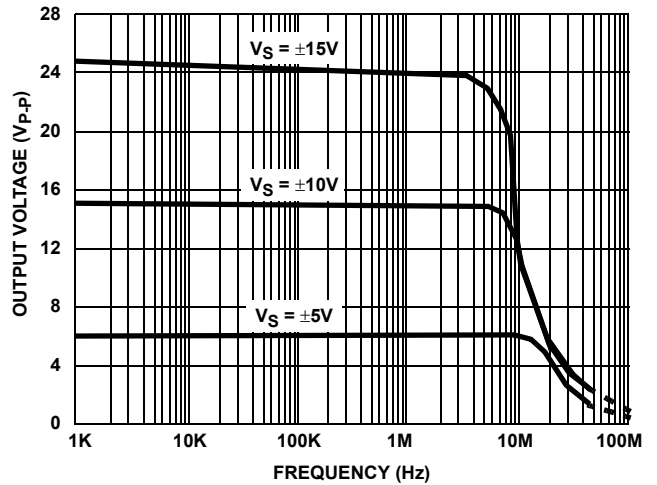


FIGURE 16. OUTPUT VOLTAGE SWING vs FREQUENCY

Typical Performance Curves (Continued)

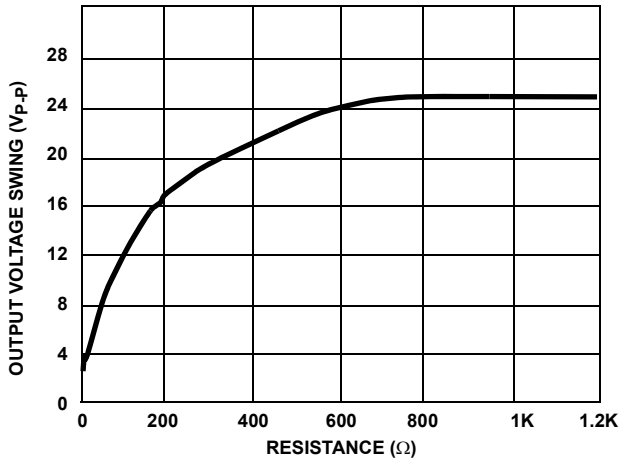


FIGURE 17. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

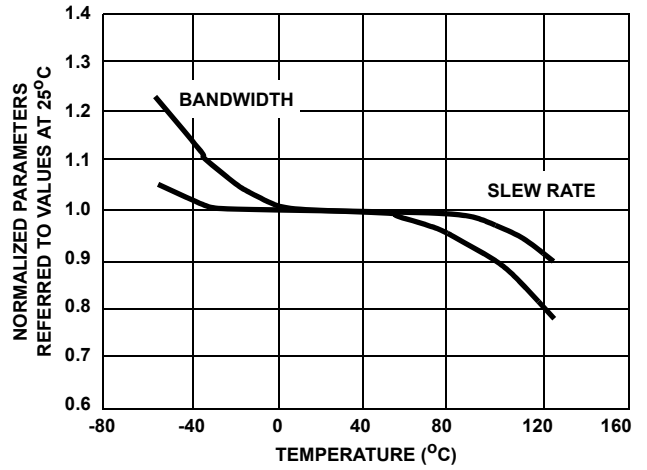


FIGURE 18. NORMALIZED AC PARAMETERS vs TEMPERATURE

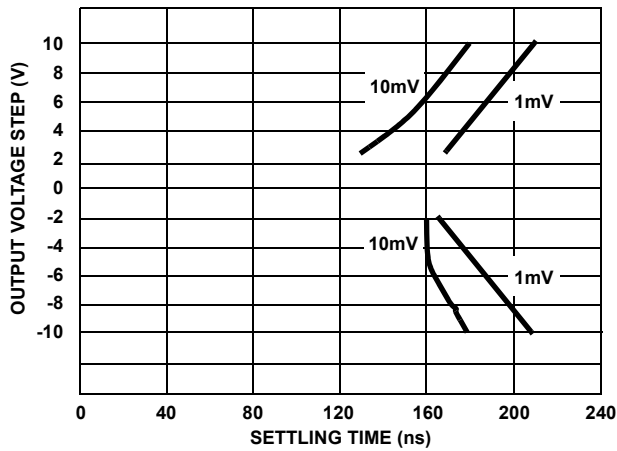


FIGURE 19. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

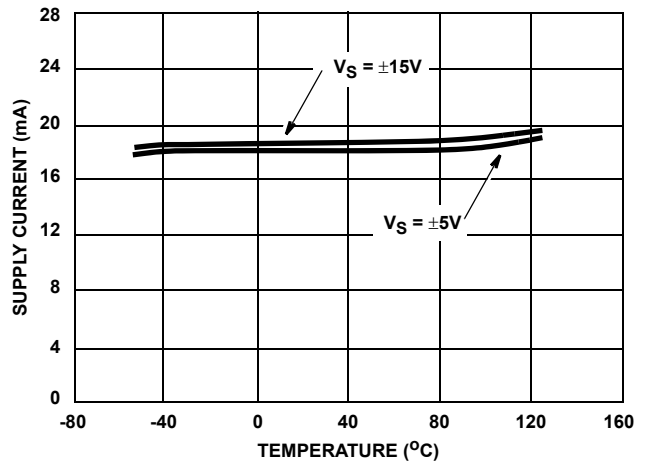


FIGURE 20. POWER SUPPLY CURRENT vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

62 mils x 76 mils x 19 mils
 1575 μ m x 1930 μ m x 483 μ m

METALLIZATION:

Type: Al, 1% Cu
 Thickness: 16k Å \pm 2k Å

PASSIVATION:

Type: Nitride (Si₃N₄) over Silox (SiO₂, 5% Phos.)
 Silox Thickness: 12k Å \pm 2k Å
 Nitride Thickness: 3.5k Å \pm 1.5k Å

SUBSTRATE POTENTIAL (POWERED UP):

V-

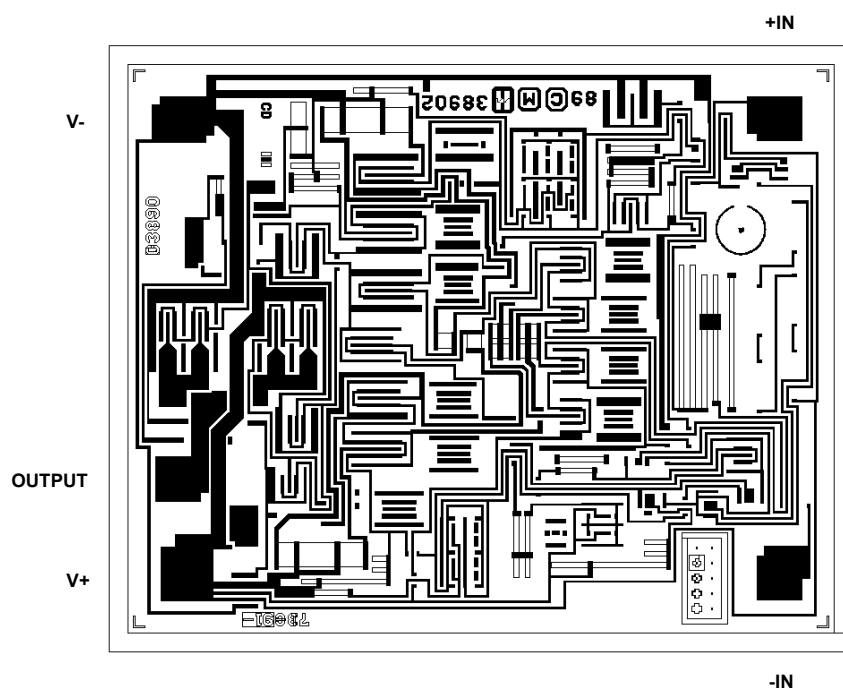
TRANSISTOR COUNT:

30

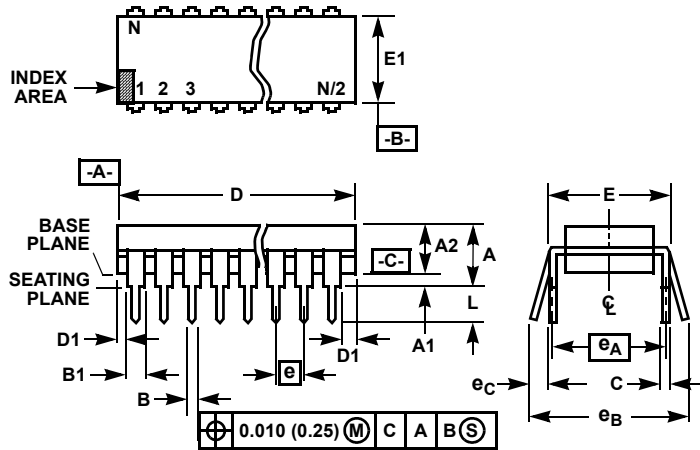
PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum $-C-$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

**E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

© Copyright Intersil Americas LLC 2003. All Rights Reserved.

All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com