

# Octal Bus Buffer/Line Driver Inverting with 3-State Outputs

The MC74VHCT240A is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT240A is an inverting 3-state buffer, and has two active-low output enables. This device is designed to be used with 3-state memory address drivers, etc.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

The VHCT240A input and output (when disabled) structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed:  $t_{PD} = 5.6ns$  (Typ) at  $V_{CC} = 5V$
- Low Power Dissipation:  $I_{CC} = 4\mu A$  (Max) at  $T_A = 25^\circ C$
- TTL-Compatible Inputs:  $V_{IL} = 0.8V$ ;  $V_{IH} = 2.0V$
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise:  $V_{OLP} = 1.1V$  (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 110 FETs or 27.5 Equivalent Gates

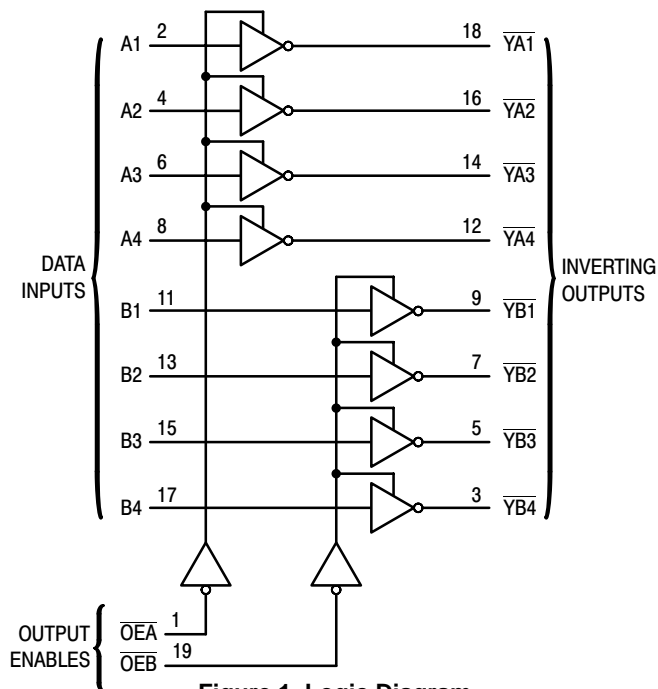
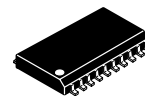


Figure 1. Logic Diagram

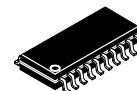
## MC74VHCT240A



**DW SUFFIX**  
20-LEAD SOIC WIDE PACKAGE  
CASE 751D-05



**DT SUFFIX**  
20-LEAD TSSOP PACKAGE  
CASE 948E-02



**M SUFFIX**  
20-LEAD SOIC EIAJ PACKAGE  
CASE 967-01

### ORDERING INFORMATION

MC74VHCTXXXADW	SOIC WIDE
MC74VHCTXXXADT	TSSOP
MC74VHCTXXXAM	SOIC EIAJ

### FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OEA}, \overline{OEB}$	A, B	$\overline{YA}, \overline{YB}$
L	L	H
L	H	L
H	X	Z

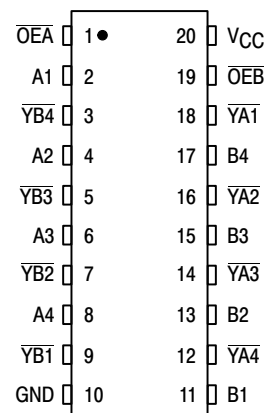


Figure 2. Pin Assignment

# MC74VHCT240A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage	- 0.5 to + 7.0	V
V <sub>out</sub>	DC Output Voltage Output in 3-State High or Low State	- 0.5 to + 7.0 - 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current	- 20	mA
I <sub>OK</sub>	Output Diode Current (V <sub>OUT</sub> < GND; V <sub>OUT</sub> > V <sub>CC</sub> )	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA
P <sub>D</sub>	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

† Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	4.5	5.5	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage Output in 3-State High or Low State	0 0	5.5 V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	- 40	+ 85	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time V <sub>CC</sub> = 5.0V ± 0.5V	0	20	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = - 50μA	4.5	4.4	4.5		4.4		V
		I <sub>OH</sub> = - 8mA	4.5	3.94		3.80			
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50μA	4.5		0.0	0.1		0.1	V
		I <sub>OL</sub> = 8mA	4.5			0.36		0.44	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I <sub>OZ</sub>	Maximum 3-State Leakage Current	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5			± 0.25		± 2.5	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5			4.0		40.0	μA

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I <sub>CC</sub> T	Quiescent Supply Current	Per Input: V <sub>IN</sub> = 3.4V Other Input: V <sub>CC</sub> or GND	5.5			1.35		1.50	mA
I <sub>OP</sub> D	Output Leakage Current	V <sub>OUT</sub> = 5.5V	0			0.5		5.0	μA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t <sub>PL</sub> H, t <sub>PH</sub> L	Maximum Propagation Delay A to $\overline{Y}$ A or B to $\overline{Y}$ B	V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		5.6 6.1	7.8 8.8	1.0 1.0	9.0 10.0	ns
t <sub>P</sub> ZL, t <sub>P</sub> ZH	Output Enable Time $\overline{OE}$ A to $\overline{Y}$ A or $\overline{OE}$ B to $\overline{Y}$ B	V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 15pF R <sub>L</sub> = 1kΩ C <sub>L</sub> = 50pF		7.7 8.2	10.4 11.4	1.0 1.0	12.0 13.0	ns
t <sub>P</sub> LZ, t <sub>P</sub> HZ	Output Disable Time $\overline{OE}$ A to $\overline{Y}$ A or $\overline{OE}$ B to $\overline{Y}$ B	V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 50pF R <sub>L</sub> = 1kΩ		8.8	11.4	1.0	13.0	ns
t <sub>OS</sub> LH, t <sub>OS</sub> HL	Output to Output Skew	V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 50pF (Note 1.)			1.0		1.0	ns
C <sub>in</sub>	Maximum Input Capacitance			4	10		10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)			9				pF

C <sub>PD</sub>	Power Dissipation Capacitance (Note 2.)	Typical @ 25°C, V <sub>CC</sub> = 5.0V		pF
		19		

- Parameter guaranteed by design. t<sub>OS</sub>LH = |t<sub>PL</sub>H<sub>m</sub> - t<sub>PL</sub>H<sub>n</sub>|, t<sub>OS</sub>HL = |t<sub>PH</sub>L<sub>m</sub> - t<sub>PH</sub>L<sub>n</sub>|.
- C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC</sub>(OPR) = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/8 (per bit). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## NOISE CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns, C<sub>L</sub> = 50pF, V<sub>CC</sub> = 5.0V)

Symbol	Parameter	T <sub>A</sub> = 25°C		Unit
		Typ	Max	
V <sub>OL</sub> P	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.9	1.1	V
V <sub>OL</sub> V	Quiet Output Minimum Dynamic V <sub>OL</sub>	-0.9	-1.1	V
V <sub>I</sub> H <sub>D</sub>	Minimum High Level Dynamic Input Voltage		2.0	V
V <sub>I</sub> L <sub>D</sub>	Maximum Low Level Dynamic Input Voltage		0.8	V

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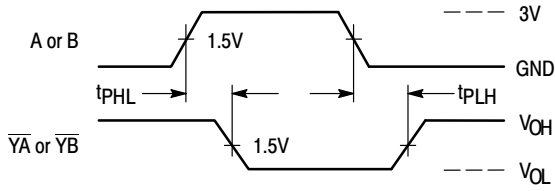


Figure 3. Switching Waveform

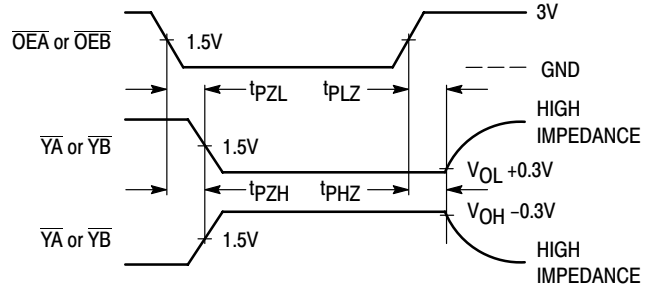
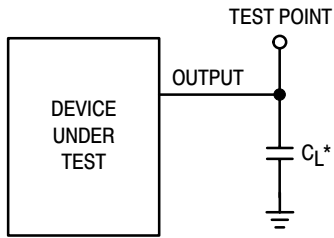
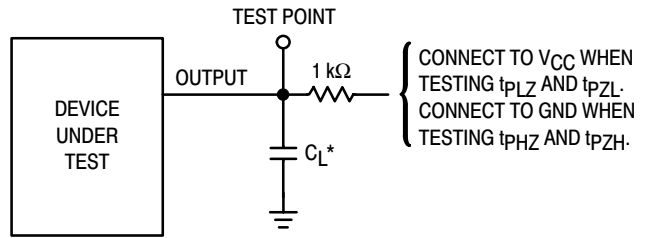


Figure 4. Switching Waveform



\*Includes all probe and jig capacitance

Figure 5. Test Circuit



\*Includes all probe and jig capacitance

Figure 6. Test Circuit

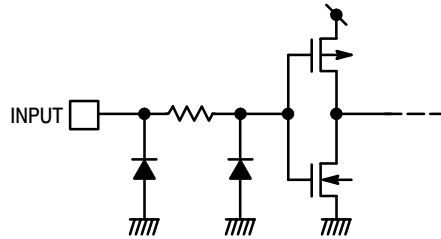


Figure 7. Input Equivalent Circuit