LOW QUIESCENT CURRENT, MULTI-MODE PMIC FOR BATTERY POWERED, ENERGY HARVESTING APPLICATIONS

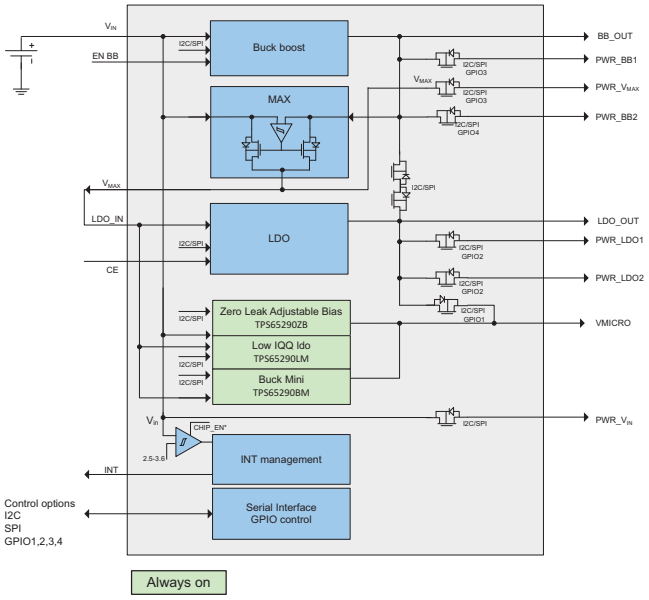
Check for Samples: TPS65290

FEATURES

- **Operating Input Voltage Range: 2.2 V to 5 V**
- **500-mA Buck-Boost Converter, Stand-Alone Operation or Serial Bus Controlled**
- **PFM/PWM Operation With Forced PWM Option**
- **150 mA LDO**
- **Stand-Alone or Serial Bus (SPI or I2C) Controlled**
- **Two Power Distribution Switches Powered from Buck-Boost Output**
- **One Power Distribution Switch Powered from the Maximum of Buck Boost or Battery Input**
- **Two Power Distribution Switches Powered from LDO Output**
- **One Power Switch Powered from Battery Input**
- **One Power Switch to Connect BB Output to LDO Output and Improve System Efficiency**
- **Automatic Power Max Function Between Battery Supply and Buck-Boost With Smart Capabilities to Maximize System Energy Management**
- **Low Power Always-On Bias Supply for Microcontroller Sleep Mode With Three Factory Selectable Options:**
  - **10-mA, 100-nA IDDQ Deep Sleep Zero Leakage Current Bias Controller With Pre-Set Voltage**
  - **10-mA, 400-nA IDDQ LDO_{MINI}**
  - **30-mA, 300-nA IDQQ $Buck_{MINI}$**
- **Input Voltage Recovery Comparator With Selectable Threshold**
- **Factory Selectable SPI/I2C Interface**
- **-40°C to 85°C Ambient Temperature Range**
- **24-Pin RHF (QFN) Package**

APPLICATIONS

- **Low Power, Energy Harvesting Systems**
- **Battery Powered Applications**



DESCRIPTION

TPS65290 is a PMIC designed to operate in applications dependent on efficient power management over a wide range of system load conditions ranging from fractions of a microamp to a few hundred miliamps. The device operates over a wide 2.2-V to 5-V input-voltage range and incorporates a very low quiescent current always-on power supply, a 500-mA buck/boost converter, a 150-mA low dropout regulator and 8 power distribution switches. The always-on supply features three different factory selectable options: 30mA buck converter with 300-nA quiescent current. 10-mA LDO with 400-nA quiescent current and 10-mA Zero IDDQ drop with 100-nA quiescent current. The buck-boost converter employs PFM/PWM operation with forced PWM option, for maximum overall efficiency. The switches can be used to support different configurations for the various loads supported by the TPS65290. For energy harvesting applications, a programmable input voltage monitor is integrated to allow for connection and disconnection of the different power blocks and switches without the intervention of the master processor.

DESCRIPTION (CONTINUED)

To maximize control flexibility, the TPS65290 includes a factory-selectable choice between SPI and I^2C interfaces. To minimize PC board footprint and reduce bill of materials (BOM) components and cost, the PMIC internally includes resistive dividers (boost/buck, LDO, V_{IN} monitor); I^2C pull-up resistors; SPI pull-down resistors; boost/buck compensation; and interrupt pull-up resistor. Only low-cost ceramic capacitors and power inductors are needed to complete a comprehensive multi-rail solution for efficient flow meter, handheld industrial, fitness and other long-term data-acquisition systems.

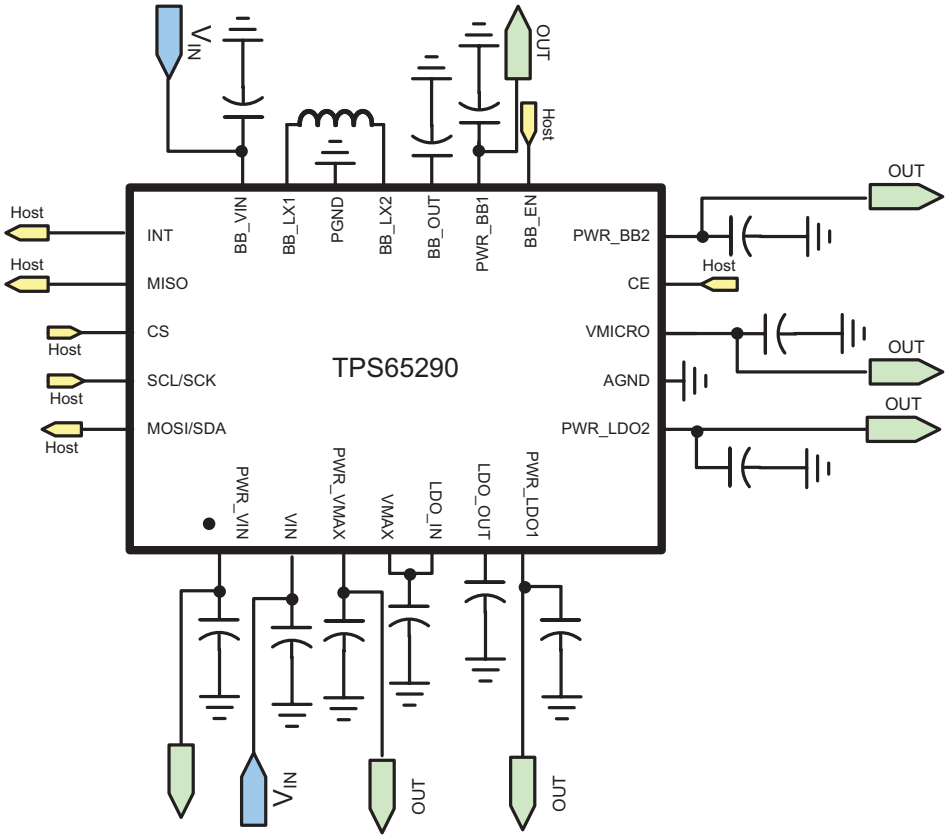
ORDERING INFORMATION

DEVICE	MARKING	FEATURES						PART NUMBER	
TPS65290		ZERO LEAK	LDO_{MINI}	$BUCK_{MINI}$	SPI	I2C	GPIO		
with zero bias IDQQ	TPS65290ZB	√			√			TPS65290ZBRHFR	reel of 3000
								TPS65290ZBRHFT	reel of 250
with LDO_{MINI}	TPS65290LM		√		√			TPS65290LMRHFR	reel of 3000
								TPS65290LMRHFT	reel of 250
with $buck_{MINI}$	TPS65290BM			√	√			TPS65290BMRHFR	reel of 3000
								TPS65290BMRHFT	reel of 250

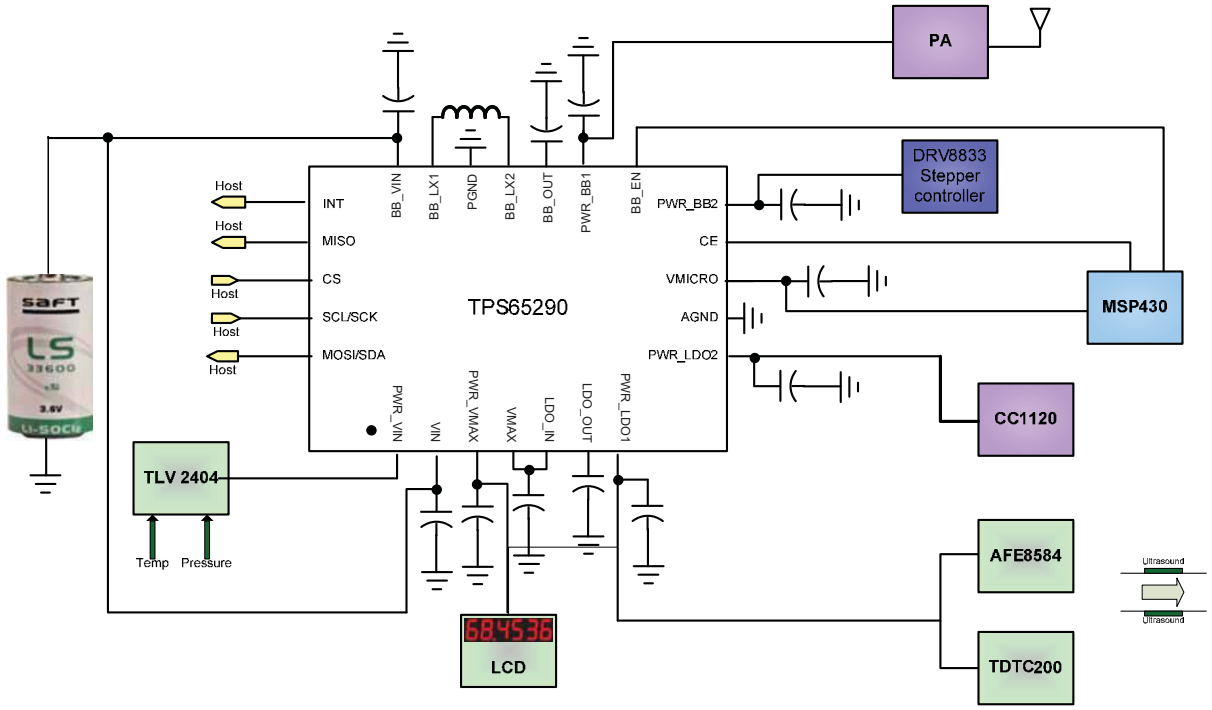
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

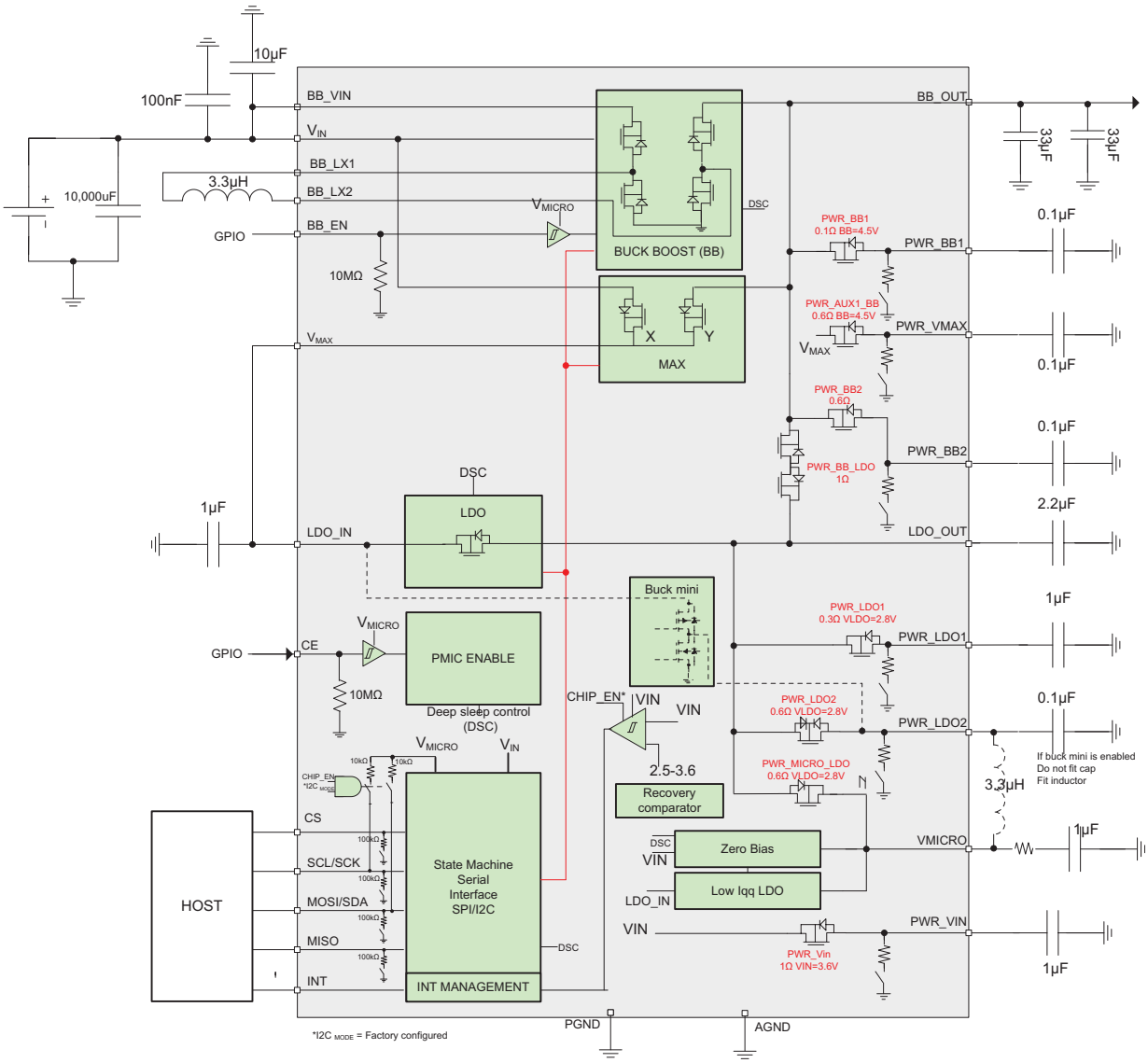
TYPICAL APPLICATION



TYPICAL FLOW METER APPLICATION



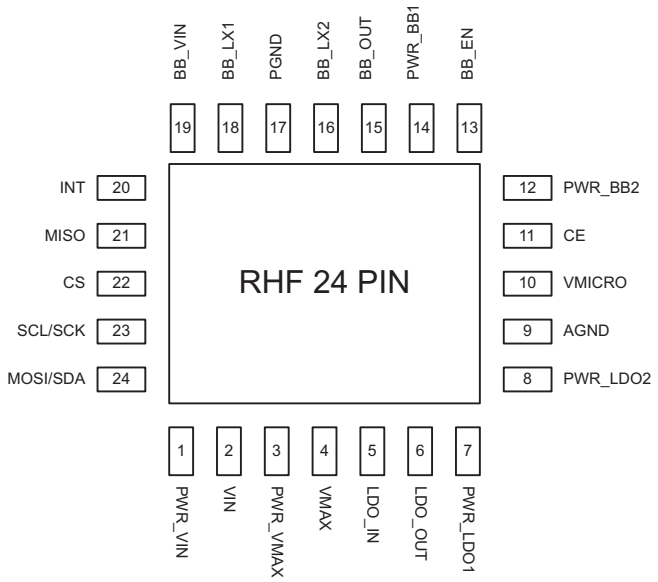
FUNCTION BLOCK DIAGRAM



BLOCK	FUNCTIONALITY			POWER SAVING OPTIONS		
		Reg	Bit		Reg	Bit
Buck boost	Enable	[0]	[0]	PFM/PWM mode	[3]	[6]
	Set voltage	[3]	[0,5]			
	UVLO disable	[3]	[5]			
LDO	Enable	[0]	[1]			
	Set voltage	[4]	[0,4]			
Zero drop, LDO_{MINI}, $BUCK_{MINI}$	Set voltage	[2]	[0,3]			
$BUCK_{MINI}$ low and high current mode	Operation Mode	[2]	[5,4]	Low current mode (for standby operation)	[2]	[5,4]
MAX	Latch on turn-off	[3]	[7]	See V_{MAX} options section		
	Turn-on options	[6]	[6,7]			
Recovery comparator	Set falling voltage	[6]	[5,3]	Enable/Disable	[8]	[0]
	Set rising voltage	[6]	[0,2]			
Power switches	Enable (BB, LDO, BAT, V_{MAX})	[0]	[2,7]	Enable/disable pull-down	[5]	[1,7]
		[7]	[1]	Fast/slow turn-on	[5]	[0]
	Enable (PWR_BB_LDO)	[7]	[0]			
Interruption management (INT)	INT status and masking	[7]	[2,7]	Power switches automatic disable when INT asserted	[8]	[1,7]
Bandgap				Enable/disable	[4]	[5]

PIN OUT

RGE PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
PWR_VIN	1	O	Power for system output from Vin
VIN	2	I	Battery supply
PWR_VMAX	3	O	Switch Controlled supply connected to VMAX. Decouple with a ceramic capacitor
VMAX	4	O	This pin shows the maximum of VBAT or VBB. Decouple with a 1µF ceramic capacitor
LDO_IN	5	I	LDO input. Decouple this pin with a 2.2µF ceramic capacitor
LDO_OUT	6	O	LDO output. Decouple this pin with a 2µF ceramic capacitor
PWR_LDO1	7	O	Switch Controlled supply connected to LDO output. Decouple with a ceramic capacitor.
PWR_LDO2	8	O	Switch Controlled supply connected to LDO output. Decouple with a ceramic capacitor.
AGND	9		Analog ground connection. Connect to PGND and power Pad.
VMICRO	10	O	Microcontroller supply
CE	11	I	When low the PMIC is in deep sleep and BIAS supply to the micro is enabled. The Interrupt output is disabled with a pull down termination. When high, the I2C/SPI is active; the internal switches can be operated, along with the interrupt logic, and Boost/Buck.
PWR_BB2	12	O	Switch Controlled supply connected to BB output. Decouple with a 1µF ceramic capacitor.
BB_EN	13	I	Buck-Boost converter enable pin
PWR_BB1	14	O	Switch Controlled supply connected to BB output. Decouple with a 1µF ceramic capacitor.
BB_OUT	15	O	Buck-Boost converter output
BB_LX2	16	O	Buck-boost Boost converter switching node
PGND	17		Power ground connection. Connect to AGND and power pad.
BB_LX1	18	O	Buck-boost Boost converter switching node
BB_VIN	19	I	Input pin to Buck-Boost converter
INT	20	O	Push-pull output, asserted when low
MISO	21	O	Serial Data Transmit interface (Master Input Slave Output)
CS	22	I	SPI bus Chip Select (active high) when SPI enabled
SCL/ SCK	23	I	Serial Data Clock (SPI and I2C)
MOSI/SDA	24	I	Serial Data Receive interface (Master Output Slave Input) for SPI and I2C

TERMINAL FUNCTIONS (continued)

NAME	NO.	I/O	DESCRIPTION
POWER PAD			Connect the pad to AGND, PGND and PCB GND. Thermal pad does not have electrical connections to IC.

OUTPUTS AND OPERATIONAL RANGE

TYPE	V_{OUT} (V)	DEFAULT	I_O MAX (mA)	SET ACCURACY	FEATURES
Buck Boost	1.0-5V, ~200mV steps	4.06V	500	3%	
LDO	0.8V for external divider 1.0-4.0V,~ 100mV steps	2.8V	150	4%	
Low bias supply	0.6-2.0V Selective drop from battery voltage, 8 steps adjustment	Vin-1.4	10	10% at 25°C	No IDQQ
	1.8-3.3 V 200mV steps	2.2V	10	5%	Low Iqq LDO
	1.8-3.3V 200mV steps	2.2V	30	5%	Low Iqq Buck
Power switches powered from BB output	PWR_BB1	Disabled	800	100 mΩ switch	1kΩ pull-down Single P mosfet
	PWR_BB2		350	600 mΩ switch,	
Power switches powered from VMAX	PWR_VMAX	Disabled	250	600 mΩ switch,	1kΩ pull-down Single P mosfet
Power switches powered from LDO output	PWR_LDO2	Disabled	250	600 mΩ switch,	1kΩ pull-down Single P mosfet
	PWR_MICRO_LDO		NA		
	PWR_LDO1	Disabled	250	300 mΩ	1kΩ pull-down Single P mosfet
Power switch connecting output of BB to LDO	PWR_BB_LDO	Disabled	250	1.0 Ω	1kΩ pull-down Back to back P mosfets
Power switch powered from battery	PWR_Vin	Disabled	100	1.0 Ω	1kΩ pull-down Single P mosfet
Recovery comparator	1.7-2.4V 100mV steps falling edge	2.0V	NA	3%	
	2.4-3.1V 100mV steps rising edge	2.4V			
MAX (Analog multiplexer)	Highest of BB and LDO	NA	150	NA	Configurable for turn-on and turn-off operation
INT (maskable)		All switches disabled by interruption			

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted)

	BB_VIN, BB_OUT, BB_FB, LDO_IN, PWR_BB2. PWR_VMAX	–0.3 to 7	V
	BB_LX1, BB_LX2	–1 to 7	V
	Any other pin	–0.3 to 5.5	V
	AGND, PGND	–0.3 to 0.3	V
T_J	Operating junction temperature range	–40 to 125	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
BB_VIN, VBAT	Input operating voltage BOOST CONVERTER	1.8	3.6	5	V
LDO_VIN	Input operating voltage LDO (V_{OUT} = 2.8V)	3		5	V
T_A	Ambient temperature	–40		125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION(1)

	MIN	MAX	UNIT
Human body model (HBM)	2000		V
Charge device model (CDM)	500		V

(1) SW_OUT1/2 pins' human body model (HBM) ESD protection rating 4 kV, and machine model (MM) rating 200V.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	T_A = 25°C Power Rating (W)	T_A = 85°C Power Rating (W)
RHF	29	30.6	3.26	1.30

ELECTRICAL CHARACTERISTICS

T_J = -40°C to 125°C, V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY UVLO AND INTERNAL SUPPLY						
V_{BAT}	Input voltage range for all blocks to be operational		2.2		5	V
IDD_Q	Quiescent current always on blocks Factory configured CHIP_EN=0	Zero bias mode		100		nA
		LDO_{MINI} mode		400		
		$BUCK_{MINI}$ mode		300		
		V_{IN} = 3.6V LDO enabled		5		
		V_{IN} = 3.6V, BB enabled V_{BB_OUT} = 4.5V PFM mode		40		
RECOVERY VOLTAGE COMPARATOR						
$COMP_{RVLEVEL}$	Threshold voltage serial interface selectable	Rising V_{IN} 8 steps 0.1V threshold	2.4		3.1	V
		Falling V_{IN} 8 steps 0.1V threshold	1.7		2.4	
$COMP_{RVACCURACY}$	Comparator accuracy			3		%
IQQ_{COMPRV}		Buck boost enabled		10		µA
		Buck boost disabled		10		
ENABLE PINS (CE, BB_EN)						
V_H	Enable high	V_{MICRO} = 2.2 TO 2.8V	1.2			V
V_L	Enable Low	V_{MICRO} = 2.2 TO 2.8V			0.4	V
BUCK-BOOST (BB)						
V_{IN}	Input voltage range		1.8		5	V
VIN_{START_UP}	Start-up voltage, no load VBB<4.5	-40°C ≤ T_A ≤ 85°C		1.8		V
	Start-up voltage, no load VBB>4.5	-40°C ≤ T_A ≤ 85°C		2.5		
$VIN_{SUSTAIN}$(1)	The minimum input voltage in which the buck-boost converter sustains it's operation after starting up	-40°C ≤ T_A ≤ 85°C		1.8		V
VBB	DC output accuracy (PWM mode)	T_J = 25°C	-3		3	%
	Maximum line regulation	V_{IN} = 3 to 3.6V I_{OUT} = 300mA		0.5		
	Maximum load regulation	I_O = 100 to 500mA		0.5		
$VBB_{OUTRANGE}$		29 steps 0.1V from 1 to 5V	1		5	V
f	Oscillator frequency			1600		kHz
$DUTY_{BUCK\_MIN}$	Minimum duty cycle in buck mode			25	30	%
I_{SW}	Average high side switch current limit	V_{IN} = 3.6 V, T_A = 25°C		2400		mA
	High side switch on resistance	V_{IN} = 3.6 V, T_A = 25°C		120		mΩ
	Low side switch on resistance	V_{IN} = 3.6 V, T_A = 25°C		120		mΩ
t_{STR_BB}	Startup time	I_{OUT} = 150mA, C_{OUT} = 2X 4.7µF, V_{OUT} = 4.0V		500		µs
LDO						
V_{LDO_IN}	Input voltage range	Full load operation	2.2		5	V
$V_{LDO\_OUT\_RANGE}$		32 steps 0.1V from 1 to 4V	1		4	V

(1) Specified by design.

ELECTRICAL CHARACTERISTICS (continued)

T_J = -40°C to 125°C, V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{LDO\_OUT\_ACCURACY}$	DC output accuracy	V_{IN} = 3.6V, V_{OUT} = 2.8V, T_J = -40°C to 125°C I_{Load} = 5mA	-4		4	%
LDO_{LINE_REG}	Line regulation	3.3V ≤ V_{IN} ≤ 6V, V_{OUT} = 2.8V, I_{OUT} = 5mA	-1		1	%
LDO_{LOAD_REG}	Load regulation	V_{IN} = 2.2~5V, 0 ≤ I_{OUT} ≤ 110mA	-2		2	%
V_{DROOP}	Dropout voltage- allow for 5% output voltage droop	V_{IN} = 3.6~6V, 0 ≤ I_{OUT} ≤ 150mA			300	mV
ICL	Output current limit	V_{LDO_OUT} = 2.8V, output voltage shorted		300		mA
PSRR	Power-supply rejection ratio 10 kHz	V_{LDO_OUT} = 2.8V, V_{IN} = 3.1V, 150mA loading		28		dB
t_{STRLDO}	Startup time, bandgap already enabled	C_{OUT} = 2.2µF, V_{OUT} = 2.8V, no load		200		µS
MICRO BIAS CIRCUIT (Different options)						
Zero Leak Adjustable Bias (TPS65290ZB)						
V_{IN}	Input voltage range		2.2		5	V
V_{MICRO_MIN}	Minimum output voltage			1.3		V
V_{BIAS_DROP}	Voltage difference between VBAT (pin#4) and Vmicro	9 200mV drop steps from 0.6 to 2V	0.6		2.0	V
V_{OUT}	DC output accuracy measured by V_{BIAS_DROP}.	T_J = +25°C, IOUT = 1µA, BAT=3.6V	-10		10	%
$ZERO_{LOAD\_REG}$	Load regulation	I_{OUT} = 100nA-10mA , T_J = +25°C, BAT = 3.6V, VMICRO[3:0] = 0000			15	%
Low IDDQ LDO, aka LDO_{MINI} (TPS65290LM)						
V_{IN}	Input voltage range		2.2		5	V
V_{LDO_RANGE}		16 steps 0.2V from 1.8 to 3.3V	1.8		3.3	V
V_{OUT}	DC output accuracy	T_J = +25°C, V_{IN} = 3.6V, I_{OUT} = 1µA	-5		5	%
LDO_{LOAD_REG}	Load regulation	1µA ≤ I_{OUT} ≤ 10mA	-5		5	%
V_{DROOP}	Dropout voltage– allow for 5% output voltage drop at V_{DROOP}.	V_{OUT} = 2.2V, I_{OUT} = 10mA			300	mV
ICL	Output current limit	V_{LDO_OUT} = 2.8V	20		50	mA
$BUCK_{MINI}$ Internal Converter Hysteretic (TPS65290BM)						
V_{IN_BM}	Input voltage range		2.2		5	V
I_{Load_BM}	Output load range		0		30	mA
F_{SW_BM} (2)	$Buck_{MINI}$ switching frequency	L_{BM} = 33µH, C_{BM} = 1µF, ESR_C_{BM} = 1Ω, No load		5		Hz
I_{PK_IND} (2)	Peak inductor current	T_J = +25°C , L_{BM} = 33µH, C_{BM} = 1µF, ESR_C_{BM} = 1Ω, V_{IN} = 3.6V, V_{OUT} = 2.5V, I_{OUT} = 30mA with high-power mode		80		mA
$I_{PK\_IND\_STARTUP}$ (2)	Peak inductor current during start up	T_J = +25°C , L_{BM} = 33µH, C_{BM} = 1µF, ESR_C_{BM} = 1Ω, V_{IN} = 3.6V, V_{OUT} = 2.5V, I_{OUT} = 30mA with high-power mode		140		mA
V_{BM_RIPPLE} (2)	Ripple voltage	T_J = +25°C , V_{IN} = 3.6V, V_{OUT} = 2.5V), L_{BM} = 33µH, C_{BM} = 1µF, ESR_C_{BM} = 1Ω,		5		%
POWER SWITCHES						
PWR_BB1	Distribution switch on resistance from BB_OUT to pin PWR_BB1 (Single P Mosfet)	V_{IN} = 3.6 V, V_{BB} = 4.5 V, T_A = 25°C		100		mΩ
PWR_VMAX_ V_{MAX}	Distribution switch on resistance from VMAX to pin PWR_VMAX (Single P Mosfet)	V_{IN} = 3.6 V, V_{BB} = 4.5 V, T_A = 25°C		600		mΩ
PWR_BB2	Distribution switch on resistance from BB_OUT to pin PWR_BB2 (Single P Mosfet)	V_{IN} = 3.6 V, V_{BB} = 4.5 V, T_A = 25°C		600		mΩ
PWR_LDO1	Distribution switch on resistance from LDO_OUT to pin PWR_LDO1 (Single P Mosfet)	V_{IN} = 3.6 V, V_{LDO} = 2.8 V, T_A = 25°C		300		mΩ
PWR_LDO2	Distribution switch on resistance from LDO_OUT to pin PWR_LDO2 (Single P Mosfet)	V_{IN} = 3.6 V, V_{LDO} = 2.8 V, T_A = 25°C		600		mΩ

(2) Specified by design.

ELECTRICAL CHARACTERISTICS (continued)

T_J = -40°C to 125°C, V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWR_MICRO_LDO	Distribution switch on resistance from LDO_OUT to pin VMICRO (Single P Mosfet)	V_{IN} = 3.6 V, V_{LDO} = 2.8 V, T_A = 25°C		600		mΩ
PWR_VIN	Distribution switch on resistance from VIN to pin PWR_VIN (Single P Mosfet)	V_{IN} = 3.6 V, T_A = 25°C		1000		mΩ
PWR_BB_LDO	Distribution switch on resistance (internal use only) from BB_OUT to LDO_OUT pin (Back to back P Mosfet)	V_{IN} = 3.6 V, V_{BB} = 4.5 V, T_A = 25°C		1000		mΩ
$R_{PULLDOWN}$	Pull-down resistance (Connection selectable by EEPROM bit)			1.2		kΩ
LOGIC LEVEL OUTPUTS (INT, MISO)						
V_{OL}	Output level low	V_{MICRO} = 2.2 to 2.8V , I_{load} = 1mA			0.4	V
V_{OH}	Output level high	V_{MICRO} =2.2 to 2.8V , I_{load} = 1mA	V_{MICRO} - 0.4			V
LOGIC LEVEL INPUT (CS, MOSI, CLK, SDA SCK)						
V_H	Input high level	V_{MICRO} = 2.2 to 2.8V	0.67 * V_{MICRO}			V
V_L	Input low level	V_{MICRO} = 2.2 to 2.8V			0.33 * V_{MICRO}	V
V_{HYS}	Input hysteresis		10			mV
R_{PULLUP}	Pull-up resistor to VMICRO When I2C mode enabled			10		kΩ
$R_{PULLDOWN}$	Pull-down resistor to GND When SPI mode enabled			100		kΩ
THERMAL SHUT-DOWN FOR BUCK BOOST CIRCUIT						
T_{TRIP_BB}				141		°C
T_{HYST_BB}				12		°C
CENTRAL THERMAL SHUTDOWN						
T_{TRIP_IC}	Thermal protection trip point	Rising temperature		160		°C
T_{HYST_IC}	Thermal protection hysteresis			20		°C

TYPICAL CHARACTERISTICS (BUCK BOOST)

T_J = 25°C (unless otherwise noted)

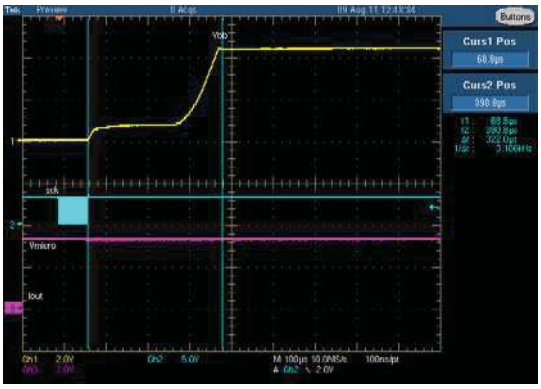


Figure 1. Buck Boost Startup Waveform with I2C Command Ch1: BB output. Ch2: I2C SCLK turns on buck-boost, Ch3: VMICRO. Startup time is 330µs. Buck Boost L and C are per application circuit.

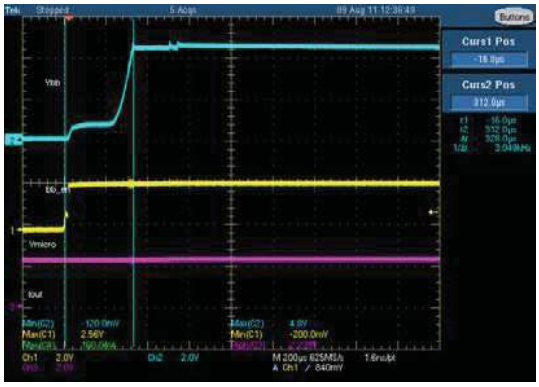


Figure 2. Buck Boost Startup Waveform with BB_EN Pin Command Ch2: BB output. Ch1: BB_EN signal. Ch3: VMICRO. Startup time is 330µs. Buck Boost L and C are per application circuit.

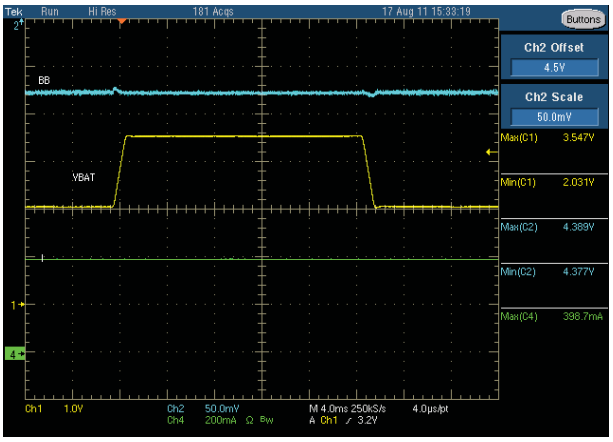


Figure 3. Buck Boost Line Regulation, Boost Mode

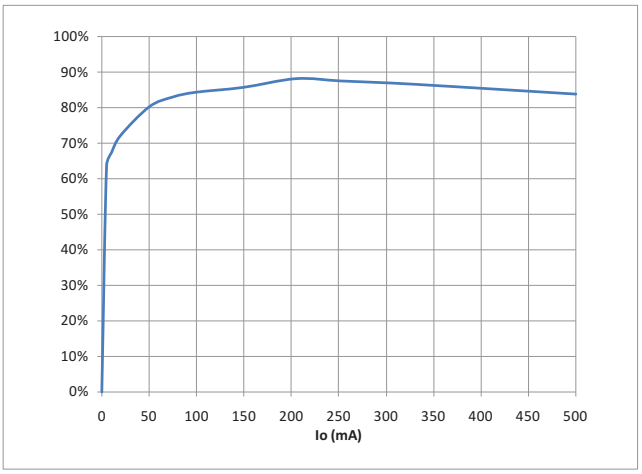


Figure 4. Buck Boost Efficiency V_{IN} = 3.6V, V_O = 4.5V

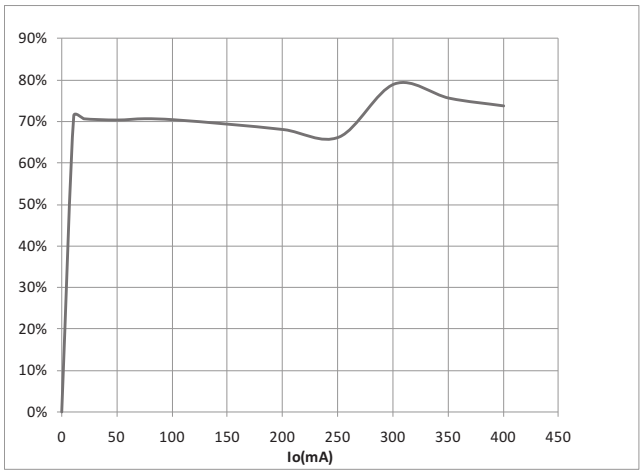


Figure 5. Buck Boost Efficiency V_{IN} = 2.5V, V_O = 4.5V

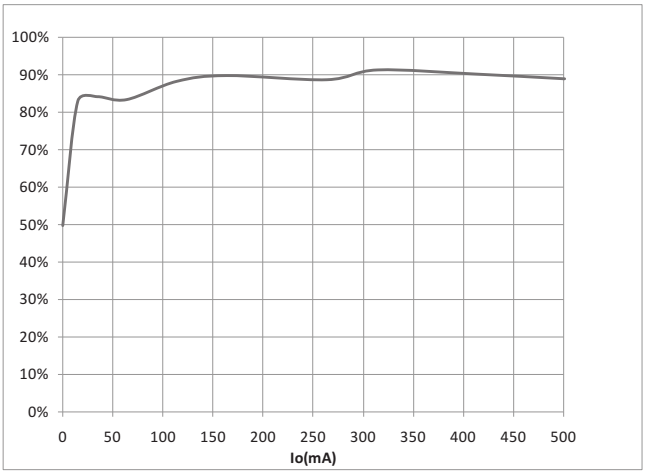


Figure 6. Buck Boost Efficiency V_{IN} = 3.6V, V_O = 2.8V

TYPICAL CHARACTERISTICS (BUCK BOOST) (continued)

T_J = 25°C (unless otherwise noted)

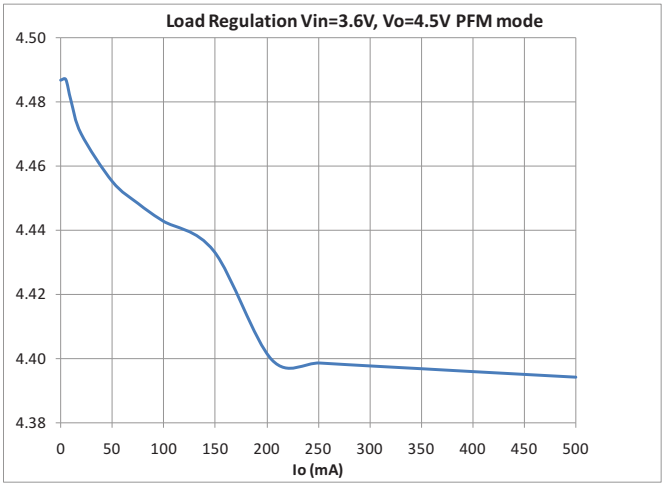


Figure 7. Buck Boost Load Regulation

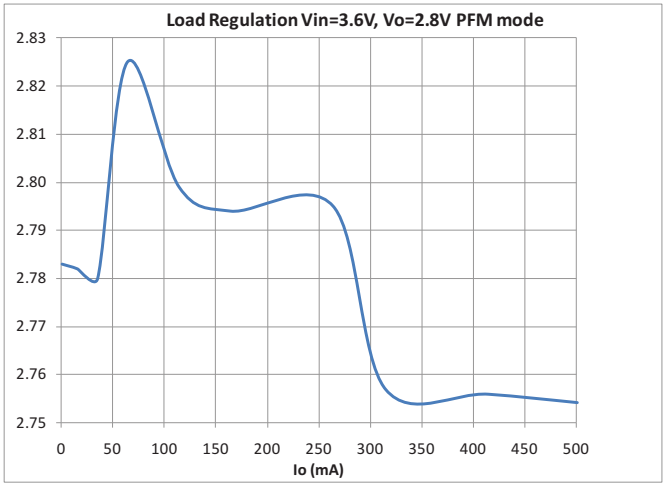
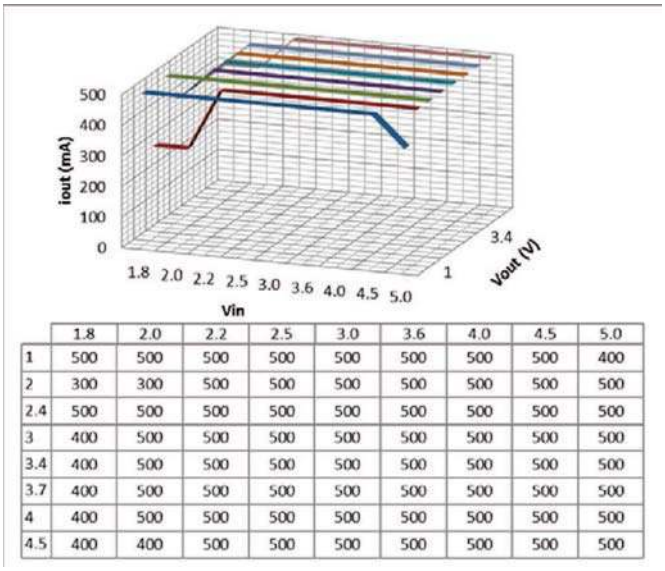
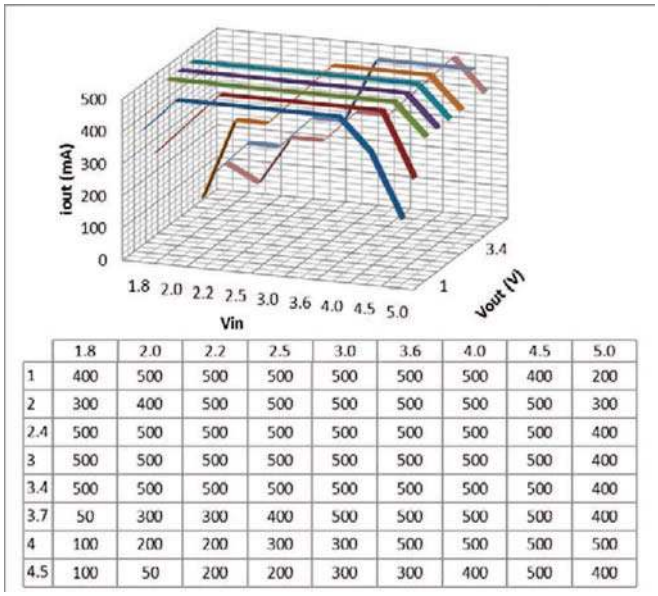


Figure 8. Buck Boost Load Regulation Buck Boost Loading 85°C Ambient V_{BB} < 4.5V



	1.8	2.0	2.2	2.5	3.0	3.6	4.0	4.5	5.0
1	500	500	500	500	500	500	500	500	400
2	300	300	500	500	500	500	500	500	500
2.4	500	500	500	500	500	500	500	500	500
3	400	500	500	500	500	500	500	500	500
3.4	400	500	500	500	500	500	500	500	500
3.7	400	500	500	500	500	500	500	500	500
4	400	500	500	500	500	500	500	500	500
4.5	400	400	500	500	500	500	500	500	500

Figure 9. Buck Boost Loading 25°C Ambient V_{BB} < 4.5V

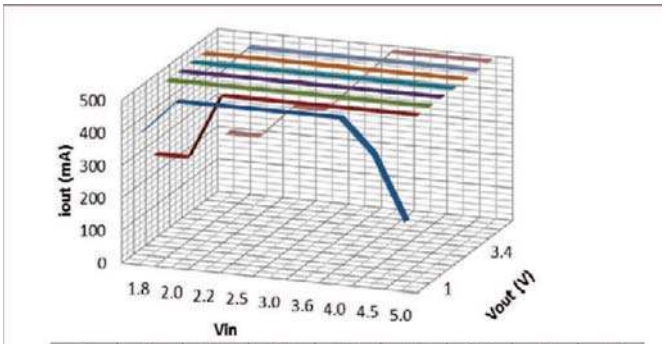


	1.8	2.0	2.2	2.5	3.0	3.6	4.0	4.5	5.0
1	400	500	500	500	500	500	500	400	200
2	300	400	500	500	500	500	500	500	300
2.4	500	500	500	500	500	500	500	500	400
3	500	500	500	500	500	500	500	500	400
3.4	500	500	500	500	500	500	500	500	400
3.7	50	300	300	400	500	500	500	500	400
4	100	200	200	300	300	500	500	500	500
4.5	100	50	200	200	300	300	400	500	400

Figure 10. Buck Boost Loading -40°C Ambient V_{BB} < 4.5V

TYPICAL CHARACTERISTICS (BUCK BOOST) (continued)

T_J = 25°C (unless otherwise noted)



	1.8	2.0	2.2	2.5	3.0	3.6	4.0	4.5	5.0
1	400	500	500	500	500	500	500	400	200
2	300	300	500	500	500	500	500	500	500
2.4	500	500	500	500	500	500	500	500	500
3	500	500	500	500	500	500	500	500	500
3.4	500	500	500	500	500	500	500	500	500
3.7	500	500	500	500	500	500	500	500	500
4	400	500	500	500	500	500	500	500	500
4.5	200	200	300	300	400	500	500	500	500

Figure 11. Buck Boost Loading -10°C Ambient V_{BB} < 4.5V

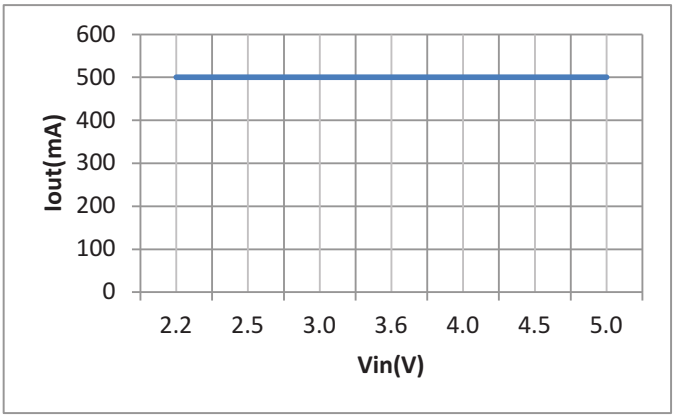


Figure 12. Buck Boost Loading 25°C Ambient V_{BB} > 4.5V

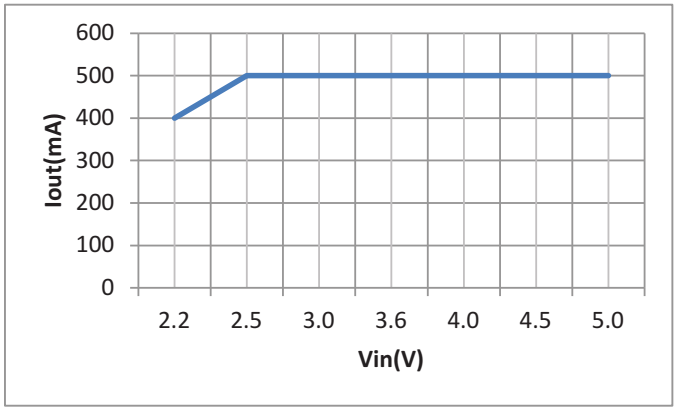


Figure 13. Buck Boost Loading 85°C Ambient V_{BB} > 4.5V

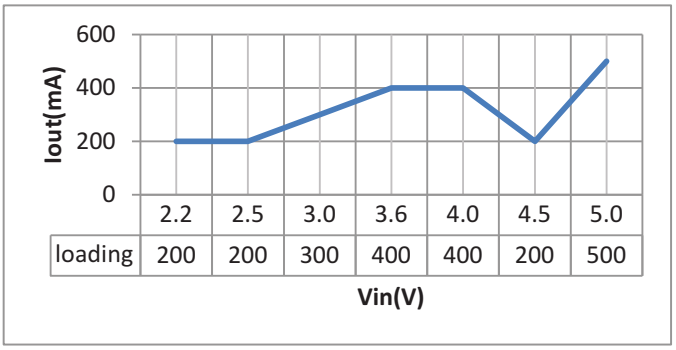


Figure 14. Buck Boost Loading -10°C Ambient V_{BB} > 4.5V

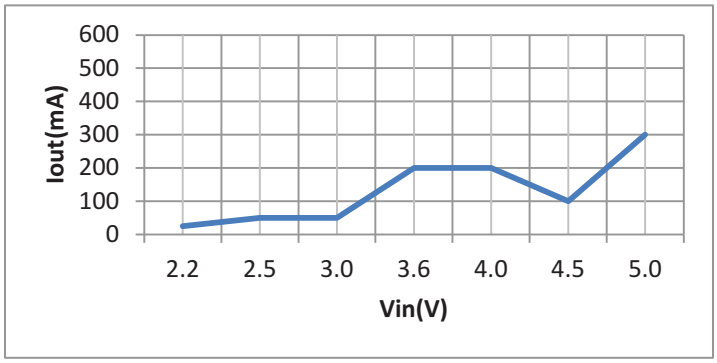


Figure 15. Buck Boost Loading -40°C Ambient V_{BB} > 4.5V

TYPICAL CHARACTERISTICS (LDO)

T_J = 25°C (unless otherwise noted)

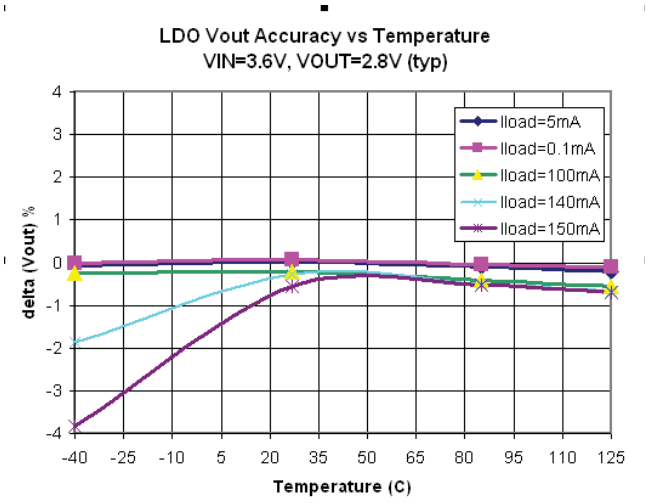


Figure 16.

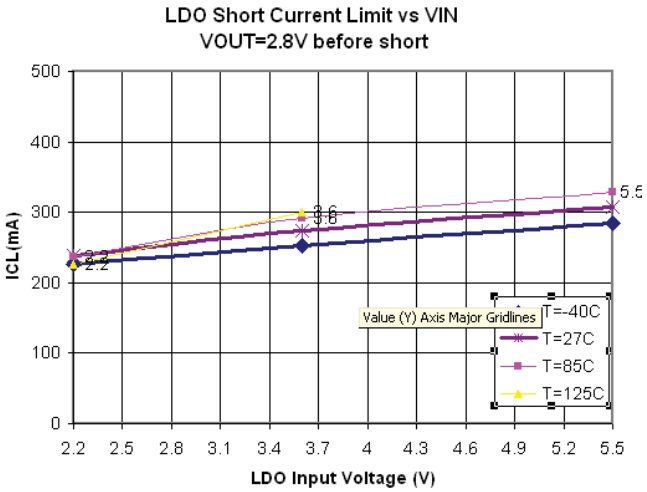


Figure 17.

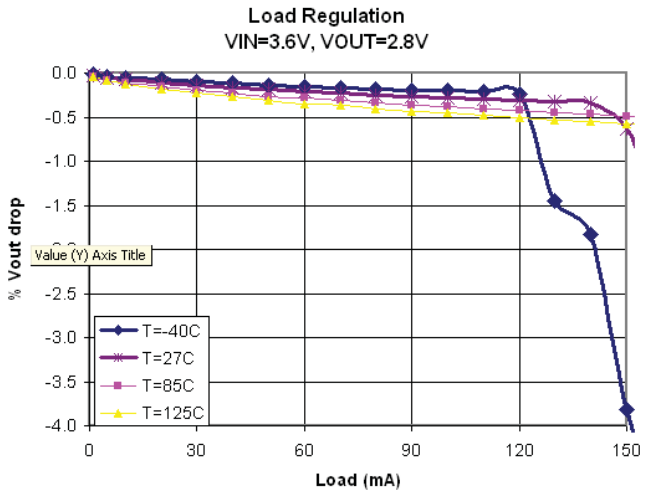


Figure 18.

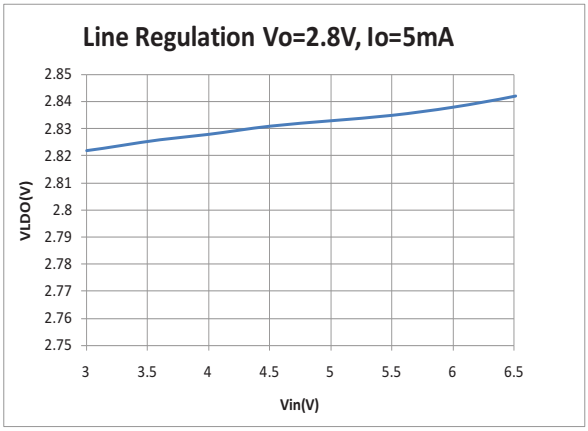


Figure 19.

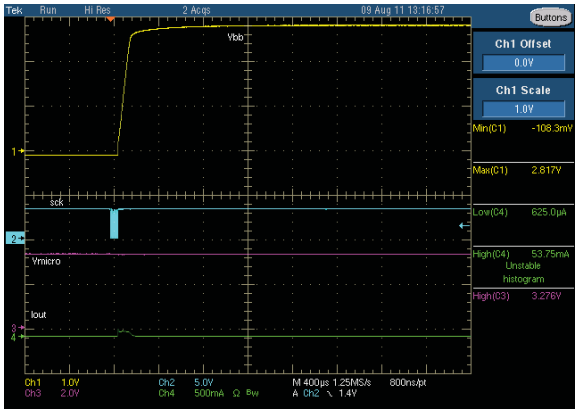


Figure 20. LDO Startup Waveform with I2C Command Ch1: LDO output. Ch 2: I2C SCLK, Ch3: VMICRO, Ch4: VIN current. Startup time is about 200µs.

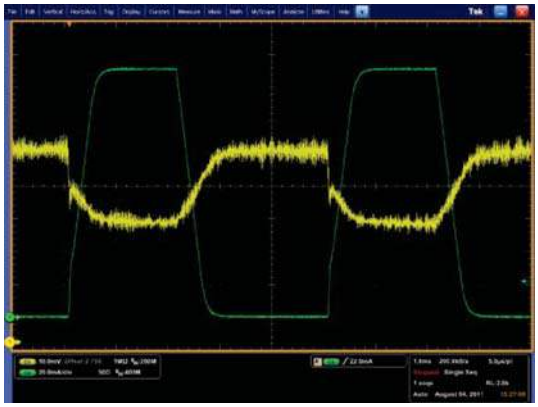


Figure 21. LDO Load Transient Response (0 to 150mA) Ch1: LDO output (10mV/div). Ch4 Load current (20mA/div).

TYPICAL CHARACTERISTICS (LDO) (continued)

T_J = 25°C (unless otherwise noted)

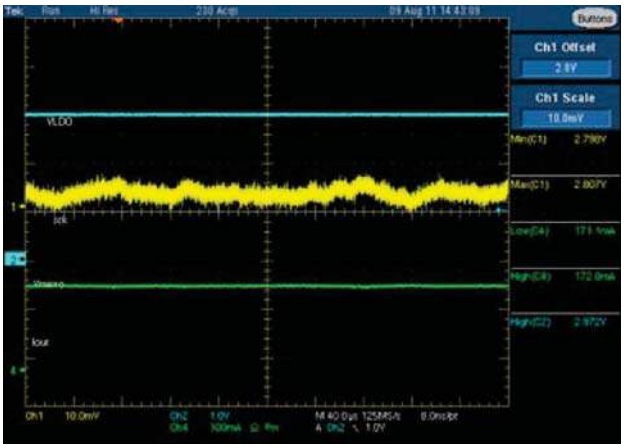


Figure 22. LDO Input to Output Voltage
Ch1: LDO output. Ch 2: LDO input, Ch3: Ch4: LDO current

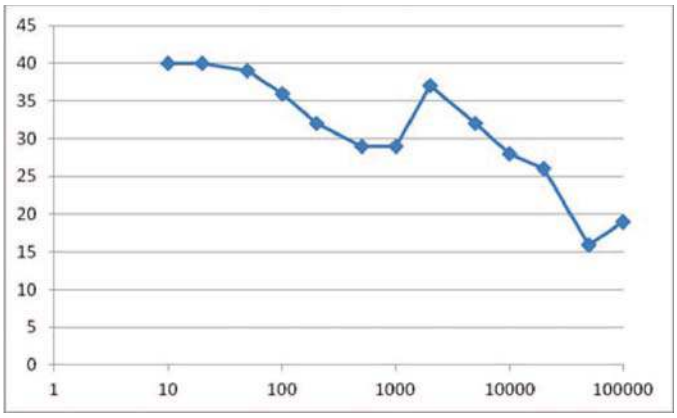


Figure 23. LDO PSRR(dB), 10 to 100kHz LDO output = 2.8V, LDO input = 3.1V, 150mA loading.

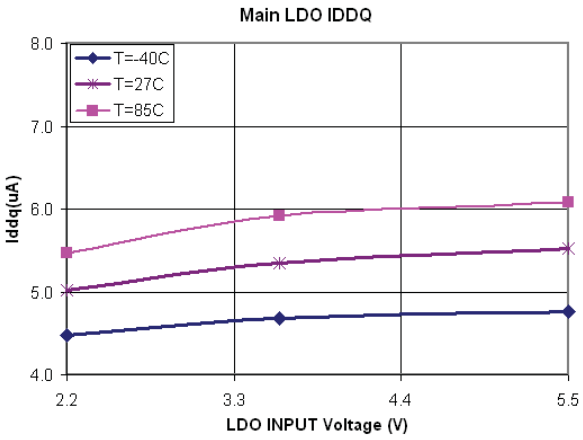


Figure 24.

TYPICAL CHARACTERISTICS (LDO_{MINI})

T_J = 25°C (unless otherwise noted)

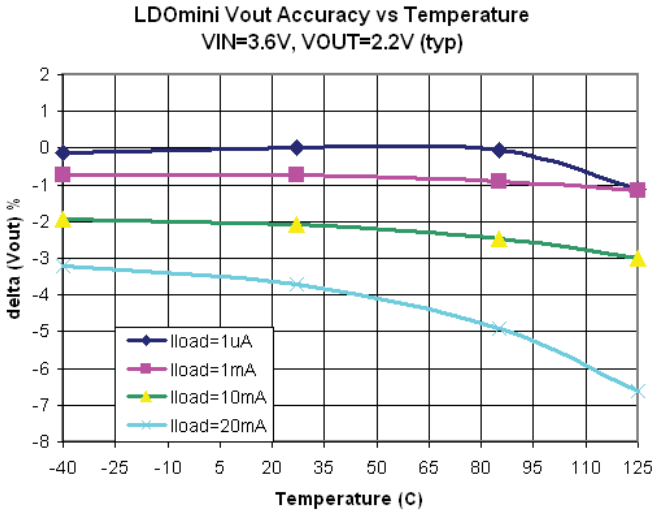


Figure 25.

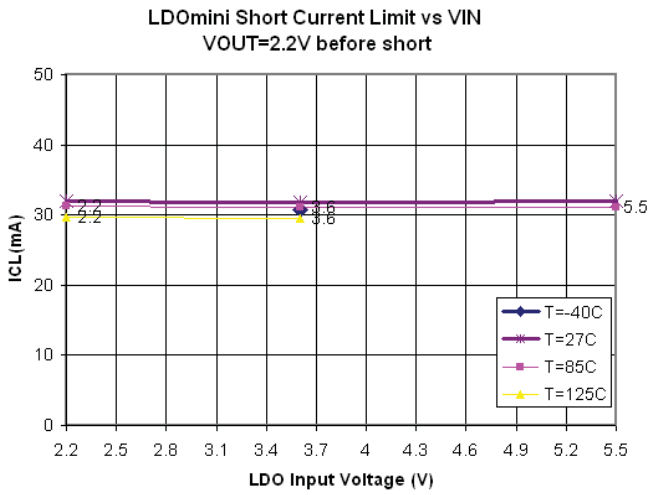


Figure 26.

TYPICAL CHARACTERISTICS (LDO_{MINI}) (continued)

T_J = 25°C (unless otherwise noted)

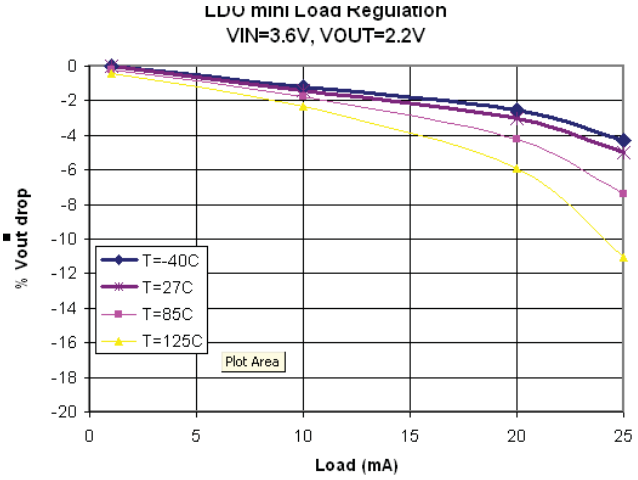


Figure 27.

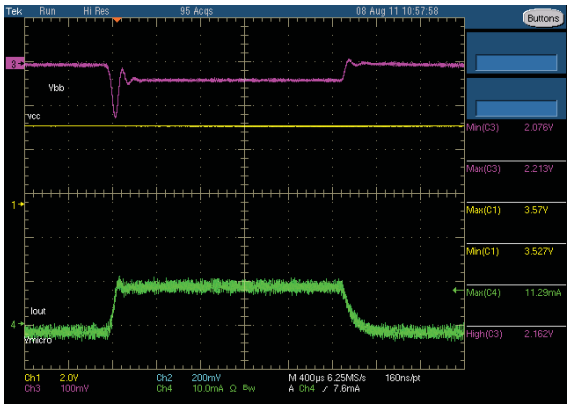


Figure 28. LDO_{MINI} Load Transient Response (0 to 10mA) Ch1: VBAT, Ch3: VMICRO (LDO_{MINI} output) (100mV/div). Ch4 Load current (10mA/div).

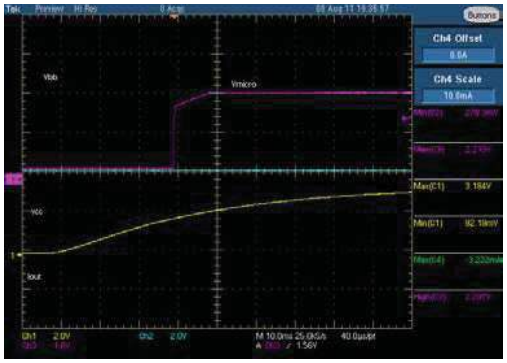


Figure 29. LDO_{MINI} Startup Waveform with VIN Rising Input battery connected to 27Ω resistor and 1000µF capacitor Ch1: VBAT rising. Ch 3: VMICRO (LDO_{MINI} output)

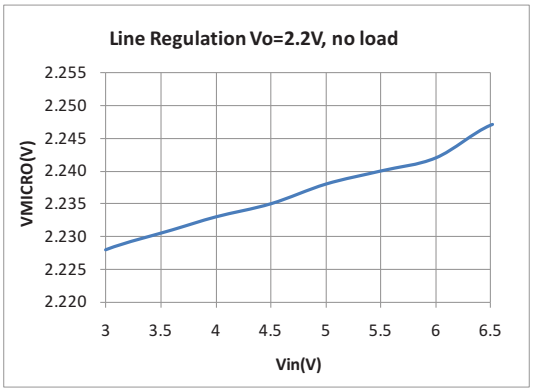


Figure 30.

TYPICAL CHARACTERISTICS (ZERO IDQQ)

T_J = 25°C (unless otherwise noted)

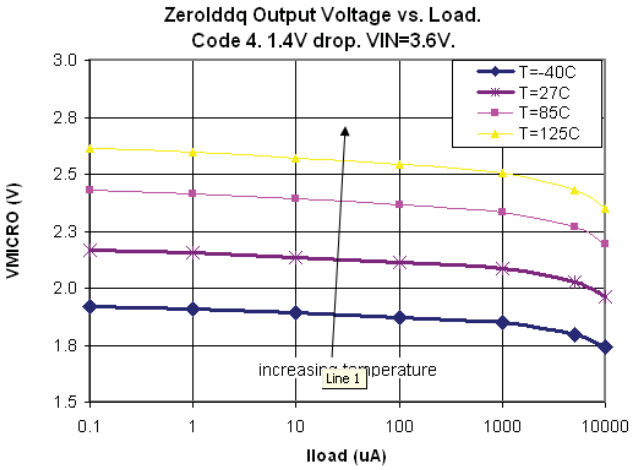


Figure 31.

Figure 32. ZEROiddq Load Transient Response (0 to 10mA) Code 4, 1.4V drop. Ch1: VBAT, Ch3: VMICRO (LDO_{MINI} output) (100mV/div). Ch4 Load current (10mA/div).

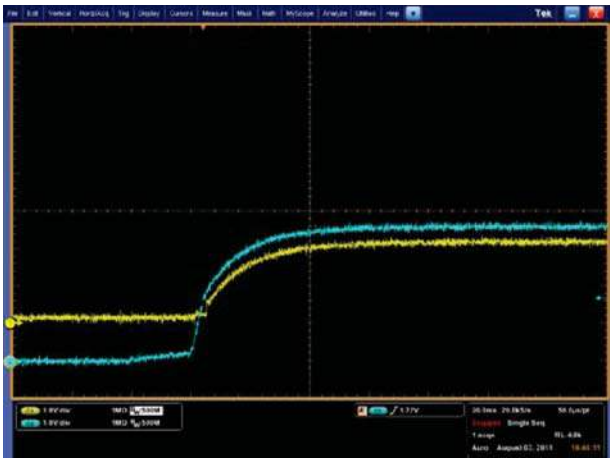


Figure 33. ZEROiddq Startup Waveform with VIN Rising Code 4, 1.4V drop Ch2: VBAT rising. Ch 3: VMICRO (ZEROIDDQ output)

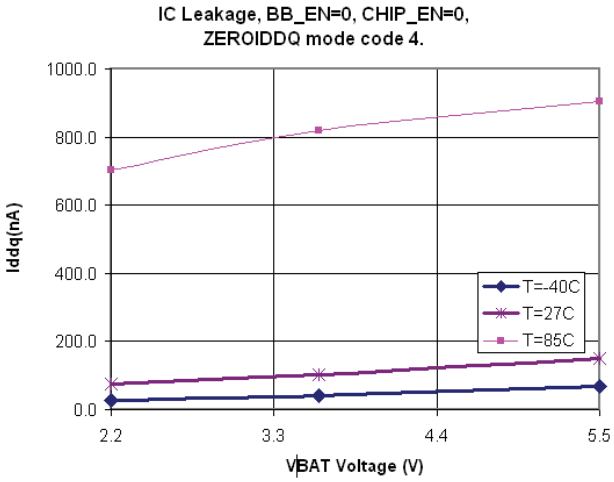


Figure 34.

TYPICAL CHARACTERISTICS ($BUCK_{MINI}$)

T_J = 25°C (unless otherwise noted)

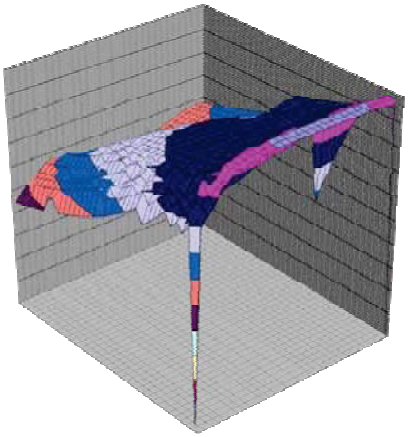


Figure 35. $BUCK_{MINI}$ Efficiency
C_O = 1µF, ESR = 1Ω, L = 33µF Automatic Mode

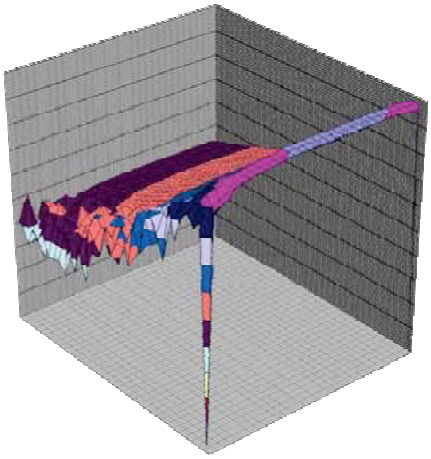


Figure 36. $BUCK_{MINI}$ Efficiency
C_O = 100µF, L = 33µF Automatic Mode

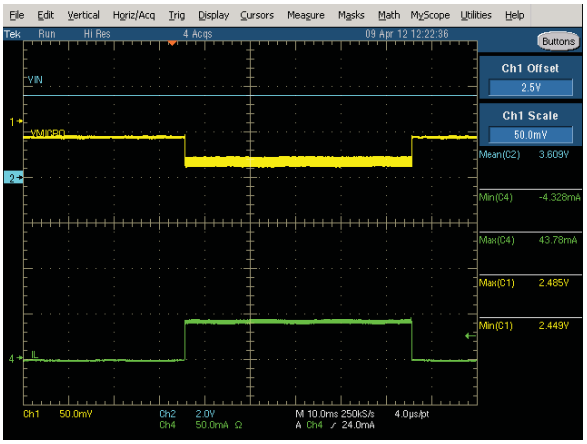


Figure 37. $BUCK_{MINI}$ Transient Response
V_{IN} = 3.6V, V_O = 2.5V 0-50mA Step

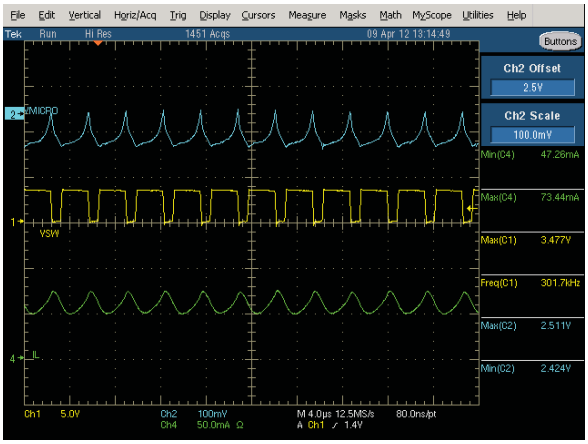


Figure 38. $BUCK_{MINI}$ Output Ripple
V_{IN} = 3.6V, V_O = 2.5V, I_O = 50mA

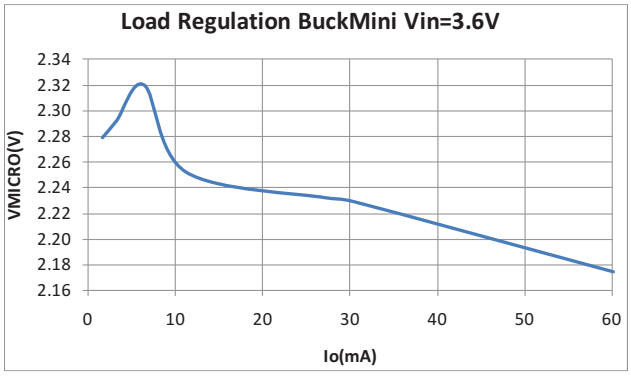


Figure 39. $BUCK_{MINI}$ Output Ripple
V_{IN} = 3.6V, V_O = 2.5V, I_O = 50mA

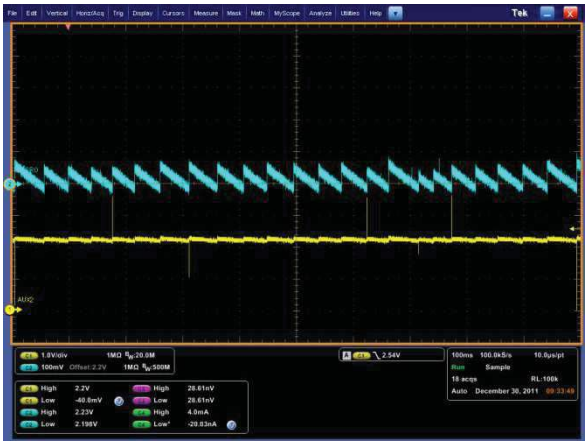


Figure 40. $BUCK_{MINI}$ Output Ripple
V_{IN} = 3.6V, V_O = 2.5V, I_O = 50mA

TYPICAL CHARACTERISTICS ($BUCK_{MINI}$) (continued)

T_J = 25°C (unless otherwise noted)

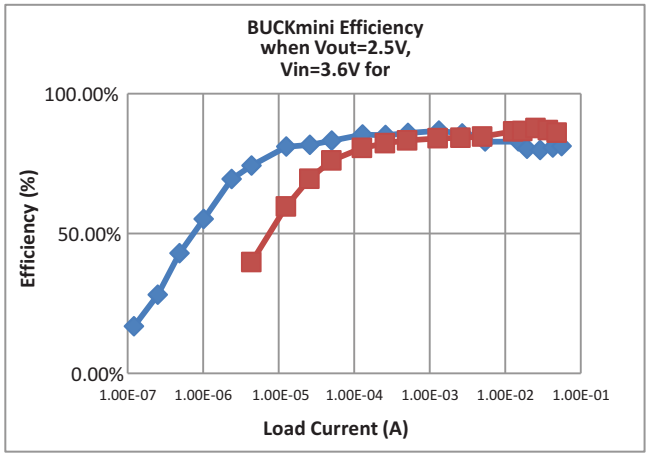


Figure 41.

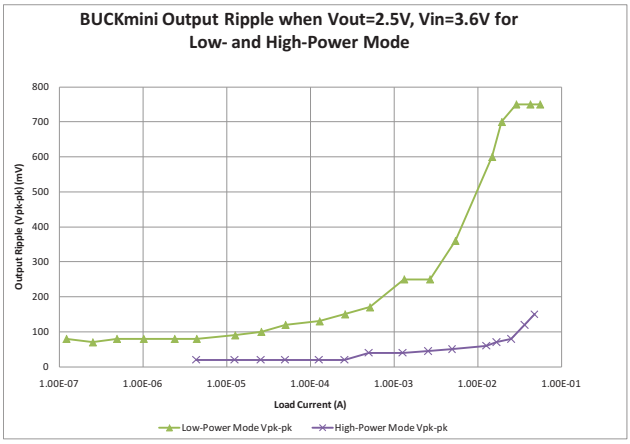


Figure 42.

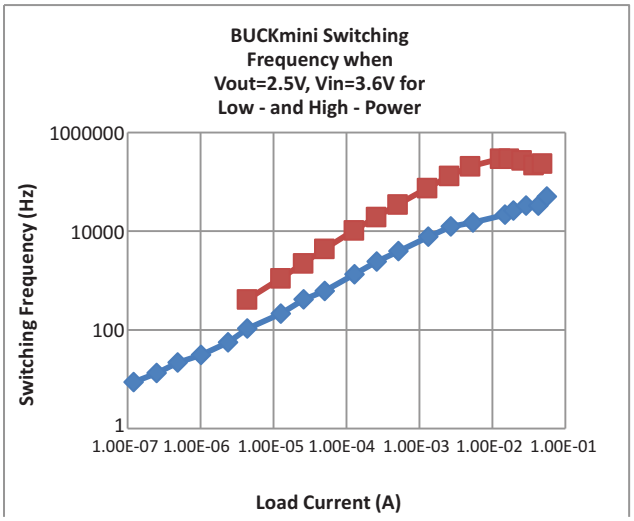


Figure 43.

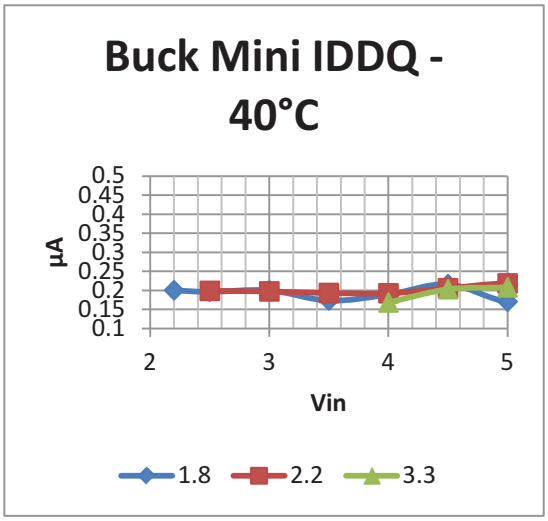


Figure 44.

TYPICAL CHARACTERISTICS ($BUCK_{MINI}$) (continued)

T_J = 25°C (unless otherwise noted)

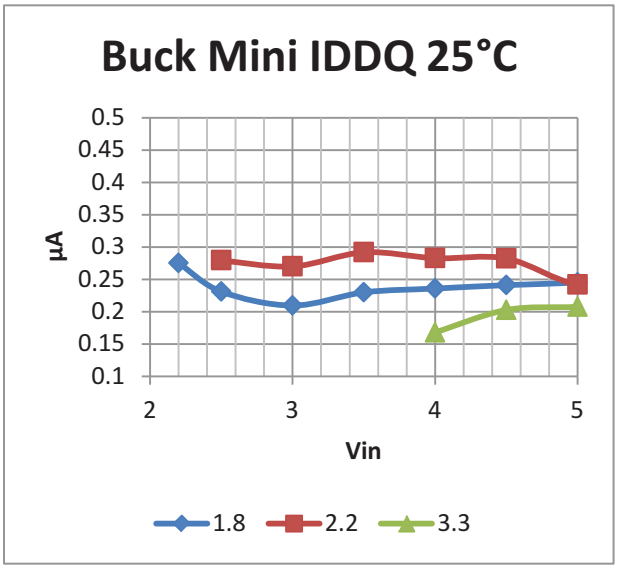


Figure 45.

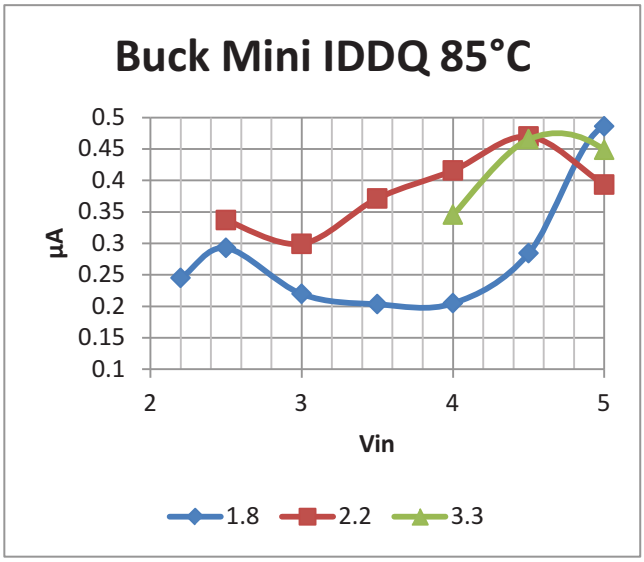


Figure 46.

TYPICAL CHARACTERISTICS (VMAX)

T_J = 25°C (unless otherwise noted)

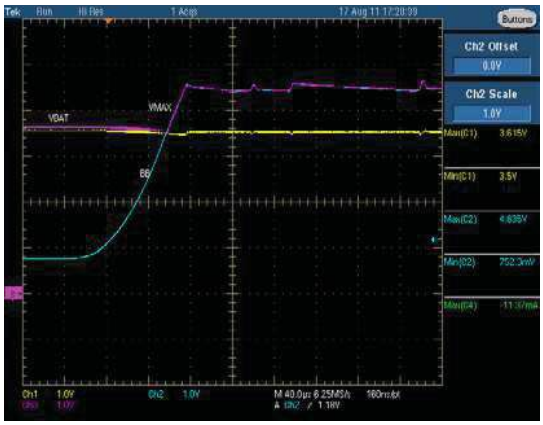


Figure 47. Typical VMAX Waveforms. Rising BB output.

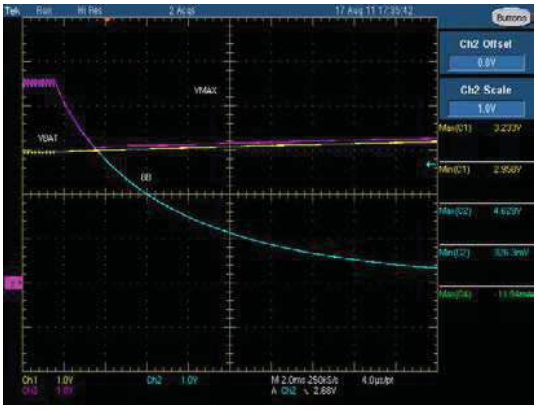


Figure 48. VMAX waveform. Falling BB output. Switch configured for VMAX = MAX(VBAT,VBBout) when BB output is disabled.

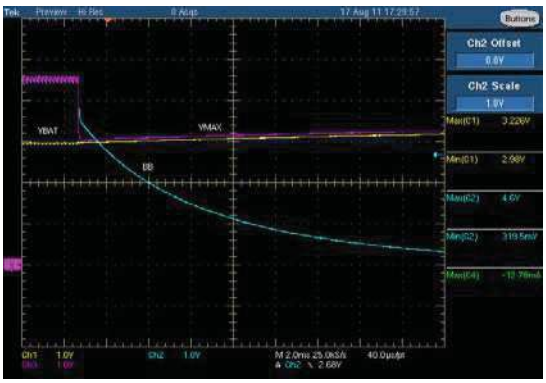


Figure 49. VMAX waveform. Falling BB output. Switch configured for VMAX = VBAT when BB output is disabled.

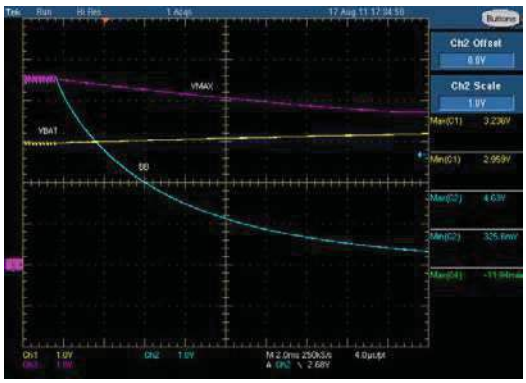


Figure 50. VMAX waveform. Falling BB output. Switch configured for VMAX = MAX(VBAT,VBBout)-diode when BB output is disabled. Note: VMAX is not loaded.

TYPICAL CHARACTERISTICS (VMAX) (continued)

T_J = 25°C (unless otherwise noted)

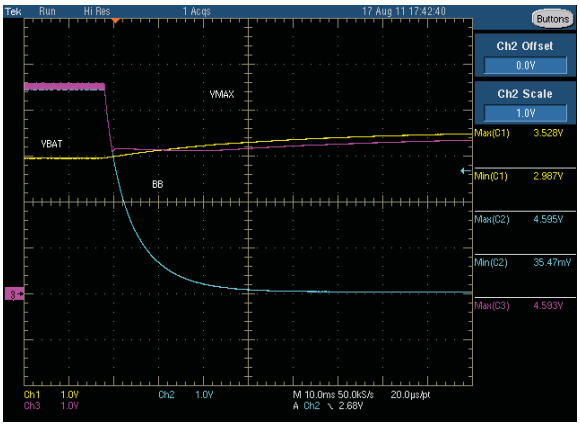


Figure 51. VMAX waveform. Falling BB output. Switch is configured for VMAX = MAX(VBAT,BBout). The VMAX comparator turns off automatically when BBout falls below VBAT at BB turn off.

CHOICE OF TPS65290 VERSION AND SERIAL INTERFACE

Once a voltage higher than 2.2V is applied to the VIN the always on supply will start as per the factory default setting. This will be the only block available within the device and will always stay on as long as the input supply does not drop beyond 2.2V.

There are 3 possible choices of always on supply. The main parameter for choice is the “efficiency” of the supply during sleep mode, mostly processor current.

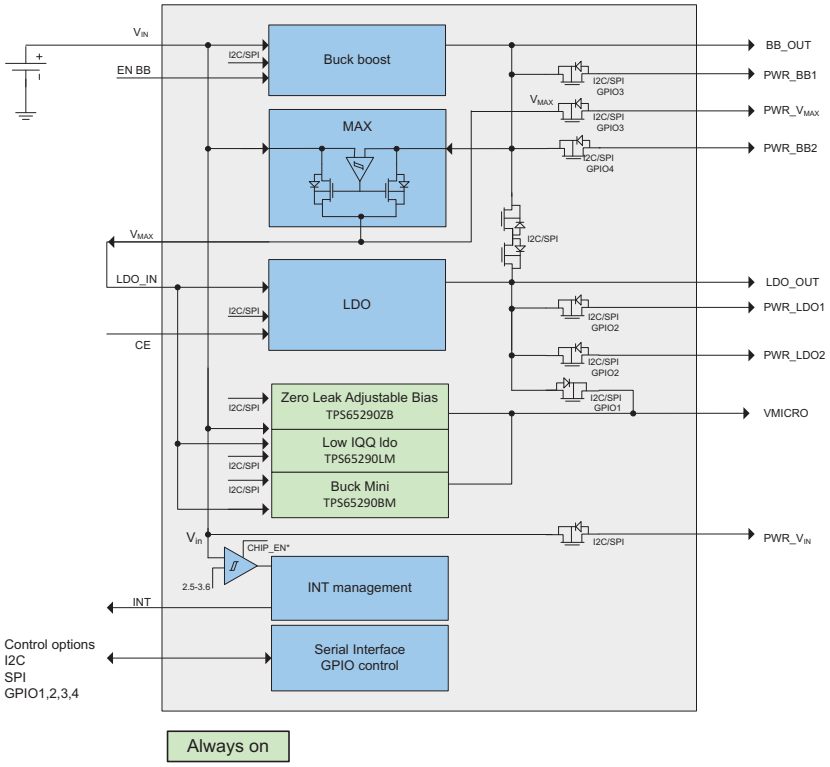


Figure 52.

Zero Bias set to V_{IN}-1.4

- Takes the least amount of quiescent current
- Provides voltage drops from 0.6 to 2V in 200mV steps
- Is not a regulated output
- Can be programmed to zero drop or to open circuit
- 10mA max

LDO_{MINI} set to 2.2V

- Provides a regulated output
- Can be programmed from 1.8 to 3.3V in 100mV steps
- 10mA max

$BUCK_{MINI}$ set to 2.2V

- Provides a regulated output
- Can be programmed from 1.8 to 3.3V in 100mV steps
- 30mA max
- Output has a ripple content
- Requires additional inductor (0603) and resistor (0402) PWR_AUX2 switch is disabled (pin becomes switching node)

The chosen serial interface for the part is SPI as I2C lines are open drain lines with internal 20kΩ pull-up resistors that guarantees 400kHz operation, but also create power losses when any of the bus lines are low. It is expected that operation with SPI will produce less average current consumption when compared to I2C. For I2C/GPIO operation please check with the factory.

FACTORY PROGRAMMED SETTINGS

The following blocks are programmed in the factory.

Buck boost

- Can be enabled or disabled when IC is enabled (can also be enabled with pin 15 high)
- Voltage can be set to
- 1.0 to 3.4V, 200mV steps
- 3.5 to 4.7V, 100mVsteps
- 4.9V, 5.0V
- Forced PWM or PFM (low power mode)
- Input UVLO comparator enabled/disabled. If disabled BB will try to operate with any input voltage higher than 1.8V LDO
- Can be disabled or enabled when IC is enabled
- Output voltage can be set to 1 to 4.0V, 100mV steps

Recovery comparator

- Can be enabled or disabled when IC is enabled
- Falling edge can be set to 1.7 to 2.4V, 100mV. An interruption is generated.
- Rising edge can be set to 2.4 to 3.1V, 100mV. The interruption is released.

Power switches

- Can be enabled or disabled when IC is enabled
- Pull-down resistance can be connected or disconnected when IC is enabled
- Power switches can be disabled when an Interruption is generated
- Switches can be turned on at slow or fast speed

USING THE TPS65290

Power UP and Enabling the IC

There are two ways of enabling the PMIC by setting the CE or BB_EN pins. If CE IS disabled only the always on blocks (as per default) and pull-down resistors are enabled by default.

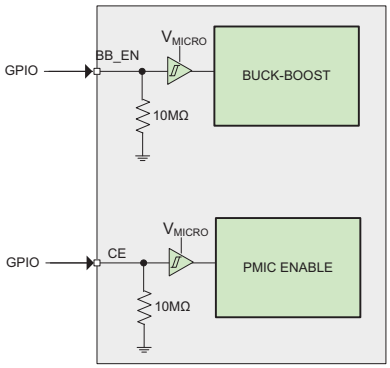


Figure 53. Power UP and Enabling the IC

When CE and BB_EN are low the PMIC is in deep sleep and bias supply to the micro is enabled. When high, the I2C/SPI is active; the internal switches can be operated, along with the interrupt logic, and Boost/Buck. The Buck boost is enabled either by BB_EN (high) or EN_BB bit (1). BB_EN can be used to enable the buck boost converter without need of the serial interface.

With the serial interface ACTIVE it is possible to enable, disable AND change settings for the power blocks. All changes on registers will be kept as long as the input supply is higher than 1.8V. If power is recycled the registers will be re-loaded with the programmed factory defaults.

Band-Gap Enable (Non EEPROM Setting)

The LDO bandgap is normally disabled to reduce consumption and it is enabled when either of the of LDO, LDO_{MINI} or $BUCK_{MINI}$ blocks are enabled. However, to speed up the power-up timing of the LDO it can be enabled in advance (register 4, bit 5)

$BUCK_{MINI}$ operation (Non EEPROM setting)

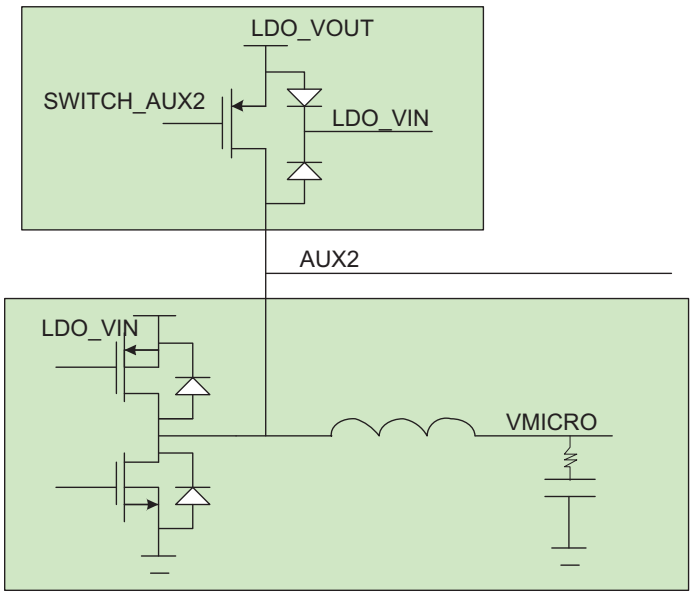


Figure 54.

$BUCK_{MINI}$ is a hysteretic buck converter that can deliver up to 30mA and therefore can be used beyond the sleep mode operation of the micro. When using this block is important to keep the following in mind:

- AUX2 output is not available as this pin is used to connect the external inductor required by the converter.
- If VMICRO has a ceramic capacitor, it is recommend to add a small resistor (0.5 to 1Ω) to guarantee a fixed ripple value at the output.
- $BUCK_{MINI}$ does not feature a current limit circuit. Overcurrent protection (if needed) needs to be provided externally.
- When used to support loads between 100µA to 1mA there is trade-off between input quiescent current and output ripple. It is suggested to use the settings for low and high power mode (Register 2, Bits [5,4]) to determine which power mode is most suitable for the application. Plots on the characteristics section show the typical trade-off between efficiency and ripple.
- $BUCK_{MINI}$ starts at automatic power selection mode. If loading higher than 100µA-1mA is required, set the $BUCK_{MINI}$ setting to (Register 2, Bits [5,4]) [11] to reduce ripple.
- Once the loading is removed, set (Register 2, Bits [5,4]) [10] to reduce power consumption

BUCK-BOOST OPERATION

Inductor Selection

To estimate the inductance of the buck-boost converter the following equations can be used:

$L_1 = (V_{IN\_MAX} - V_{OUT}) \times 0.5 \times (\mu s/A)$ (1)

$L_2 = V_{OUT} \times 0.5 \times (\mu s/A)$ (2)

L_1 is used for step down mode operation . VIN is the maximum input voltage. L_2 is used for boost mode operation is calculated. The recommended minimum inductor value is either L_1 or L_2 whichever is higher. As an example, a suitable inductor for generating 3.3V from a Li-ion battery with a battery voltage range from 2.5V up to 4.2V is 2.2µH. The recommended inductor range is between 1.5µH and 4.7µH. In general, this means that at high voltage conversion rates, higher inductor values offer better performance.

The table below shows the recommended inductance for input and output voltage combinations. The highest inductance among the region of interest is recommended.

Figure 55. Recommended Inductance for Input and Output Voltage Combination (µH)

Vout\Vin	1.8	1.9	2	2.2	2.5	3	3.6	4	4.5	5
1	0.4	0.45	0.5	0.6	0.75	1	1.3	1.5	1.75	2
2	1	1	1	0.1	0.25	0.5	0.8	1	1.25	1.5
2.4	1.2	1.2	1.2	1.2	0.05	0.3	0.6	0.8	1.05	1.3
3	1.5	1.5	1.5	1.5	1.5	1.5	0.3	0.5	0.75	1
3.4	1.7	1.7	1.7	1.7	1.7	1.7	0.1	0.3	0.55	0.8
4	2	2	2	2	2	2	2	2	0.25	0.5
4.5	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	0.25
5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5

With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. Equation 3 shows how to calculate the peak current I_1 in step down mode operation and Equation 4 show how to calculate the peak current I_2 in boost mode operation.

$$I_1 = \frac{I_{OUT}}{0.8} + \frac{V_{OUT}(V_{IN\_MAX} - V_{OUT})}{2 \bullet V_{OUT} \bullet f \bullet L} \quad (3)$$

$$I_2 = \frac{V_{OUT} \bullet I_{OUT}}{0.8 \bullet V_{IN\_MIN}} + \frac{V_{IN\_MIN}(V_{OUT} - V_{IN\_MIN})}{2 \bullet V_{OUT} \bullet f \bullet L} \quad (4)$$

In both equations f is the switching frequency. The critical current value for selecting the right inductor is the higher value of I_1 and I_2. It also needs to be taken into account that load transient and error conditions may cause higher inductor currents. This also needs to be taken into account when selecting an appropriate inductor.

The table below shows the recommended inductor current rating for input and output voltage combinations with assumption of 1.6MHz switching frequency, 500mA loading, 3.3µH inductance. The highest current rating among the region of interest is recommended.

Figure 56. Recommended Inductor Current Rating for Input and Output Voltage Combination with 3.3µH Inductor, 1.6MHz Switching Frequency and 500mA load (A)

Vout\Vin	1.8	1.9	2	2.2	2.5	3	3.6	4	4.5	5
1	0.79	0.79	0.80	0.80	0.81	0.81	0.82	0.82	0.82	0.82
2	0.85	0.80	0.75	0.77	0.79	0.81	0.83	0.84	0.85	0.86
2.4	1.04	0.98	0.93	0.84	0.76	0.79	0.82	0.84	0.85	0.86
3	1.32	1.25	1.19	1.08	0.94	0.75	0.80	0.82	0.84	0.86
3.4	1.49	1.42	1.35	1.23	1.08	0.88	0.77	0.80	0.83	0.85
4	1.76	1.67	1.59	1.45	1.29	1.07	0.87	0.75	0.79	0.82
4.5	1.97	1.88	1.79	1.64	1.45	1.22	1.00	0.88	0.75	0.79
5	2.19	2.08	1.99	1.82	1.61	1.36	1.13	1.01	0.87	0.75

Buck-Boost Input Capacitor Selection

A 10µF ceramic capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the buck-boost input pin and power ground of the IC is recommended.

Battery Input Pin Capacitor Selection

To make sure that the internal control circuits are supplied with a stable low noise supply voltage, a capacitor can be connected between VIN and AGND. Using a ceramic capacitor with a value of 0.1µF is recommended. The value of this capacitor should not be higher than 0. 22µF

Buck-Boost Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the BB_OUT and PGND. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the BB_OUT and PGND pins of the IC.

To get an estimate of the recommended minimum output capacitance, the following equation can be used.

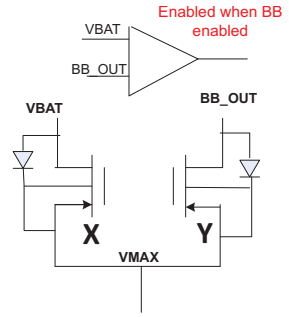
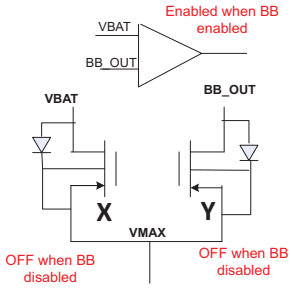
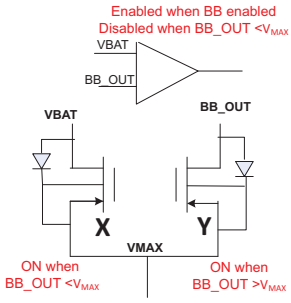
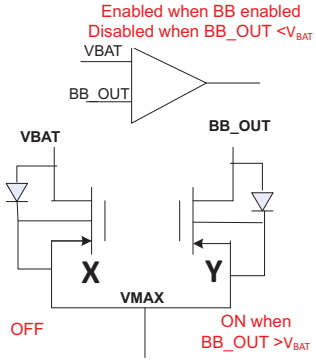
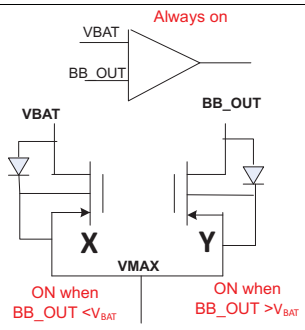
(5)

A capacitor with a value in the range of the calculated minimum should be used. There are no additional requirements regarding minimum ESR. There is also no upper limit for the output capacitor value. Larger capacitors will cause lower output voltage ripple as well as lower output voltage drop during load transients.

Setting V_{MAX} (Non EEPROM Setting)

The operation of V_{MAX} is not set on EEPROM and the switches inside the block can be programmed for specific conditions such as diode drops, To connect to VBAT, To follow the maximum voltage with its logic enabled or to follow the maximum voltage and to connect to VBAT when VBB is lower than VBAT and to disconnect the V_{MAX} logic. The following table shows the options available.

Table 1. Setting V_{MAX} (Non EEPROM Setting)

REG6_BIT6 VMAXx_DIS	REG6_BIT7 VMAXx_EN	REG3_BIT7 VMAX_LATCH	OPERATION	
0	0	0	V_{MAX} switch comparator is enabled when BB is enabled. When BB is disabled, the switch that connects V_{MAX} to V_{BAT} is turned on.	
1	0	0	V_{MAX} switch comparator is enabled when BB is enabled. When BB is disabled, the V_{MAX} switches are BOTH turned off.	
0	0	1	V_{MAX} switch comparator is enabled when BB is enabled. When BB is disabled, the comparator remains on until BB_OUT goes below V_{MAX}. V_{MAX} follows BB output until BB output voltage goes below V_{BAT} voltage. At that point, V_{MAX} switch comparator is disabled, and V_{MAX} is connected to V_{BAT} with 0 Iddq static logic.	
1	0	1	V_{MAX} switch comparator is enabled when BB is enabled. When BB is disabled and BB_OUT drops below V_{BAT}, both switches in V_{MAX} block are disabled and V_{MAX} will be a diode below V_{BAT} when BB is turned off.	
X	1	X	When VMAX_EN=1 regardless of other bits status, V_{MAX} logic is always ON and monitors VBAT vs. BB_OUT voltage and connect to the maximum voltage. The comparator consumes about 25µA. VMAX_EN can be set to 1 before transmission phase and then set to zero at the end of transmission phase when chip goes to sleep mode.	

LDO Output Capacitor

A 2.2µH capacitor is recommended to be placed as close as possible to the LDO output pin and AGND . In particular, a good ground plane for the TPS65290 and the LDO output capacitor is highly recommended to prevent LDO overshoot during the buck-boost converter operation.

Recovery Comparator (EEPROM Setting)

The recovery comparator is designed to track the operation of a high output impedance battery. When a load is applied the battery voltage collapses and the input voltage monitor detects the falling edge and issues and interruption when the programmable falling edge threshold an interruption is generated and the PMIC switches are automatically disabled as per the choice set in register 8. Once the switches are disabled the loading on the battery will collapse and its voltage will rise. The recovery comparator will monitor this rising edge (as per the programmed setting) and will automatically re-start the switches disabled when the battery voltage collapsed.

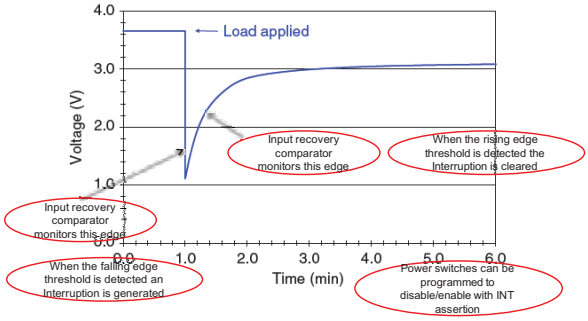


Figure 57. Recovery Comparator (EEPROM Setting)

Thermal Shut Down

TPS65290 has two over temperature sensors. The buck boost temperature sensor is close to the buck boost power FETs and monitors the power and heat going into the buck-boost block. The central temperature sensor is monitoring the rest of the chip and its temperature is set at a higher temperature. At the digital core level, outputs of both temperature sensors are ORed together. The following diagrams show the logic for buck-boost enable (BB_EN) and power switches. In the example below, the diagram for BB_PWR_PA switch is shown. The same diagram applies to 1Wire, SEI, AUX1, AUX2, RF, and LDOBB switches.

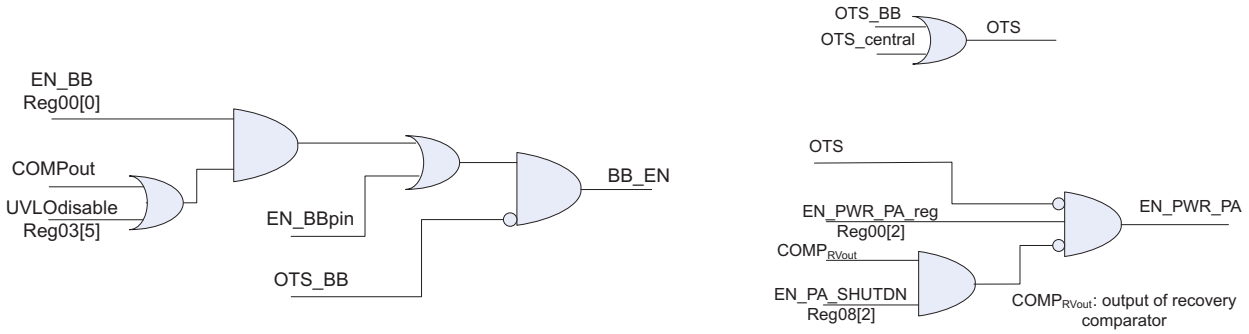


Figure 58. Thermal Shut Down

Operation of the IC During RF Transmission at Full Power

For high power output transmission, BB output voltage will power up the power amplifier with a voltage set to 3V to 5V at buck boost output. Pulse currents of tens to hundreds of mA are common in wireless sensor systems during transmit and receive modes. These high current pulses place special demands on batteries. Repeated delivery of pulse currents exceeding the recommended load current of a given chemistry diminishes the useful life of the cell. The effects can be severe, depending on the amplitude of the current and the particular cell chemistry and construction. Also the internal impedance of the cell often results in an internal voltage drop that precludes the cell from delivering the pulse current at the voltage necessary to operate the external circuit.

One method of mitigating these effects is to place a low equivalent series resistance (ESR) capacitor across the battery. The battery charges the capacitor between discharge pulses, and the capacitor delivers the pulse current to the load. To determine the required capacitance the following parameters are required:

- Battery impedance (at temperature and state-of-charge)
- Battery voltage (as a function of state-of-charge)
- Operating temperatures
- Pulse current amplitude
- Pulse current duration
- Allowable voltage drop during pulse discharge

The following equations are used to calculate the output capacitance needed to deliver the specified pulse current of a known duration and the latency time that must be imposed between pulses to allow the capacitor to be recharged by the battery. Both formulas assume that the capacitor ESR is sufficiently low to result in negligible internal voltage drop while delivering the specified pulse current; consequently, only the battery resistance is considered in the formula used to compute capacitor charging time, and only the load resistance is considered when computing the capacitance needed to deliver the discharge current.

The first step in creating a battery-capacitor couple for pulse-current applications is to size the capacitance using the following discharge formula:

$$C = t / R \times [-\ln (V_{MIN} / V_{MAX})] \quad (6)$$

Where:

C = output capacitance in parallel with battery

t = pulse duration

R = load resistance = V_{OUT}(average) / Ipulse

V_{MIN} and V_{MAX} are determined by the combination of the battery voltage at a given state-of-charge and the operating voltage requirement of the external circuit. Once the capacitance has been determined, the capacitor charging time can be calculated using the following charge formula:

$$t = R \times C \times [-\ln (1 - V_{MIN} / V_{MAX})] \quad (7)$$

Where:

t = capacitor charging time from V_{MIN} to V_{MAX}

R = battery resistance

C = output capacitance in parallel with battery

Again, V_{MIN} and V_{MAX} are functions of the battery voltage and the circuit operating specifications. Battery resistance varies according to temperature and state-of-charge as described above. Worst-case conditions are often applied to the calculations to ensure proper system operation over temperature extremes, battery condition, capacitance tolerance, etc.

Due to high input impedance of the battery used, a high input capacitor in order of thousands of µF is therefore placed at battery input to store charge. During the RF transmission phase that takes in order of 5-10msec, the storage capacitor provides power for transition. The input voltage VBAT is dropping from 3.6V at beginning of operation to about 2V at the receive time. Main LDO is powered by VMAX, which would be at buck boost output during this transition. The blocks that would see low voltage operation of VBAT are buck-boost and digital logic. Buck boost is designed to work down to 1.8V of typical falling input voltage (note: this is for when buck boost was enabled at higher input voltage, started up successfully and then its input voltage is falling. If buck boost starts from a disable mode, rising VIN voltage is higher).

Digital reset (nPUC) is designed for rising VBAT voltage of 1.76V and falling voltage of 1.25V. To prevent digital logic from reset, the recovery voltage comparator levels should be set higher than falling voltage (i.e., 1.9V).

If recovery voltage is lower, or the feature is disabled, PMIC can be reset. When reset happens, PMIC disables both main LDO, BB block (if BB_EN=0), and all switches. However, VMICRO function will be still provided. After digital reset and when all blocks are disabled, the input voltage will rise again, and PMIC starts again with default register values.

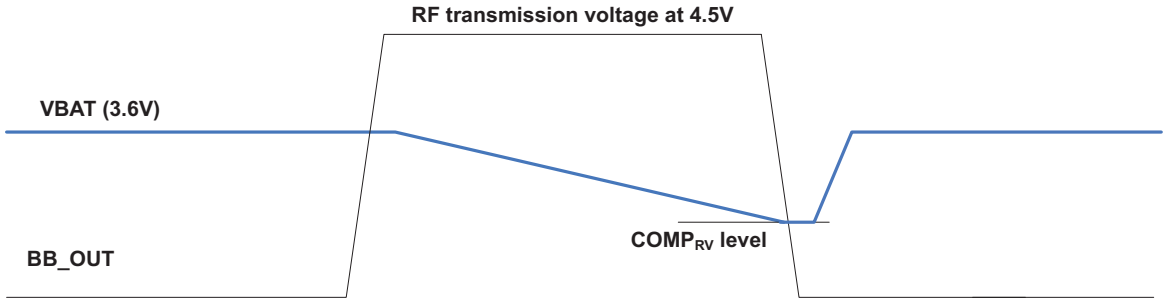
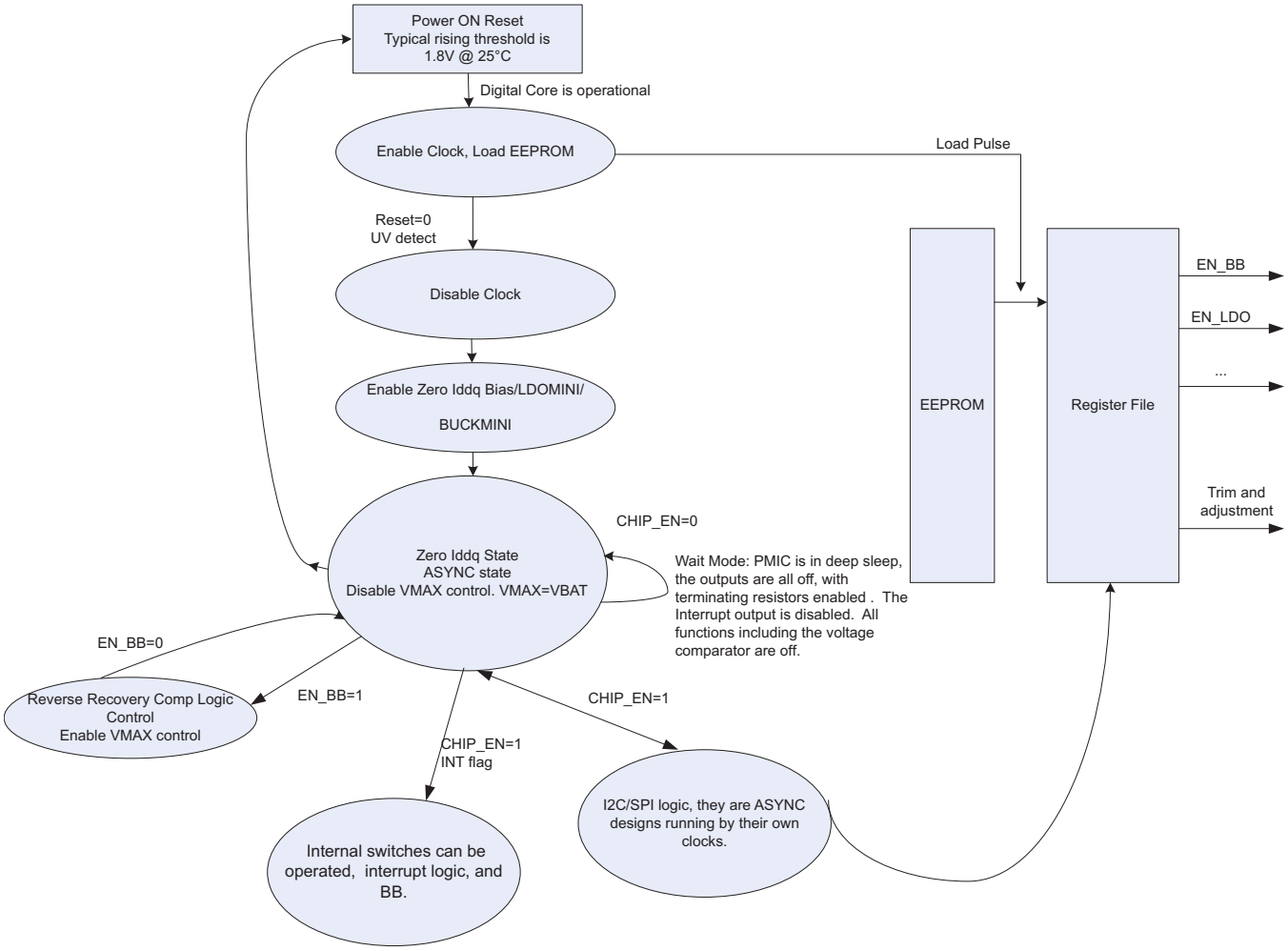


Figure 59. Operation of the IC During RF Transmission at Full Power

APPLICATION INORMATION

State Machine



Serial Interface

The following pins are allocated to the serial interface:

Table 2. Serial Interface

NO.	PIN	SPI INTERFACE	I2C INTERFACE	COMMENT
1	SCL/SCK	Clock	Clock	Can be pulled down to ground with 100kΩ Setting Bit 1, Register 5
2	MOSI/SDA	Master to slave data	Data	Can be pulled down to ground with 100kΩ Setting Bit 1, Register 5
22	INT	Interruption pin	Interruption pin	Push-pull interruption output, powered from VMICRO
23	MISO	Slave to master data	Not used. Connect to ground	1 mA output drive. Can be pulled down to ground with 100kΩ Setting Bit 1, Register 5
24	CS	Slave select (active high)	Not used. Connect to ground	Can be pulled down to ground with 100kΩ Setting Bit 1, Register 5

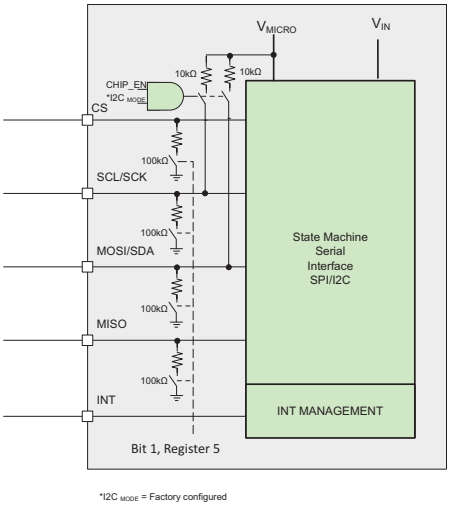


Figure 60. State Machine Serial Interface

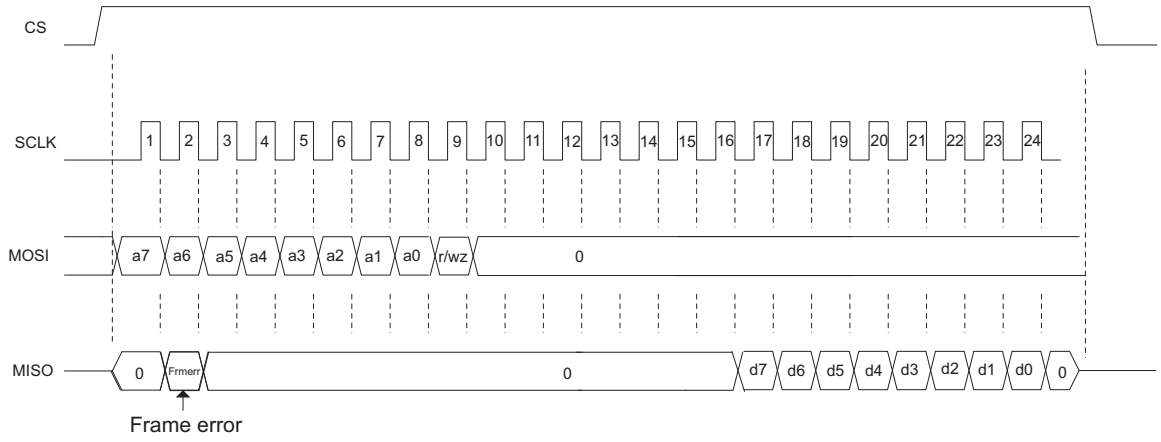
NOTE

CS level must be low when the device is powered-up . Using SPI the interface should be powered with V_{MICRO} to avoid level shifting issues.

SPI Interface Timing Diagram

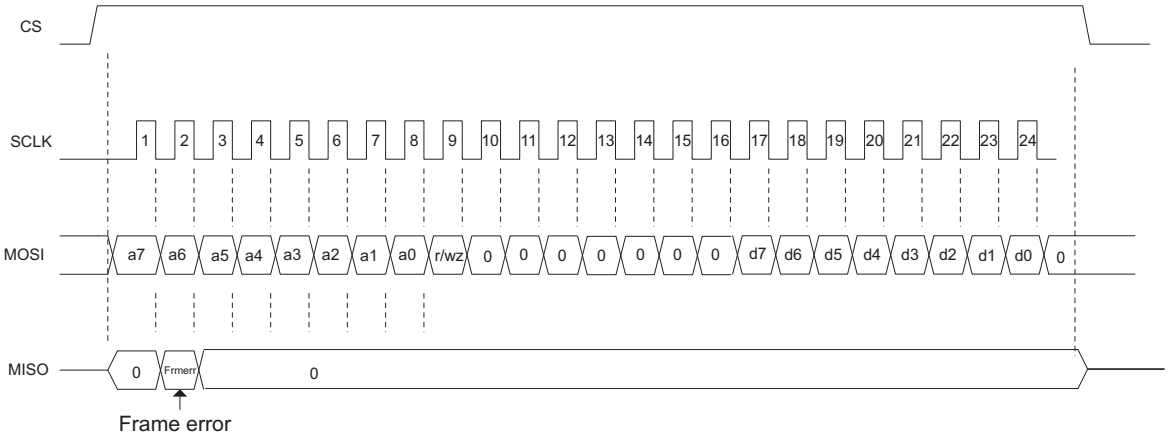
The SPI frequency range is from 32kHz to 10MHz with a minimum voltage of 2.2V. Operation at 1.8V requires a maximum clock frequency of 5MHz.

The following figures show SPI write and read transaction timing diagram. It assumes SPI master drives CS and MOSI at falling edge of SCK clock and SPI slave drives MOSI at falling edge of SCK. It requires enough CS idle time of at least four SPI clock cycles between transactions. CS idle time means the time CS is low. CS is chip select and it is active high. SPI master drives CS and MISO at falling edge of SCK and SPI slave samples MISO data at rising edge of SCK during address phase and data phase of write transaction. SPI host samples MOSI data at rising edge of SCK. Frame error is used to indicate frame error from the previous transaction. If Frmerr (frame error) is 1, it indicates the previous transaction does not contain exact 24 clock cycles. The write data will be ignored if frame error occur.



SPI read transaction timing diagram
r/wz= 1 to read data
MOSI when reading 0x02 register
0000 // 0010 // 1 000 // 0000 // 0000 // 0000

Figure 61. SPI Read Transaction



SPI write transaction timing diagram
r/wz=0 to write data
MOSI when writing 0xA5 date to 0x02 register to iridium
0000 // 0010 // 0 000 // 0000 // 1010 // 0101

Figure 62. SPI Write Transaction

Table 3. SPI Interface Timing (Minimum Supply Voltage is 2.2V)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$t_{c(CLK)}$	Cycle time CLK	1 (see timing diagram)	100			ns
$t_{w(CLKH)}$	Pulse duration, CLK high	2 (see timing diagram)	40			ns
$t_{w(CLKL)}$	Pulse duration, CLK low	3 (see timing diagram)	40			ns
$t_{su(MISO-CLKH)}$	Delay time, MISO valid before CLK high, CLOAD= 20 pF	4 (see timing diagram)			20	ns
$t_{su(MOSI - CLKH)}$	Setup time, MOSI valid before CLK high	5 (see timing diagram)	25			ns
$T_{h(CLKH - MOSI)}$	Hold time, MOSI valid after CLK high	6 (see timing diagram)	25			ns
$t_{su(CS - CLKH)}$	CS setup rising time to CLK high	7 (see timing diagram)	50			ns
$T_{h(CS - CLKH)}$	CS Hold time falling after CLK high	7 (see timing diagram)	50			ns

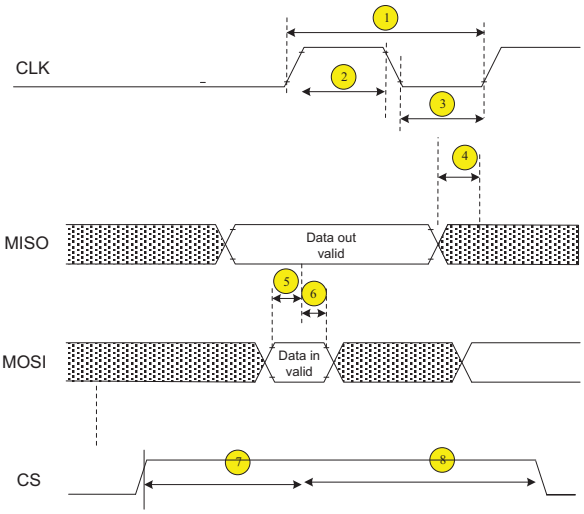


Figure 63. Timing Diagram

I2C Interface

The serial interface is compatible with the standard and fast mode I2C specifications, allowing transfers at up to 400kHz. The device has a 7bit address: '01010110'. Attempting to read data from register addresses not listed in this section will result in 00h being read out. For normal data transfer, SDA is allowed to change only when SCK is low. Changes when SCK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Eh data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the device generates an knowledge bit after the reception of eh byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the knowledge bit. The device must pull down the SDA line during the knowledge clock pulse so that the SDA line is a stable low during the high period of the knowledge clock pulse. The SDA line is a stable low during the high period of the knowledge–related clock pulse. Setup and hold times must be taken into count. During read operations, a master must signal the end of data to the slave by not generating an knowledge bit on the last byte that was clocked out of the slave. In this case, the slave device must leave the data line high to enable the master to generate the stop condition.

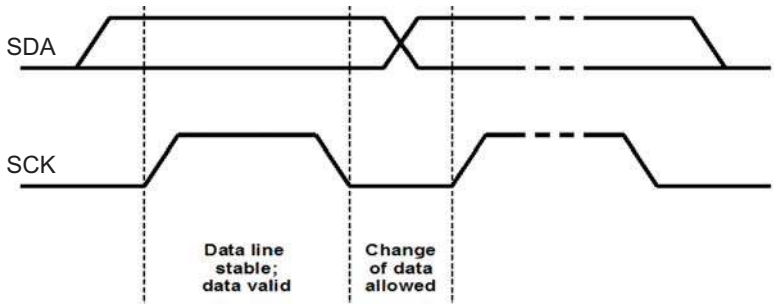


Figure 64. Bit Transfer on the Serial Interface

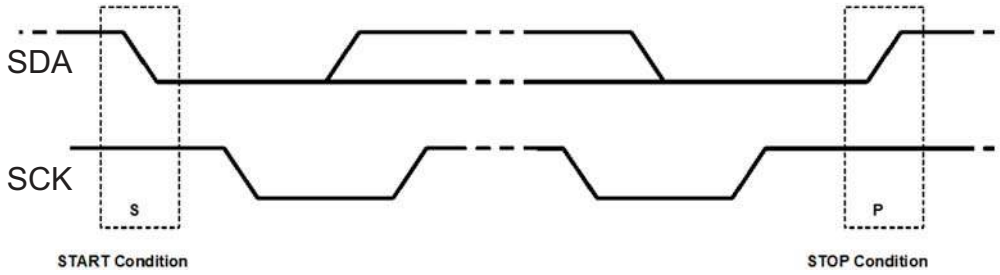


Figure 65. START and STOP Conditions

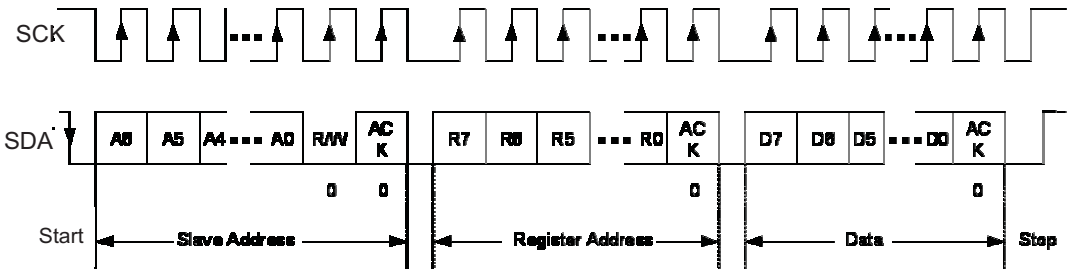


Figure 66. Serial i/f WRITE to Device

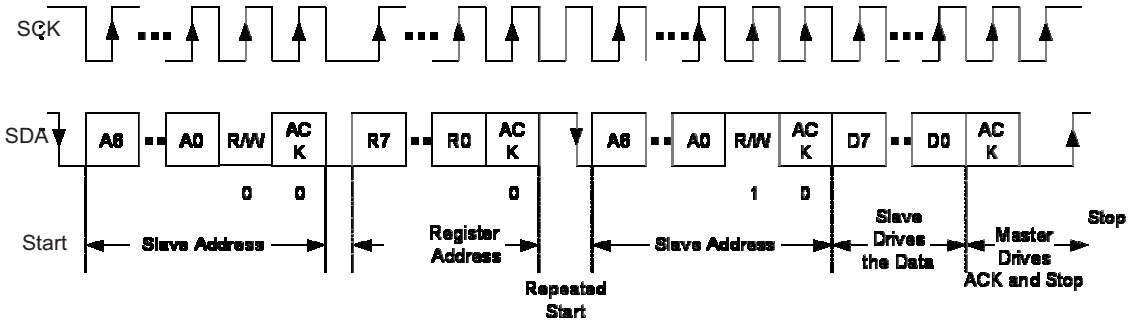


Figure 67. Serial i/f READ Protocol A

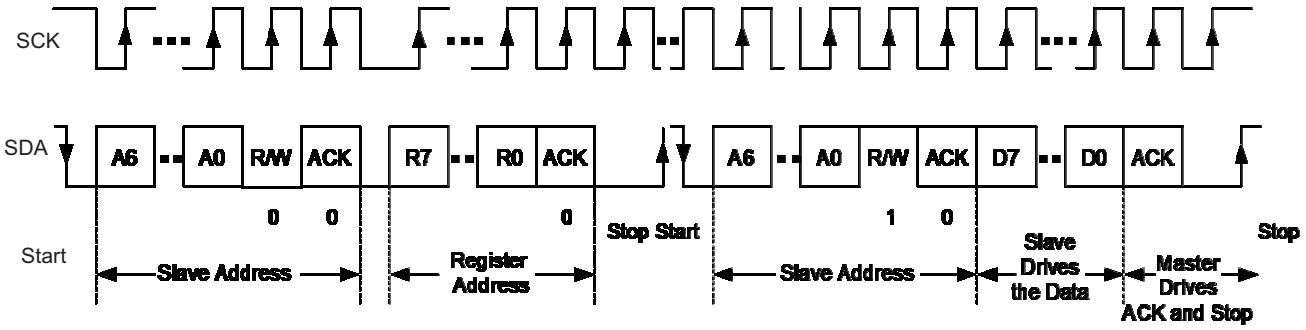


Figure 68. Serial i/f READ Protocol B

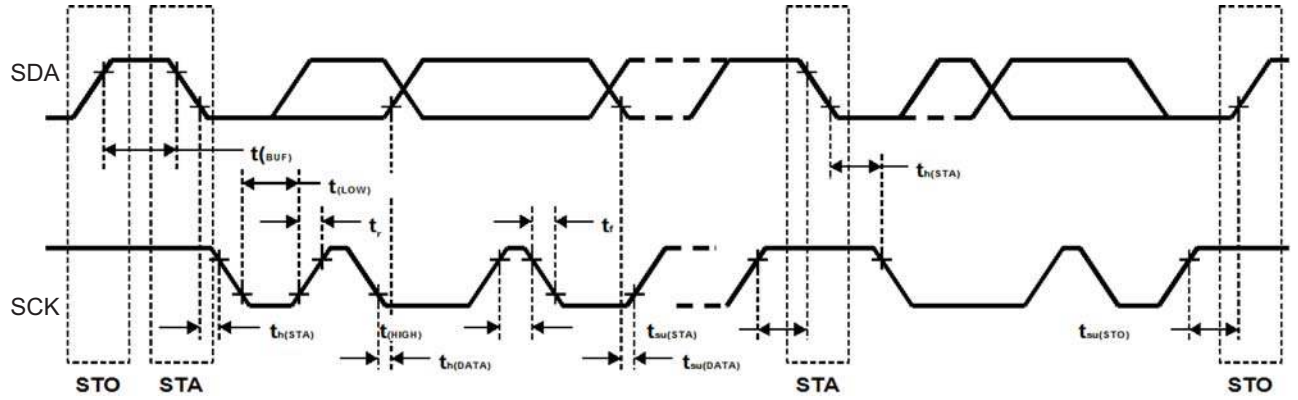


Figure 69. Serial i/f Timing Diagram

		MIN	MAX	UNIT
f_{MAX}	Clock frequency		400	kHz
$t_{wH(HIGH)}$	Clock high time	600		ns
$t_{wL(LOW)}$	Clock low time	1300		ns
t_R	SDA and CLK rise time		300	ns
t_F	SDA and CLK fall time		300	ns
$t_{h(STA)}$	Hold time (repeated) START condition (after this period the first clock pulse is generated)	600		ns
$t_{h(SDA)}$	Setup time for repeated START condition	600		ns
$t_{h(SDA)}$	Data input hold time	0		ns
$t_{su(SDA)}$	Data input setup time	100		ns
$t_{su(STO)}$	STOP condition setup time	600		ns
$t_{(BUF)}$	Bus free time	1300		ns

Register Tables

NOTE

To access registers: Write 1 to bit 7, register 1

To lock registers write 0 to bit 7, register 1

Register 0, Block Enable, Address 00H

This register enables the buck boost converter, the main LDO and most of the power switches. All options can be pre-set with EEPROM bits. The enable logic for all switches and power blocks is:

0 Disabled

1 Enabled

Note that the buck boost block can be enabled either by a register OR the BB_EN pin (15) high.

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
EN_PWR_VIN_VIN	7	PWR_ON	R/W	Y	0	Enables switch from VIN to 1WIRE power
EN_PWR_MICRO_LDO	6	PWR_ON	R/W	Y	0	Enables switch from LDO output to VMICRO
EN_PWR_LDO2_LDO	5	PWR_ON	R/W	Y	0	Enables switch from LDO to AUX2
EN_PWR_LDO1_LDO	4	PWR_ON	R/W	Y	0	Enables switch from LDO output to RF
EN_PWR_VMAX_VMAX	3	PWR_ON	R/W	Y	0	Enables switch from VMAX output to AUX1
EN_PWR_BB2_BB	2	PWR_ON	R/W	Y	0	Enables switch from BB output to Power Amplifier
EN_LDO	1	PWR_ON	R/W	Y	0	Enables LDO
EN_BB	0	PWR_ON	R/W	Y	0	Enables Buck Boost

Register 1, Rev ID and write protect , Address 01H

Bit 7 must be set to 1 before any other register can be read o write. If set to 0 all registers are locked Bits 0 to 3 are for TI internal usage to track IC revisions.

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
WRITE_EN	7	GLOBAL	R/W	N	N.A.	If 1, allows access to TI internal registers
Revision[3]	3	GLOBAL	R	N	0	Revision ID
Revision[2]	2	GLOBAL	R	N	1	Revision ID
Revision[1]	1	GLOBAL	R	N	1	Revision ID
Revision[0]	0	GLOBAL	R	N	0	Revision ID

Register 2, VMICRO_VOUT, Address 02H

Depending on the factory setting, this register sets the voltage drop from battery to V_{MICRO} for the zero leak bias or the V_{MICRO} set voltage (LDO_{MINI}, $BUCK_{MINI}$ options).

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION		
BMINI[1]	7	$BUCK_{MINI}$	R/W	N	0	BMINI[1]	BMINI[0]	Low power mode
						1	0	
BMINI[0]	6	$BUCK_{MINI}$	R/W	N	0	1	1	High power mode
RESERVED	5	RESERVED	R/W	N	0			
RESERVED	4	RESERVED	R/W	N	0			
VMICRO_VOUT[3]	3	VMICRO	R/W	Y	0	Zero Leak Bias, LDO_{MINI} (only one is set to work as per factory setting)		
VMICRO_VOUT[2]	2	VMICRO	R/W	Y	1			
VMICRO_VOUT[1]	1	VMICRO	R/W	Y	0			
VMICRO_VOUT[0]	0	VMICRO	R/W	Y	0			

SETTING	VMICRO[3]	VMICRO[2]	VMICRO[1]	VMICRO[0]	LDO_{MINI} (V)	$BUCK_{MINI}$ (V)	ZERO LEAK BIAS (V)
0	0	0	0	0	1.806	1.806	VBAT-0.6
1	0	0	0	1	1.903	1.903	VBAT-0.8
2	0	0	1	0	1.998	1.998	VBAT-1
3	0	0	1	1	2.101	2.101	VBAT-1.2
4	0	1	0	0	2.194	2.194	VBAT-1.4
5	0	1	0	1	2.295	2.295	VBAT-1.6
6	0	1	1	0	2.407	2.407	VBAT-1.8
7	0	1	1	1	2.496	2.496	VBAT-2
8	1	0	0	0	2.592	2.592	VBAT
9	1	0	0	1	2.696	2.696	VBAT
10	1	0	1	0	2.806	2.806	VBAT
11	1	0	1	1	2.885	2.885	VBAT
12	1	1	0	0	2.969	2.969	VBAT
13	1	1	0	1	3.058	3.058	VBAT
14	1	1	1	0	3.152	3.152	N/A
15	1	1	1	1	3.254	3.254	Disconnect

Register 3, BUCK-BOOST_VOUT, Address 03H

The buck boost voltage is set with this register (bits 0 to 4) which can be set by EEPROM.

UVLO operation on the buck boost can be enabled/disabled by setting bit 5.

Forced PWM operation can be set with bit 6.

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
VMAX_LATCH	7	VMAX	R/W	Y	0	When 0 VMAX switches off instantaneously when disabled. When 1 VMAX Switches off when VBB goes below VBAT
BB_FORCE_PWM	6	BUCK_BOOST	R/W	Y	0	If 0, automatic PWM/PFM. If 1, is forced PWM.
UVLO disable	5	BUCK_BOOST	R/W	Y	1	If 1, UVLO comparator does NOT shut down BB. INT is still generated.
VBB_VOUT[4]	4	BUCK_BOOST	R/W	Y	1	
VBB_VOUT[3]	3	BUCK_BOOST	R/W	Y	0	
VBB_VOUT[2]	2	BUCK_BOOST	R/W	Y	0	
VBB_VOUT[1]	1	BUCK_BOOST	R/W	Y	1	
VBB_VOUT[0]	0	BUCK_BOOST	R/W	Y	1	

SETTING	VBUCK_BOOST[4]	VBUCK_BOOST[3]	VBUCK_BOOST[2]	VBUCK_BOOST[4]	VBUCK_BOOST[1]	VBB
0	0	0	0	0	0	0.995
1	0	0	0	0	1	1.194
2	0	0	0	1	0	1.394
3	0	0	0	1	1	1.594
4	0	0	1	0	0	1.784
5	0	0	1	0	1	1.985
6	0	0	1	1	0	2.189
7	0	0	1	1	1	2.381
8	0	1	0	0	0	2.587
9	0	1	0	0	1	2.779
10	0	1	0	1	0	2.972
11	0	1	0	1	1	3.161
12	0	1	1	0	0	3.374
13	0	1	1	0	1	3.452
14	0	1	1	1	0	3.576
15	0	1	1	1	1	3.664
16	1	0	0	0	0	3.756
17	1	0	0	0	1	3.853
18	1	0	0	1	0	3.954
19	1	0	0	1	1	4.062
20	1	0	1	0	0	4.176
21	1	0	1	0	1	4.235
22	1	0	1	1	0	4.359
23	1	0	1	1	1	4.424
24	1	1	0	0	0	4.559
25	1	1	0	0	1	4.779
26	1	1	0	1	0	4.857
27	1	1	0	1	1	4.938
28	1	1	1	0	0	5.022

Register 4, LDO_VOUT, BANDGAP Address 04H

The LDO voltage is set with this register (bits 0 to 4) which can be set by EEPROM.

To speed up system start-up the internal bandgap can be enabled before the LDO and switches are enabled.

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
	7					
	6					
BGLP_EN	5	Bandgap	R/W	N		When 1, Enables internal bandgap.
LDO_VOUT[4]	4	LDO	R/W	Y	1	
LDO_VOUT[3]	3	LDO	R/W	Y	0	
LDO_VOUT[2]	2	LDO	R/W	Y	0	
LDO_VOUT[1]	1	LDO	R/W	Y	1	
LDO_VOUT[0]	0	LDO	R/W	Y	0	

SETTING	VLDO[4]	VLDO[3]	VLDO[2]	VLDO[1]	VLDO[0]	VLDO
0	0	0	0	0	0	1.001
1	0	0	0	0	1	1.103
2	0	0	0	1	0	1.202
3	0	0	0	1	1	1.303
4	0	0	1	0	0	1.399
5	0	0	1	0	1	1.506
6	0	0	1	1	0	1.606
7	0	0	1	1	1	1.712
8	0	1	0	0	0	1.81
9	0	1	0	0	1	1.921
10	0	1	0	1	0	2.019
11	0	1	0	1	1	2.127
12	0	1	1	0	0	2.23
13	0	1	1	0	1	2.33
14	0	1	1	1	0	2.438
15	0	1	1	1	1	2.534
16	1	0	0	0	0	2.637
17	1	0	0	0	1	2.725
18	1	0	0	1	0	2.845
19	1	0	0	1	1	2.948
20	1	0	1	0	0	3.031
21	1	0	1	0	1	3.148
22	1	0	1	1	0	3.243
23	1	0	1	1	1	3.343
24	1	1	0	0	0	3.449
25	1	1	0	0	1	3.563
26	1	1	0	1	0	3.643
27	1	1	0	1	1	3.769
28	1	1	1	0	0	3.858
29	1	1	1	0	1	3.952
30	1	1	1	1	0	4.05
31	1	1	1	1	1	0.803

Register 5, Pull-down resistors, Address 05H

The power switches can be pulled-down when disabled using bits 1 to 7.

The enable logic for all pull-downs is:

0 Disable

1 Enable

Bit 0 is used to increase the turn-on speed of the switches.

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
EN_PWR_VIN_VIN Pull-down	7	PWR_ON	R/W	Y	1	Enable pull-down resistor from VIN to PWR_VIN
EN_PWR_BB1_BB Pull-down	6	PWR_ON	R/W	Y	1	Enable pull-down resistor from Buck Boost (BB). BB output to switch
EN_PWR_LDO2_LDO Pull-down	5	PWR_ON	R/W	Y	0	Enable pull-down resistor from LDO to switch
EN_PWR_LDO1_LDO Pull-down	4	PWR_ON	R/W	Y	0	Enable pull-down resistor from LDO output to switch
EN_PWR_VMAX_VMAX Pull-down	3	PWR_ON	R/W	Y	0	Enable pull-down resistor from BB output to switch
EN_PWR_BB2_BB Pull-down	2	PWR_ON	R/W	Y	0	Enable pull-down resistor from BB output to switch
SPI pull-down resistor	1	PWR_ON	R/W	Y	1	Enable pull-down resistor for serial interface pins
FAST	0	PWR_ON	R/W	Y	0	If 1 makes switch turn on 10x faster.

Register 6, VMAX control and Recovery comparator, Address 06H

Bits 5 to 3 are used to set the threshold for falling voltage on the recovery comparator.

Bits 2 to 0 are used to set the threshold for rising voltage on the recovery comparator.

Bits 7 and 6 are used to set the VMAX operation (see V_{MAX} options section).

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
VMAX_DIS	7	VMAX	R/W	N	0	See V_{MAX} OPTIONS
VMAX_EN	6	VMAX	R/W	N	0	
VRECOVERY[2]_FALLING	5	VINPUT	R/W	Y	0	INT pin will be asserted when VIN reaches the falling threshold voltage. And will be cleared when VIN recovers to the rising threshold voltage. See table below
VRECOVERY[1]_FALLIING	4	VINPUT	R/W	Y	1	
VRECOVERY[0]_FALLIING	3	VINPUT	R/W	Y	1	
VRECOVERY[2]_RISING	2	VINPUT	R/W	Y	0	See Table below
VRECOVERY[1]_RISING	1	VINPUT	R/W	Y	0	
VRECOVERY[0]_RISING	0	VINPUT	R/W	Y	0	

SETTING	VRECOVERY_FALLING[2]	VRECOVERY_FALLING[1]	VRECOVERY_FALLING[0]	VRECOVERY COMPARATOR
0	0	0	0	1.7
1	0	0	1	1.8
2	0	1	0	1.9
3	0	1	1	2
4	1	0	0	2.1
5	1	0	1	2.2
6	0	1	1	2.3
7	1	1	1	2.4
SETTING	**VRECOVERY_FALLING[2]**	**VRECOVERY_FALLING[1]**	**VRECOVERY_FALLING[0]**	**VRECOVERY COMPARATOR**
0	0	0	0	2.4
1	0	0	1	2.5
2	0	1	0	2.6
3	0	1	1	2.7
4	1	0	0	2.8
5	1	0	1	2.9
6	0	1	1	3
7	1	1	1	3.1

Register 7, PWR_BB_LDO switch control AND interruption management, Address 07H

The alarm status of the device can be verified with this register.

Bit 7 and 3 report on the UVLO comparator status. Bit 5 masks this alarm.

Bit 6 and 2 report on the over temperature status. Bit 4 masks this alarm.

Bits 1 and 0 are used to control the switches associated with the internal connection between the LDO and the buck boost converter..

The enable logic for the switches is:

0 Disabled

1 Enabled

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
UVLO_INT	7	INT	R	N	0	Set to 1 when recovery comparator is asserted (falling edge), cleared to 0 when register is read by serial interface.
OTS_INT	6	INT	R	N	0	Set to 1 when over temperature is asserted, cleared to 0 when register is read by serial interface.
UVLO_MASK	5	INT	R/W	N	0	Masks the recovery comparator assertion (falling edge). Reported to the INT PIN
OTS_MASK	4	INT	R/W	N	1	Masks the over temperature assertion. Reported to the INT PIN
UVLO_STATUS	3	INT	RD only	N	0	Status report of recovery comparator fault
OTS_STATUS	2	INT	RD only	N	0	Status report of an overt temperature fault
EN_PWR_SEL_BB	1	PWR_ON	R/W	Y	0	Enable switch to SEL from Buck Boost (BB) BB output OR LDO
EN_PWR_BB_LDO	0	PWR_ON	R/W	Y	0	Enables the back to back switch from Ldo output to BB output

Register 8, interruption block disable, Address 08H

Bit 7 to 1 can be used to automatically disable the power switches when an interruption is asserted.

Bit 0 disables the recovery comparator to reduce power consumption.

NAME	BIT	CATEGORY	R/W	EEPROM BIT	DEFAULT	DESCRIPTION
EN_Vin_SHUTDN	7	Pull down	R/W	Y	1	If 1, switch turns off at interruption.
EN_BB2_SHUTDN	6	Pull down	R/W	Y	0	If 1, switch turns off at interruption.
EN_LDO2_SHUTDN	5	Pull down	R/W	Y	1	If 1, switch turns off at interruption.
EN_LDO1_SHUTDN	4	Pull down	R/W	Y	1	If 1, switch turns off at interruption.
EN_AUX1_SHUTDN	3	Pull down	R/W	Y	1	If 1, switch turns off at interruption.
EN_BB1_SHUTDN	2	Pull down	R/W	Y	0	If 1, switch turns off at interruption.
EN_LDOBBbb_SHUTDN	1	Pull down	R/W	Y	1	If 1, PWR_BB_LDO switch turns off at INT
COMPrv_ENmask	0	Pull down	R/W	Y	1	If 1, COMPrv is disabled

Recommended Board Layout

This section provides the recommendation of the TPS65290 board layout based on TI evaluation board. Close placement to the chip and to the ground plane is required for power components including C21, C2, C6, C15, C15a, L1, C10 and C4. The priority among the components is C21 → C2 → C8 → C6 → C15 → C15A → L1 → C10 → C4. In particular, a good ground plane for the TPS65290 and the LDO output capacitor (C6) is highly recommended to prevent LDO overshoot during the buck-boost converter operation. A good ground connection for C21 and C2 is also required for the high performance of the buck-boost converter. The pin is regarded as a noise generator because of the buck-boost converter switching operation. Therefore, do not tap the trace to pin2 from the trace from C21. Use star connection for two inputs of pin 19 and pin 4 from the power supply.

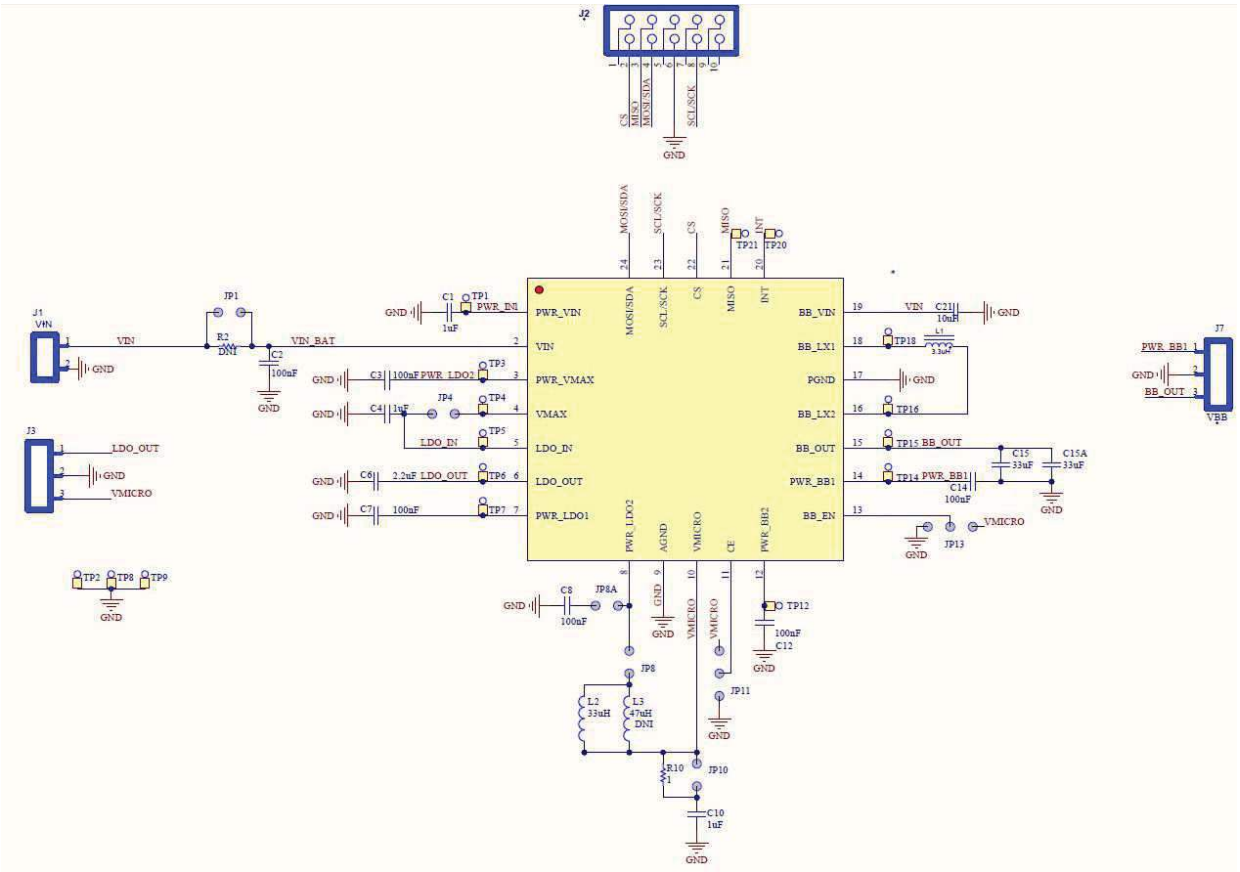


Figure 70. Schematic

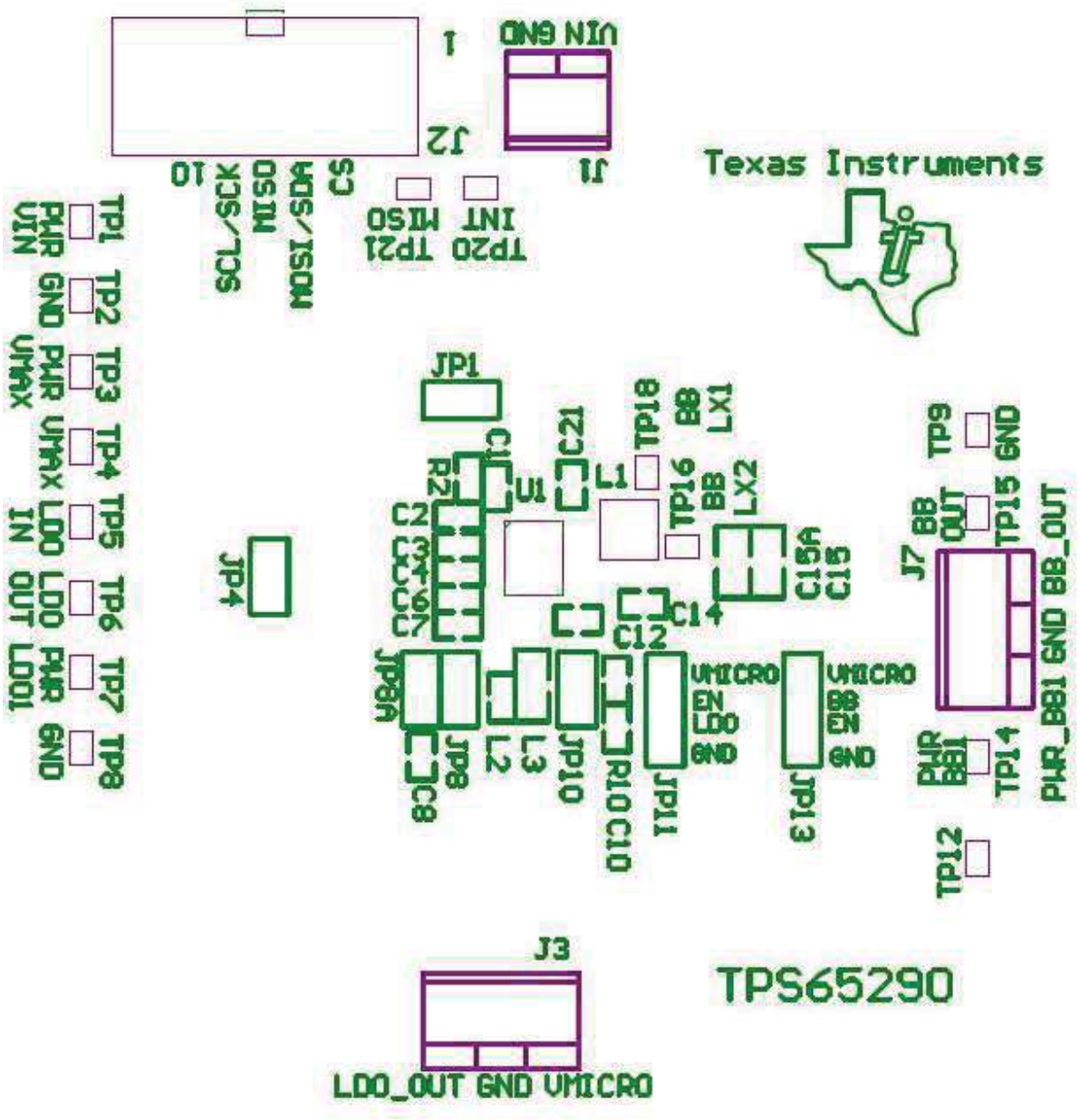


Figure 71. Component Placement

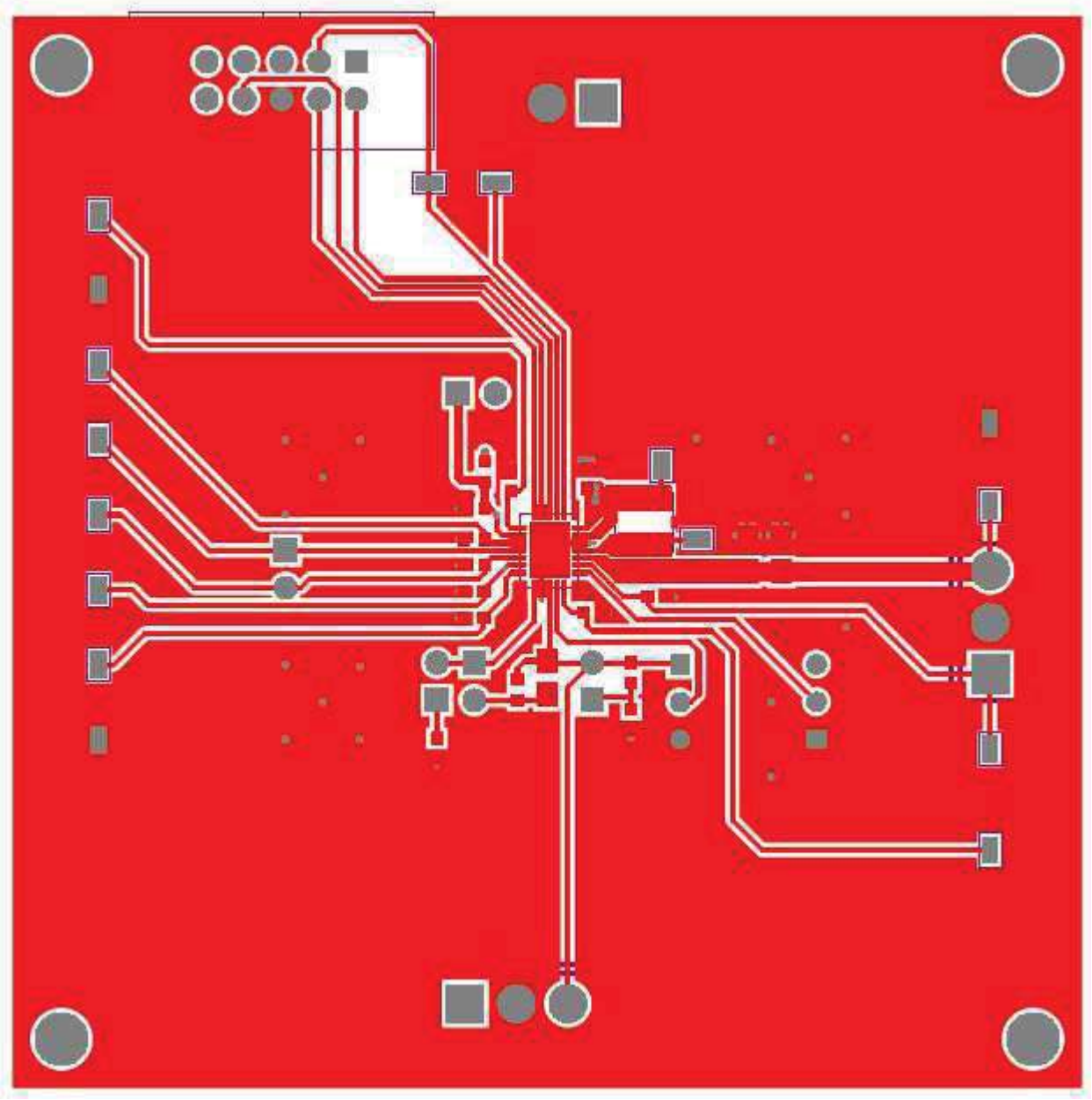


Figure 72. Top Layer

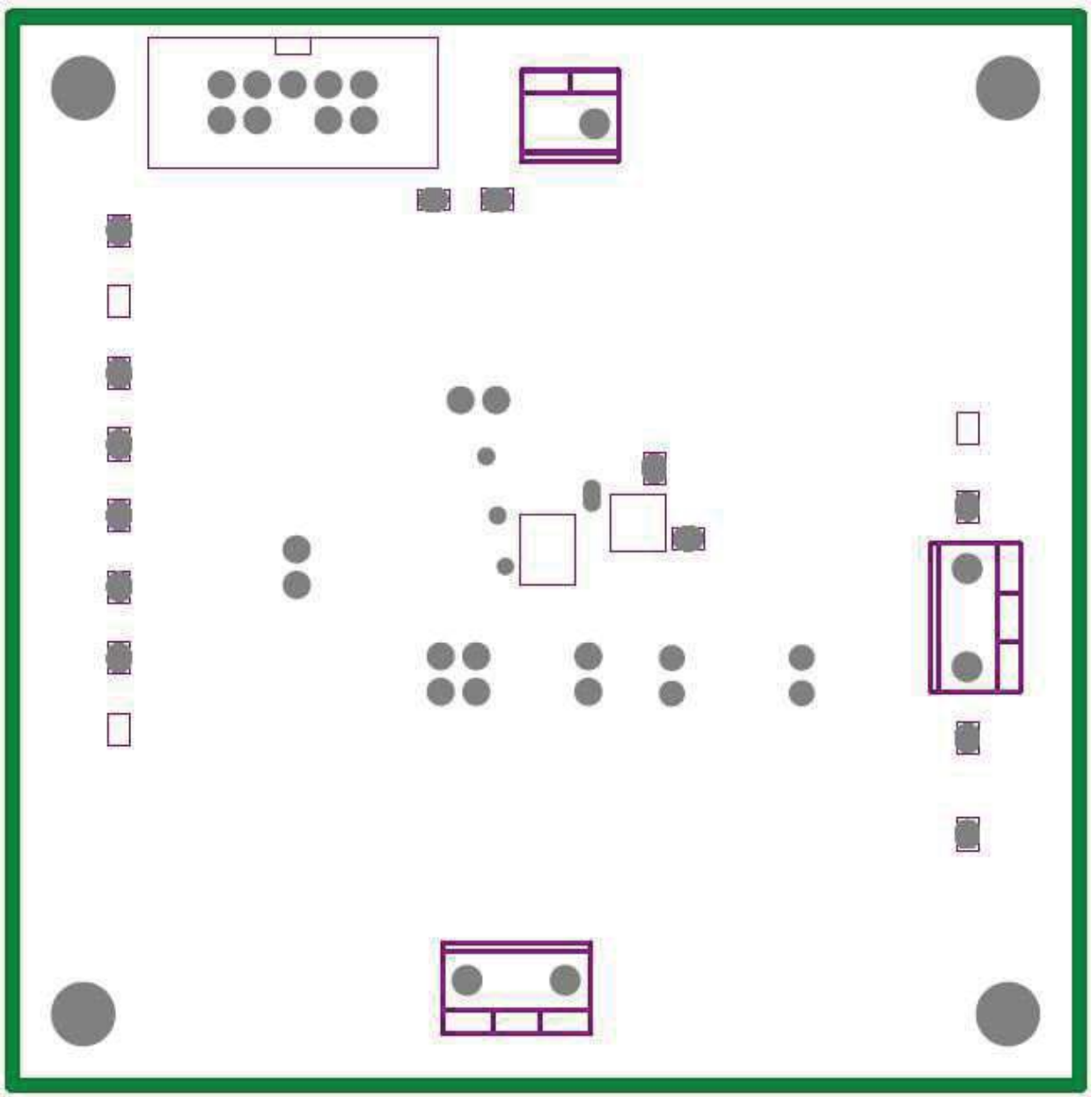


Figure 73. Second Layer (Full Copper Ground Plane)

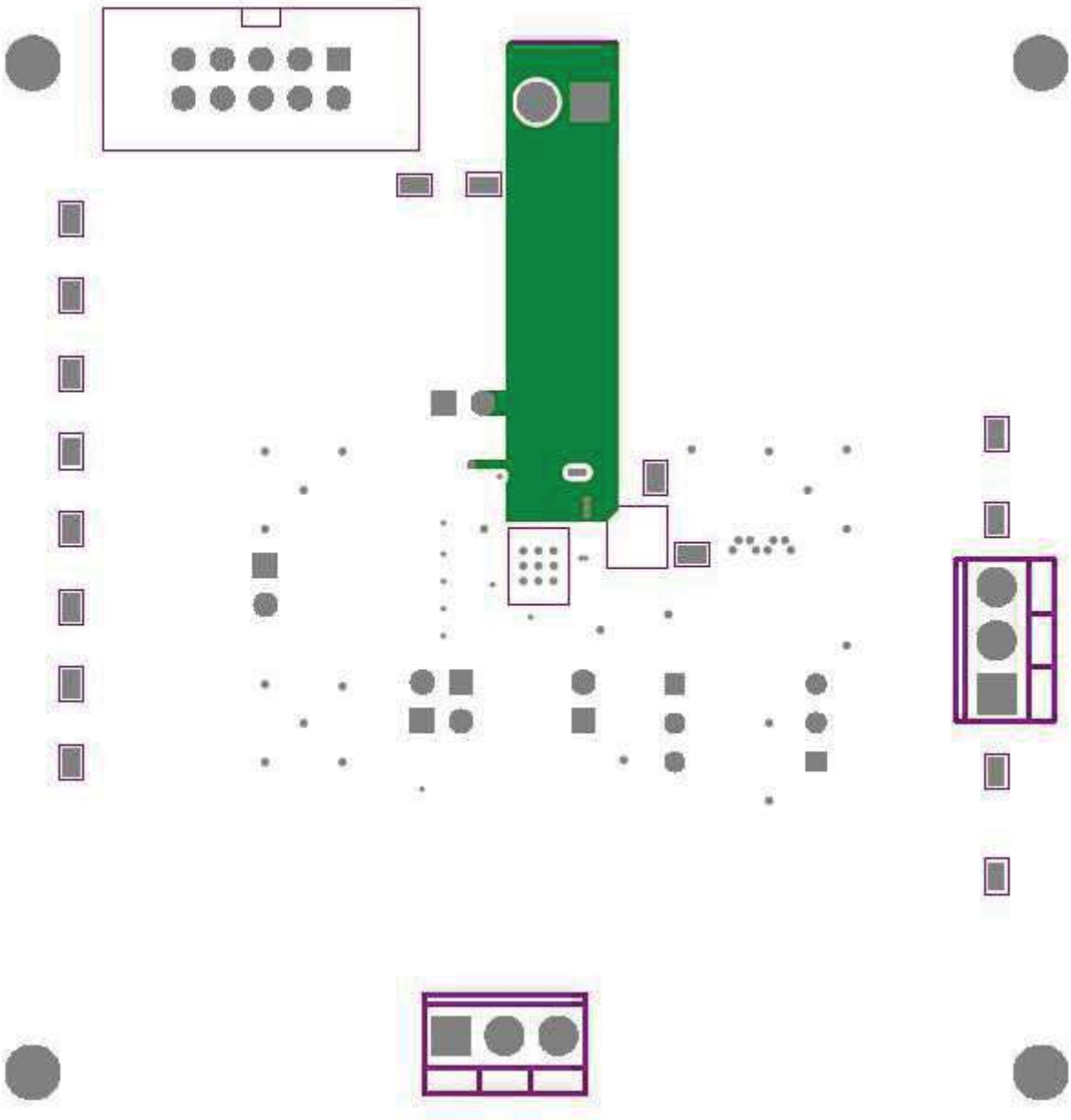


Figure 74. Third Layer

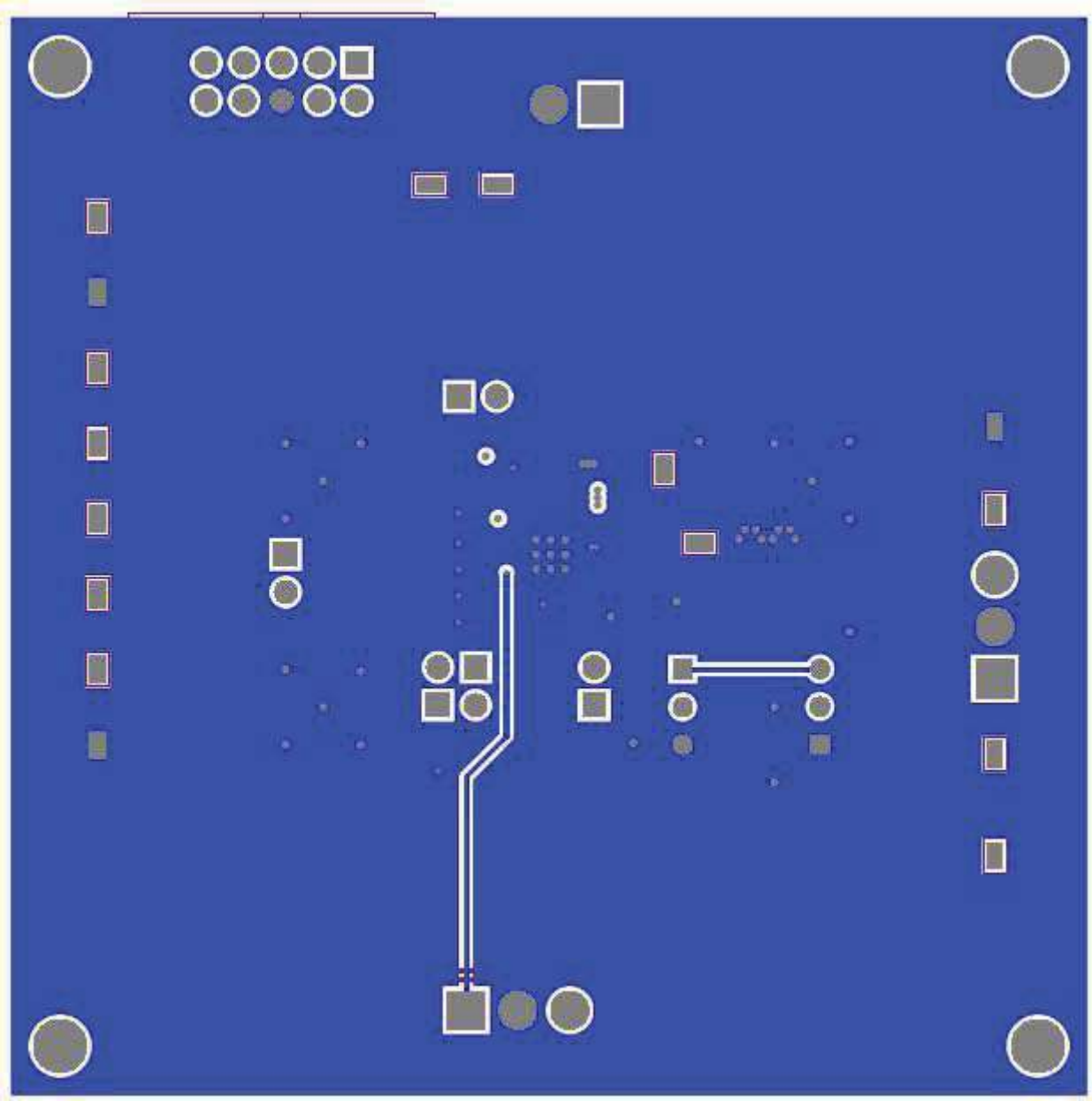


Figure 75. Bottom Layer

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS65290BMRHFR	ACTIVE	VQFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65290BM	Samples
TPS65290BMRHFT	ACTIVE	VQFN	RHF	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65290BM	Samples
TPS65290LMRHFR	ACTIVE	VQFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65290LM	Samples
TPS65290LMRHFT	ACTIVE	VQFN	RHF	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65290LM	Samples
TPS65290ZBRHFR	ACTIVE	VQFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65290ZB	Samples
TPS65290ZBRHFT	ACTIVE	VQFN	RHF	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65290ZB	Samples

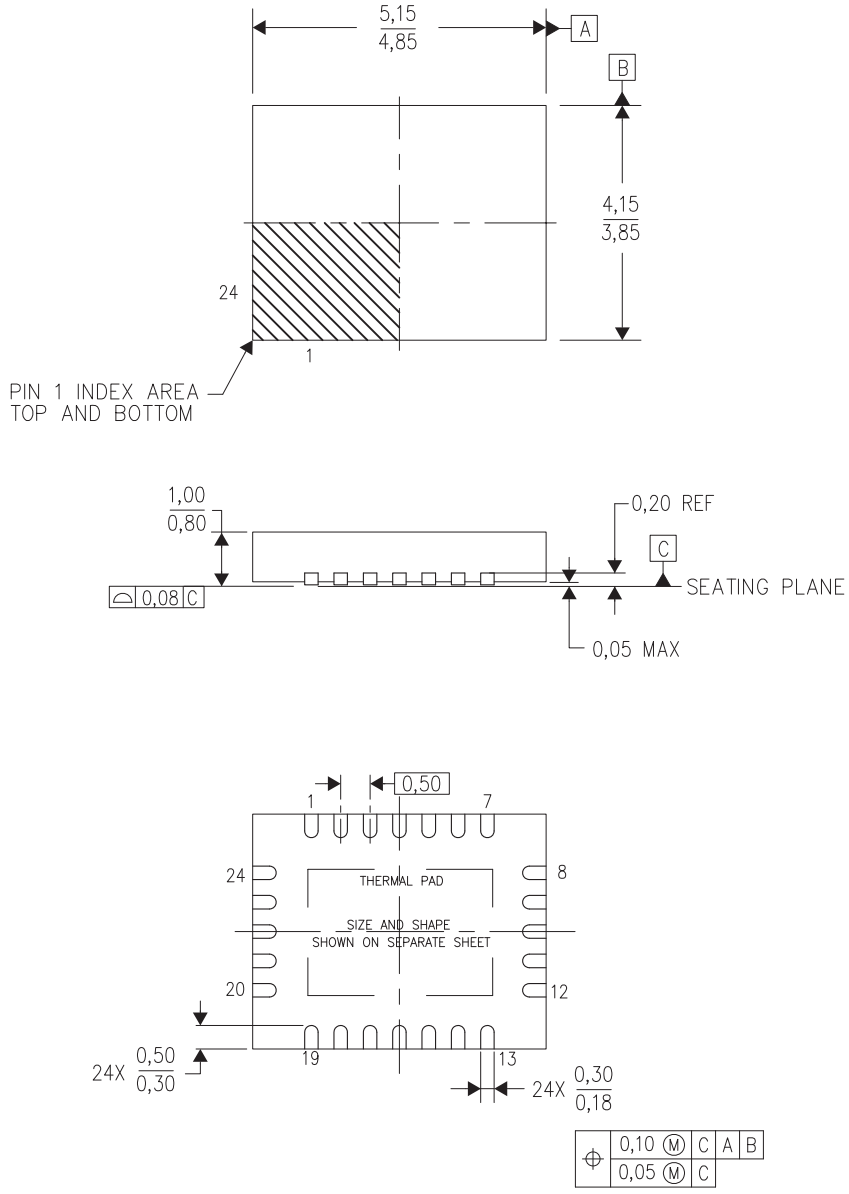
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



4204845–2/H 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

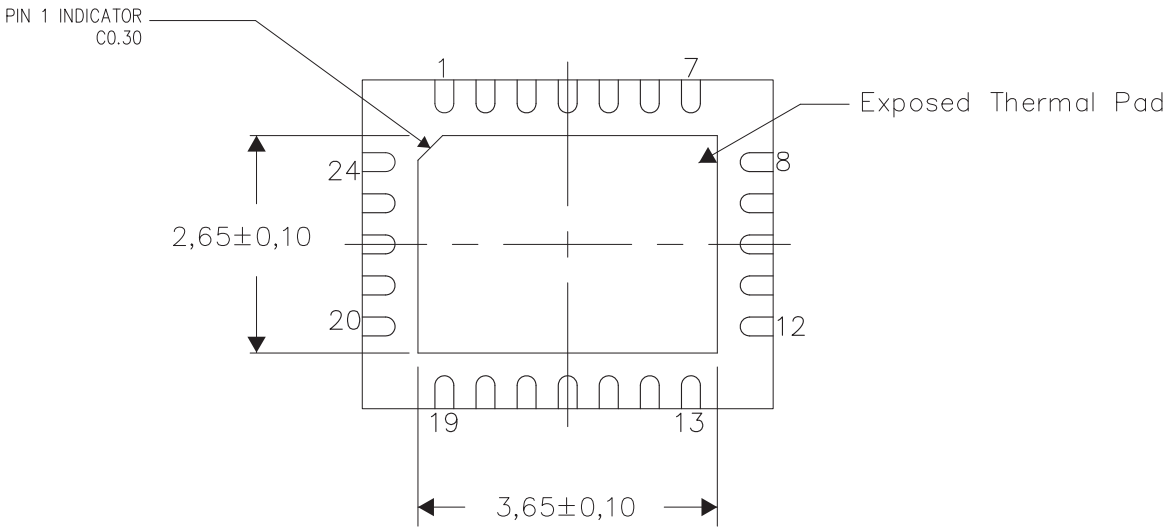
RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



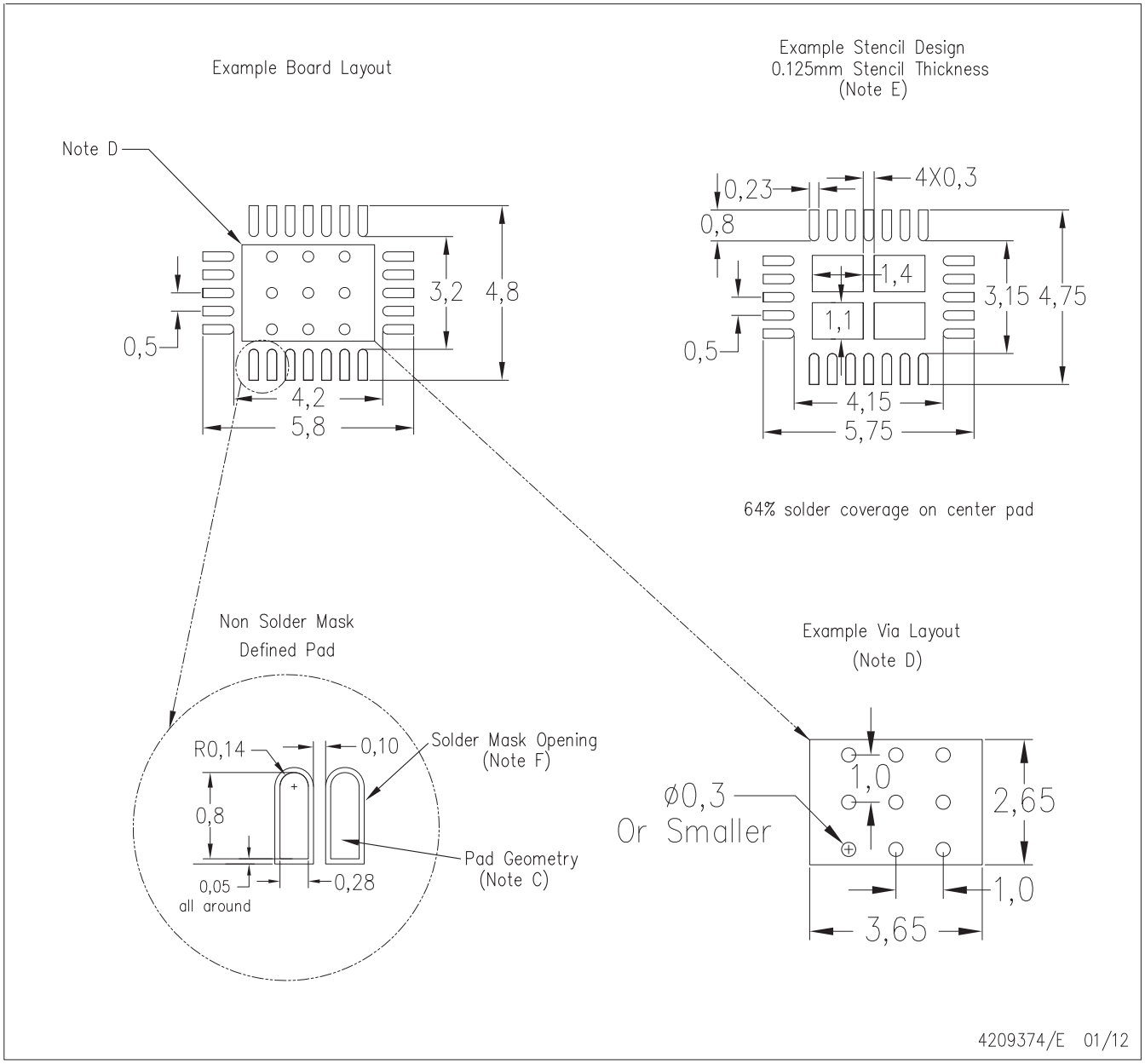
Bottom View

Exposed Thermal Pad Dimensions

4206360–3/J 01/12

NOTE: All linear dimensions are in millimeters

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265