Not Recommended for New Designs

This product was manufactured for Maxim by an outside wafer foundry using a process that is no longer available. It is not recommended for new designs. The data sheet remains available for existing users.

A Maxim replacement or an industry second-source may be available. Please see the QuickView data sheet for this part or contact technical support for assistance.

For further information, contact Maxim's Applications Tech Support.

19-0418; Rev 1; 8/95

MAXIM

Low Offset Voltage Operational Amplifier

OP07

General Description

The OP07 is a precision operational amplifier with very low input offset voltage (10μV typ., 25μV max. for the OP07A), input offset drift of 0.2μV/°C and low input bias current of 0.7nA. The wide input common mode range of ±14V combined with high CMRR of 110dB minimum (OP07A), plus high input impedance and high open-loop gain make these devices particularly useful for high-gain instrumentation applications.

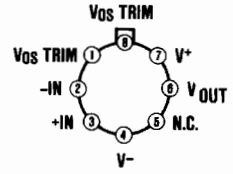
The excellent linearity and gain accuracy are maintained at high open-loop gains, over both time and temperature. The OP07 has become an industry standard and Maxim's reliability and quality are added advantages.

Applications

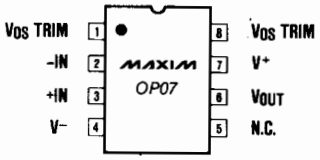
Precision Amplifiers
Thermocouple Amplifiers
Low Level Signal Processing
Medical Instrumentation
Strain Gauge Amplifiers
High Accuracy Data Acquisition

Pin Configuration

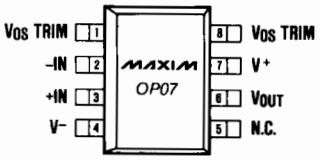
Top View



8 Lead TO-99



8 Lead Dip



8 Lead Small Outline

Features

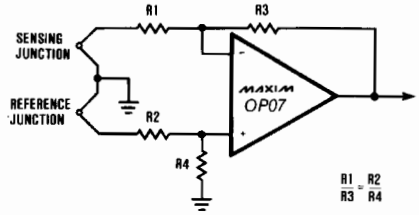
- ◆ **Ultra Low Offset Voltage: 10μV**
- ◆ **Ultra Low Offset Voltage Drift: 0.2μV/°C**
- ◆ **Ultra Stable vs. Time: 0.2μV/Month**
- ◆ **Ultra Low Noise: 0.35μV_{p-p}**
- ◆ **Wide Supply Voltage: ±3V to ±18V**
- ◆ **High Common Mode Input: ±14V**
- ◆ **No External Components Required**
- ◆ **Fits AD510, 725, 108A/308A, 741 Sockets**

Ordering Information

PART	TEMP. RANGE	PACKAGE
OP07AJ	-55°C to +125°C	TO-99
OP07J	-55°C to +125°C	TO-99
OP07EJ	0°C to +70°C	TO-99
OP07CJ	0°C to +70°C	TO-99
OP07DJ	0°C to +70°C	TO-99
OP07EP	0°C to +70°C	8 Lead Plastic Dip
OP07CP	0°C to +70°C	8 Lead Plastic Dip
OP07DP	0°C to +70°C	8 Lead Plastic Dip
OP07AZ	-55°C to +125°C	8 Lead Hermetic Dip
OP07Z	-55°C to +125°C	8 Lead Hermetic Dip
OP07EZ	0°C to +70°C	8 Lead Hermetic Dip
OP07CZ	0°C to +70°C	8 Lead Hermetic Dip
OP07ECSA	0°C to +70°C	8 Lead Small Outline
OP07CCSA	0°C to +70°C	8 Lead Small Outline
OP07DCSA	0°C to +70°C	8 Lead Small Outline
OP07D/D	0°C to +70°C	Dice

** Contact factory for dice specifications.*

Typical Operating Circuit



High-Stability
Thermocouple Amplifier

Low Offset Voltage Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) ..... ±22V
Internal Power Dissipation 500mW
TO-99(J) — derate at 7.1mW/°C above +80°C
Hermetic Dip(Z) — derate at 6.7mW/°C above +75°C
Plastic Dip(P) — derate at 5.6mW/°C above +36°C
Small Outline — derate at 5mW/°C above +55°C
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
OP07AJ, OP07AZ, OP07J and OP07Z ..... -55°C to +125°C
All Other Parts ..... 0°C to +70°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Duration of Output Short Circuit ..... Indefinite
Junction Temperature (T_J) ..... -65°C to +160°C

Note 1: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07A			OP07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 2)		10	25		30	75	µV
Long Term Input Offset Voltage Stability	V_{OS}/Time	(Note 3)		0.2	1.0		0.2	1.0	µV/ Month
Input Offset Current	I_{OS}			0.3	2.0		0.4	2.8	nA
Input Bias Current	I_B			±0.7	±2.0		±1.0	±3.0	nA
Input Noise Voltage	$e_{N\,P-P}$	0.1Hz to 10Hz (Note 4)		0.35	0.6		0.35	0.6	μV_{P-P}
Input Noise Voltage Density	e_N	f_O = 10Hz (Note 4) f_O = 100Hz (Note 4) f_O = 1000Hz (Note 4)		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
Input Noise Current	$I_{N\,P-P}$	0.1Hz to 10Hz (Note 4)		14	30		14	30	pA_{P-P}
Input Noise Current Density	I_N	f_O = 10Hz (Note 4) f_O = 100Hz (Note 4) f_O = 1000Hz (Note 4)		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
Input Resistance Differential-Mode	R_{IN}	(Note 5)	30	80		20	60		MΩ
Input Resistance Common-Mode	R_{INCM}			200			200		GΩ
Input Voltage Range	IVR		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	110	126		110	126		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V		4	10		4	10	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±0.5V V_S = ±3V (Note 5)	300 150	500 400		200 150	500 400		V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V

Note 2: OP07A grade V_{OS} is measured one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
Note 3: Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV. Parameter is sample tested.
Note 4: Sample tested.
Note 5: Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued)

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07A			OP07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 6)	0.1	0.3		0.1	0.3		V/μS
Closed-Loop Bandwidth	BW	A_{VCL} = +1V (Note 6)	0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_O	V_O = 0V, I_O = 0		60			60		Ω
Power Consumption	P_D	V_S = ±15V, No Load V_S = ±3V, No Load		75 4	120 6		75 4	120 6	mW
Offset Adjustment Range		R_P = 20kΩ		±4			±4		mV

Note 6: Sample tested.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07A			OP07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 7)		25	60		60	200	μV
Average Temperature Coefficient of Input Offset Voltage	TCV_{OS}	(Note 8)		0.2	0.6		0.3	1.3	μV/°C
Input Offset Current	I_{OS}			0.8	4.0		1.2	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 8)		5	25		8	50	pA/°C
Input Bias Current	I_B			±1.0	±4.0		±2.0	±6.0	nA
Average Input Bias Current Drift	TCI_B	(Note 8)		8	25		13	50	pA/°C
Input Voltage Range	IVR		±13	±13.5		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123		106	123		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V		5	20		5	20	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	200	400		150	400		V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±12.6		±12.0	±12.6		V

Note 7: OP07A grade Offset Voltage is measured one minute after application of power. For all other grades V_{OS} is measured 0.5 seconds after power on.

Note 8: Sample tested.

Low Offset Voltage Operational Amplifier

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07E			OP07C			OP07D			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	V_{OS}	(Note 1)		30	75		60	150		60	150	µV
Long Term Input Offset Voltage Stability	V_{OS}/Time	(Note 2)		0.3	1.5		0.4	2.0		0.5	3.0	µV/ Month
Input Offset Current	I_{OS}			0.5	3.8		0.8	6.0		0.8	6.0	nA
Input Bias Current	I_B			±1.2	±4.0		±1.8	±7.0		±2.0	±12.0	nA
Input Noise Voltage	$e_{N\ P-P}$	0.1Hz to 10Hz (Note 3)		0.35	0.6		0.38	0.65		0.38	0.65	μV_{P-P}
Input Noise Voltage Density	e_N	f_O = 10Hz (Note 3) f_O = 100Hz (Note 3) f_O = 1000Hz (Note 3)		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5		10.5 10.3 9.8	20.0 13.5 11.5	nV/√Hz
Input Noise Current	$I_{N\ P-P}$	0.1Hz to 10Hz (Note 3)		14	30		15	35		15	35	pA_{P-P}
Input Noise Current Density	I_N	f_O = 10Hz (Note 3) f_O = 100Hz (Note 3) f_O = 1000Hz (Note 3)		0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18		0.35 0.15 0.13	0.90 0.27 0.18	pA/√Hz
Input Resistance Differential-Mode	R_{IN}	(Note 4)	15	50		8	33		7	31		MΩ
Input Resistance Common-Mode	R_{INCM}			160			120			120		GΩ
Input Voltage Range	IVR		±13	±14		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	106	123		100	120		94	110		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V		5	20		7	32		7	32	µV/V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V R_L ≥ 500Ω, V_O = ±0.5V V_S = ±3V (Note 5)	200 150	500 400		120 100	400 400		120	400 400		V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ R_L ≥ 2kΩ R_L ≥ 1kΩ	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		±12.0 ±11.5	±13.0 ±12.8 ±12.0		±12.0 ±11.5	±13.0 ±12.8 ±12.0		V
Slew Rate	SR	R_L ≥ 2kΩ (Note 3)	0.1	0.3		0.1	0.3		0.1	0.3		V/µS
Closed-Loop Bandwidth	BW	A_{VCL} = +1V (Note 3)	0.4	0.6		0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_O	V_O = 0V, I_O = 0		60			60			60		Ω
Power Consumption	Pd	V_S = ±15V, No Load V_S = ±3V, No Load		75 4	120 6		80 4	150 8		80 4	150 8	mW
Offset Adjustment Range		R_P = 20kΩ		±4			±4			±4		mV

Note 1: Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Note 2. Long-Term Input Offset Stability refers to the average trend line of V_{OS} vs Time over extended periods after the first 30 days of operation.

Note 3. Sample tested.

Note 4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP07E			OP07C			OP07D			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	V_{OS}	(Note 5)		45	130		85	250		85	250	µV
Average Temperature Coefficient of Input Offset Voltage	TCV_{OS}	(Note 6)		0.3	1.3		0.4	1.8		0.7	2.5	µV/°C
Input Offset Current	I_{OS}			0.9	5.3		1.6	8.0		1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 6)		8	35		12	50		12	50	pA/°C
Input Bias Current	I_B			±1.5	±5.5		±2.2	±9.0		±3.0	±14	nA
Average Input Bias Current Drift	TCI_B	(Note 6)		13	35		18	50		18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	103	123		97	120		94	106		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V		7	32		10	51		10	51	µV/V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	180	400		100	400		100	400		V/mV
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12.0	±12.6		±11.0	±12.6		±11.0	±12.6		V

Note 5: Input Offset Voltage is measured 0.5 seconds after application of power.
Note 6: Sample tested.

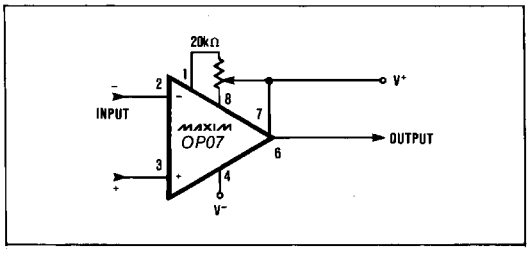


Figure 1. Optional Offset Nulling Circuit.

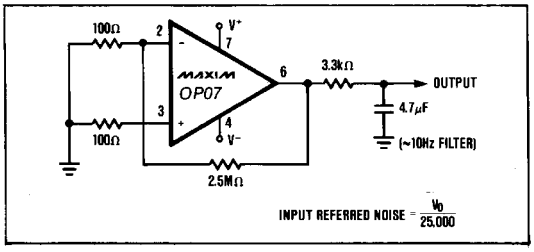
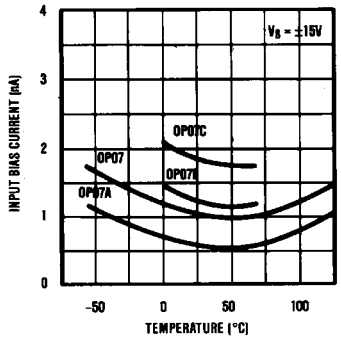
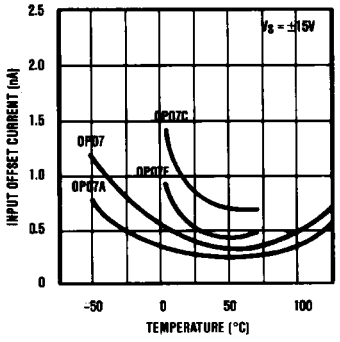


Figure 2. Low Frequency Noise Test Circuit.

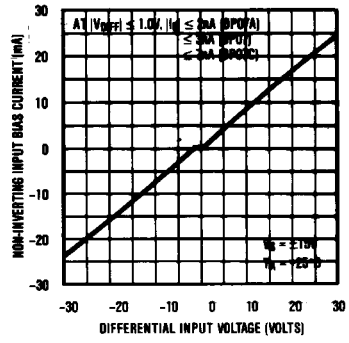
INPUT BIAS CURRENT vs. TEMPERATURE



INPUT OFFSET CURRENT vs. TEMPERATURE

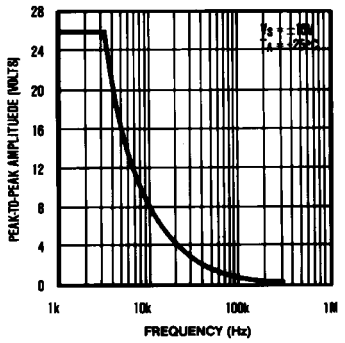


INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE

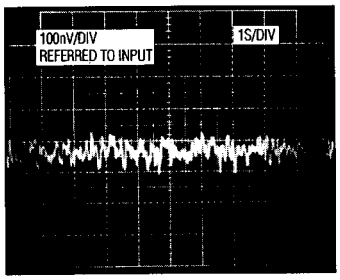


Low Offset Voltage Operational Amplifier

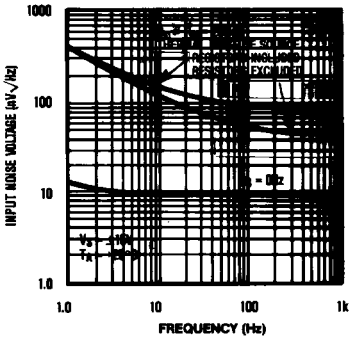
MAXIMUM OUTPUT SWING vs. FREQUENCY



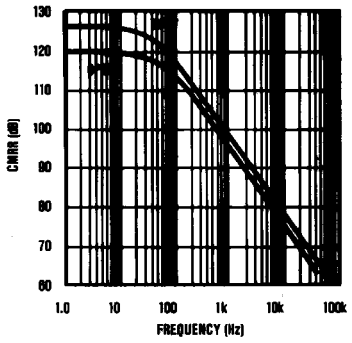
LOW FREQUENCY NOISE



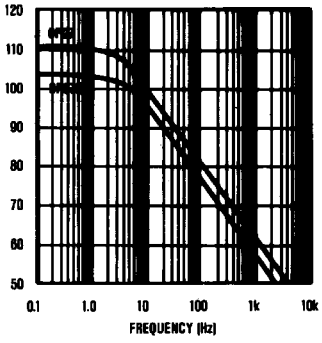
TOTAL INPUT NOISE VOLTAGE vs. FREQUENCY



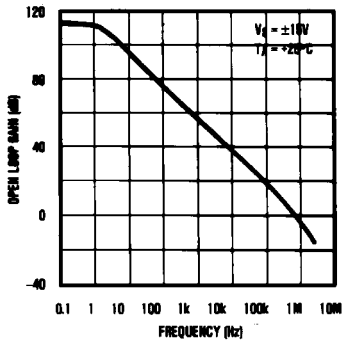
CMRR vs. FREQUENCY



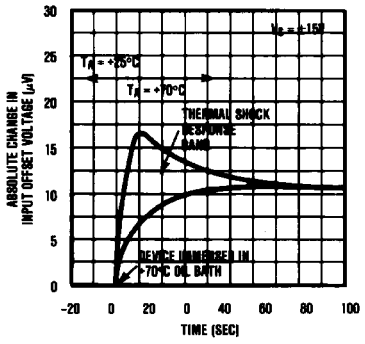
PSRR vs. FREQUENCY



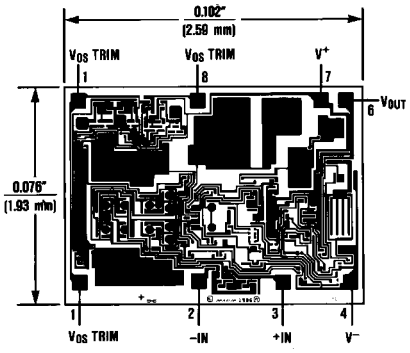
OPEN LOOP FREQUENCY RESPONSE



OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK

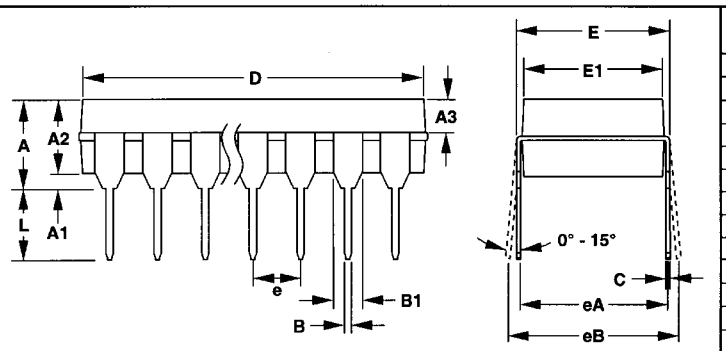


Chip Topography



Low Offset Voltage Operational Amplifier

Package Information

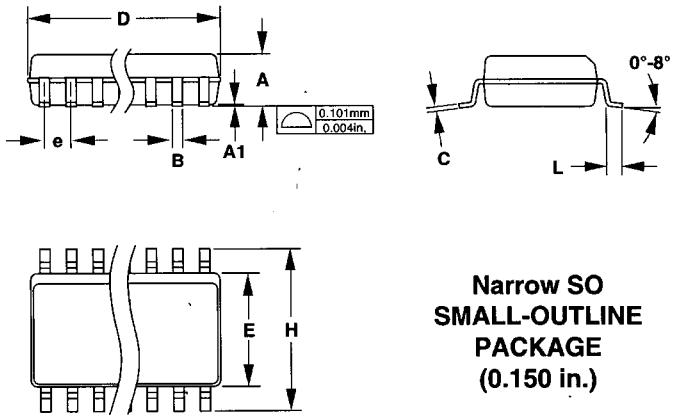


Plastic DIP PLASTIC DUAL-IN-LINE PACKAGE (0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A



Narrow SO SMALL-OUTLINE PACKAGE (0.150 in.)

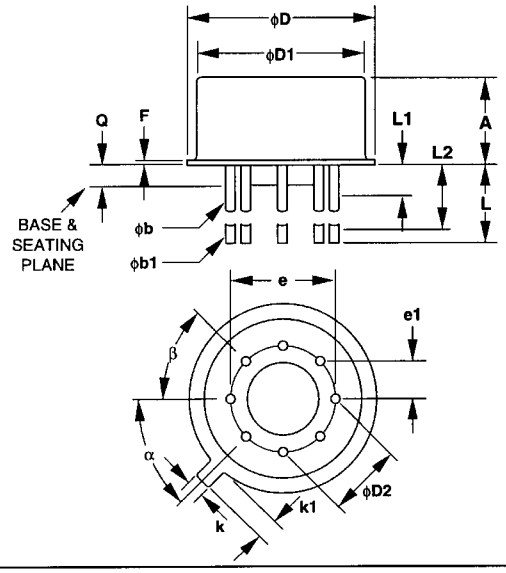
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A

Low Offset Voltage Operational Amplifier

Package Information (continued)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.185	4.19	4.70
φb	0.016	0.019	0.41	0.48
φb1	0.016	0.021	0.41	0.53
φD	0.335	0.375	8.51	9.40
φD1	0.305	0.335	7.75	8.51
φD2	0.110	0.160	2.79	4.06
e	0.200 BSC		5.08 BSC	
e1	0.100 BSC		2.54 BSC	
F	–	0.040	–	1.02
k	0.027	0.034	0.69	0.86
k1	0.027	0.045	0.69	1.14
L	0.500	0.750	12.70	19.05
L1	–	0.050	–	1.27
L2	0.250	–	6.35	–
Q	0.010	0.045	0.25	1.14
α	45° BSC		45° BSC	
β	45° BSC		45° BSC	

21-0022A

8-PIN TO-99 METAL CAN PACKAGE