Dual Full-Bridge PWM Motor Driver

Last Time Buy

This part is in production but has been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: November 1, 2010

Deadline for receipt of LAST TIME BUY orders: April 30, 2011

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

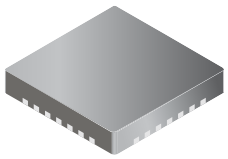
NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Dual Full-Bridge PWM Motor Driver

Features and Benefits

- ±650 mA continuous output current
- 30 V output voltage rating
- Internal fixed-frequency PWM current control
- Satlington® sink drivers
- User-selectable blanking window
- Internal ground-clamp and flyback diodes
- Internal thermal-shutdown circuitry
- Crossover-current protection and UVLO protection

Package: 28 pin QFN (suffix ET)



Approximate scale

Description

The A3969 is designed to drive both windings of a two-phase bipolar stepper motor. The device includes two H-bridges capable of continuous output currents of ±650 mA and operating voltages to 30 V. Motor winding current can be controlled by the internal fixed-frequency, pulse-width modulated (PWM), current-control circuitry. The peak load current limit is set by the user's selection of a reference voltage and current-sensing resistors.

The fixed-frequency pulse duration is set by a user-selected external RC timing network. The capacitor in the RC timing network also determines a user-selectable blanking window that prevents false triggering of the PWM current-control circuitry during switching transitions.

To reduce on-chip power dissipation, the H-bridge power outputs have been optimized for low saturation voltages. The sink drivers feature the Allegro® patented Satlington® output structure. The Satlington outputs combine the low voltage drop of a saturated transistor and the high peak current capability of a Darlington.

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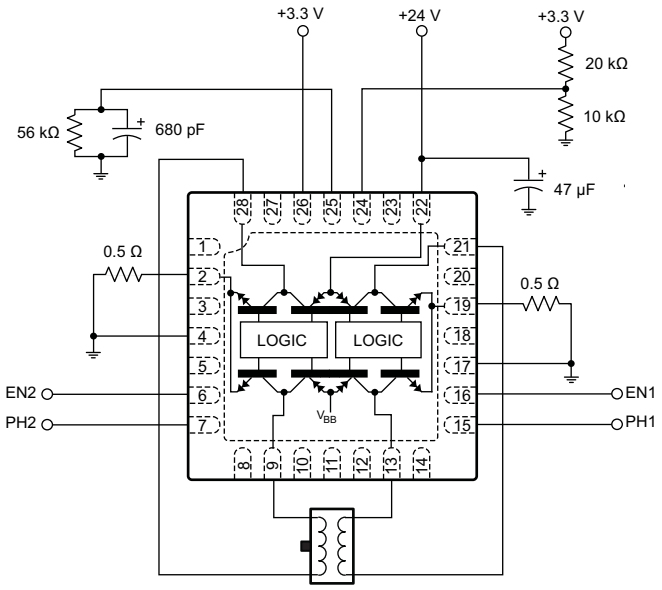
Typical Application



Description (continued)

For each bridge, a PHASE input controls load-current polarity by selecting the appropriate source and sink driver pair. For each bridge, an ENABLE input, when held high, disables the output drivers. Special power-up sequencing is not required. Internal circuit protection includes thermal shutdown with hysteresis, ground-clamp and flyback diodes, and crossover-current protection.

The A3969 is supplied in a 28-pin QFN lead (Pb) free plastic package with exposed thermal pad and 100% matte tin leadframe plating. It has a 5 x 5 mm footprint and 0.90 mm nominal height.

Selection Guide

Part Number	Packing*	Package
A3969SETTR-T	Tape, 3000 pieces/reel	5 x 5 mm QFN, 28 pin

*Contact Allegro for additional packing options

Absolute Maximum Ratings

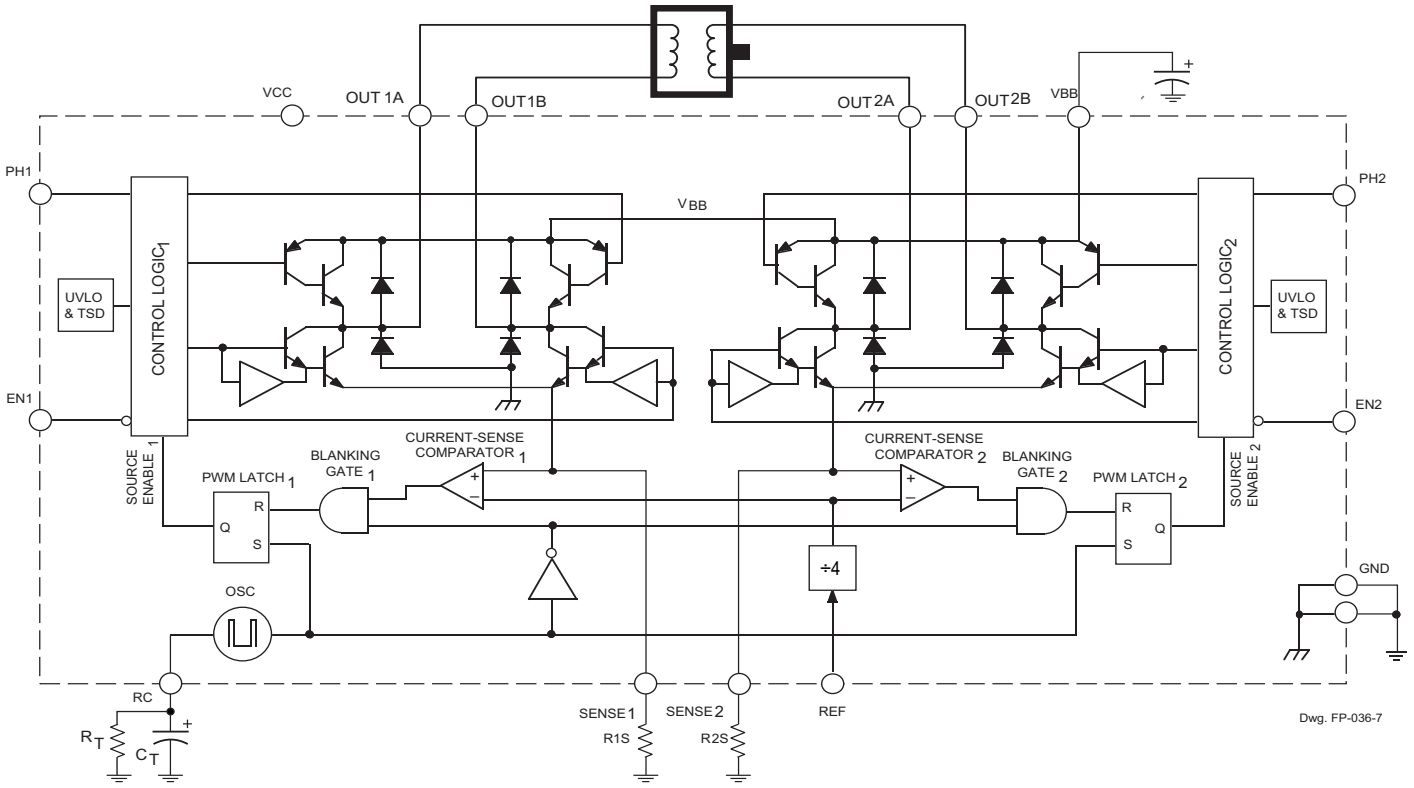
Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		30	V
Output Current	I_{OUT}	Peak	±750	mA
		Continuous. Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.	±650	mA
Logic Supply Voltage	V_{CC}		7	V
Input Voltage	V_{in}		-0.3 to V_{CC} + 0.3	V
Sense Voltage	V_S		0.45	V
Operating Ambient Temperature	T_A	Range S	–20 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Thermal Characteristics* (additional data available on Allegro Web site)

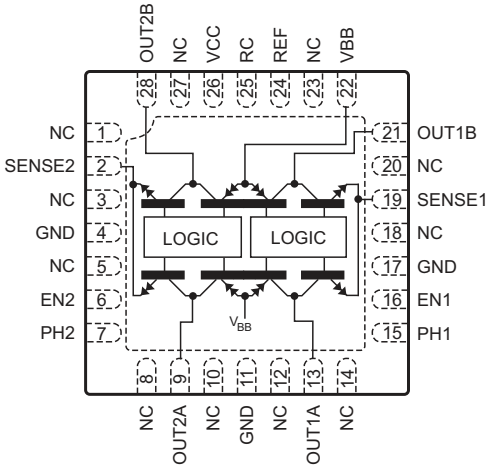
Characteristic	Symbol	Notes	Rating	Units
Package Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	4-layer PCB, based on JEDEC standard	32	°C/W
Package Thermal Resistance, Junction-to-Tab	$R_{\theta JT}$		2	°C/W
Package Power Dissipation	P_D(max)	$R_{\theta JA}$ = 32 °C/W, T_A = 25°C	3.9	W

* Per SEMI G42-88 Specification, *Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages.*

Functional Block Diagram



Pin-out Diagram



ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 30 V, V_{CC} = 3.0 V to 3.6 V, V_{REF} = 1.7 V, V_S = 0 V, 56 kΩ and 680 pF RC to Ground (unless noted otherwise)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating, I_{OUT} = ±650 mA, L = 3 mH	5	—	30	V
Output Leakage Current	I_{CEX}	V_{OUT} = 30 V	—	<1.0	50	µA
		V_{OUT} = 0 V	—	<-1.0	-50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Source Driver, I_{OUT} = -400 mA	—	1.7	2.0	V
		Source Driver, I_{OUT} = -650 mA	—	1.8	2.1	V
		Sink Driver, I_{OUT} = +400 mA, V_S = 0.425 V	—	0.3	0.5	V
		Sink Driver, I_{OUT} = +650 mA, V_S = 0.425 V	—	0.7	1.3	V
Clamp Diode Forward Voltage	V_F	I_F = 400 mA	—	1.1	1.4	V
		I_F = 650 mA	—	1.4	1.6	V
Motor Supply Current (No Load)	$I_{BB(ON)}$	$V_{ENABLE1}$ = $V_{ENABLE2}$ = 0.8 V	—	3.0	5.0	mA
	$I_{BB(OFF)}$	$V_{ENABLE1}$ = $V_{ENABLE2}$ = 2.4 V	—	<1.0	200	µA
Control Logic						
Logic Supply Voltage Range	V_{CC}	Operating	3.00	—	3.60	V
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	<-20	-200	µA
Reference Input Volt. Range	V_{REF}	Operating	0.1	–	1.7	V
Reference Input Current	I_{REF}		-2.5	0	1.0	µA
Reference Divider Ratio	V_{REF}/V_{TRIP}		3.8	4.0	4.2	—
Current-Sense Comparator Input Offset Voltage	V_{IO}	V_{REF} = 0 V	-6.0	0	6.0	mV
Current-Sense Comparator Input Voltage Range	V_S	Operating	-0.3	—	0.425	V
Sense-Current Offset	I_{SO}	$I_S - I_{OUT}$, 50 mA ≤ I_{OUT} ≤ 650 mA	12	18	24	mA

NOTES:

1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 30 V, V_{CC} = 3.0 V to 3.6 V, V_{REF} = 1.7 V, V_S = 0 V, 56 kΩ and 680 pF RC to Ground (unless noted otherwise) (cont.)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Control Logic (continued)						
PWM RC Frequency	f_{osc}	C_T = 680 pF, R_T = 56 kΩ	22.9	25.4	27.9	kHz
PWM Propagation Delay Time	t_{PWM}	Comparator Trip to Source OFF	—	1.0	1.4	µs
		Cycle Reset to Source ON	—	0.8	1.2	µs
Cross-Over Dead Time	t_{codt}	100 Ω Load to 15 V	0.2	1.3	3.0	µs
Propagation Delay Times	t_{pd}	I_{OUT} = ±650 mA, 50% to 50%; V_{BB} = 15 V:				
		ENABLE ON to Source ON	—	125	—	ns
		ENABLE OFF to Source OFF	—	500	—	ns
		ENABLE ON to Sink ON	—	200	—	ns
		ENABLE OFF to Sink OFF	—	200	—	ns
		PHASE Change to Sink ON	—	1500	—	ns
		PHASE Change to Sink OFF	—	200	—	ns
		PHASE Change to Source ON	—	1500	—	ns
		PHASE Change to Source OFF	—	200	—	ns
Thermal Shutdown Temp.	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	15	—	°C
UVLO Enable Threshold	$V_{T(UVLO)+}$	Increasing V_{CC}	—	2.75	3.0	V
UVLO Hysteresis	$V_{T(UVLO)hys}$		0.07	0.10	—	V
Logic Supply Current	$I_{CC(ON)}$	$V_{ENABLE\ 1}$ = $V_{ENABLE\ 2}$ = 0.8 V	—	—	50	mA
	$I_{CC(OFF)}$	$V_{ENABLE\ 1}$ = $V_{ENABLE\ 2}$ = 2.4 V	—	—	9.0	mA

NOTES:

1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.

FUNCTIONAL DESCRIPTION

Internal PWM Current Control. The A3969 dual H-bridge is designed to drive both windings of a bipolar stepper motor. Load current can be controlled in each motor winding by an internal fixed-frequency PWM control circuit. The current-control circuitry works as follows: when the outputs of the H-bridge are turned on, current increases in the motor winding. The load current is sensed by the current-control comparator via an external sense resistor (R_S). Load current continues to increase until it reaches the predetermined value, set by the selection of external current-sensing resistors and reference input voltage (V_{REF}) according to the equation:

$$I_{TRIP} = I_{OUT} + I_{SO} = V_{REF}/(4\ R_S)$$

where I_{SO} is the sense-current error (typically 18 mA) due to the base-drive current of the sink driver transistor.

At the trip point, the comparator resets the source-enable latch, turning off the source driver of that H-bridge. The source turn off of one H-bridge is independent of the other H-bridge. Load inductance causes the current to recirculate through the sink driver and ground-clamp diode. The current decreases until the internal clock oscillator sets the source-enable latches of both H-bridges, turning on the source drivers of both bridges. Load current increases again, and the cycle is repeated.

The frequency of the internal clock oscillator is set by the external timing components R_TC_T. The frequency can be approximately calculated as:

$$f_{osc} = 1/(R_T\ C_T + t_{blank})$$

where t_{blank} is defined below.

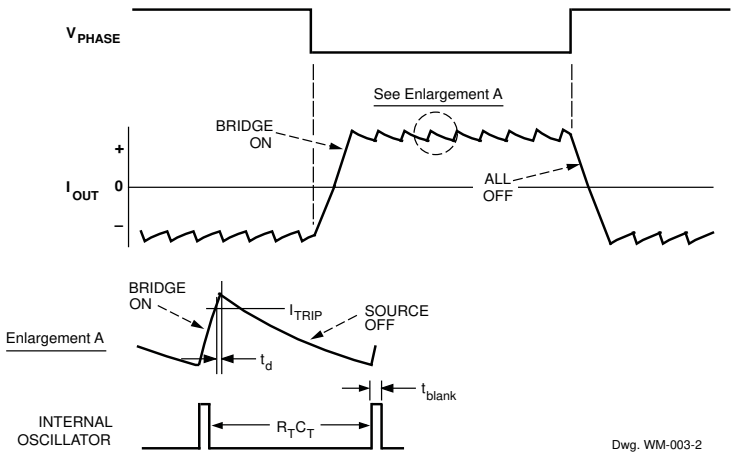
The range of recommended values for R_T and C_T are 20 kΩ to 100 kΩ and 470 pF to 1000 pF respectively. Nominal values of 56 kΩ and 680 pF result in a clock frequency of 25 kHz.

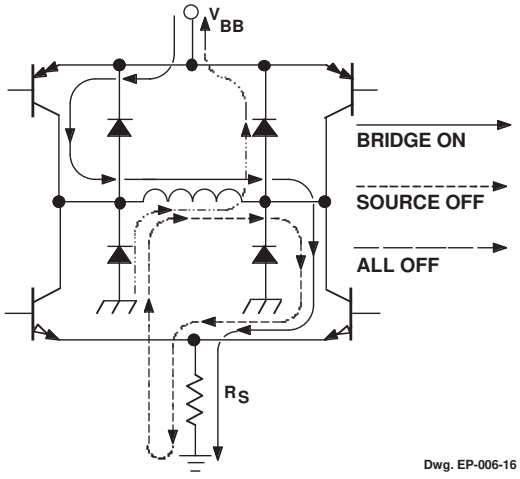
Current-Sense Comparator Blanking. When the source driver is turned on, a current spike occurs due to the reverse-recovery currents of the clamp diodes and switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source enable latch, the current-control comparator output is blanked for a short period of time when the source driver is turned on. The blanking time is set by the timing component C_T according to the equation:

$$t_{blank} = 1900\ C_T\ (\mu s).$$

A nominal C_T value of 680 pF will give a blanking time of 1.3 µs.

The current-control comparator is also blanked when the H-bridge outputs are switched by the PHASE or ENABLE inputs. This internally generated blank time is approximately 1 µs.





FUNCTIONAL DESCRIPTION (continued)

Load Current Regulation. Due to internal logic and switching delays (t_d), the actual load current peak will be slightly higher than the I_{TRIP} value. These delays, plus the blanking time, limit the minimum value the current control circuitry can regulate. To produce zero current in a winding, the ENABLE terminal should be held high, turning off all output drivers for that H-bridge.

Logic Inputs. A logic high on the PHASE input results in current flowing from OUT_A to OUT_B of that H-bridge. A logic low on the PHASE input results in current flowing from OUT_B to OUT_A. An internally generated dead time (t_{codt}) of approximately 1 µs prevents cross-over current spikes that can occur when switching the PHASE input.

A logic high on the ENABLE input turns off all four output drivers of that H-bridge. This results in a fast current decay through the internal ground clamp and flyback diodes. A logic low on the ENABLE input turns on the selected source and sink driver of that H-bridge.

The ENABLE inputs can be pulse-width modulated for applications that require a fast current-decay PWM. If external current-sensing circuitry is used, the internal current-control logic can be disabled by connecting the R_TC_T terminal to ground.

The REFERENCE input voltage is typically set with a resistor divider from V_{CC}. This reference voltage is internally divided down by 4 to set up the current-comparator trip-voltage threshold. The reference input voltage range is 0 to 1.7 V.

Output Drivers. To minimize on-chip power dissipation, the sink drivers incorporate a Satlington structure. The Satlington output combines the low $V_{CE(sat)}$ features of a saturated transistor and the high peak-current capability of a Darlington (connected) transistor. A graph showing typical output saturation voltages as a function of output current is on the next page.

Miscellaneous Information. Thermal protection circuitry turns off all output drivers should the junction temperature reach +165 °C (typical). This is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. Normal operation is resumed when the junction temperature has decreased about 15°C.

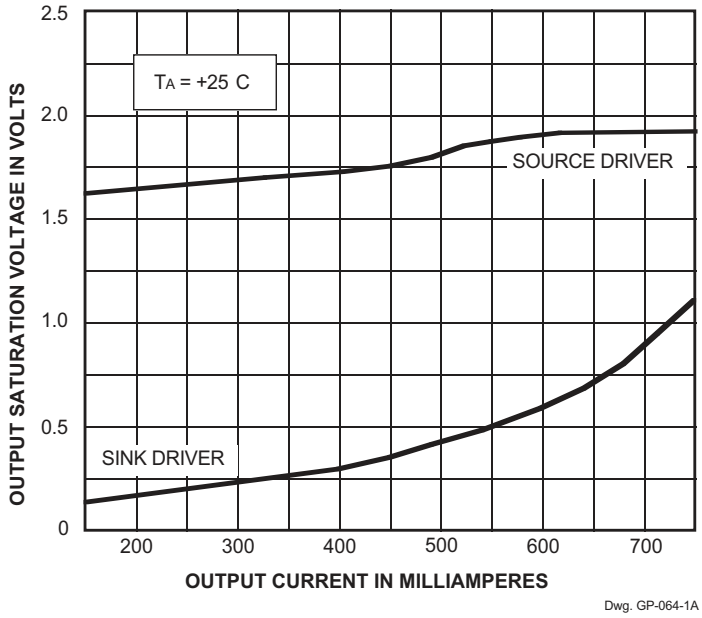
The A3969 current control employs a fixed-frequency, variable duty cycle PWM technique. As a result, the current-control regulation may become unstable if the duty cycle exceeds 50%.

To minimize current-sensing inaccuracies caused by ground trace I_R drops, each current-sensing resistor should have a separate return to the ground terminal of the device. For low-value sense resistors, the I x R drops in the printed-wiring board can be significant and should be taken into account. The use of sockets should be avoided as their contact resistance can cause variations in the effective value of R_S.

The LOAD SUPPLY terminal, V_{BB}, should be decoupled with an electrolytic capacitor (47 µF recommended) placed as close to the device as physically practical. To minimize the effect of system ground I x R drops on the logic and reference input signals, the system ground should have a low-resistance return to the load supply voltage.

The frequency of the clock oscillator will determine the amount of ripple current. A lower frequency will result in higher current ripple, but reduced heating in the motor and driver IC due to a corresponding decrease in hysteretic core losses and switching losses respectively. A higher frequency will reduce ripple current, but will increase switching losses and EMI.

Typical output saturation voltages showing Satlington sink-driver operation.

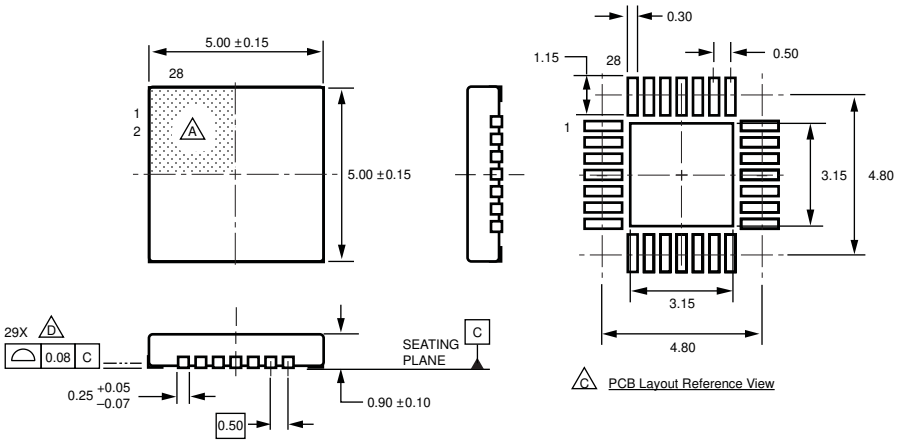


TRUTH TABLE

PHASE	ENABLE	OUT_A	OUT_B
X	H	Off	Off
H	L	H	L
L	L	L	H

X = Irrelevant

Package ET, 28-Pin QFN



For Reference Only
(reference JEDEC MO-220VHHD-1)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals