74LVCV2G66

Overvoltage tolerant bilateral switch

Rev. 6 — 22 July 2015 Product data sheet

1. General description

The 74LVCV2G66 is a low-power, low-voltage, high-speed Si-gate CMOS device.

The 74LVCV2G66 provides two single pole single throw analog or digital switches. Each switch includes an overvoltage tolerant input/output terminal (pin nZ), an output/input terminal (pin nY) and low-power active HIGH enable input (pin nE).

The overvoltage tolerant switch terminals allow the switching of signals in excess of V_{CC}. The low-power enable input eliminates the necessity of using current limiting resistors in portable applications when using control logic signals much lower than V_{CC}. These inputs are also overvoltage tolerant.

2. Features and benefits

- Wide supply voltage range from 2.3 V to 5.5 V
- Ultra low-power operation
- Very low ON resistance:
  - 8.0 Ω (typical) at V_{CC} = 2.7 V
  - 7.5 Ω (typical) at V_{CC} = 3.3 V
  - 7.3 Ω (typical) at V_{CC} = 5.0 V.
- 5 V tolerant input for interfacing with 5 V logic
- High noise immunity
- Switch handling capability of 32 mA
- CMOS low-power consumption
- Latch-up performance exceeds 250 mA
- Incorporates overvoltage tolerant analog switch technology
- Switch accepts voltages up to 5.5 V independent of V_{CC}
- Multiple package options
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVCV2G66DP	−40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVCV2G66DC	−40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVCV2G66GT	−40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVCV2G66GD	−40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm	SOT996-2
74LVCV2G66GM	−40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-2

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74LVCV2G66DP	Y66
74LVCV2G66DC	Y66
74LVCV2G66GT	Y66
74LVCV2G66GD	Y66
74LVCV2G66GM	Y66

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

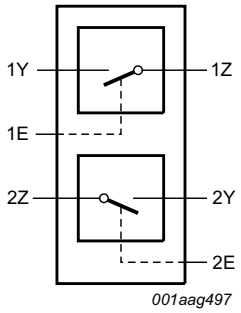


Fig 1. Logic symbol

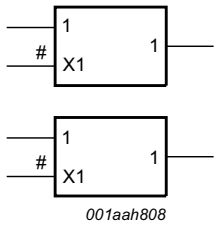


Fig 2. IEC logic symbol

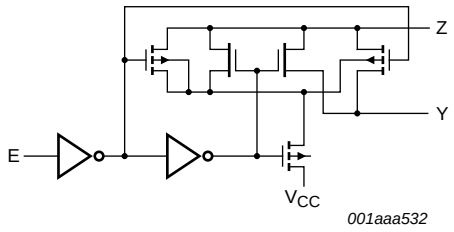


Fig 3. Logic diagram (one switch)

6. Pinning information

6.1 Pinning

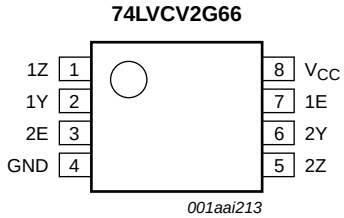


Fig 4. Pin configuration SOT505-2 and SOT765-1

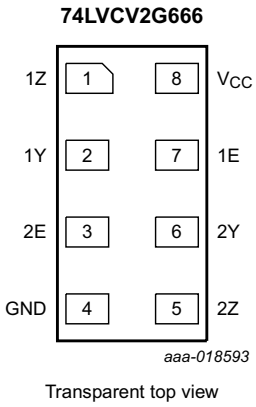


Fig 5. Pin configuration SOT833-1

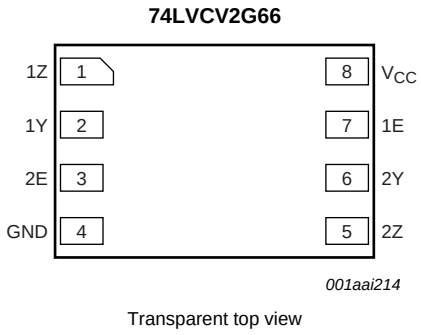


Fig 6. Pin configuration SOT996-2

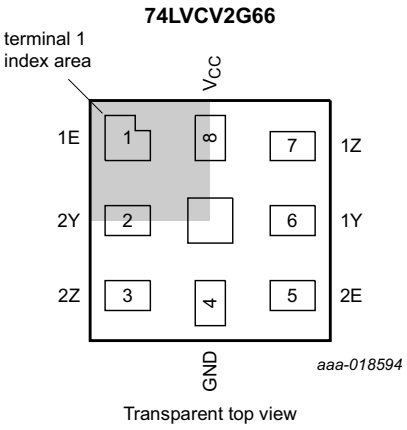


Fig 7. Pin configuration SOT902-2

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT765-1, SOT996-2 and SOT833-1	SOT902-2	
1Z	1	7	independent input or output (overvoltage tolerant)
1Y	2	6	independent input or output
2E	3	5	enable input (active HIGH)
GND	4	4	ground (0 V)
2Z	5	3	independent input or output (overvoltage tolerant)
2Y	6	2	independent input or output
1E	7	1	enable input (active HIGH)
V_{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table[1]

Input nE	Switch
L	OFF-state
H	ON-state

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+6.5	V
V_I	input voltage	[1]	−0.5	+6.5	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > 6.5$ V	−50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V or $V_I > 6.5$ V	-	±50	mA
V_{SW}	switch voltage	enable and disable mode	−0.5	+6.5	V
I_{SW}	switch current	$V_{SW} > -0.5$ V or $V_{SW} < 6.5$ V	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		−100	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C, the value of P_{tot} derates linearly with 2.5 mW/K.
For VSSOP8 package: above 110 °C, the value of P_{tot} derates linearly with 8 mW/K.
For XSON8 and XQFN8 packages: above 118 °C, the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			2.3	-	5.5	V
V_I	input voltage			0	-	5.5	V
V_{SW}	switch voltage	enable and disable mode	[1]	0	-	5.5	V
T_{amb}	ambient temperature			−40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.3 V to 2.7 V	[2]	-	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	[2]	-	-	10	ns/V

[1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current flows from terminal nY. In this case, there is no limit for the voltage drop across the switch.

[2] Applies to control signal levels.

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.6V_{CC}	-	-	0.6V_{CC}	-	V
		V_{CC} = 3.0 V to 3.6 V		2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V		0.55V_{CC}	-	-	0.55V_{CC}	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 V to 2.7 V		-	-	0.1V_{CC}	-	0.1V_{CC}	V
		V_{CC} = 3.0 V to 3.6 V		-	-	0.5	-	0.5	V
		V_{CC} = 4.5 V to 5.5 V		-	-	0.15V_{CC}	-	0.15V_{CC}	V
I_I	input leakage current	pin nE; V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	[2]	-	±0.1	±5	-	±5	µA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 2.3 V to 5.5 V; see Figure 8	[2][3]	-	±0.1	±10	-	±10	µA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 2.3 V to 5.5 V; see Figure 9	[2][3]	-	±0.1	±10	-	±10	µA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{SW} = GND or V_{CC}; V_{CC} = 2.3 V to 5.5 V	[2]	-	0.1	10	-	40	µA
ΔI_{CC}	additional supply current	pin nE; V_I = V_{CC} − 0.6 V; V_{SW} = GND or V_{CC}; V_{CC} = 3.0 V to 5.5 V	[2]	-	0.1	5	-	50	µA
C_I	input capacitance			-	2.5	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance			-	8.0	-	-	-	pF

Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

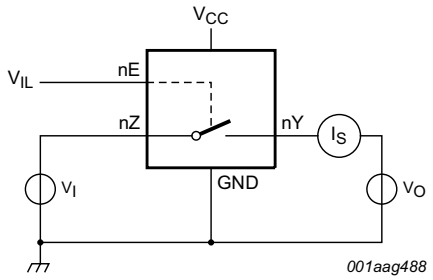
Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$C_{S(ON)}$	ON-state capacitance		-	16	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

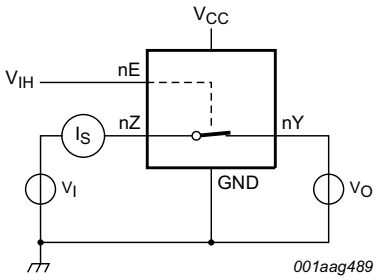
[3] For overvoltage signals ($V_{SW} > V_{CC}$), the condition $V_Y < V_Z$ must be observed.

10.1 Test circuits



V_I = GND and V_O = GND or 5.5 V.

Fig 8. Test circuit for measuring OFF-state leakage current



V_I = 5.5 V or GND and V_O = open circuit.

Fig 9. Test circuit for measuring ON-state leakage current

10.2 ON resistance

Table 8. Resistance R_{ON}

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see Figure 11 and Figure 12.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	V_{SW} = GND to V_{CC}; $V_I = V_{IH}$; see Figure 10						
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	13	30	-	30	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	10	25	-	25	Ω
		I_{SW} = 24 mA; V_{CC} = 3.0 V to 3.6 V	-	8.3	20	-	20	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	7.4	15	-	15	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_{SW} = GND; $V_I = V_{IH}$; see Figure 10						
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	8.5	20	-	20	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	8.0	18	-	18	Ω
		I_{SW} = 24 mA; V_{CC} = 3.0 V to 3.6 V	-	7.5	15	-	15	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	7.3	10	-	10	Ω
		$V_{SW} = V_{CC}$; $V_I = V_{IH}$						
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	8.5	20	-	20	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	7.2	18	-	18	Ω
		I_{SW} = 24 mA; V_{CC} = 3.0 V to 3.6 V	-	6.5	15	-	15	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	5.7	10	-	10	Ω

Table 8. Resistance R_{ON} *...continued*

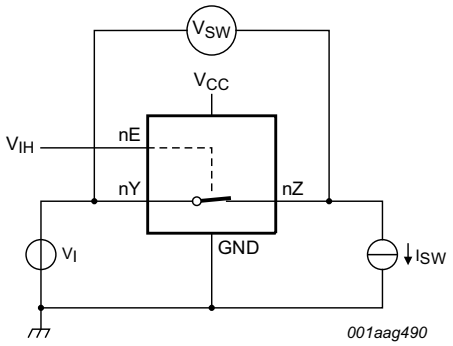
At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see Figure 11 and Figure 12.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(flat)}$	ON resistance (flatness)	V_{SW} = GND to V_{CC}; $V_I = V_{IH}$ [2]						
		I_{SW} = 8 mA; V_{CC} = 2.5 V	-	17	-	-	-	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	10	-	-	-	Ω
		I_{SW} = 24 mA; V_{CC} = 3.3 V	-	5	-	-	-	Ω
		I_{SW} = 32 mA; V_{CC} = 5.0 V	-	3	-	-	-	Ω

[1] All typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

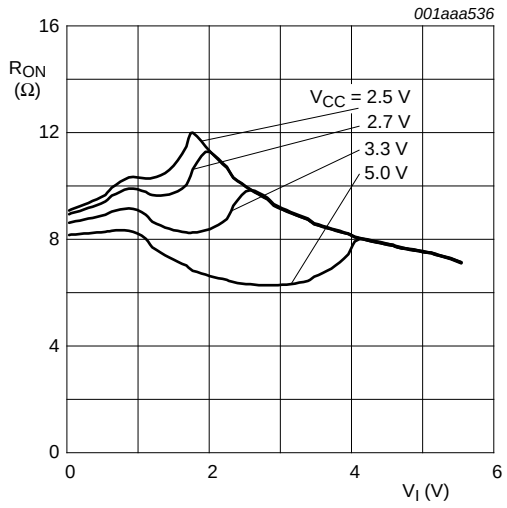
[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3 ON resistance test circuit and graphs



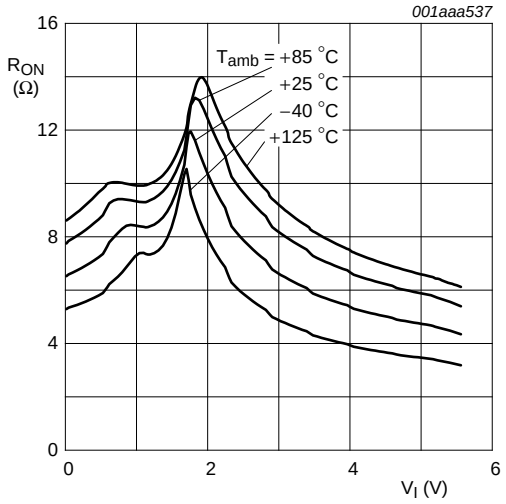
V_I = GND to 5.5 V; $R_{ON} = V_{SW} / I_{SW}$.

Fig 10. Test circuit for measuring ON resistance

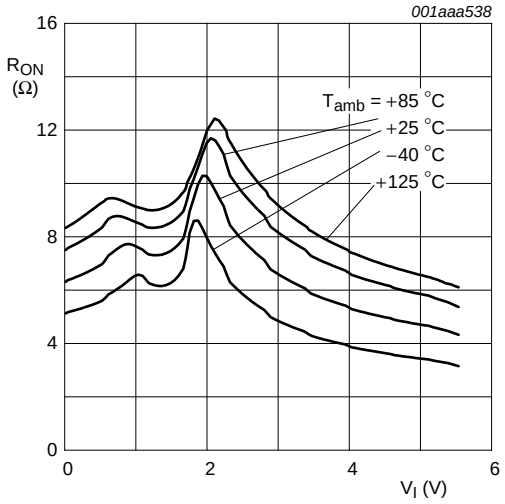


V_I = GND to 5.5 V; T_{amb} = 25 °C.

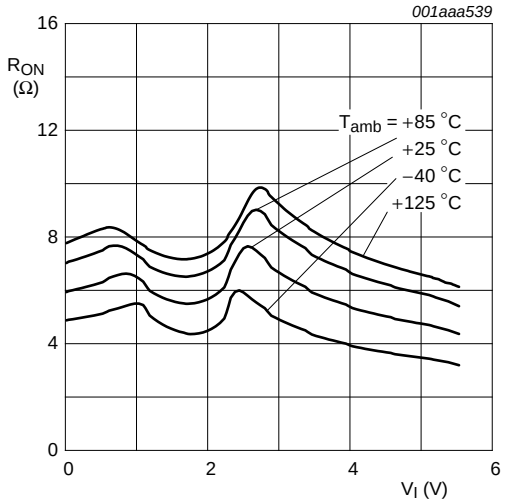
Fig 11. Typical ON resistance as a function of input voltage



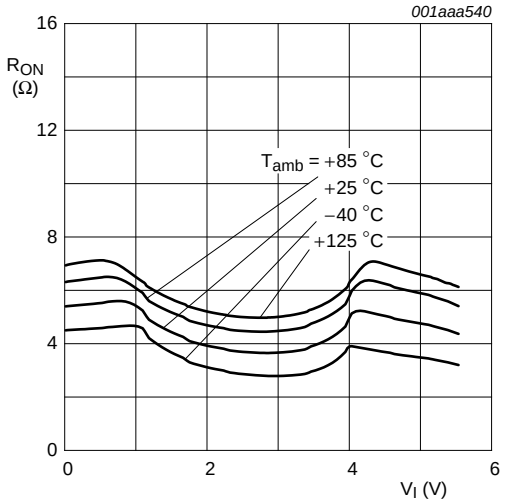
a. V_{CC} = 2.5 V



b. V_{CC} = 2.7 V



c. V_{CC} = 3.3 V



d. V_{CC} = 5.0 V

Fig 12. ON resistance as a function of input voltage at various supply voltages

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 15.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nY to nZ or nZ to nY; see Figure 13 [2][3]						
		V_{CC} = 2.3 V to 2.7 V	-	0.4	1.2	-	2.0	ns
		V_{CC} = 2.7 V	-	0.4	1.0	-	1.5	ns
		V_{CC} = 3.0 V to 3.6 V	-	0.3	0.8	-	1.5	ns
		V_{CC} = 4.5 V to 5.5 V	-	0.2	0.6	-	1.0	ns

Table 9. Dynamic characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 15.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{en}	enable time	nE to nY or nZ; see Figure 14 [4]						
		V_{CC} = 2.3 V to 2.7 V	1.0	4.7	12	1.0	15	ns
		V_{CC} = 2.7 V	1.0	4.4	8.5	1.0	11	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.8	7.5	1.0	9.5	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	2.7	5.0	1.0	6.5	ns
t_{dis}	disable time	nE to nY or nZ; see Figure 14 [5]						
		V_{CC} = 2.3 V to 2.7 V	1.0	6.0	16	1.0	20	ns
		V_{CC} = 2.7 V	1.0	7.9	15	1.0	19	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	6.5	13.5	1.0	17	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	4.4	9.0	1.0	11.5	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 10 MHz; V_I = GND to 5.5 V [6]						
		V_{CC} = 2.5 V	-	9.7	-	-	-	pF
		V_{CC} = 3.3 V	-	10.3	-	-	-	pF
		V_{CC} = 5.0 V	-	11.3	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

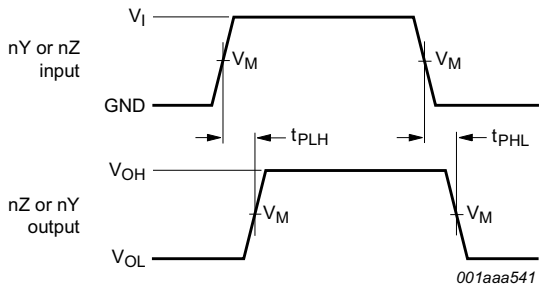
[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

[4] t_{en} is the same as t_{PZH} and t_{PZL}.

[5] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\}$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
$C_{S(ON)}$ = maximum ON-state switch capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma\{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\}$ = sum of the outputs.

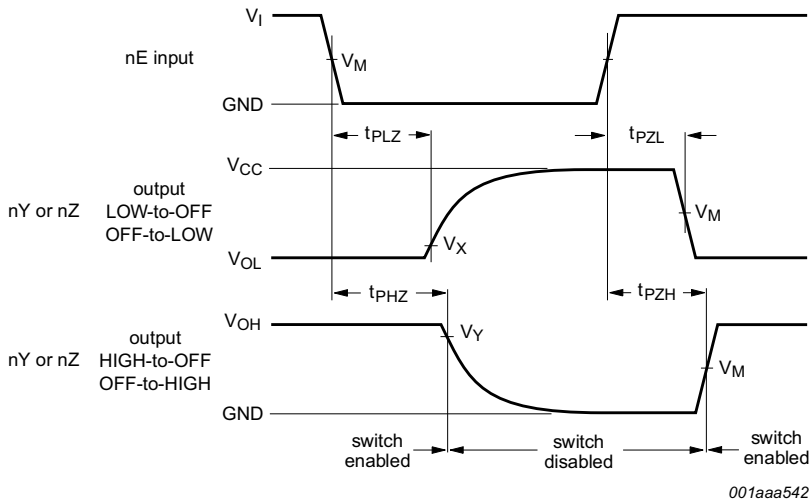
11.1 Waveforms and test circuit



Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 13. Input (nY or nZ) to output (nZ or nY) propagation delays



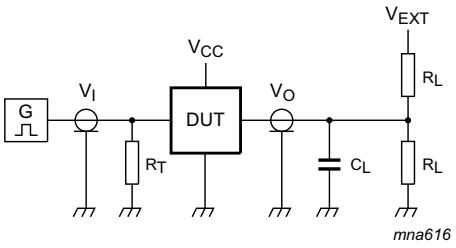
Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 14. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 11.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

V_{EXT} = External voltage for measuring switching times.

Fig 15. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6.0 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6.0 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$

11.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

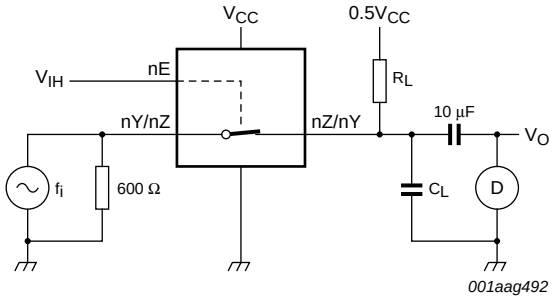
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	f_i = 1 kHz; R_L = 10 kΩ; C_L = 50 pF; see Figure 16				
		V_{CC} = 2.3 V	-	0.42	-	%
		V_{CC} = 3.0 V	-	0.36	-	%
		V_{CC} = 4.5 V	-	0.47	-	%
		f_i = 10 kHz; R_L = 10 kΩ; C_L = 50 pF; see Figure 16				
		V_{CC} = 2.3 V	-	0.11	-	%
		V_{CC} = 3.0 V	-	0.07	-	%
		V_{CC} = 4.5 V	-	0.01	-	%
$f_{(-3dB)}$	−3 dB frequency response	R_L = 600 Ω; C_L = 50 pF; see Figure 17				
		V_{CC} = 2.3 V	-	160	-	MHz
		V_{CC} = 3.0 V	-	200	-	MHz
		V_{CC} = 4.5 V	-	210	-	MHz
		R_L = 50 Ω; C_L = 5 pF; see Figure 17				
		V_{CC} = 2.3 V	-	180	-	MHz
		V_{CC} = 3.0 V	-	180	-	MHz
		V_{CC} = 4.5 V	-	180	-	MHz

Table 12. Additional dynamic characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{iso}	isolation (OFF-state)	R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; see Figure 18				
		V_{CC} = 2.3 V	-	−65	-	dB
		V_{CC} = 3.0 V	-	−65	-	dB
		V_{CC} = 4.5 V	-	−62	-	dB
		R_L = 50 Ω; C_L = 5 pF; f_i = 1 MHz; see Figure 18				
		V_{CC} = 2.3 V	-	−37	-	dB
		V_{CC} = 3.0 V	-	−36	-	dB
		V_{CC} = 4.5 V	-	−36	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; $t_r = t_f$ = 2 ns; see Figure 19				
		V_{CC} = 2.3 V	-	91	-	mV
		V_{CC} = 3.0 V	-	119	-	mV
		V_{CC} = 4.5 V	-	205	-	mV
Xtalk	crosstalk	between switches; R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; see Figure 20				
		V_{CC} = 2.3 V	-	−56	-	dB
		V_{CC} = 3.0 V	-	−55	-	dB
		V_{CC} = 4.5 V	-	−55	-	dB
		between switches; R_L = 50 Ω; C_L = 5 pF; f_i = 1 MHz; see Figure 20				
		V_{CC} = 2.3 V	-	−29	-	dB
		V_{CC} = 3.0 V	-	−28	-	dB
		V_{CC} = 4.5 V	-	−28	-	dB
Q_{inj}	charge injection	C_L = 0.1 nF; V_{gen} = 0 V; R_{gen} = 0 Ω; f_i = 1 MHz; R_L = 1 MΩ; see Figure 21				
		V_{CC} = 2.5 V	-	< 0.003	-	pC
		V_{CC} = 3.3 V	-	0.003	-	pC
		V_{CC} = 4.5 V	-	0.0035	-	pC
		V_{CC} = 5.5 V	-	0.0035	-	pC

11.3 Test circuits



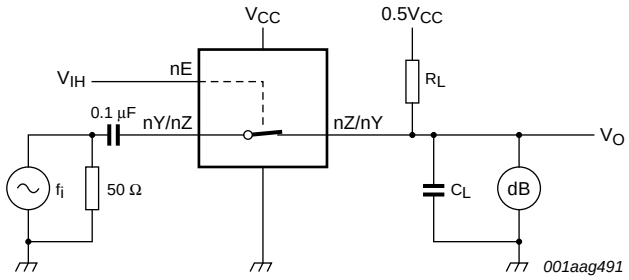
Test conditions:

V_{CC} = 2.3 V: V_i = 2 V (p-p).

V_{CC} = 3 V: V_i = 2.5 V (p-p).

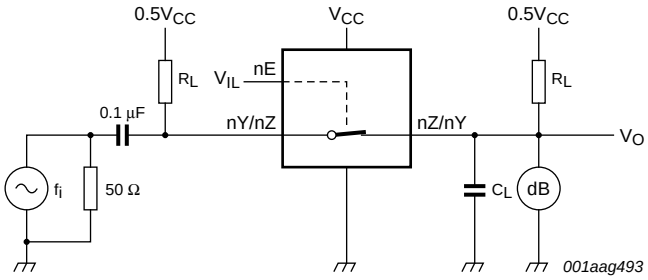
V_{CC} = 4.5 V: V_i = 4 V (p-p).

Fig 16. Test circuit for measuring total harmonic distortion



To obtain 0 dBm level at the output, adjust f_i voltage. Increase f_i frequency until dB meter reads −3 dB.

Fig 17. Test circuit for measuring the frequency response when switch is in ON-state



To obtain 0 dBm level at the input, adjust f_i voltage.

Fig 18. Test circuit for measuring isolation (OFF-state)

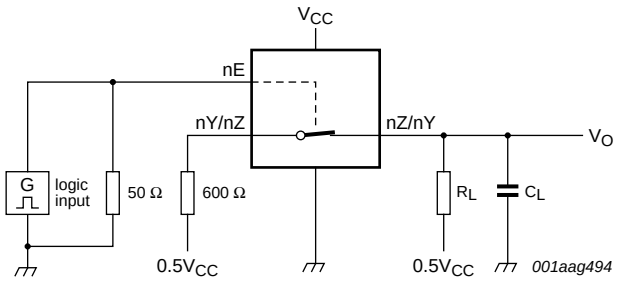
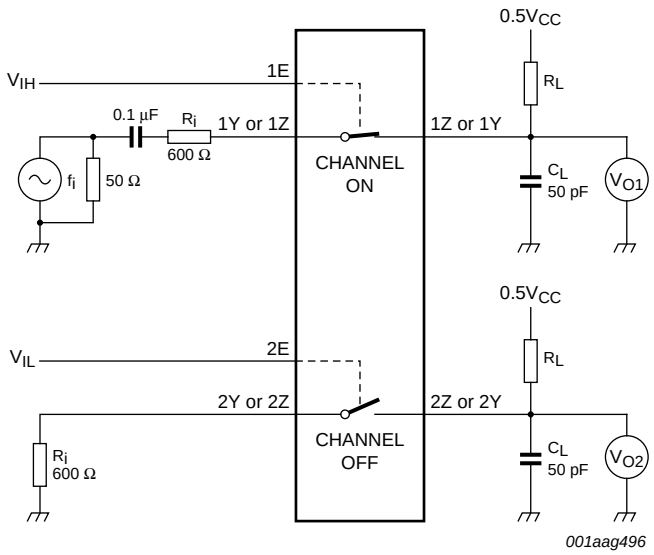
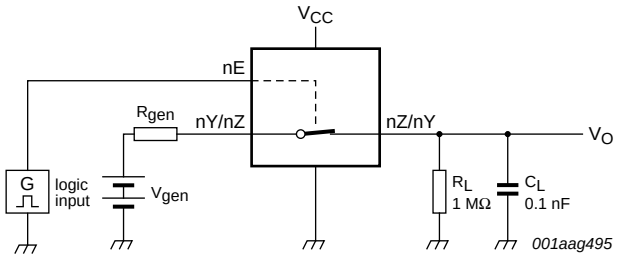


Fig 19. Test circuit for measuring crosstalk voltage (between digital inputs and switch)

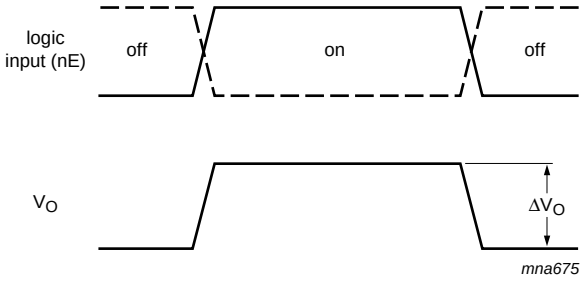


$20 \log_{10} (V_{O2} / V_{O1})$ or $20 \log_{10} (V_{O1} / V_{O2})$.

Fig 20. Test circuit for measuring crosstalk between switches



a. Test circuit



b. Input and output pulse definitions

$Q_{inj} = \Delta V_O \times C_L$.

ΔV_O = output voltage variation.

R_{gen} = generator resistance.

V_{gen} = generator voltage.

Fig 21. Test circuit for measuring charge injection

12. Application information

The 74LVCV2G66 is used to reduce component count and footprint in low-power portable applications.

Typical '66' devices do not have low-power enable inputs causing a high ΔI_{CC}. To reduce power consumption in portable (battery) applications, a current limiting resistor is used. (see Figure 22a). The low-power enable inputs of the 74LVCV2G66 have much lower ΔI_{CC}, eliminating the necessity of the current limiting resistor (see Figure 22b).

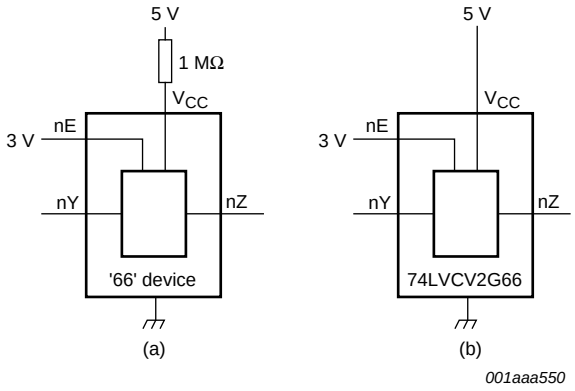
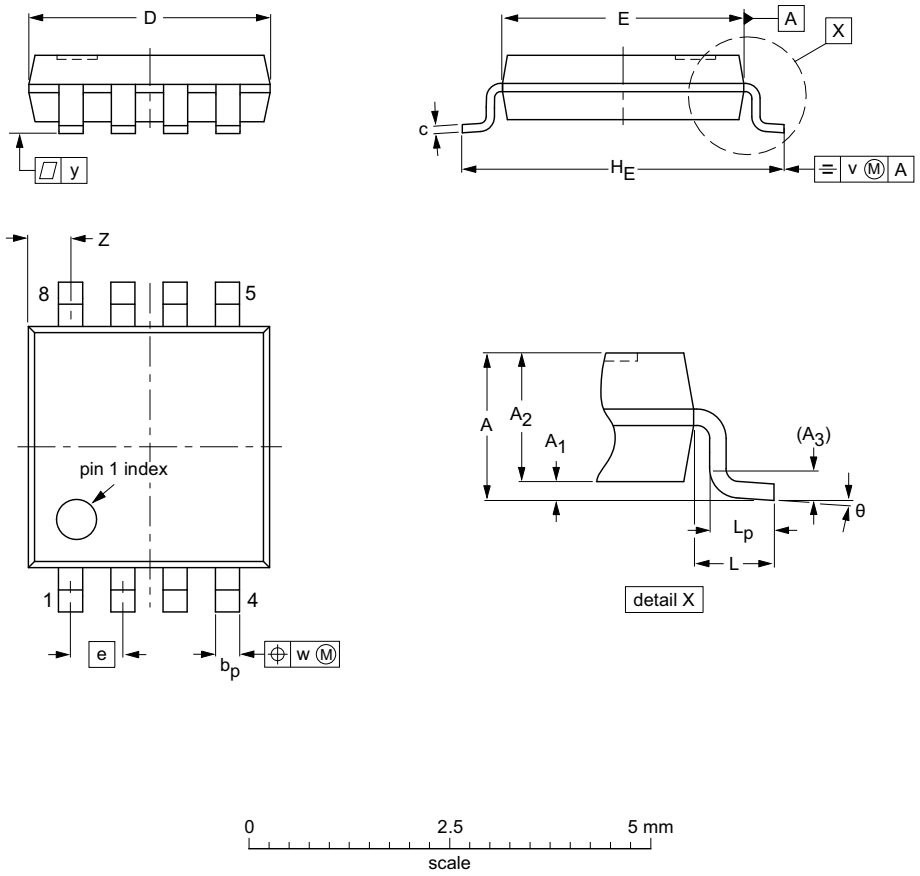


Fig 22. Application example

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

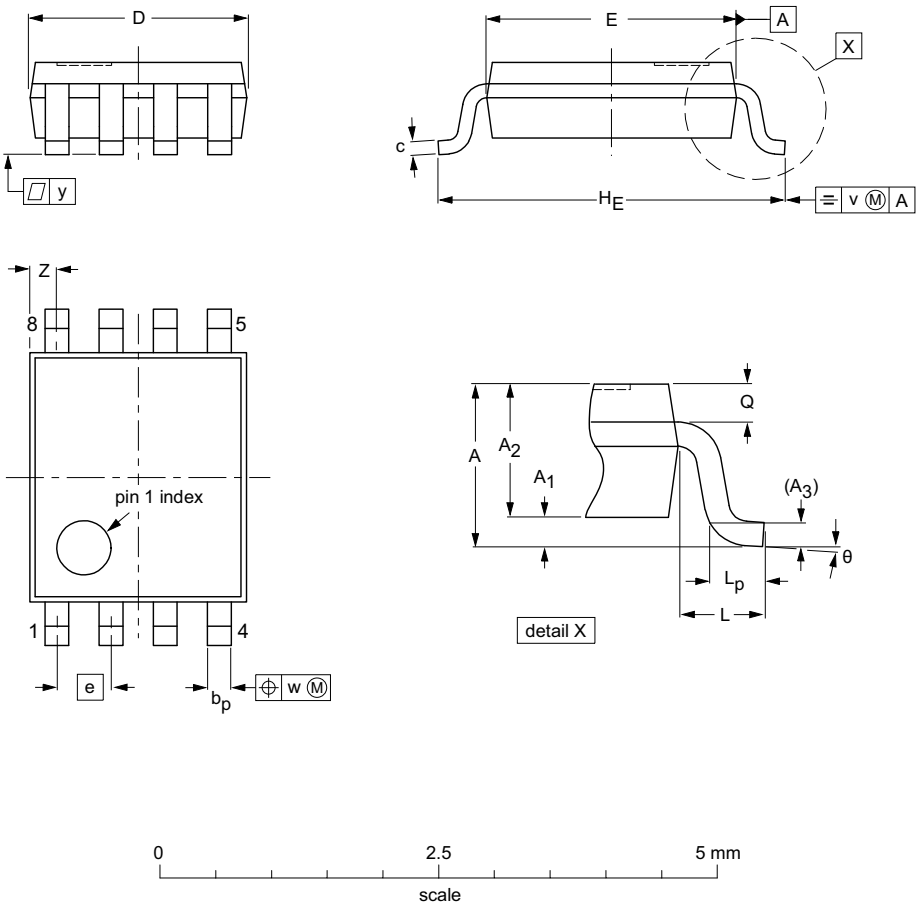
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 23. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

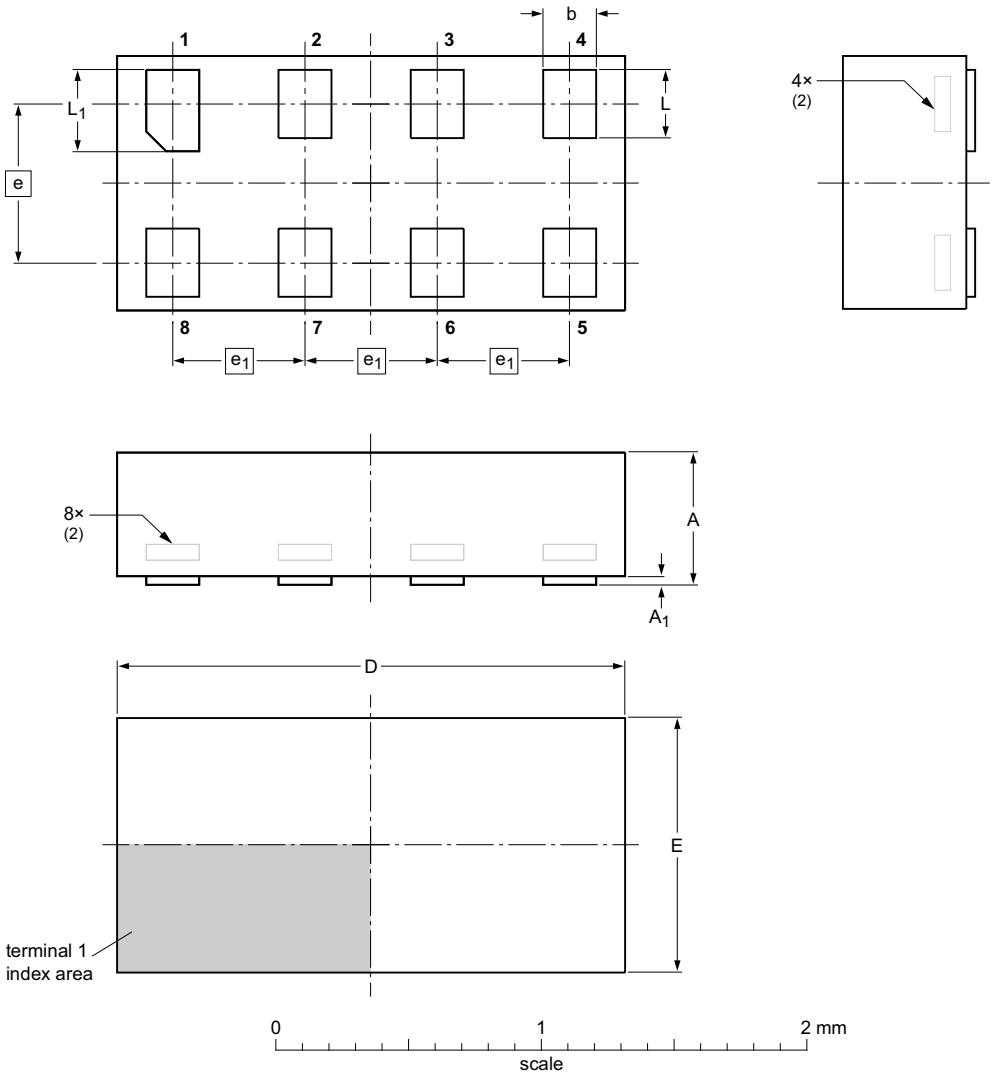
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 24. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

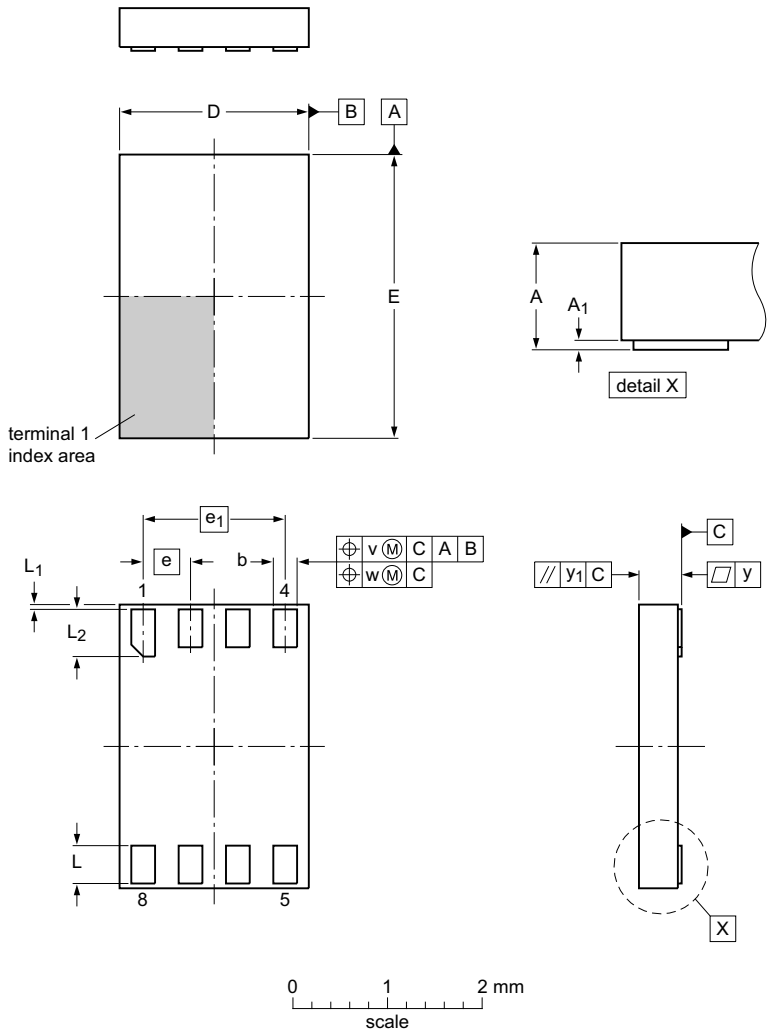
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig 25. Package outline SOT833-1 (XSON8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 3 x 2 x 0.5 mm **SOT996-2**



Dimensions (mm are the original dimensions)

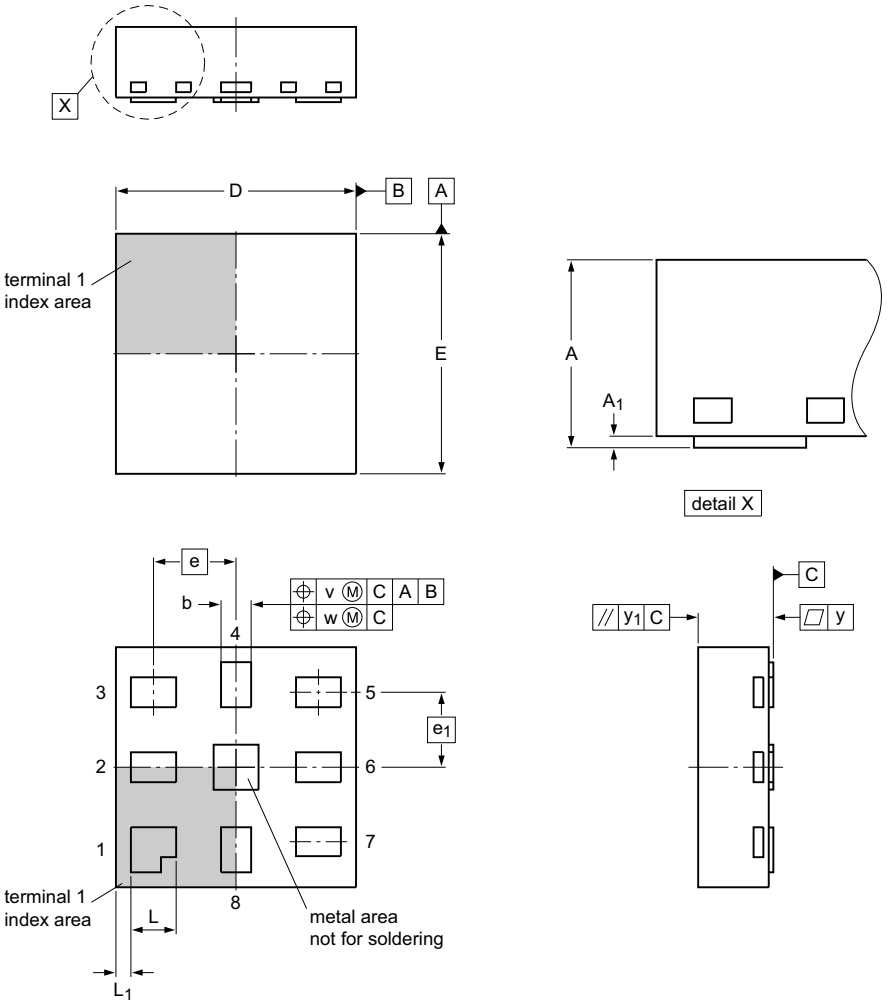
Unit(1)		A	A_1	b	D	E	e	e_1	L	L_1	L_2	v	w	y	y_1
mm	max	0.5	0.05	0.35	2.1	3.1	0.5	1.5	0.5	0.15	0.6	0.1	0.05	0.05	0.1
	nom														
	min		0.00	0.15	1.9	2.9			0.3	0.05	0.4				

sot996-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT996-2						~~07-12-21~~ 12-11-20

Fig 26. Package outline SOT996-2 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm **SOT902-2**



Dimensions

Unit[1]		A	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	max	0.5	0.05	0.25	1.65	1.65	0.55	0.5	0.35	0.15	0.1	0.05	0.05	0.05
	nom			0.20	1.60	1.60			0.30	0.10				
	min		0.00	0.15	1.55	1.55			0.25	0.05				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot902-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT902-2	- - -	MO-255	- - -			~~10-11-02~~ 11-03-31

Fig 27. Package outline SOT902-2 (XQFN8)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVCV2G66 v.6	20150722	Product data sheet	-	74LVCV2G66 v.5
Modifications:	• Added type numbers 74LVCV2G66GT and.74LVCV2G66GM			
74LVCV2G66 v.5	20130329	Product data sheet	-	74LVCV2G66 v.4
Modifications:	• For type number 74LVCV2G66GD XSON8U has changed to XSON8.			
74LVCV2G66 v.4	20111122	Product data sheet	-	74LVCV2G66 v.3
Modifications:	• Legal pages updated.			
74LVCV2G66 v.3	20100616	Product data sheet	-	74LVCV2G66 v.2
74LVCV2G66 v.2	20080703	Product data sheet	-	74LVCV2G66 v.1
74LVCV2G66 v.1	20040402	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

18. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 22 July 2015
Document identifier: 74LVCV2G66