To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

DATA SHEET

RENESAS

MOS FIELD EFFECT TRANSISTOR
NP55N055SDG

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The NP55N055SDG is N-channel MOS Field Effect Transistor designed for high current switching applications.

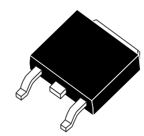
ORDERING INFORMATION

PART NUMBER	PACKAGE
NP55N055SDG	TO-252 (MP-3ZK)

FEATURES

- Channel temperature 175 degree rating
- Super low on-state resistance
  $R_{DS(on)1}$ = 9.5 mΩ MAX. (V_{GS} = 10 V, I_D = 28 A)
- Low C_{iss}: C_{iss} = 3200 pF TYP.
- Logic level drive type

(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	55	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±55	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±220	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	77	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Repetitive Avalanche Current Note2	I_{AR}	27	A
Repetitive Avalanche Energy Note2	E_{AR}	73	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. T_{ch} < 150°C, V_{DD} = 28 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.95	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	°C/W

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

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Date Published January 2005 NS CP(K)
Printed in Japan

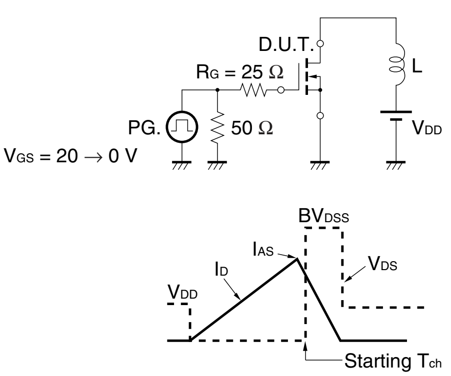
The mark ★ shows major revised points.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

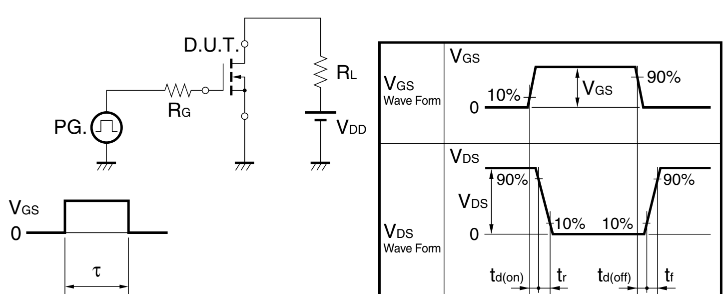
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 55 V, V_{GS} = 0 V			1.0	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	| y_{fs} |	V_{DS} = 10 V, I_D = 28 A	15	32		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 28 A		7.4	9.5	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 28 A		8.9	12	mΩ
Input Capacitance	C_{iss}	V_{DS} = 25 V		3200	4800	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		270	410	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		170	310	pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 28 V, I_D = 28 A		17	38	ns
Rise Time	t_r	V_{GS} = 10 V		16	40	ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		71	142	ns
Fall Time	t_f			6	15	ns
Total Gate Charge	Q_G	V_{DD} = 44 V		64	96	nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		10		nC
Gate to Drain Charge	Q_{GD}	I_D = 55 A		18		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 55 A, V_{GS} = 0 V		0.94	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 55 A, V_{GS} = 0 V		35		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		38		nC

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

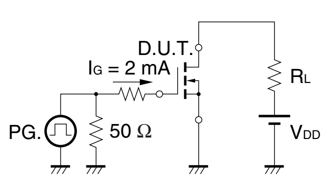


TEST CIRCUIT 2 SWITCHING TIME



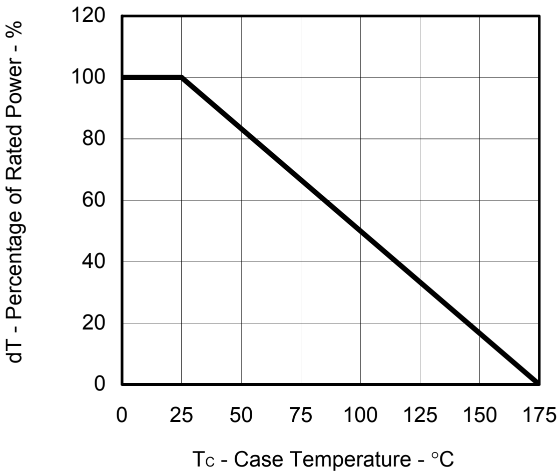
τ = 1 μs
Duty Cycle ≤ 1%

TEST CIRCUIT 3 GATE CHARGE

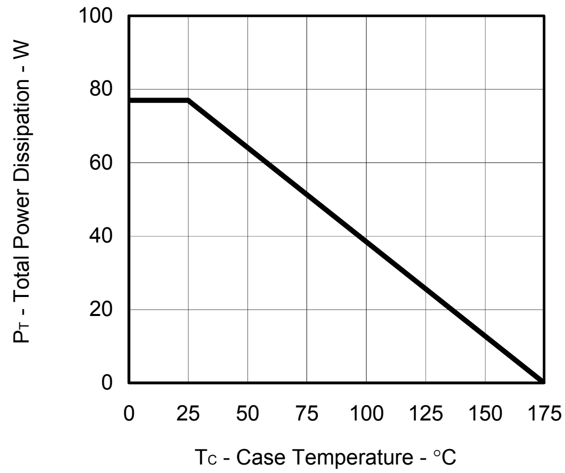


TYPICAL CHARACTERISTICS (T_A = 25°C)

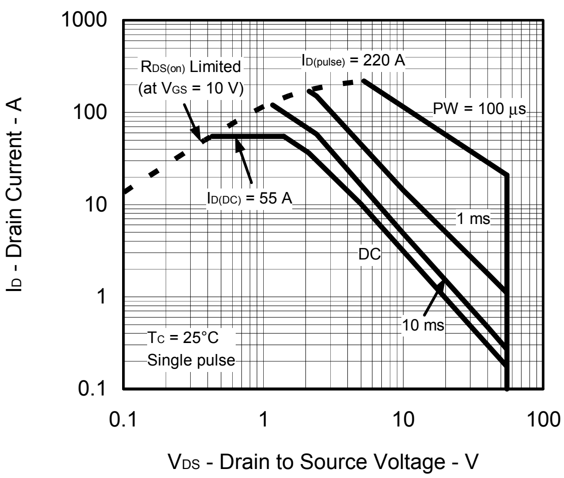
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



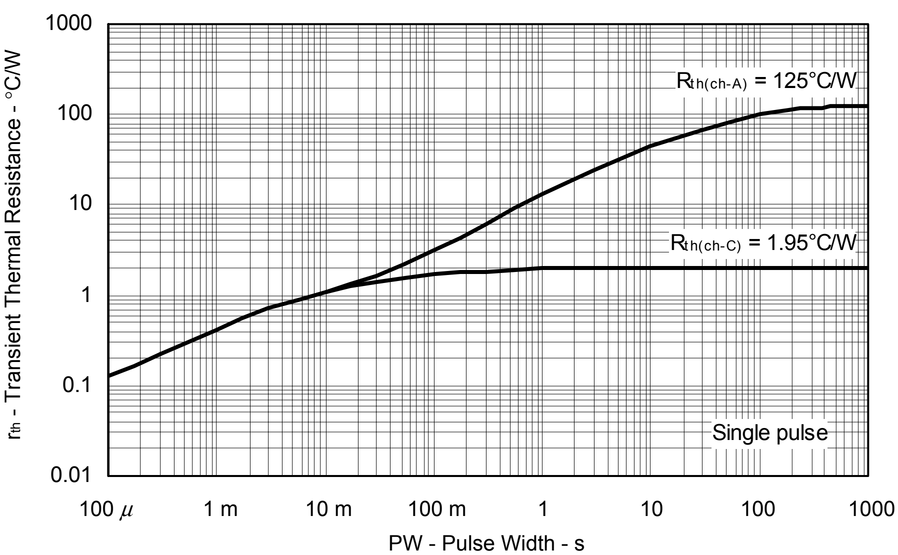
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



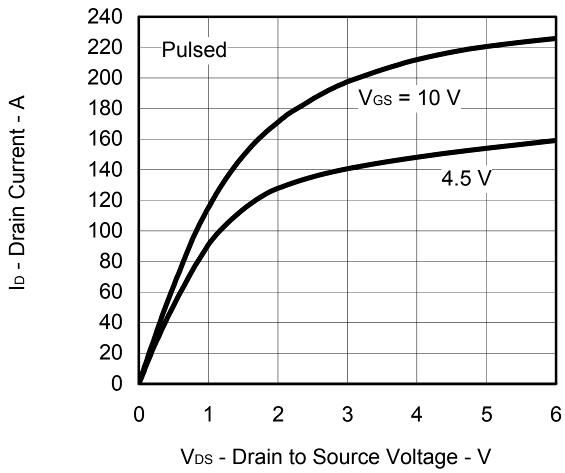
FORWARD BIAS SAFE OPERATING AREA



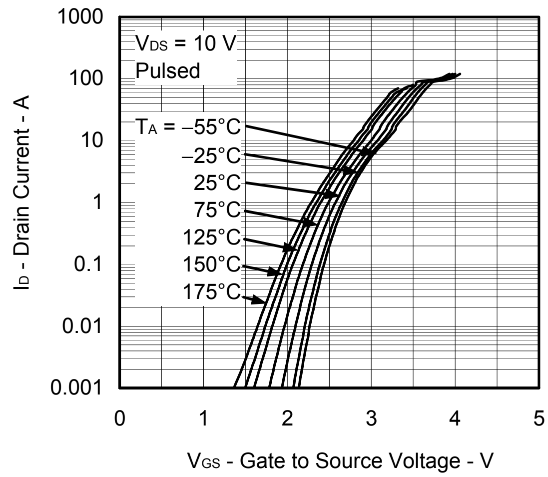
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



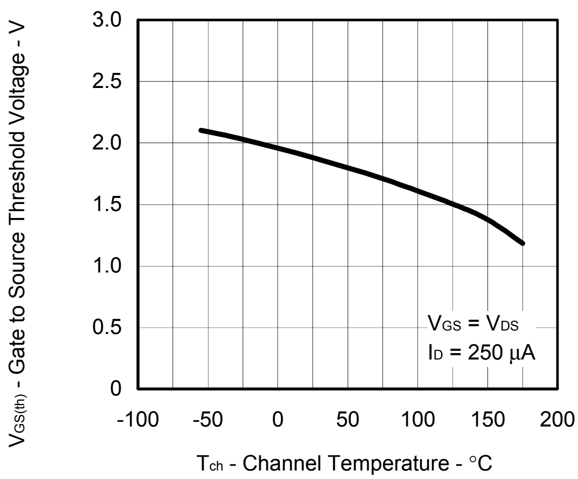
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



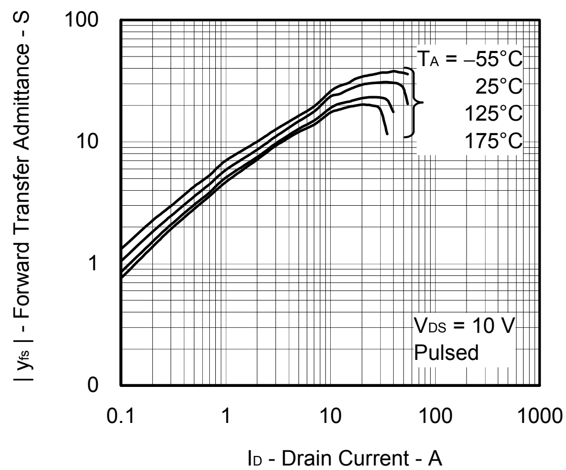
FORWARD TRANSFER CHARACTERISTICS



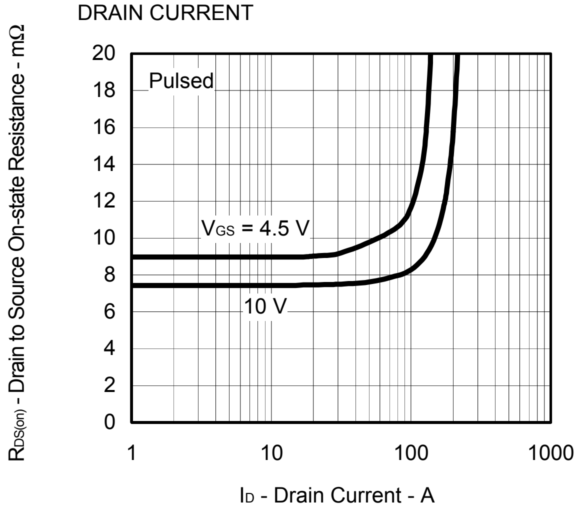
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



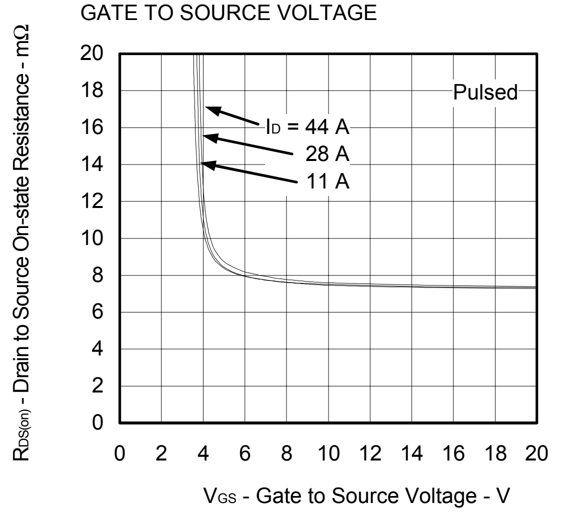
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



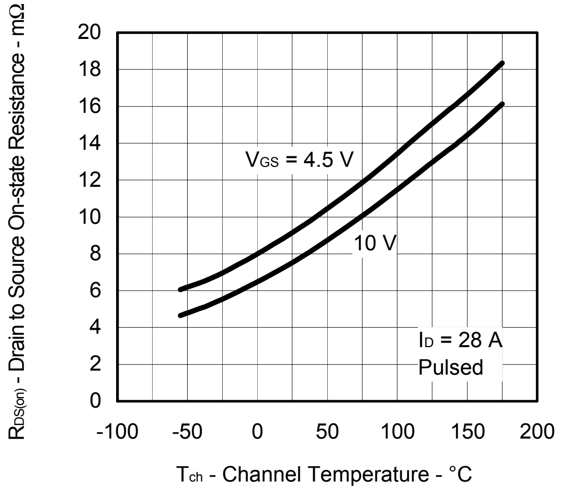
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



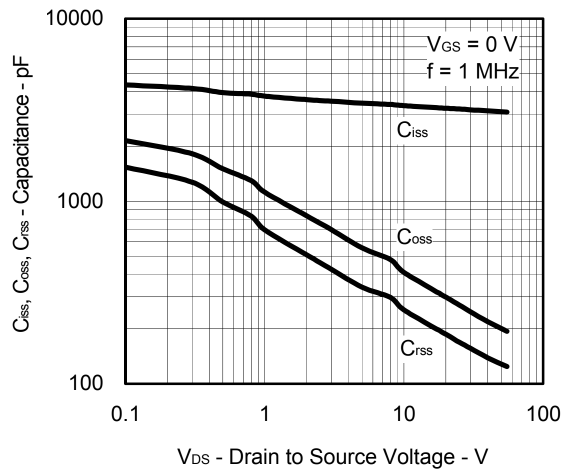
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



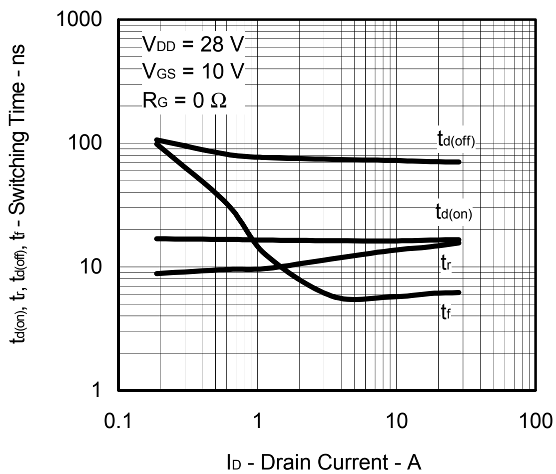
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



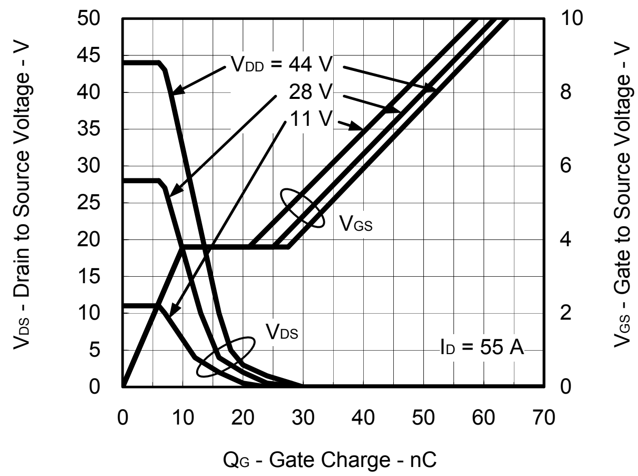
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



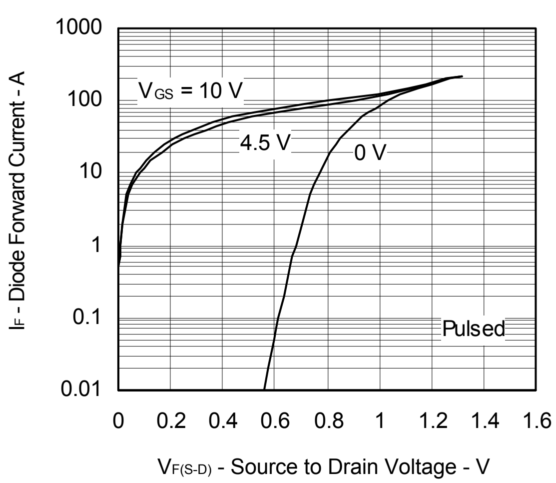
SWITCHING CHARACTERISTICS



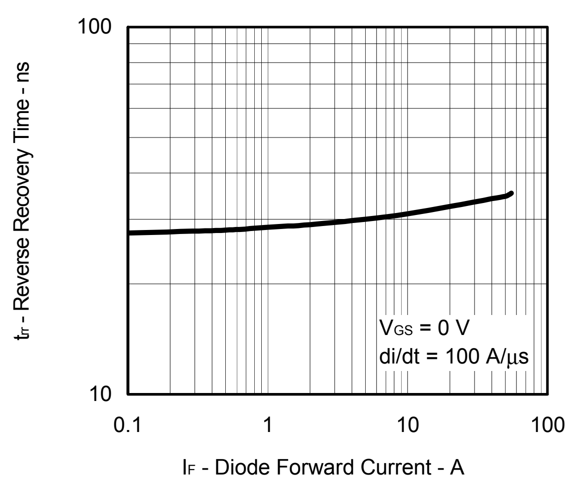
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

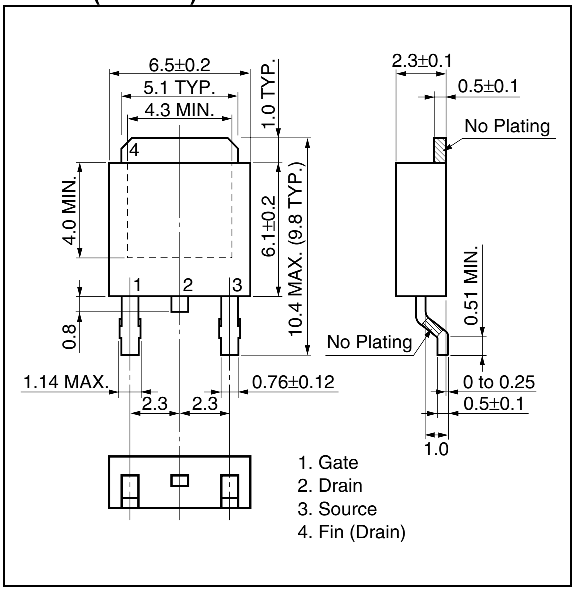


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

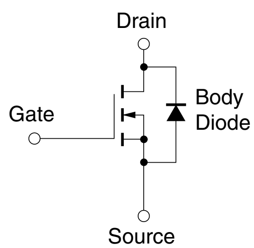


★ PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.