

## N-Channel 30 V (D-S) MOSFET

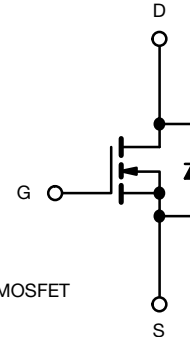
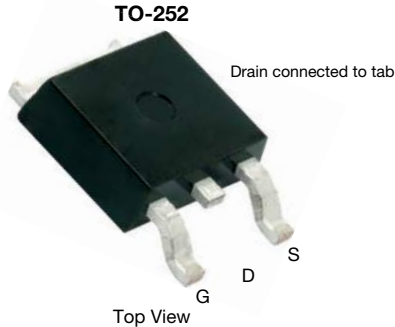
PRODUCT SUMMARY		
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>
30	0.0120 at V <sub>GS</sub> = 10 V	16.8
	0.0175 at V <sub>GS</sub> = 4.5 V	13.9

### FEATURES

- TrenchFET® power MOSFET
- 100 % R<sub>g</sub> and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



### Ordering Information:

SUD50N03-12P-GE3 (lead (Pb)-free and halogen-free)

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage	V <sub>DS</sub>	30	V		
Gate-Source Voltage	V <sub>GS</sub>	± 20			
Continuous Drain Current <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25 °C	16.8	A	
		T <sub>A</sub> = 100 °C	10.6		
Pulsed Drain Current	I <sub>DM</sub>	40			
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	3.6			
Avalanche Current	I <sub>AS</sub>	L = 0.1 mH	30		mJ
Single Pulse Avalanche Energy			E <sub>AS</sub>	45	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	39	W	
		T <sub>A</sub> = 25 °C	5.4 <sup>a</sup>		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C		

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	t ≤ 10 s	18	23	°C/W
		Steady State	40	50	
Maximum Junction-to-Case	R <sub>thJC</sub>	2.6	3.2		

### Note

a. Surface mounted on FR4 board, t ≤ 10 s.



SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP. <sup>a</sup>	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	-	3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	40	-	-	A
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	-	0.0100	0.0120	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.0170	
		$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$	-	0.0138	0.0175	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$	15	-	-	S
<b>Dynamic <sup>a</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	1600	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$		-	285	-	
Reverse Transfer Capacitance	$C_{rss}$		-	140	-	
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 50\text{ A}$	-	28	42	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$		-	6	-	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$		-	5	-	
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.3	1.5	3.0	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 0.3\text{ }\Omega$ $I_D \cong 50\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\text{ }\Omega$	-	9	15	ns
Rise Time <sup>c</sup>	$t_r$		-	15	25	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$		-	20	30	
Fall Time <sup>c</sup>	$t_f$		-	12	20	
<b>Source-Drain Diode Ratings and Characteristics (<math>T_C = 25\text{ }^\circ\text{C}</math>)</b>						
Pulsed Current	$I_{SM}$		-	-	100	A
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$I_F = 40\text{ A}, V_{GS} = 0\text{ V}$	-	1.2	1.5	V
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	25	70	ns

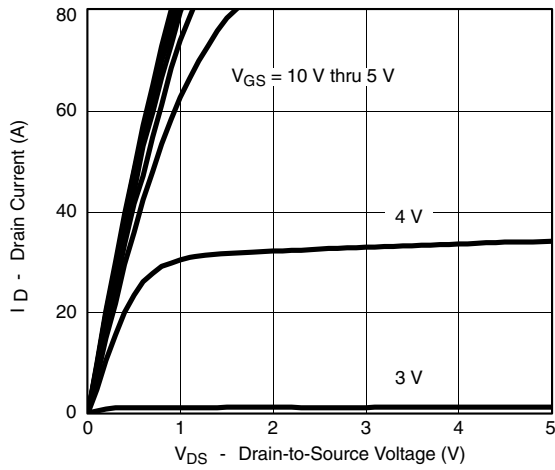
**Notes**

- a. Guaranteed by design, not subject to production testing.  
b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
c. Independent of operating temperature.

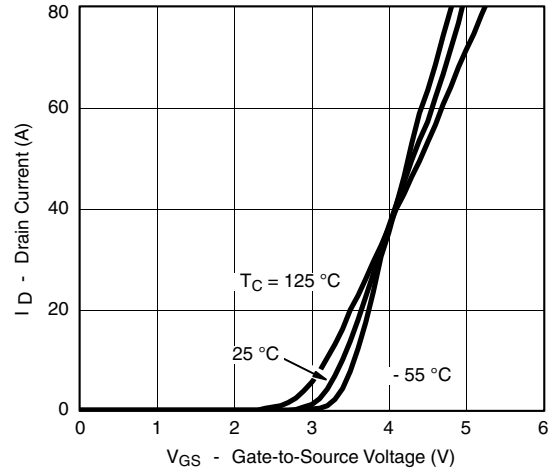
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



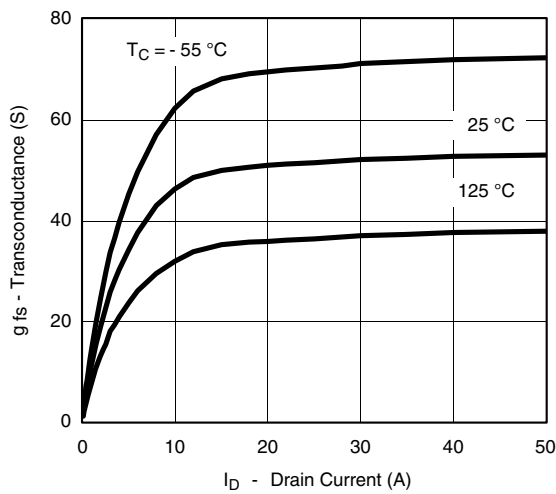
TYPICAL CHARACTERISTICS (25 °C unless noted)



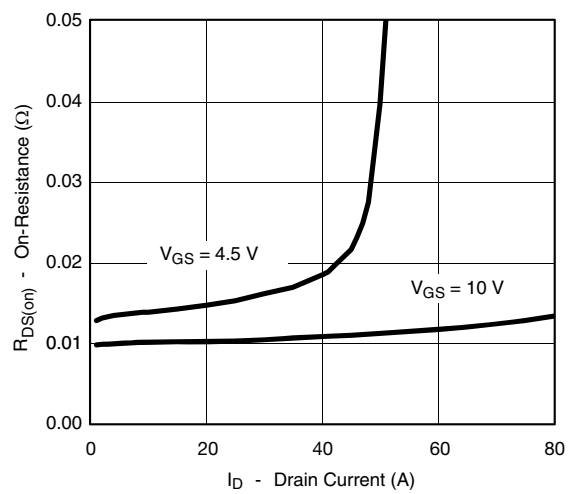
Output Characteristics



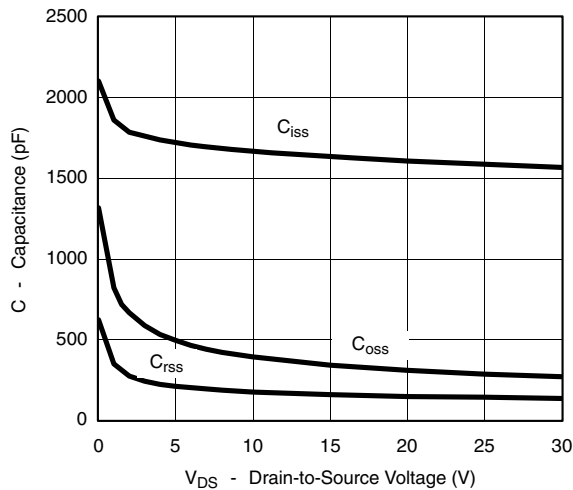
Transfer Characteristics



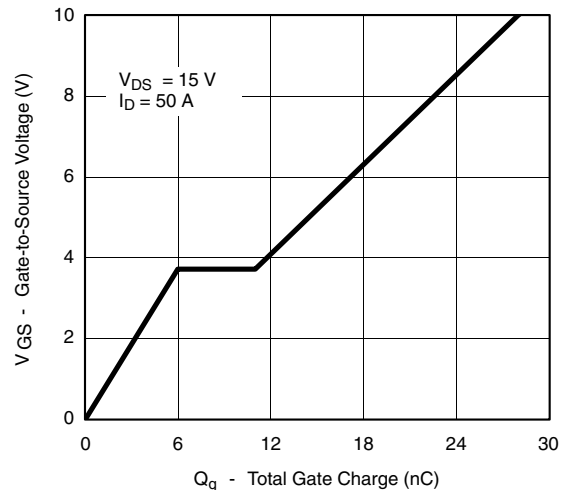
Transconductance



On-Resistance vs. Drain Current



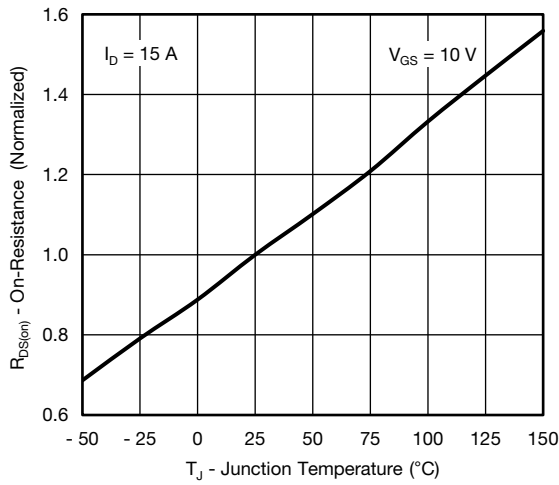
Capacitance



Gate Charge



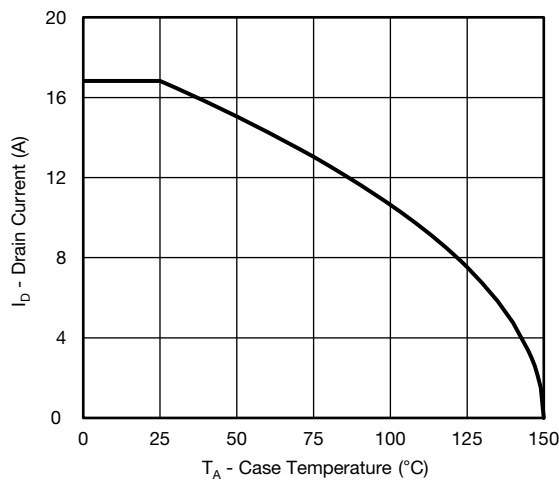
THERMAL RATINGS



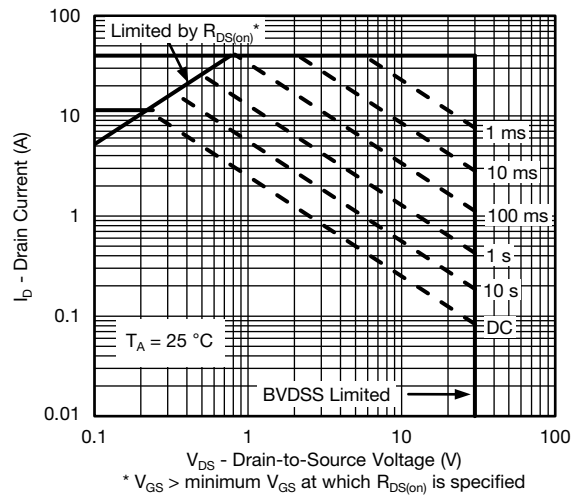
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



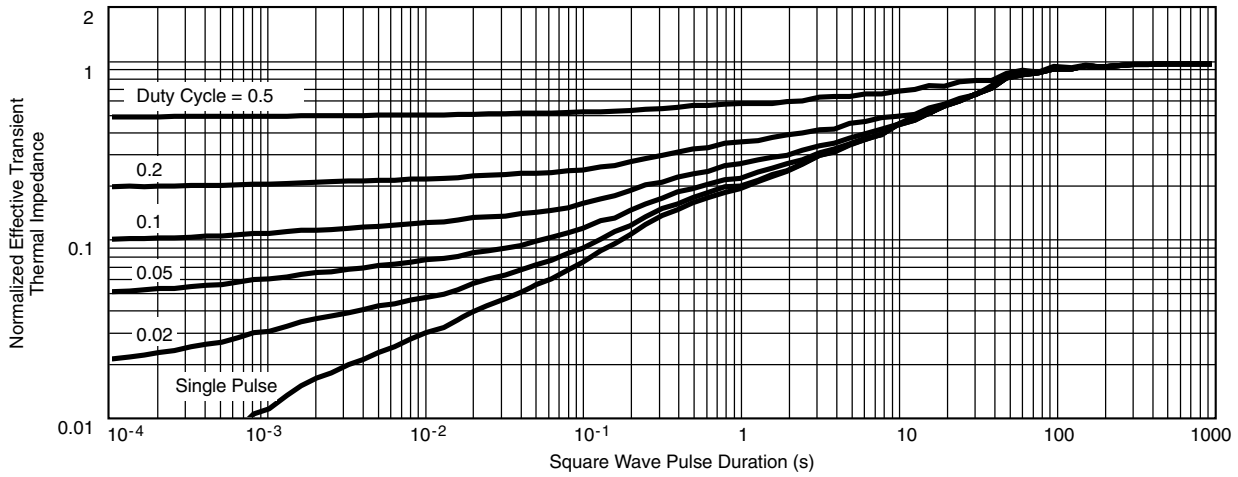
Maximum Drain Current vs. Ambient Temperature



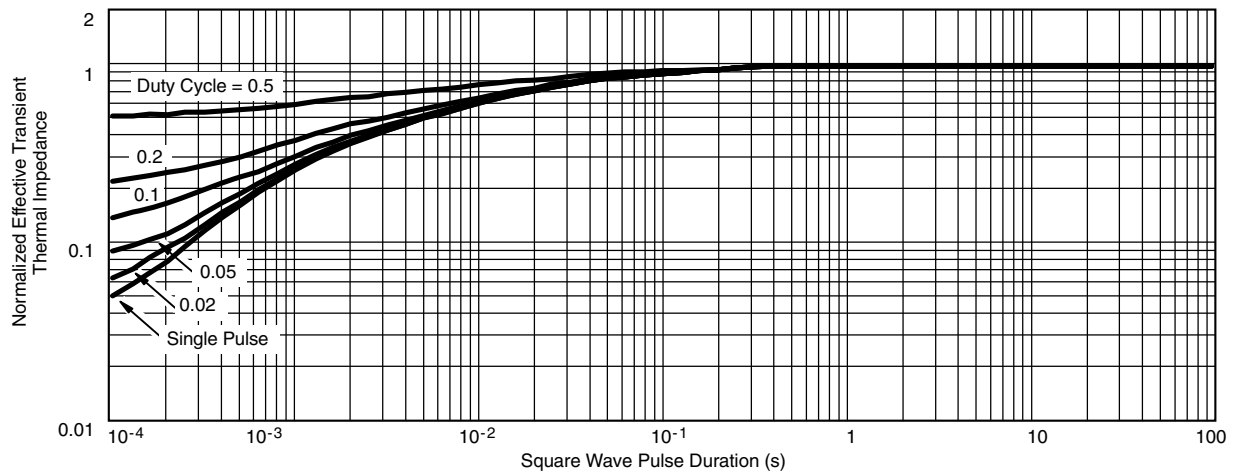
Safe Operating Area



**THERMAL RATINGS**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

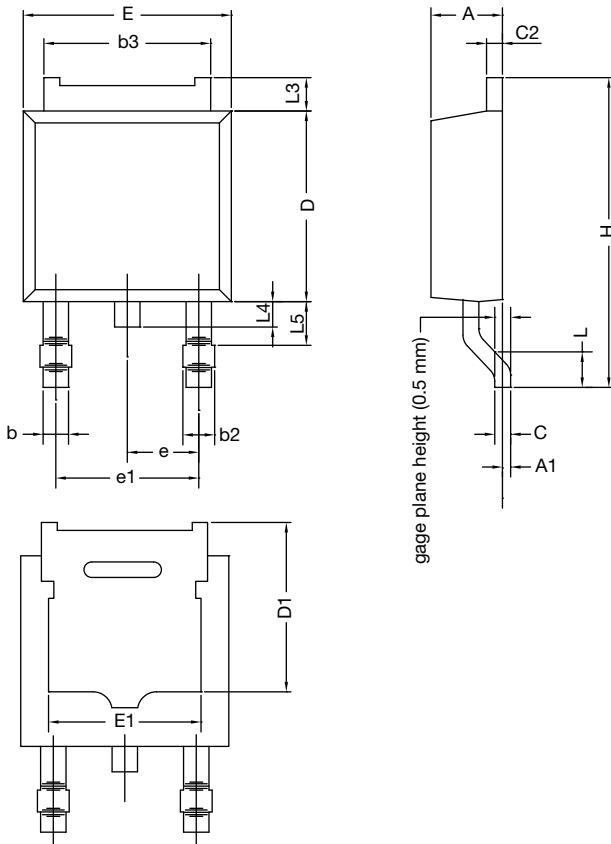


**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?67357](http://www.vishay.com/ppg?67357).



### TO-252AA Case Outline

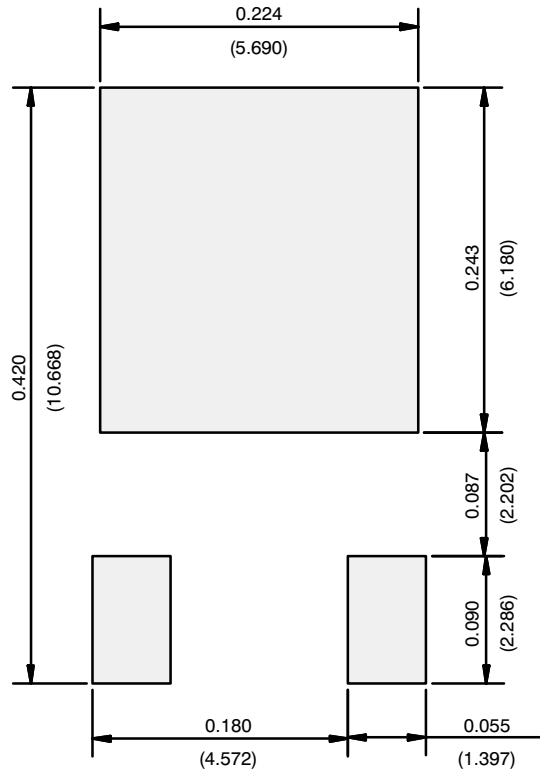


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

**Notes**

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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