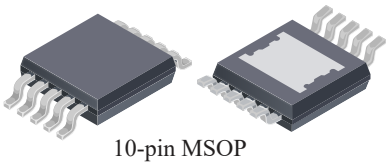
A3909

Dual Full Bridge Motor Driver

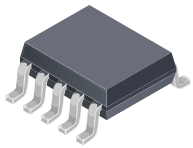
FEATURES AND BENEFITS

- Low $R_{DS(on)}$ outputs
- Drives two DC motors or single stepper motor
- Low power standby (Sleep) mode with zero current drain
- Thermal shutdown protection
- Parallel operation option for 1.8 A, single DC motor
- Overcurrent protection:
  - Output to supply short
  - Output to GND short
  - Output load short

PACKAGES:



10-pin MSOP
with exposed thermal pad
(LY package)



10-pin SSOP
(LN package)

Not to scale

DESCRIPTION

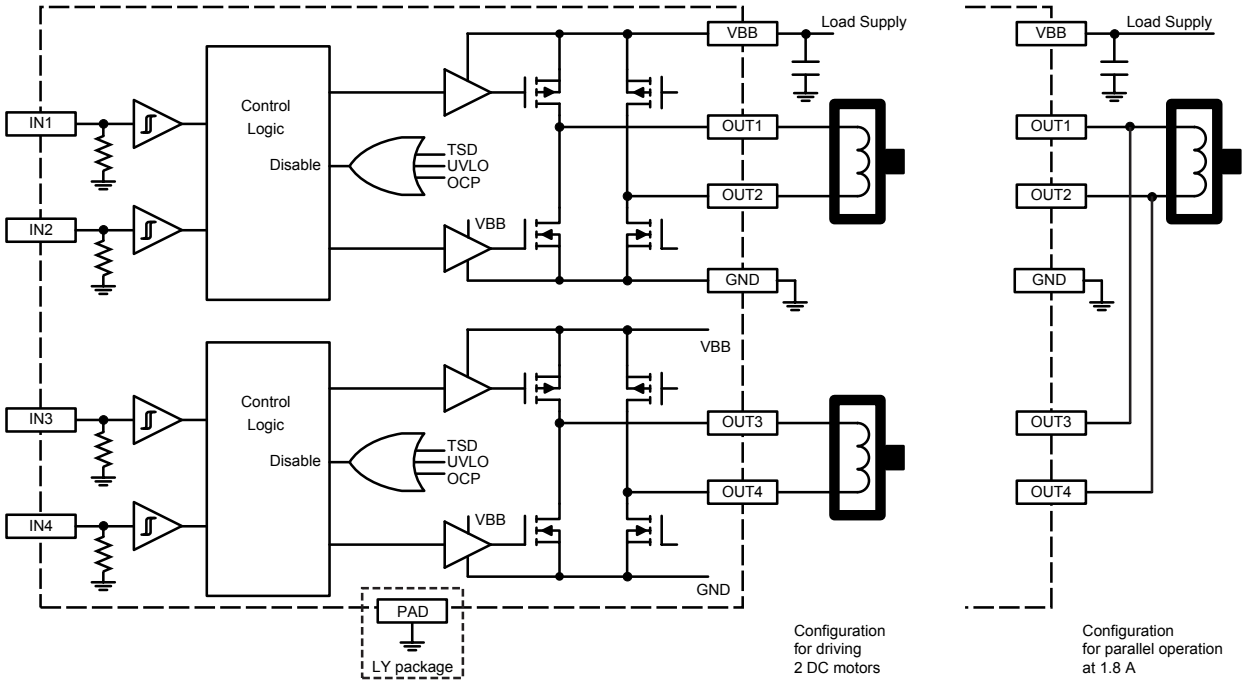
The A3909 is a dual full bridge motor driver, designed for 12 V medium power applications. The outputs are rated for operation through a power supply range of 4 to 18 V, and capable of up to 1 A per phase.

Paralleling the outputs is possible for higher amperage single DC motor applications.

The four inputs (IN1 to IN4) can control DC motors in forward, reverse, brake, and coast modes, or a bipolar stepper motor in full- and half-step modes.

The A3909 is supplied in a 10-pin MSOP package with exposed thermal pad (suffix LY) and a 10-pin SSOP (suffix LN) for wave solder applications. Both packages are lead (Pb) free with 100% matte-tin leadframe plating.

Functional Block Diagram



SELECTION GUIDE

Part Number	Package	Packing
A3909GLNTR-T*	10-pin SSOP	3000 pieces per 13-in. reel
A3909GLYTR-T	10-pin MSOP with exposed thermal pad	4000 pieces per 13-in. reel

*Contact Allegro Sales for availability of this package option.

ABSOLUTE MAXIMUM RATINGS

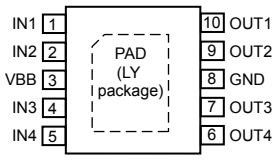
Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		18	V
Logic Input Voltage Range	V_{IN}		–0.3 to 6	V
Output Current	I_{OUT}		1	A
Output Voltage	V_{OUT}		–0.3 to V_{BB} + 1	V
Operating Ambient Temperature	T_A	G temperature range	–40 to 105	°C
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LN package (estimated), on 1-layer PCB with copper limited to pin area	130	°C/W
		LY package, on 2-layer PCB with 2.260 in.^{2} of copper area each side	48	°C/W

*Additional thermal information available on the Allegro website.

Pinout Diagram



LN and LY packages

Terminal List Table

Number	Name	Function
1	IN1	Logic input
2	IN2	Logic input
3	VBB	Input supply
4	IN3	Logic input
5	IN4	Logic input
6	OUT4	Motor terminal
7	OUT3	Motor terminal
8	GND	Ground
9	OUT2	Motor terminal
10	OUT1	Motor terminal
–	PAD	(LY package) Exposed thermal pad

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ELECTRICAL CHARACTERISTICS*: Valid at T_A = 25°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBB Voltage Range	V_{BB}		4	–	18	V
VBB Supply Current	I_{BB}		–	4	8	mA
		Standby Mode	–	<1	10	µA
Total Driver On-Resistance (Sink + Source)	$R_{DS(on)tot}$	I = 1 A, T_J = 25°C, V_{BB} = 12 V	–	1.6	2	Ω
		I = 1 A, T_J = 25°C, V_{BB} = 4 V	–	2.7	3.5	Ω
Source Driver On-Resistance	$R_{DS(on)src}$	I = 1 A, T_J = 25°C, V_{BB} = 12 V	–	1.12	–	Ω
Sink Driver On-Resistance	$R_{DS(on)snk}$	I = 1 A, T_J = 25°C, V_{BB} = 12 V	–	0.48	–	Ω
Input Logic Low Level	$V_{IL(Standby)}$	All inputs low	–	–	0.4	V
Input Logic Low Level	V_{IL}		–	–	0.8	V
Input Logic High Level	V_{IH}		2	–	–	V
Input Hysteresis	V_{HYS}		100	300	500	mV
Logic Input Current	I_{IN}	V_{IN} = 5 V (Pull down = 50 kΩ)	–	100	150	µA
VBB UVLO	V_{BBUVLO}	V_{BB} rising	–	3.6	3.95	V
VBB UVLO Hysteresis	V_{BBHYS}		100	300	500	mV
Standby Timer	t_{STB}	IN1 = IN2 = IN3 = IN4 < $V_{IL(Standby)}$	–	1	1.5	ms
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	150	165	180	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	20	–	°C

*Specified limits are tested at a single temperature and assured through operating temperature range by design and characterization.

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Table 1: Motor Operation Truth Table

STEPPER MOTOR									
IN1	**IN2**	**IN3**	**IN4**	**OUT1**	**OUT2**	**OUT3**	**OUT4**	**Function**	
0	0	0	0	Off	Off	Off	Off	Sleep Mode	Sleep Mode
1	0	1	0	H	L	H	L	Step 1	Step 1
0	0	1	0	Off	Off	H	L	–	Step 2
0	1	1	0	L	H	H	L	Step 2	Step 3
0	1	0	0	L	H	Off	Off	–	Step 4
0	1	0	1	L	H	L	H	Step 3	Step 5
0	0	0	1	Off	Off	L	H	–	Step 6
1	0	0	1	H	L	L	H	Step 4	Step 7
1	0	0	0	H	L	Off	Off	–	Step 8
DC MOTORS (DUAL)									
IN1 or IN3		**IN2 or IN4**		**OUT1**	**OUT2**	**OUT3**	**OUT4**	**Function**	
0		0		Off	Off	Off	Off	High Impedance (Sleep Mode) / Coast	
1		0		H	L	H	L	Forward	
0		1		L	H	L	H	Reverse	
1		1		L	L	L	L	Brake	
DC MOTOR (SINGLE, PARALLELED)									
IN1 or IN3		**IN2 or IN4**		**OUT1**	**OUT2**	**OUT3**	**OUT4**	**Function**	
0		0		Off	Off	Off	Off	High Impedance (Sleep Mode) / Coast	
1		0		H	L	H	L	Forward	
0		1		L	H	L	H	Reverse	
1		1		L	L	L	L	Brake	
DC MOTOR (EXTERNAL PWM)									
IN1 or IN3		**IN2 or IN4**		**OUT1**	**OUT2**	**OUT3**	**OUT4**	**Function**	
1		0		H	L	H	L	Forward	
0		0		Off	Off	Off	Off	Fast Decay	
0		1		L	H	L	H	Reverse	
0		0		Off	Off	Off	Off	Fast Decay	
1		0		H	L	H	L	Forward	
1		1		L	L	L	L	Slow Decay	
0		1		L	H	L	H	Reverse	
1		1		L	L	L	L	Slow Decay	

NOTE: 0 = logic low with $V_{INx} < V_{IN(0)}$(max), 1 = logic high with $V_{INx} > V_{IN(1)}$(min), H = voltage high, source driver on, L = voltage low, sink driver on

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FUNCTIONAL DESCRIPTION

Device Operation

The 3909 is designed to operate two DC motors or a single stepper motor. The outputs are PMOS source drivers combined with low $R_{DS(on)}$ DMOS sink drivers.

Protection circuitry includes internal thermal shutdown, protection against shorted loads, and against outputs shorted to GND or supply. Undervoltage lockout prevents damage by keeping the outputs off until the driver has enough voltage to operate normally.

A low power standby (Sleep) mode is activated when all inputs are low for longer than 1 ms. Sleep mode disables all of the circuitry making the IC ideal for battery operated applications.

Overcurrent Protection (OCP)

The A3909 is protected against accidental shorts or motor outputs to ground and supply, as well as a shorted load condition. For the source drivers, the current is monitored after the MOSFET is turned on. If the current exceeds 1.8 A for longer than 2 µs, then a fault condition is asserted. The sink driver utilizes a drain-to-source voltage monitor. If the voltage exceeds 2 V for longer than 2 µs, the fault condition is asserted.

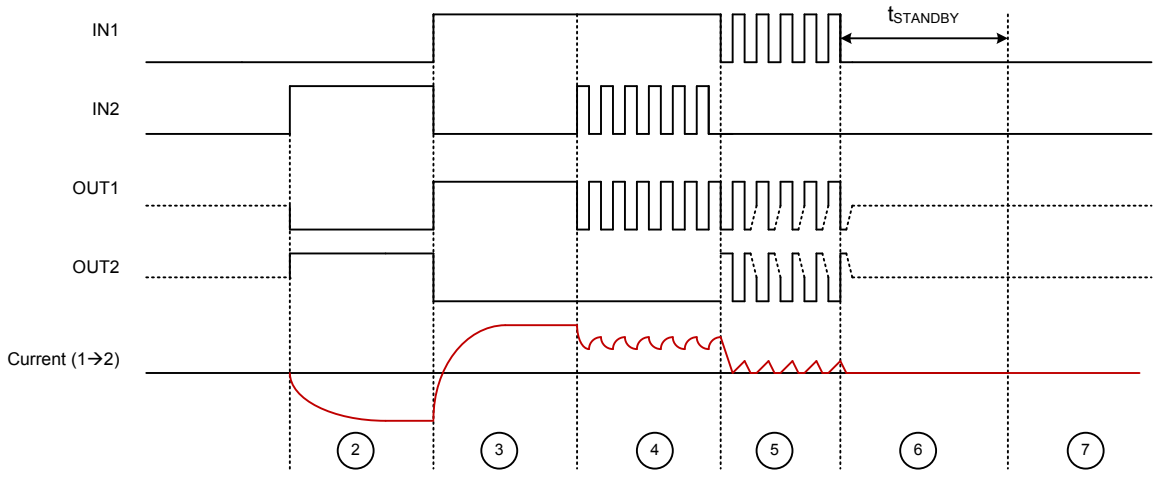
When a fault occurs, the IC immediately disables both sides of the full bridge where the fault occurred. The full bridge input commands will be ignored for a 2 ms period before being allowed to retry. Each channel has independent overcurrent protection.

During OCP events, the absolute ratings may be exceeded for a short period of time before the outputs are disabled.

Thermal Shutdown

If the die temperature increases to T_{JTSD}, then all outputs are disabled until the internal temperature falls below a hysteresis level, T_{TSDHYS}, of 20°C. Internal UVLO is detected on VBB to prevent output drivers from turning on when below the UVLO threshold.

DC Motor Timing Diagram



1) Low power standby (Sleep) mode (I_{BB} = 0)
2) On, reverse – 100% duty cycle
3) On, forward – 100% duty cycle
4) Slow decay PWM
5) Fast decay PWM
6) Coast
7) Low power standby (Sleep) mode after t_{STANBY} (I_{BB} = 0)

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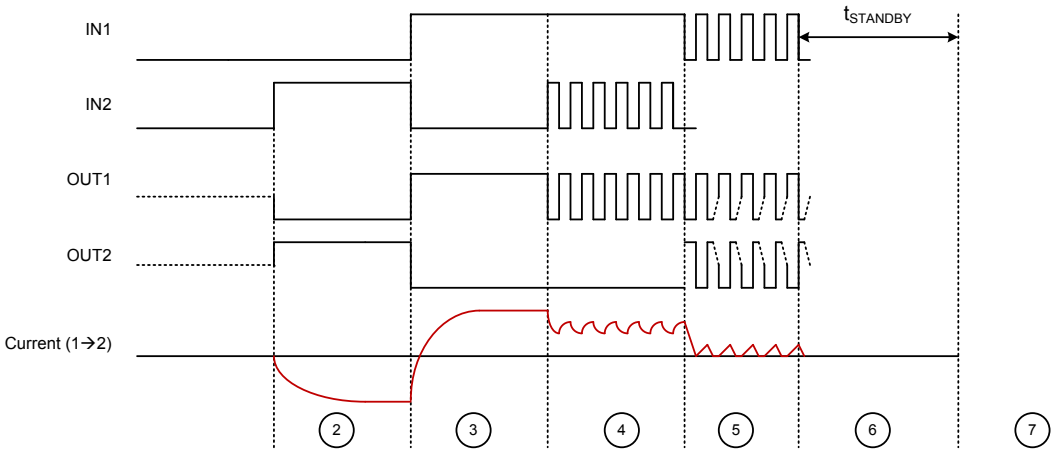
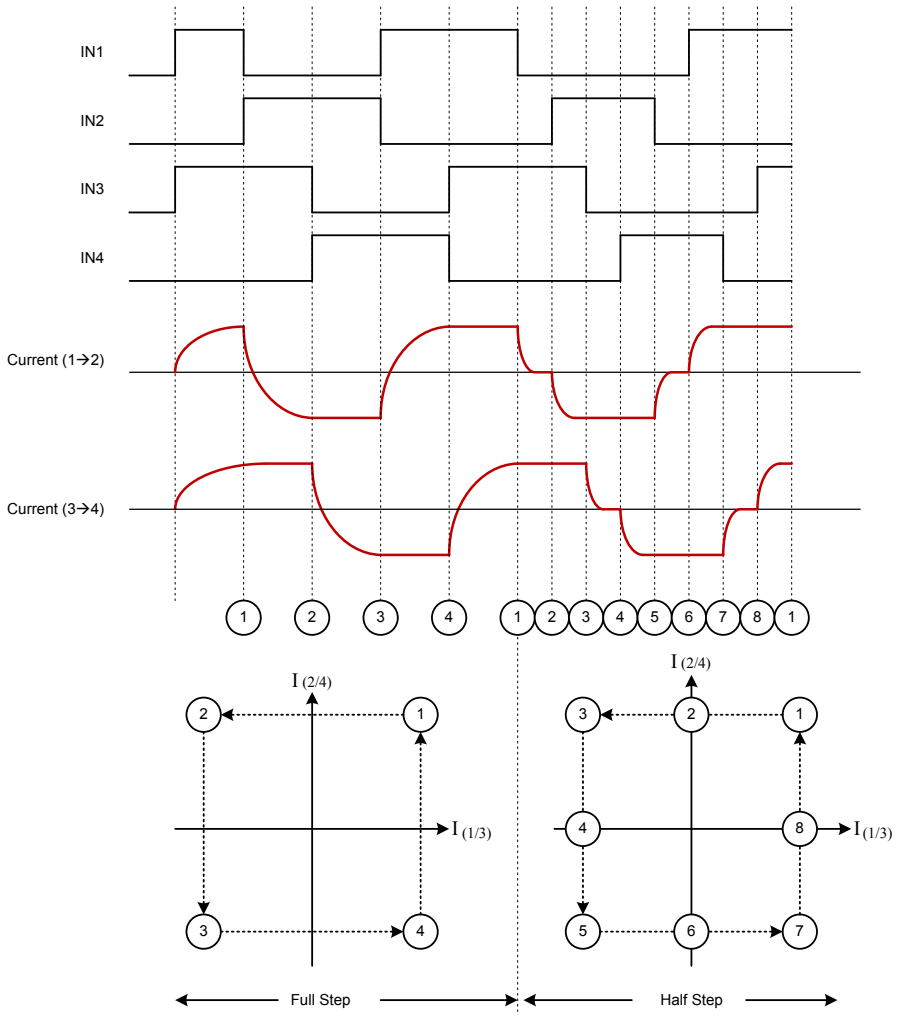
Stepper Motor Timing Diagram





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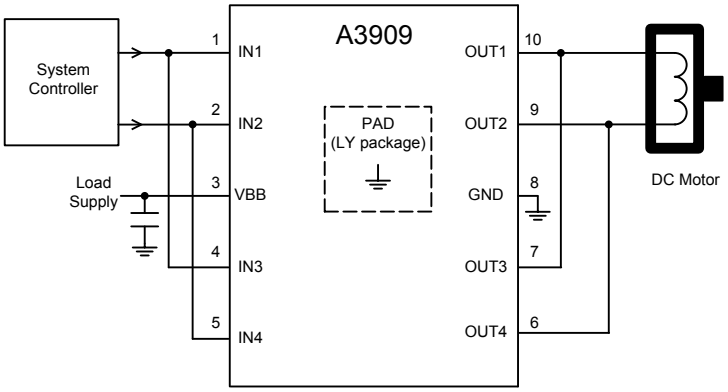
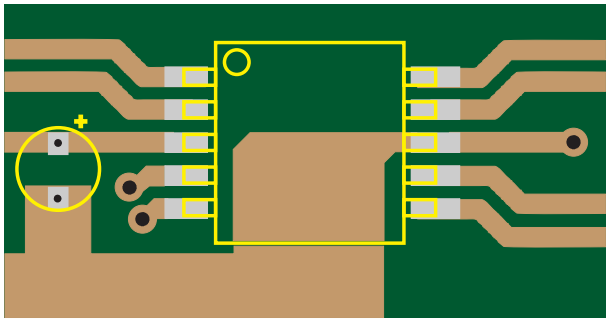
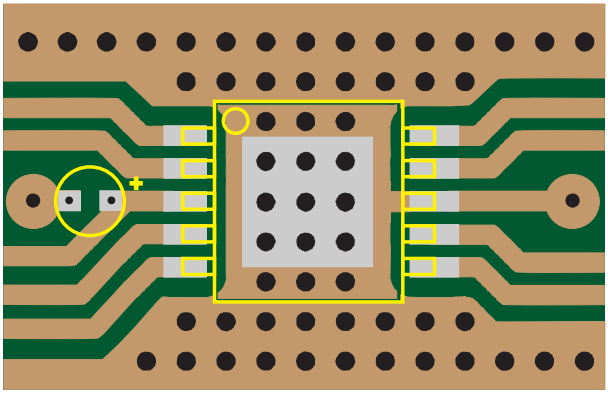
APPLICATION INFORMATION



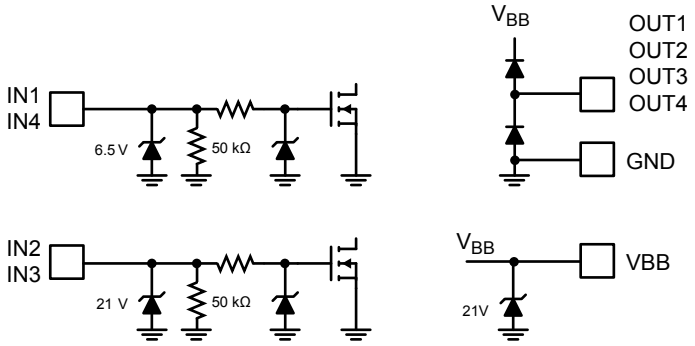
Configuration for parallel operation with 1.8 A output current capability



LN package board



LY package board via layout for thermal dissipation



Input Output Pin Structures

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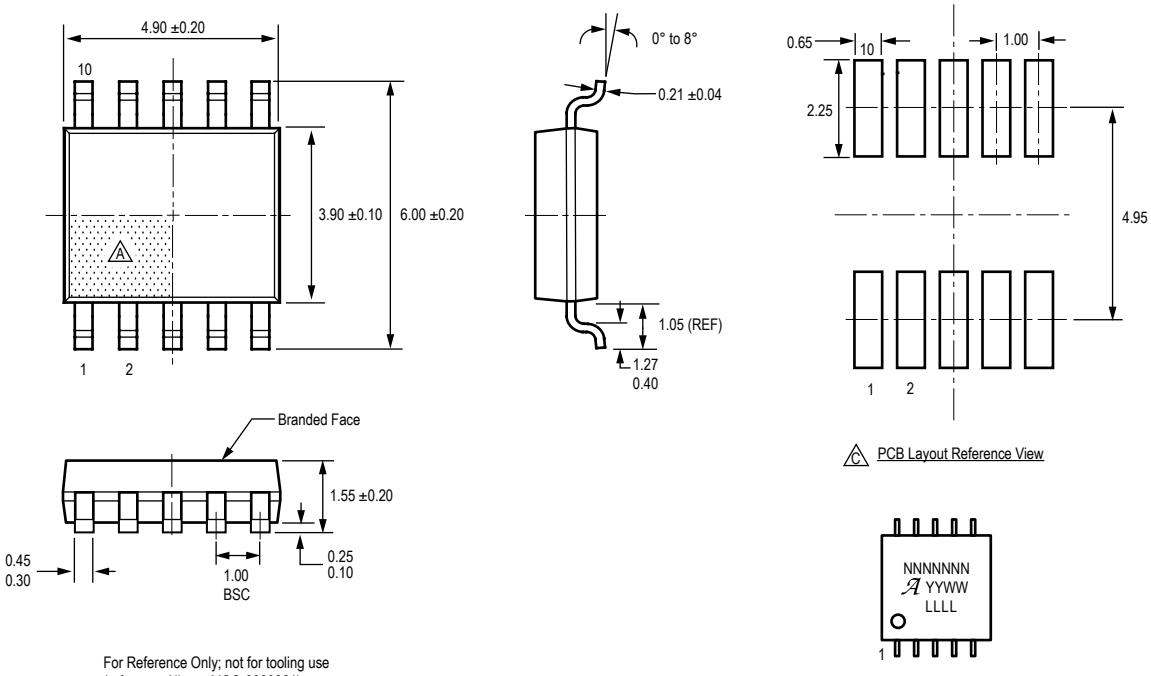
Package LN, 10-Pin SSOP



C PCB Layout Reference View

For Reference Only; not for tooling use
(reference Allegro MCO-0000061)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Branding scale and appearance at supplier discretion

C Reference land pattern layout. All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias near the pin lands can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-7)

B Standard Branding Reference View

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

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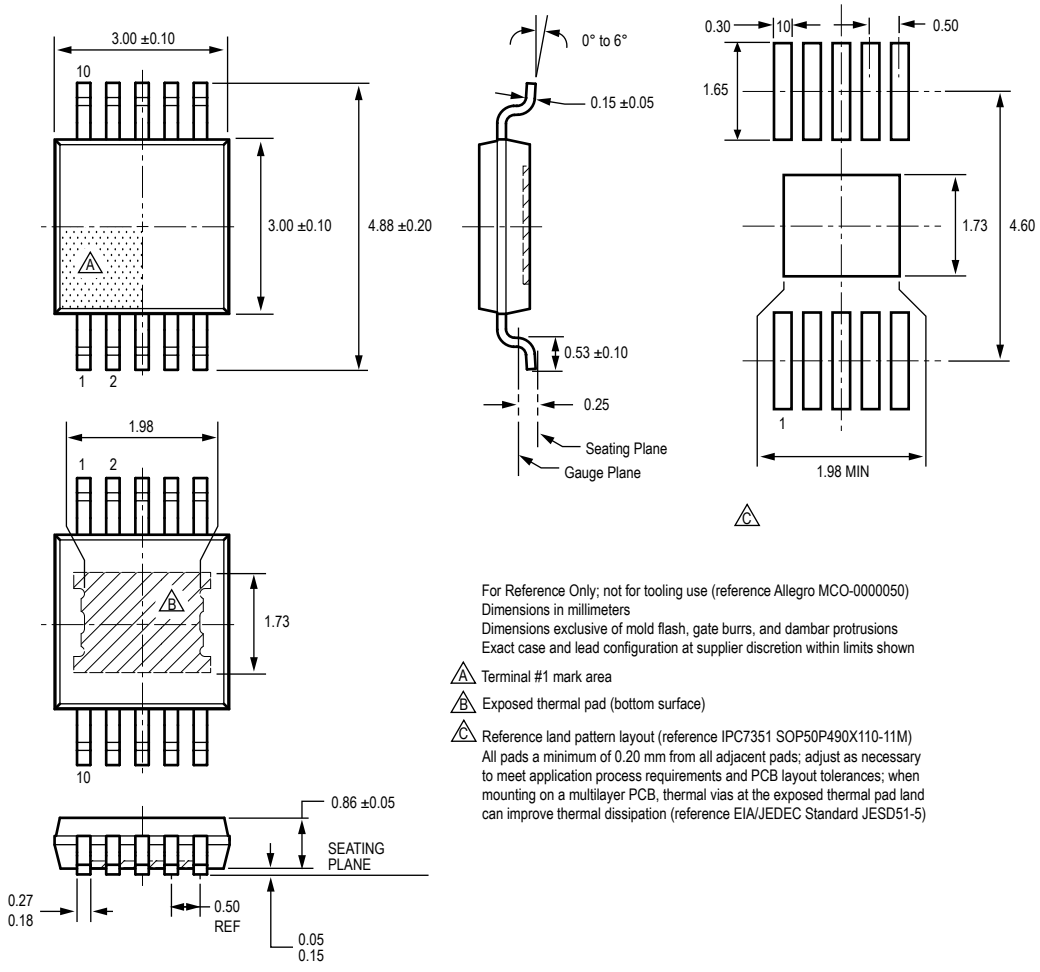
Package LY, 10-Pin MSOP
With Exposed Thermal Pad



For Reference Only; not for tooling use (reference Allegro MCO-0000050)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP50P490X110-11M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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Revision History

Number	Date	Description
–	November 15, 2018	Corrected Output Current units in Absolute Maximum Ratings table (page 2)
1	December 6, 2019	Minor editorial updates
2	January 20, 2021	Updated Package Outline Drawing reference numbers (pages 8-9).
3	November 7, 2022	Updated Selection Guide (page 2)

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