Title	***Reference Design Report for a 30 W Single Output Flyback Converter Using LinkSwitch™-HP LNK6766E***
Specification	90 VAC – 265 VAC Input; 12 V, 2.5 A Output
Application	Adapter
Author	Applications Engineering Department
Document Number	RDR-313
Date	September 14, 2012
Revision	1.2

Summary and Features

- Primary side regulated isolated flyback converter with ±5% regulation.
- 132 kHz switching frequency for small transformer and output filter size
- Full load continuous conduction mode operation for improved efficiency and reduced output capacitor ripple currents
- Multimode operation maximizes efficiency over full load range
- Below 30 mW power consumption with 230 VAC.
- Extensive protection features including OVP, OTP, brown-in/out, line overvoltage, and lost-regulation (auto-restart)
- Meets EN-550022 and CISPR-22 Class B conducted EMI with 5 dB margin.
- Meets IEC61000-4-5, 1 kV / 2 kV surge.

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This report describes a universal input, 12 V, 30 W isolated flyback converter employing LNK6766E from the LinkSwitch-HP family of ICs. It contains the complete specification of the power supply, a detailed circuit diagram, the entire bill of materials required to build the supply, extensive documentation of the power transformer, along with test data and waveform plots of the most important electrical waveforms.

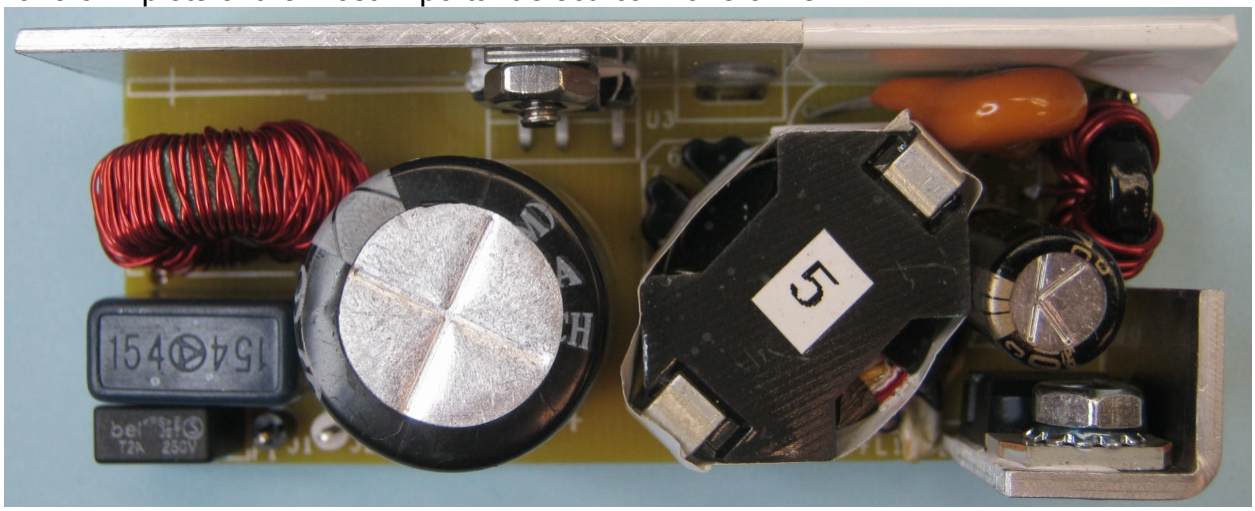

Figure 1 – Prototype Top View.

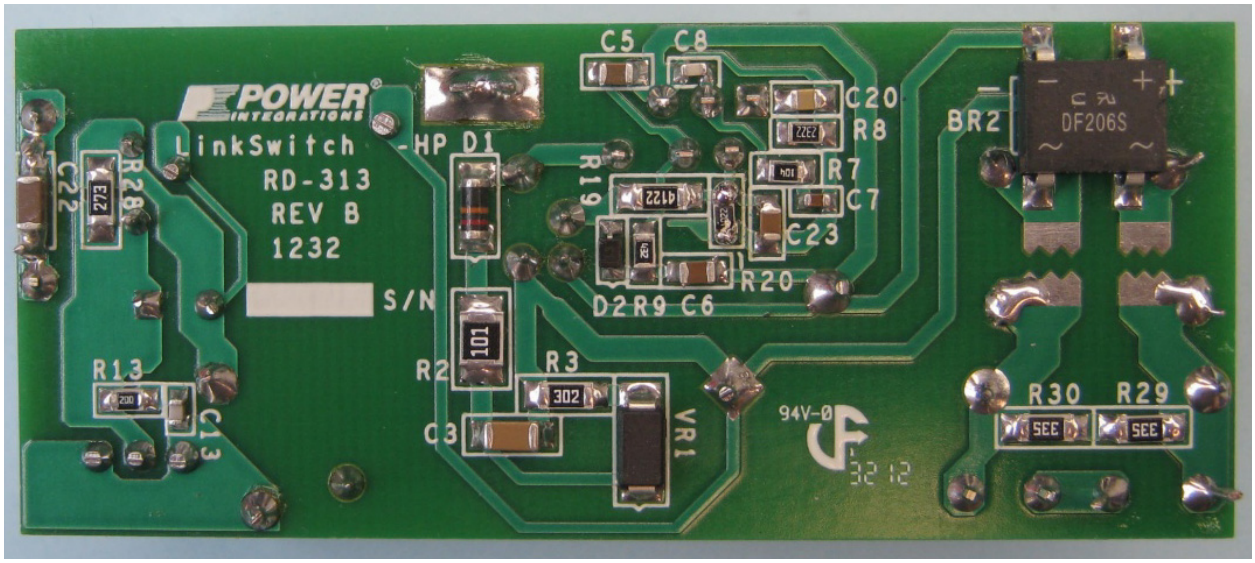

Figure 2 – Prototype Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
Input Power at standby				30	mW	230 VAC
Output						
Output Voltage	V_{OUT}	11.4	12	12.6	V	
Output Ripple Voltage	V_{RIPPLE}			120	mVpp	20 MHz bandwidth with steady state load
Output Current	I_{OUT}	0.0		2.5	A	
Overshoot Voltage	$V_{OVERSHOOT}$			18	V	Standby Load and AC input cycling
Total Output Power						
Continuous Output Power	P_{OUT}	0		30	W	
Efficiency						
Full load efficiency	η	85			%	90 VAC and Full Load
Environmental						
Conducted EMI		Meets EN55022B				5dB Margin
Safety		Designed to meet IEC950, UL1950 Class II				
Surge	**DM**	1			kV	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
	CM	2				
ESD	**Air**	-15		15	kV	Air discharge onto output connector
	Contact	-8		8	kV	Contact discharge onto output connector
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level

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3 Schematic

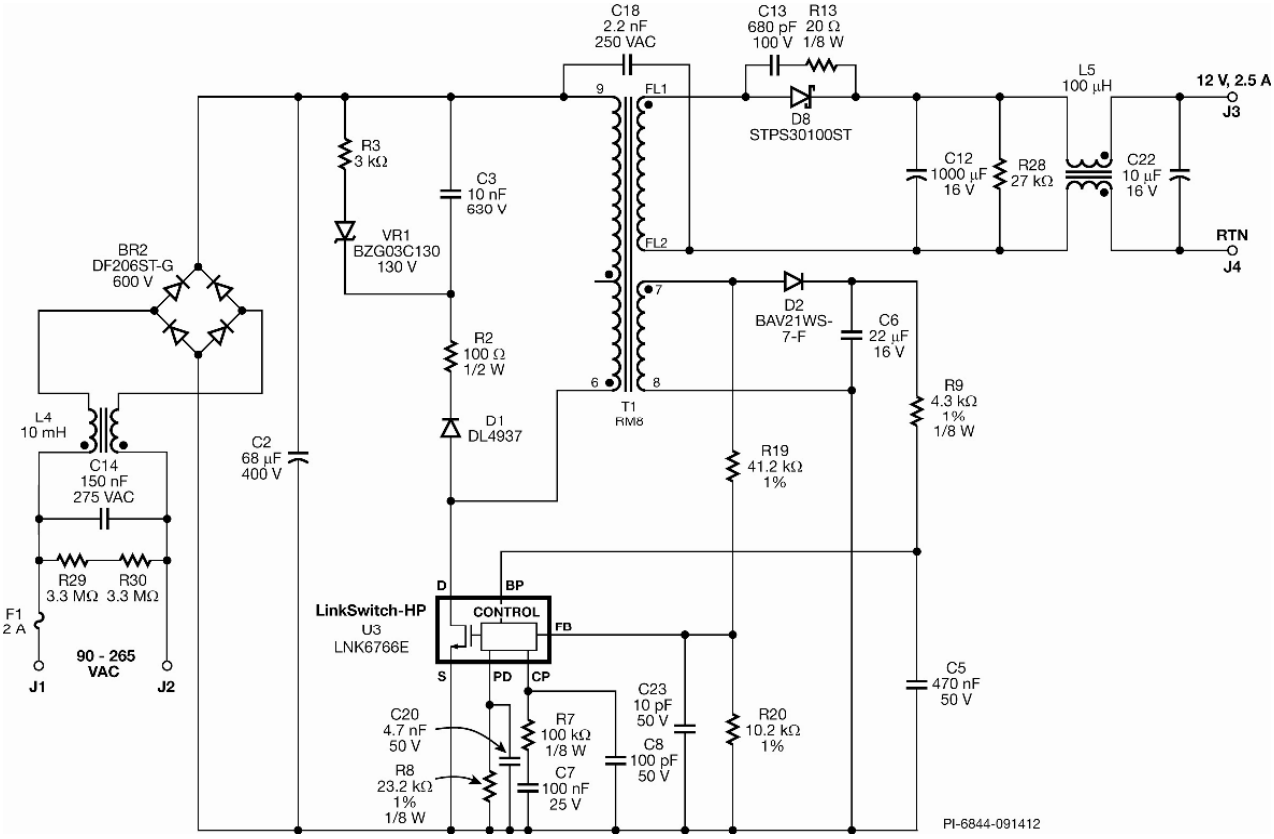

Figure 3 – Schematic.

4 Circuit Description

4.1 Input Rectification and Filtering

Bridge rectifier BR1 rectifies the AC input which is filtered by C2. Inductor L4, C14 and C2 are used to attenuate differential mode and common mode conducted EMI. Shielding techniques were used in the construction of transformer T1 to reduce common mode EMI displacement currents. This filter arrangement, the shield techniques together with the IC's frequency jitter function provide excellent EMI performance for this solution with a Y-capacitor and a primary-side RZCD clamp circuit.

4.2 LinkSwitch-HP Primary

The LNK6766E device (U3) integrates an oscillator, an error amplifier and multi-mode control circuit, start-up and protection circuitry and a high-voltage power MOSFET all in one monolithic IC.

One side of the power transformer is connected to the high-voltage bus and the other side is connected to the DRAIN (D) pin of U3. At the start of a switching cycle, the controller turns the power MOSFET on and current ramps up in the primary winding, which stores energy in the core of the transformer. When that current reaches the limit threshold which is set by the output of internal error amplifier (COMPENSATION (CP) pin voltage), the controller turns the power MOSFET off. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy then induces a voltage across the secondary winding, which forward biases the output diode, and the stored energy is delivered to the output capacitor.

Capacitor C5 (0.47 μF) connected to the BYPASS (BP) pin sets overvoltage protection (OVP) and over-temperature protection (OTP) to latching and lost regulation protection to automatic restart attempts (auto-restart) after a given off-period (typ. 1500 ms).

4.3 Primary RZCD Clamp

Diode D1, VR1, C3, R2 and R3 form a RZCD snubber that is used to limit the voltage stress across the LinkSwitch-HP. Peak drain voltage is therefore limited to typically less than 540 V at 265 VAC – providing significant margin to the 650 V drain voltage (BV_{DSS}). Zener VR1 prevents the capacitor C3 from fully discharging every switching cycle to reduce power consumption during standby operation.

Diode D1, R2, VR1, C3, R5 and R6 form a RCD snubber that is used to limit the voltage stress across the LinkSwitch-HP. Peak drain voltage is therefore limited to typically less than 580 V at 265 VAC – providing significant margin to the 700 V drain voltage (BV_{DSS}).

4.4 Output Rectification

Output rectification of 12 V output is provided by diode D8 and filtering is provided by capacitor C12, C21 and inductor L5 and C22. The snubber formed by R13 and C13 provides high frequency filtering for improved EMI.

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4.5 External Current Limit Setting-

The maximum cycle-by-cycle current limit is set by the resistor R8 connected to the PROGRAM (PD) pin. A 23.2 kΩ resistor in the design sets the maximum current limit to 60% of the LNK6766E's default current limit.

4.6 Feedback and Compensation Network

The output voltage is sensed through bias winding and resistor divider (R19 and R20) during the flyback period. The sensed output voltage is compared to the FEEDBACK (FB) pin threshold to regulate the output or to stop switching in case an overvoltage condition is detected (OVP). This primary side regulation solution not only reduces the system cost, but also improves the lifetime of the system as no optocoupler (which reduces the life of the power supply significantly) is necessary for power suppliers designed with LinkSwitch-HP.

Voltage divider R19 and R20 is also used to indirectly monitor the bus voltage during the integrated power MOSFET on-time. At start-up the IC enables switching only if the bus voltage has typically reached 100 V (brown-in threshold). If the bus voltage drops for instance during a brown-out condition below typically 40 V the device stops switching (brown-out protection). In case the bus voltage reaches excessive levels (e.g. caused by line surge) the device stops switching. Additionally the cycle-by-cycle current limit is compensated over line to limit the available overload power. See the device data sheet for further details.

The voltage sensed at the FB pin produces a control voltage at the CP pin. Resistor R7 and capacitors C7 and C8 are used for control loop compensation. The operating peak primary current and the operating switching frequency are determined by the CP pin voltage.

5 PCB Layout

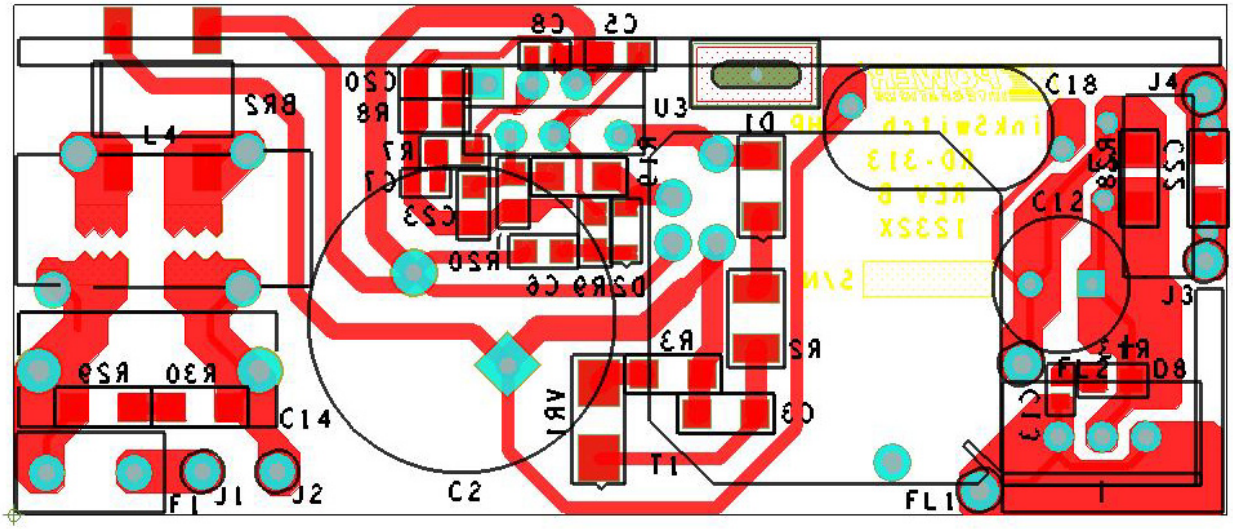

Figure 4 – PCB Top/Bottom Side 2.76” (70.1 mm) x 1.16” (29.4 mm).

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR2	600 V, 2 A, Bridge Rectifier, SMD, DFS	DF206ST-G	Comchip
2	1	C2	68 μF, 400 V, Electrolytic, (18 x 20)	ERT686M2GL20RR	Samxon
3	1	C3	10 nF, 630 V, Ceramic, X7R, 1206	C1206C103KBRACTU	Kemet
4	1	C5	470 nF, 50 V, Ceramic, X7R, 0805	GRM21BR71H474KA88L	Murata
5	1	C6	22 μF, 16 V, Ceramic, X7R, 0805	C2012X5R1C226K	TDK
6	1	C7	100 nF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KNXAO	Vishay
7	1	C8	100 pF 50 V, Ceramic, NPO, 0603	CC0603JRNPO9BN101	Yageo
8	1	C12	1000 μF, 16 V, Electrolytic, Low ESR, 8 x 20)	16MCZ100M8X20	Rubycon
9	1	C13	680 pF 100 V, Ceramic, NPO, 0603	CGA3E2C0G2A681J	TDK
10	1	C14	150 nF, 275 VAC, Film, X2	LE154-M	OKAYA
11	1	C18	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
12	1	C20	4.7 nF, 50 V, Ceramic, X7R, 0805	08055C472KAT2A	AVX
13	1	C22	10 μF, 16 V, Ceramic, X7R, 1206	C3216X7R1C106M	TDK
14	1	C23	10 pF, 50 V, Ceramic, NPO, 0805	C0805C100J5GACTU	Kemet
15	1	D1	600 V, 1 A, Rectifier, Fast Recovery, MELF (DL-41)	DL4937-13-F	Diodes, Inc.
16	1	D2	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
17	1	D8	100 V, 30 A, Schottky, TO-220AB	STPS30100ST	ST Micro
18	1	F1	2 A, 250 V, Slow, Long Time Lag, RST	RST 2	Belfuse
19	2	FL1 FL2	PCB Terminal Hole, #22 AWG	N/A	N/A
20	2	J1 J3	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
21	2	J2 J4	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
22	1	L4	Common Mode Choke Toroidal Common Mode Choke Assembly	P/N T22148-902S SNX-R1655	Fontaine Tech Santronics USA
23	1	L5	Core, K5, Toroidal, 10 mm O.D. x 4 mm Th x 6 mm I.D. Common Mode Choke Assembly	K5B T 10*4*6 SNX-1654	Kingcore TWN Santronics USA
24	1	R2	100 Ω, 5%, 1/2 W, Thick Film, 1210	ERJ-14YJ101U	Panasonic
25	1	R3	3 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ302V	Panasonic
26	1	R7	100 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
27	1	R8	23.2 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2322V	Panasonic
28	1	R9	4.3 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ432V	Panasonic
29	1	R13	20 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ200V	Panasonic
30	1	R19	41.2 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF4122V	Panasonic
31	1	R20	10.2 kΩ, 1%, 1/4 W, Thick Film, 0805	ERJ-6ENF1022V	Panasonic
32	1	R28	27 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ273V	Panasonic
33	2	R29 R30	3.3 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ335V	Panasonic
34	1	T1	Bobbin, RM8, Vertical, 12 pins Transformer Assembly	RM8/12/1 SNX-1653	Schwartzpunkt Santronics USA
35	1	TE1	Terminal, Eyelet, Tin Plated Brass, Zierick PN 190	190	Zierick
36	1	U3	LinkSwitch-HP, eSIP-7F	LNK6766E	Power Integrations
37	1	VR1	130 V, 1.25 W, 5%, DO214AC (SMA)	BZG03C130TR	Vishay

7 Transformer Design Spreadsheet

ACDC_LinkSwitch-HP_051612; Rev.0.13; Copyright Power Integrations 2012	INPUT	OUTPUT	UNIT	LinkSwitch-HP Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES				
VACMIN	90	90	V	Minimum AC Input Voltage
VACMAX	265	265	V	Maximum AC Input Voltage
fL	50	50	Hz	AC Mains Frequency
VO	12	12	V	Output Voltage (main)
PO	30	30	W	Output Power
n	0.84	0.84		Efficiency Estimate
Z	0.50	0.50		Loss Allocation Factor
VB	10	10	V	Bias Voltage
tC	3	3	ms	Bridge Rectifier Conduction Time Estimate
CIN	68	68	uF	Input Filter Capacitor
ENTER LINKSWITCH-HP VARIABLES				
LinkSwitch-HP	**LNK6766E**	**LNK6766E**		Selected LinkSwitch-HP
ILIMITMIN		1.814	A	Minimum Current limit
ILIMITMAX		2.087	A	Maximum current limit
KI	0.60	0.600	A	Current limit reduction factor
ILIMITMIN_EXT		1.088	A	External Minimum Current limit
ILIMITMAX_EXT		1.252	A	External Maximum current limit
fS		132000	Hz	LinkSwitch-HP Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin		124000	Hz	LinkSwitch-HP Minimum Switching Frequency
fSmax		140000	Hz	LinkSwitch-HP Maximum Switching Frequency
KP	0.59	0.59		Ripple to Peak Current Ratio (0.4 < KP < 6.0)
VOR	100	100.00	V	Reflected Output Voltage
Voltage Sense				
VUVON	100	100.00	V	Undervoltage turn on
VUVOFF		42.14	V	Undervoltage turn off
VOV		446.44	V	Overvoltage threshold
FMAX_FULL_LOAD		139135	Hz	Maximum switching frequency at full load
FMIN_FULL_LOAD		123234	Hz	Minimum switching frequency at full load
TSAMPLE_FULL_LOAD		3.51	us	Minimum available Diode conduction time at full load. This should be greater than 2.5 us
TSAMPLE_LIGHT_LOAD		1.76	us	Minimum available Diode conduction time at light load. This should be greater than 1.11 us
Rpd		23.20	k-ohm	Program delay Resistor
Cpd	4.7	4.70	nF	Program delay Capacitor
Total programmed delay		0.03	sec	Total program delay
VDS	3.64	3.64	V	LinkSwitch-HP on-state Drain to Source Voltage
VD	0.5	0.50	V	Output Winding Diode Forward Voltage Drop
VDB	0.70	0.70	V	Bias Winding Diode Forward Voltage Drop
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Core Type	**RM8**			
Core		#N/A		Selected Core
Custom Core				Enter name of custom core is applicable
AE	0.5200	0.52	cm^2	Core Effective Cross Sectional Area
LE	3.3500	3.35	cm	Core Effective Path Length
AL	2600.0	2600	nH/T^2	Ungapped Core Effective Inductance
BW	9.0	9	mm	Bobbin Physical Winding Width
M	2.00	2.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3.00	3		Number of Primary Layers

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NS	7.00	7		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS				
VMIN	100	100	V	Minimum DC Input Voltage
VMAX	375	375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS				
DMAX		0.51		Maximum Duty Cycle
IAVG		0.36	A	Average Primary Current
IP		0.99	A	Peak Primary Current
IR		0.59	A	Primary Ripple Current
IRMS		0.51	A	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS				
LP_TYP		693	uH	Typical Primary Inductance
LP_TOL	7	7	%	Primary inductance Tolerance
NP		56		Primary Winding Number of Turns
NB		6		Bias Winding Number of Turns
ALG		221	nH/T^2	Gapped Core Effective Inductance
BM		2368	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP		3189	Gauss	Peak Flux Density (BP<3700)
BAC		699	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		1333		Relative Permeability of Ungapped Core
LG		0.27	mm	Gap Length (Lg > 0.1 mm)
BWE		15	mm	Effective Bobbin Width
OD	0.40	0.40	mm	Maximum Primary Wire Diameter including insulation
INS		0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.34	mm	Bare conductor diameter
AWG		28	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		161	Cmils	Bare conductor effective area in circular mils
CMA		313	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
FEEDBACK SENSING SECTION				
RFB1		41.20	k-ohms	Feedback divider upper resistor
RFB2		9.53	k-ohms	Feedback divider lowerr resistor
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)				
Lumped parameters				
ISP		7.96	A	Peak Secondary Current
ISRMS		4.04	A	Secondary RMS Current
IO		2.50	A	Power Supply Output Current
IRIPPLE		3.18	A	Output Capacitor RMS Ripple Current
CMS		809	Cmils	Secondary Bare Conductor minimum circular mils
AWGS		21	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS		0.73	mm	Secondary Minimum Bare Conductor Diameter
ODS		0.71	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS		-0.01	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS				
VDRAIN		605	V	Peak voltage acoss drain to source of Linkswitch-HP
PIVS		59	V	Output Rectifier Maximum Peak Inverse Voltage
PIVB		50	V	Bias Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)				
1st output				
VO1		12	V	Output Voltage
IO1		2.50	A	Output DC Current
PO1		30.00	W	Output Power
VD1		0.5	V	Output Diode Forward Voltage Drop
NS1		7.00		Output Winding Number of Turns

ISRMS1		4.043	A	Output Winding RMS Current
IRIPPLE1		3.18	A	Output Capacitor RMS Ripple Current
PIVS1		59	V	Output Rectifier Maximum Peak Inverse Voltage
CMS1		809	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1		21	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1		0.73	mm	Minimum Bare Conductor Diameter
ODS1		0.71	mm	Maximum Outside Diameter for Triple Insulated Wire

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8 Transformer Specification

8.1 Electrical Diagram

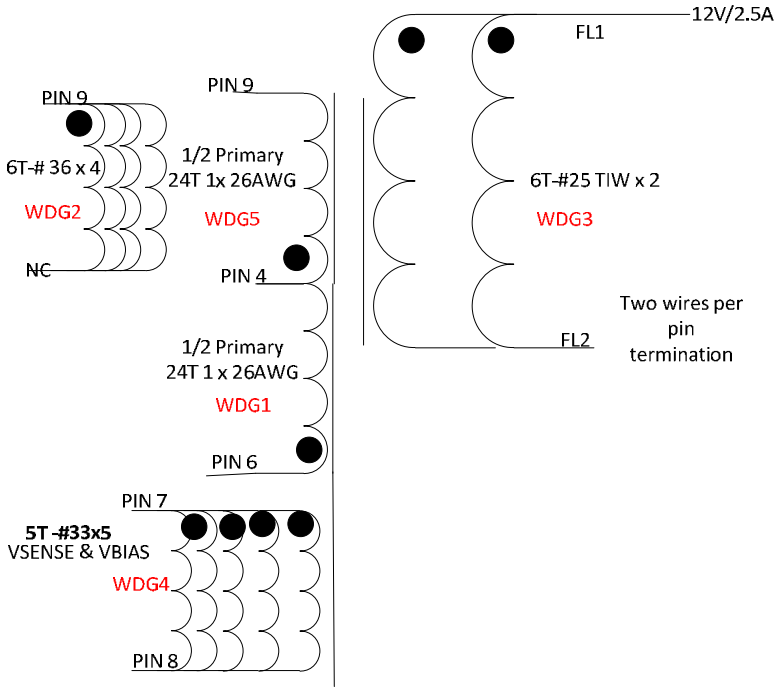


Figure 5 – Transformer Electrical Diagram.

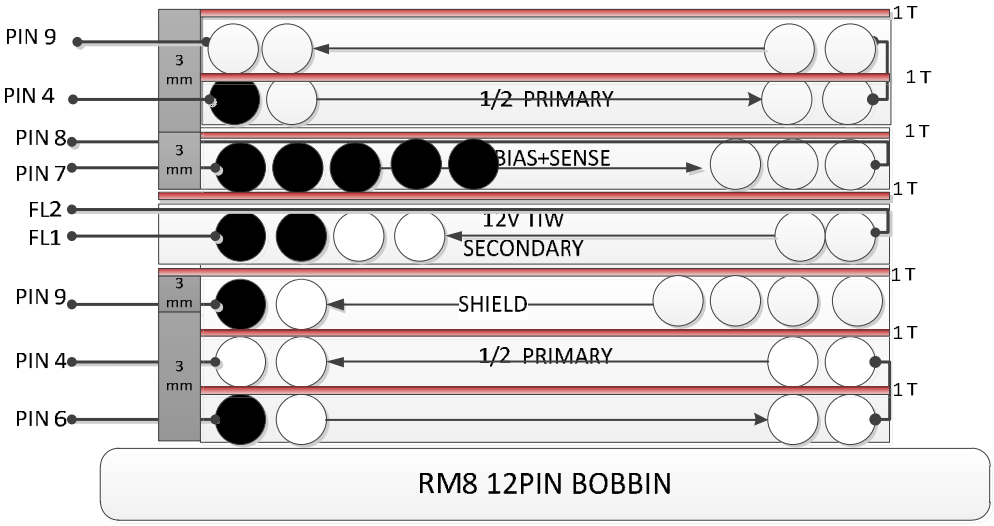
8.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-3 to pins 6-10.	3000 VAC
Primary Inductance	Pins 6-9, all other windings open, measured at 100 kHz, 0.4 $V_{RMS.}$	0.693 mH, ±7%
Resonant Frequency	Pins 6-9, all other windings open.	1400 kHz (Min.)
Primary Leakage Inductance	Pins 6-9, with all other pins shorted, measured at 100 kHz, 0.4 $V_{RMS.}$	15 µH (Max.)

8.3 Materials

Item	Description
[1]	Core: RM8, NC-2H (Nicera) or Equivalent, gapped for ALG of 219 nH/t².
[2]	Bobbin: Vertical 12 pin.
[3]	Magnet Wire: #26 AWG.
[4]	Magnet Wire: #33, #36 AWG.
[5]	TIW Wire: #25 AWG.
[5]	Tape: 3M 1298 Polyester Film, 2.0 mils thick, 9.8 mm wide.

8.4 Transformer Build Diagram



Electrical Test Specifications

Parameter	Condition	Spec
Electrical Strength, VAC	60 Hz 1 second, from pins 5-9 to pins 1,2,3,4,10-12.	3000
Nominal Primary Inductance, µH	Measured at 1 V pk-pk, typical switching frequency, between pin 6 to pin 9, with all other Windings open.	693
Tolerance, ±%	Tolerance of Primary Inductance	10.0
Maximum Primary Leakage, µH	Measured between Pin 6 to Pin 9, with all other Windings shorted.	15

Figure 6 – Transformer Build Diagram.

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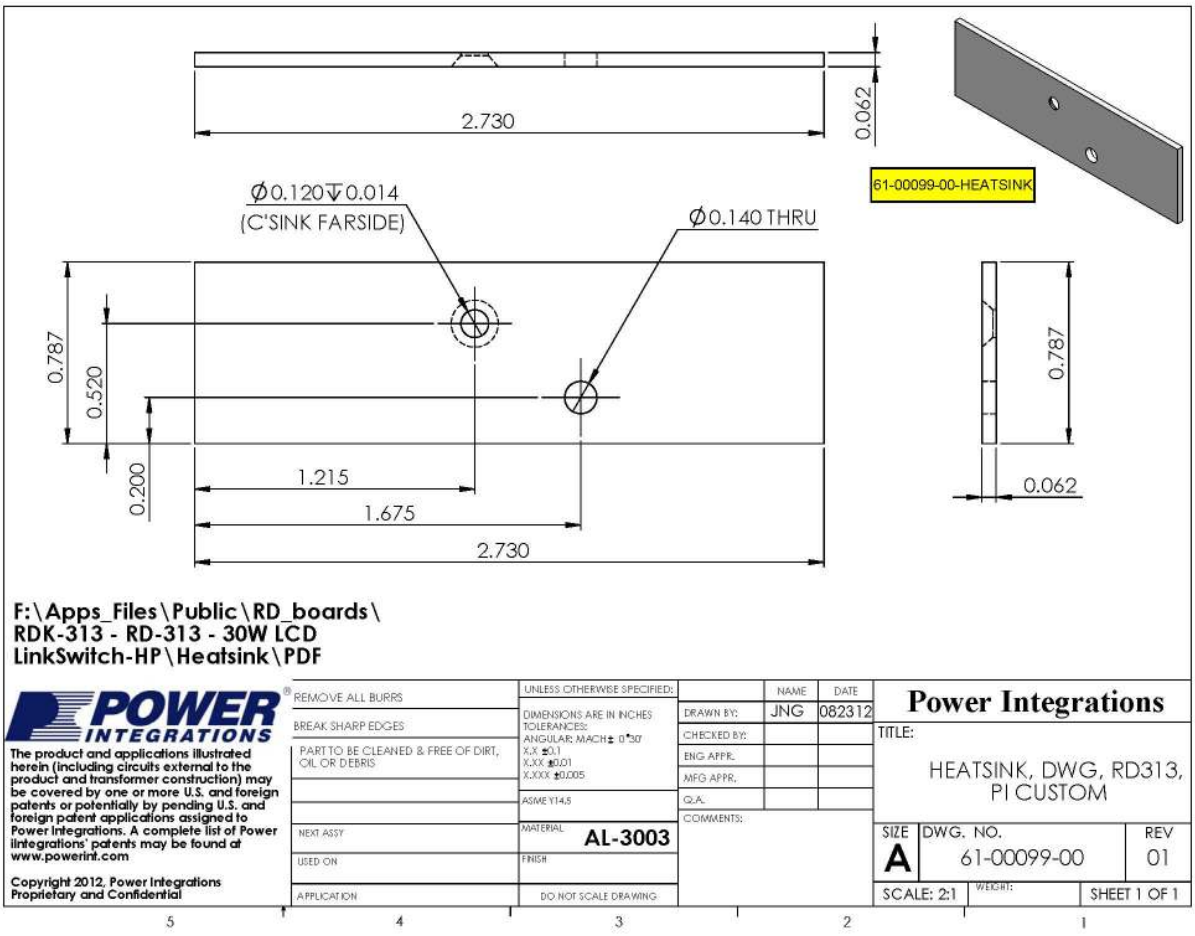
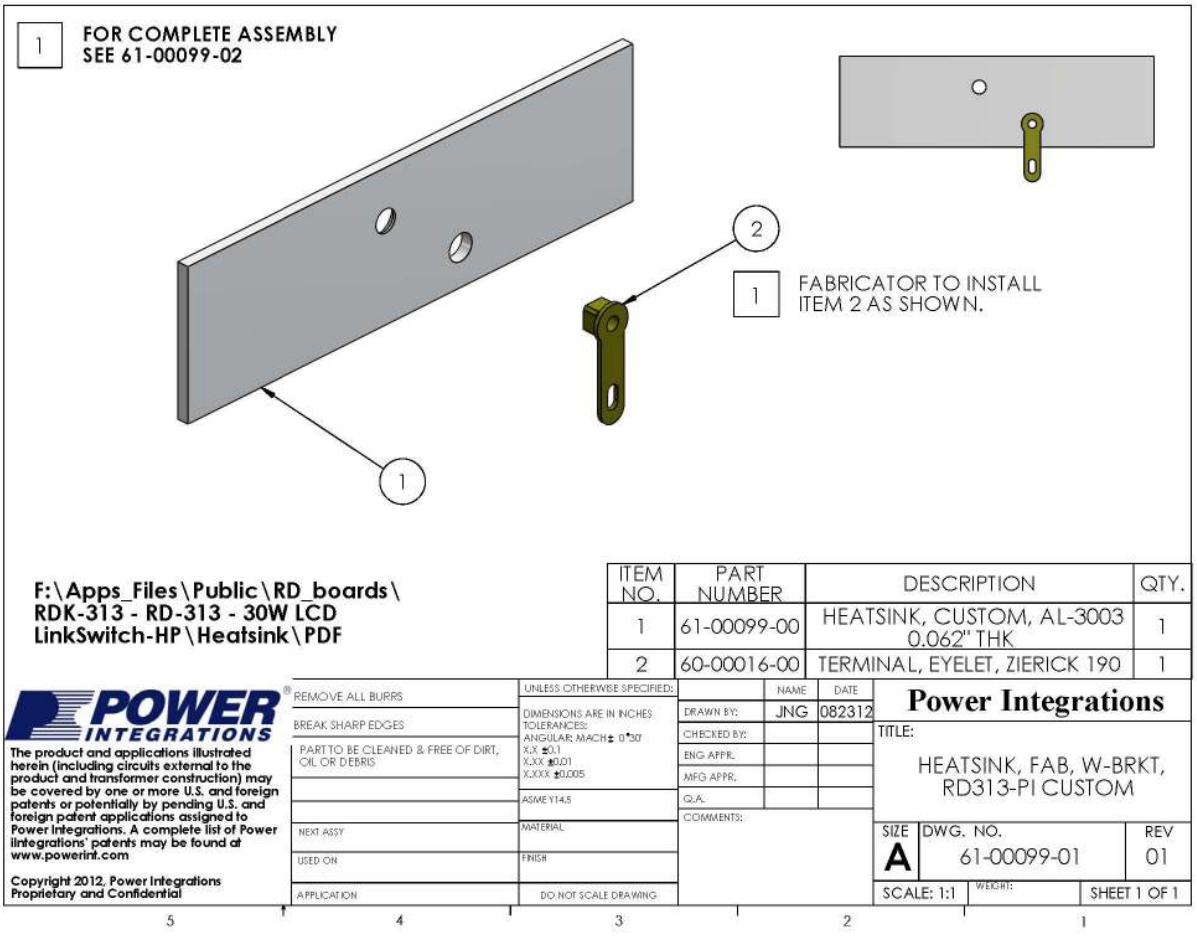
9 Heat Sink Assemblies

9.1 eSIP Heat Sink

9.1.1 eSIP Heat Sink Fabrication Drawing



9.1.2 eSIP Heat Sink Assembly Drawing



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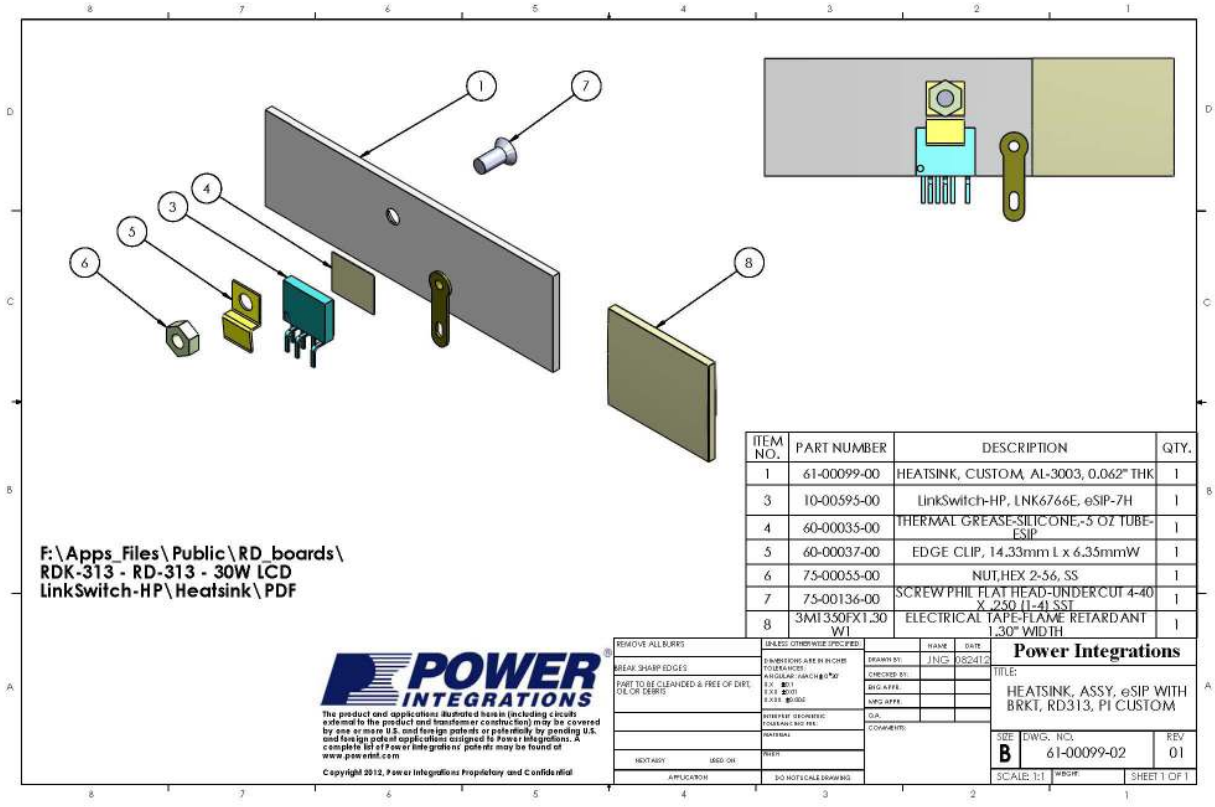
9.1.3 ESIP and Heat Sink Assembly Drawing

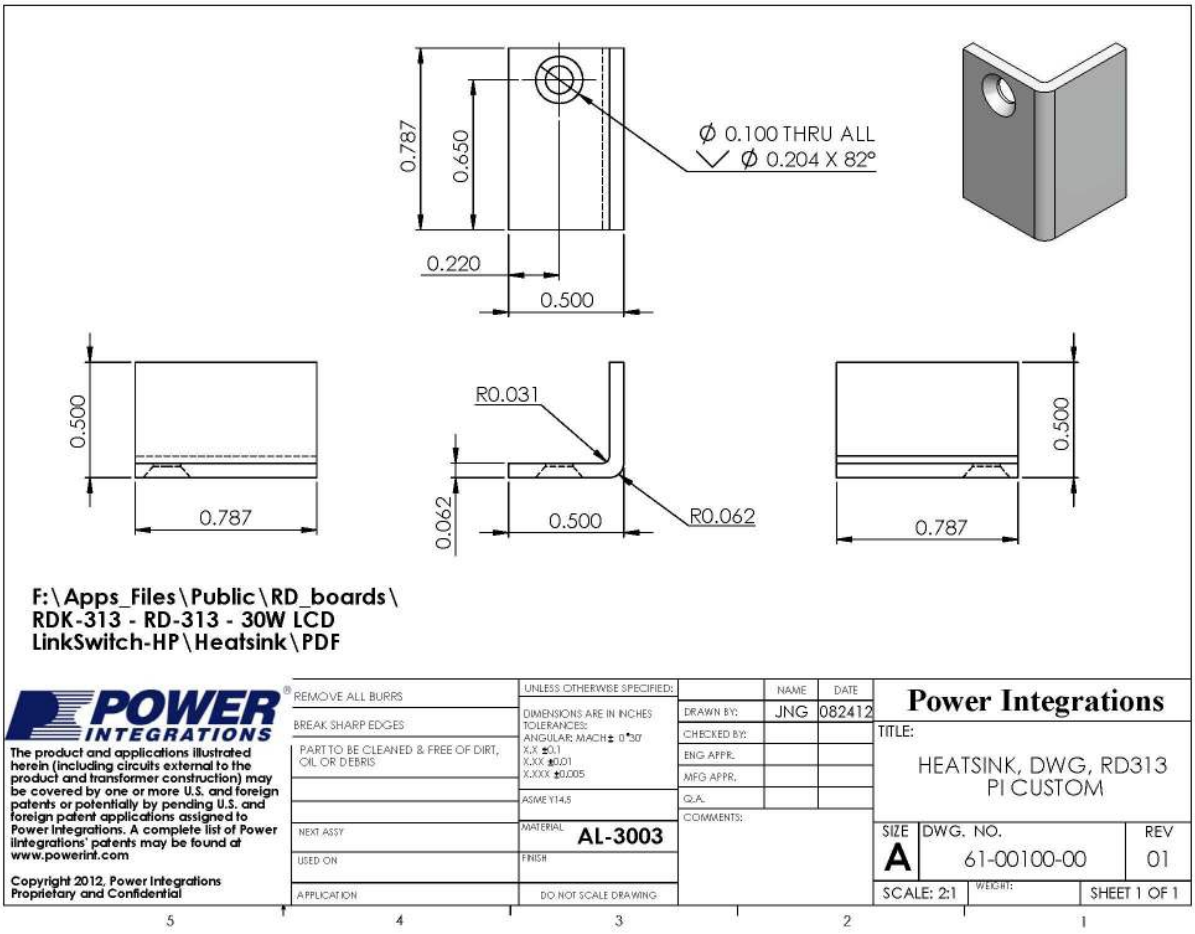


ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00099-00	HEATSINK, CUSTOM, AL-3003, 0.062" THK	1
3	10-00595-00	LinkSwitch-HP, LNK6766E, eSIP-7H	1
4	60-00035-00	THERMAL GREASE-SILICONE,-5 OZ TUBE-ESIP	1
5	60-00037-00	EDGE CLIP, 14.33mm L x 6.35mmW	1
6	75-00055-00	NUT,HEX 2-56, SS	1
7	75-00136-00	SCREW PHIL FLAT HEAD-UNDERCUT 4-40 X .250 (1-4) SST	1
8	3M1350FX1.30 W1	ELECTRICAL TAPE-FLAME RETARDANT 1.30" WIDTH	1

Power Integrations
TITLE: HEATSINK, ASSY, eSIP WITH BRKT, RD313, PI CUSTOM
SIZE B | DWG. NO. 61-00099-02 | REV 01
SCALE: 1:1 | SHEET 1 OF 1

9.2 Diode Heat Sink

9.2.1 Diode Heat Sink Fabrication Drawing



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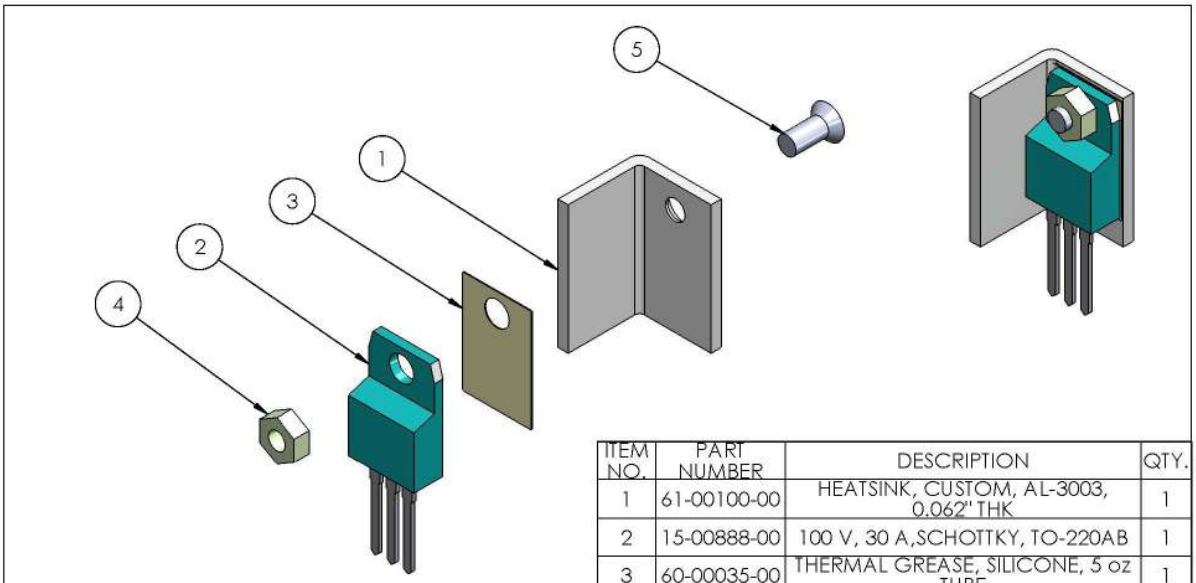
9.2.2 Diode and Heat Sing Assembly Drawing



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00100-00	HEATSINK, CUSTOM, AL-3003, 0.062" THK	1
2	15-00888-00	100 V, 30 A,SCHOTTKY, TO-220AB	1
3	60-00035-00	THERMAL GREASE, SILICONE, 5 oz TUBE	1
4	75-00055-00	NUT,HEX 2-56, SS	1
5	75-00136-00	SCREW PHIL FLAT HEAD-UNDERCUT 4-40 X .250 (1-4) SST	1

F:\Apps_Files\Public\RD_boards\
RDK-313 - RD-313 - 30W LCD
LinkSwitch-HP\Heatsink\PDF

POWER INTEGRATIONS

REMOVE ALL BURRS
BREAK SHARP EDGES
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS
NEXT ASSY
USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGULAR: MACH ± 0°30'
X.X ±0.1
X.XX ±0.01
X.XXX ±0.005
ASME Y14.5
MATERIAL
FINISH
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	JNG	082412
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		
COMMENTS:		

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TITLE: HEATSINK, ASSY, DIODE, RD313, PI CUSTOM

SIZE	DWG. NO.	REV
A	61-00100-02	01
SCALE: 1:1	WEIGHT:	SHEET 1 OF 1

5 4 3 2 1

10 Performance Data

All measurements performed at room temperature and 50 Hz line frequency, except where otherwise stated. For all tests, the full load is 2.5 A.

10.1 Active Mode Efficiency

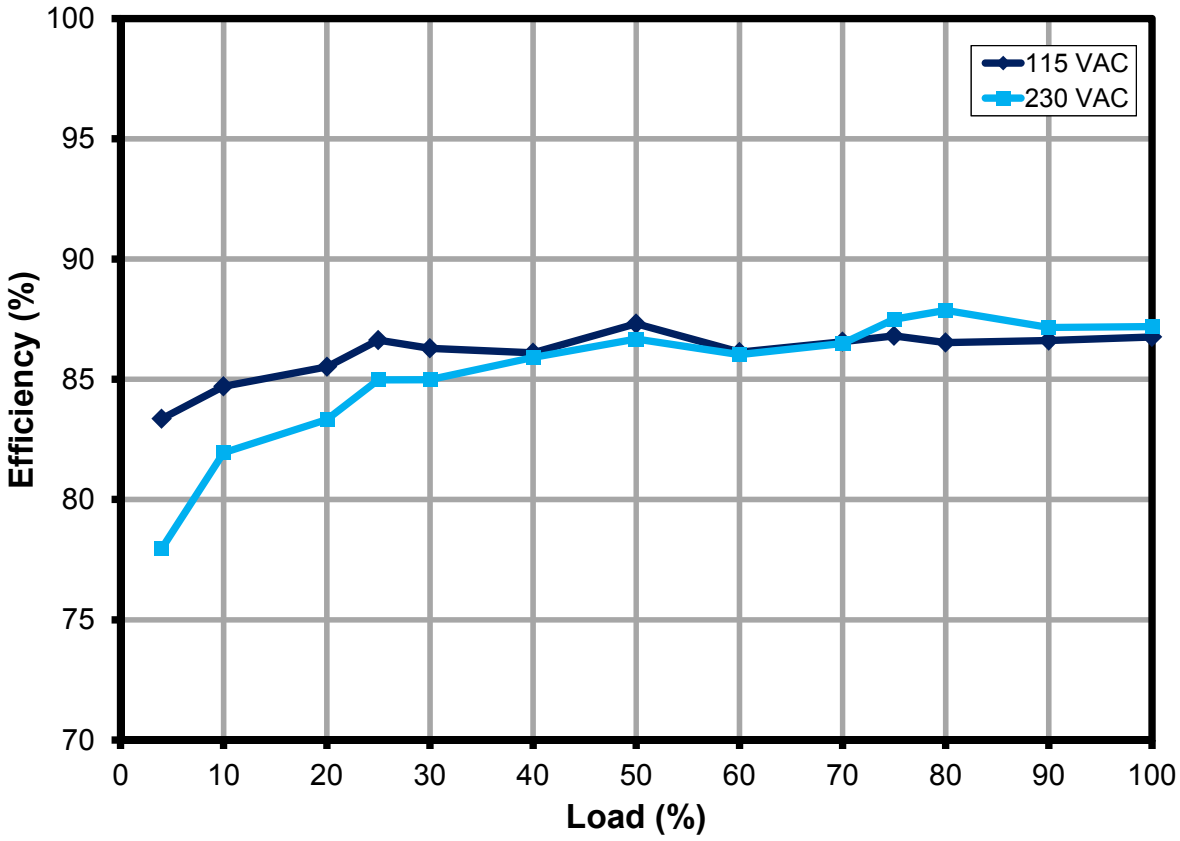

Figure 7– Active mode Efficiency, Room Temperature

115 VAC			
V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	η
12.1	0.625	8.73	86.63%
12	1.251	17.18	87.3%
11.94	1.875	25.79	86.8%
11.91	2.5	34.32	86.76%
		Avg	86.88%

230 VAC			
V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	η
12.1	0.625	8.9	84.97%
12.01	1.251	17.32	86.7%
11.97	1.875	25.65	87.5%
11.94	2.5	34.25	87.19%
		Avg	86.58%

Table 1 – Four Point Average Efficiency (25%, 50%, 75% and 100%), Room Temperature.

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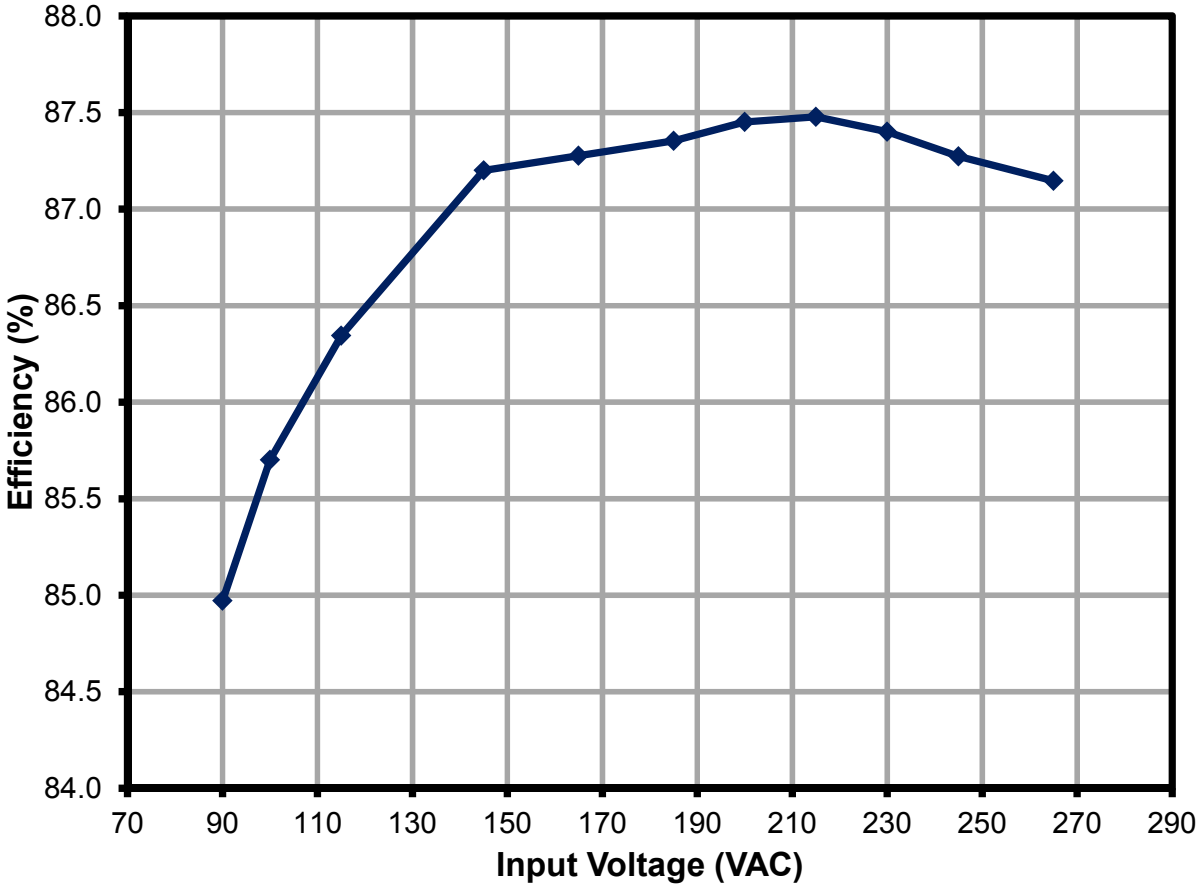

Figure 8 – Full Load Efficiency vs. Input Voltage, Room Temperature.

10.2 No-Load Input Power

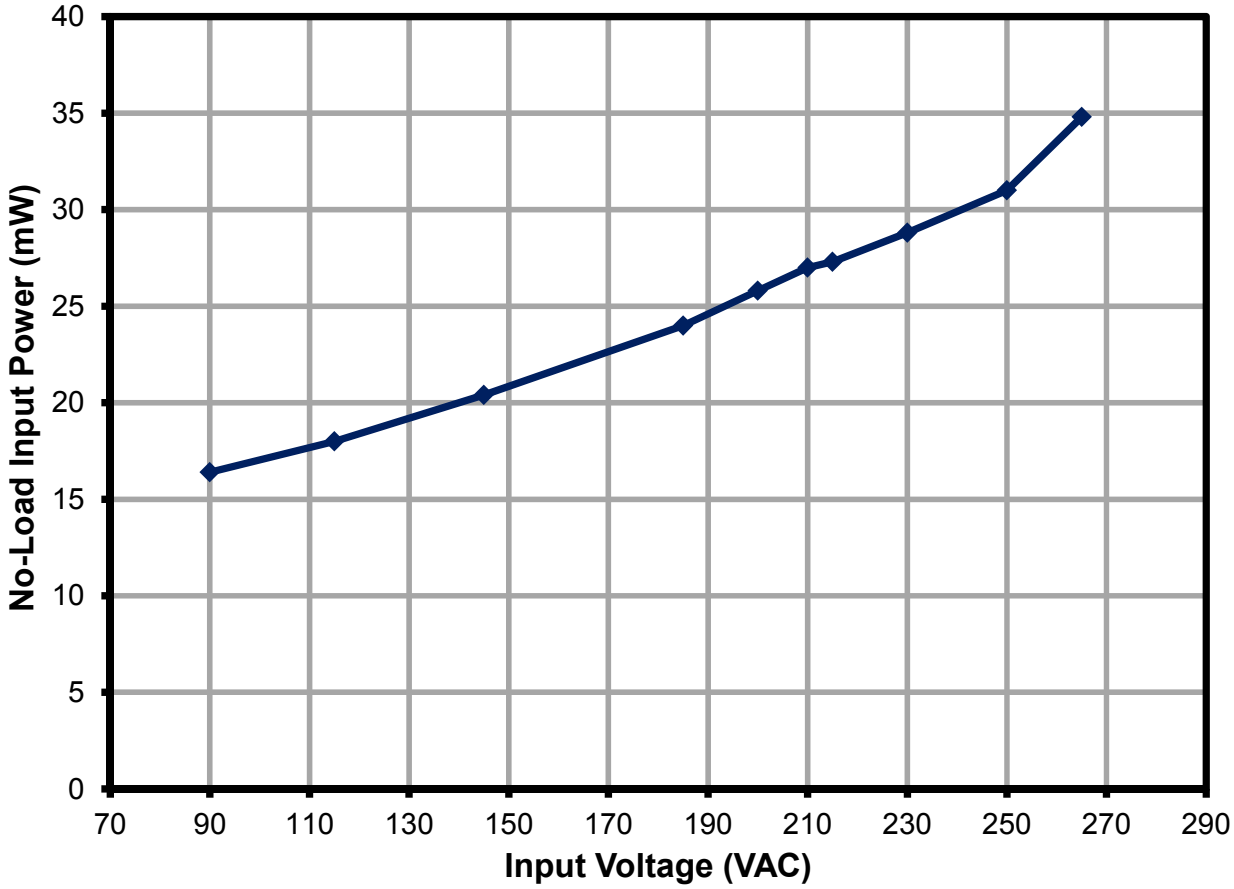

Figure 9 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

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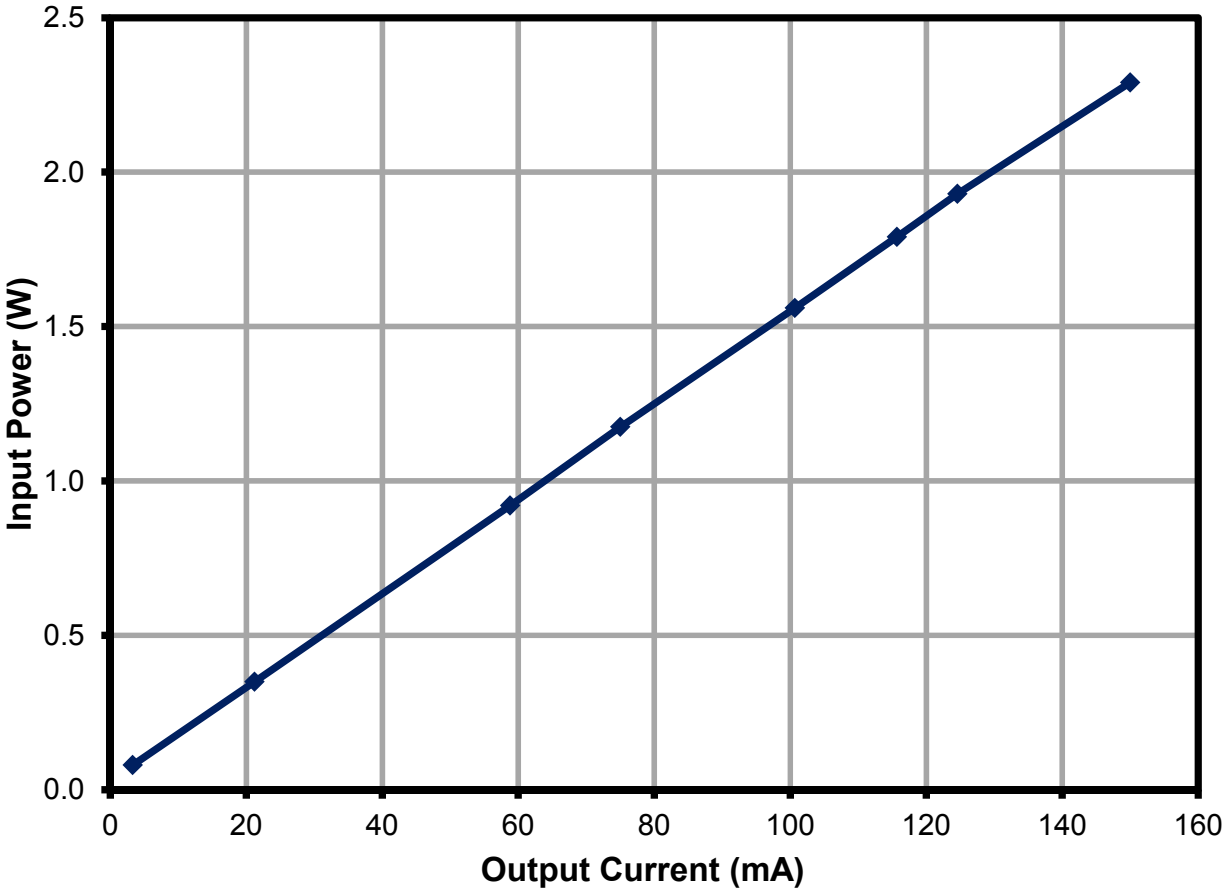

Figure 10 – Standby Performance at 230 VAC, Room Temperature.

10.3 Line Regulation

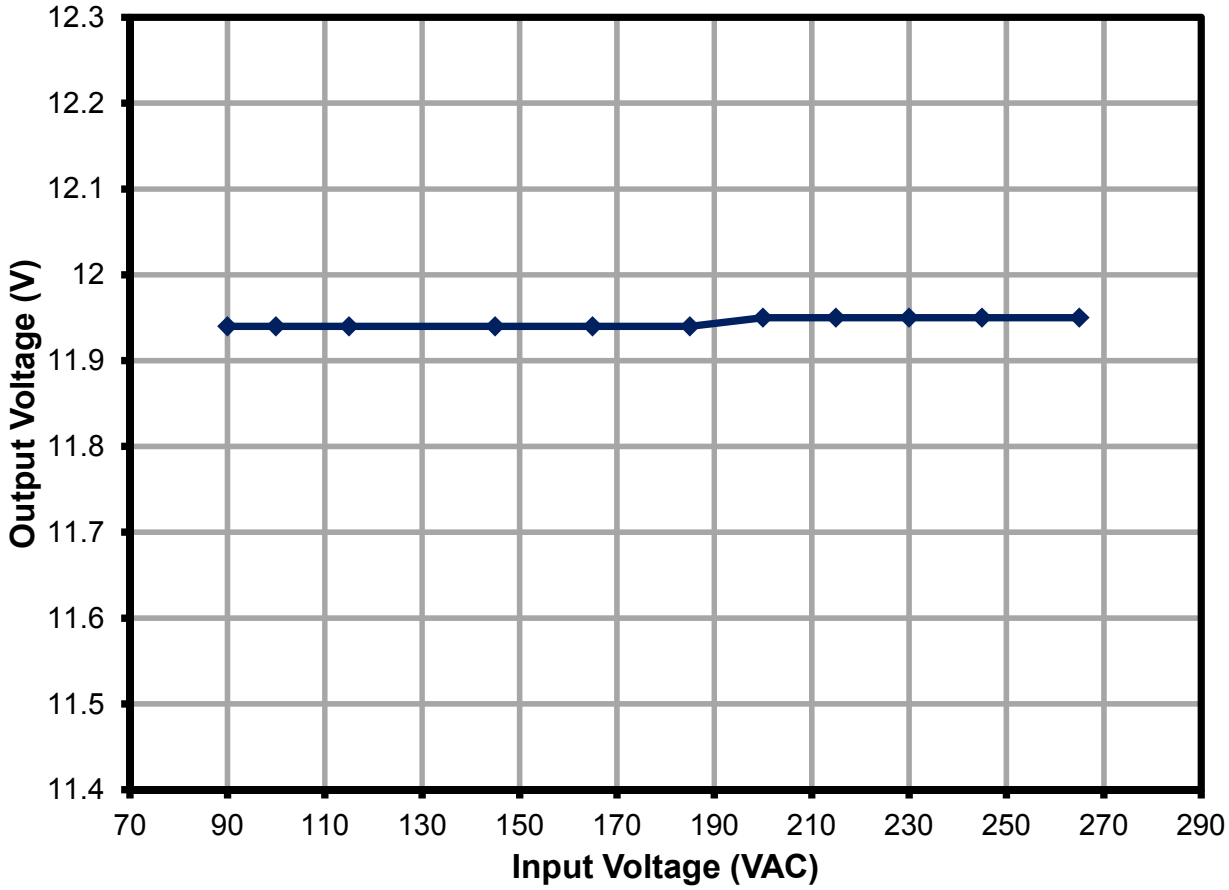

Figure 11 – Line Regulation under Full Load, Room Temperature.

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10.4 Load Regulation

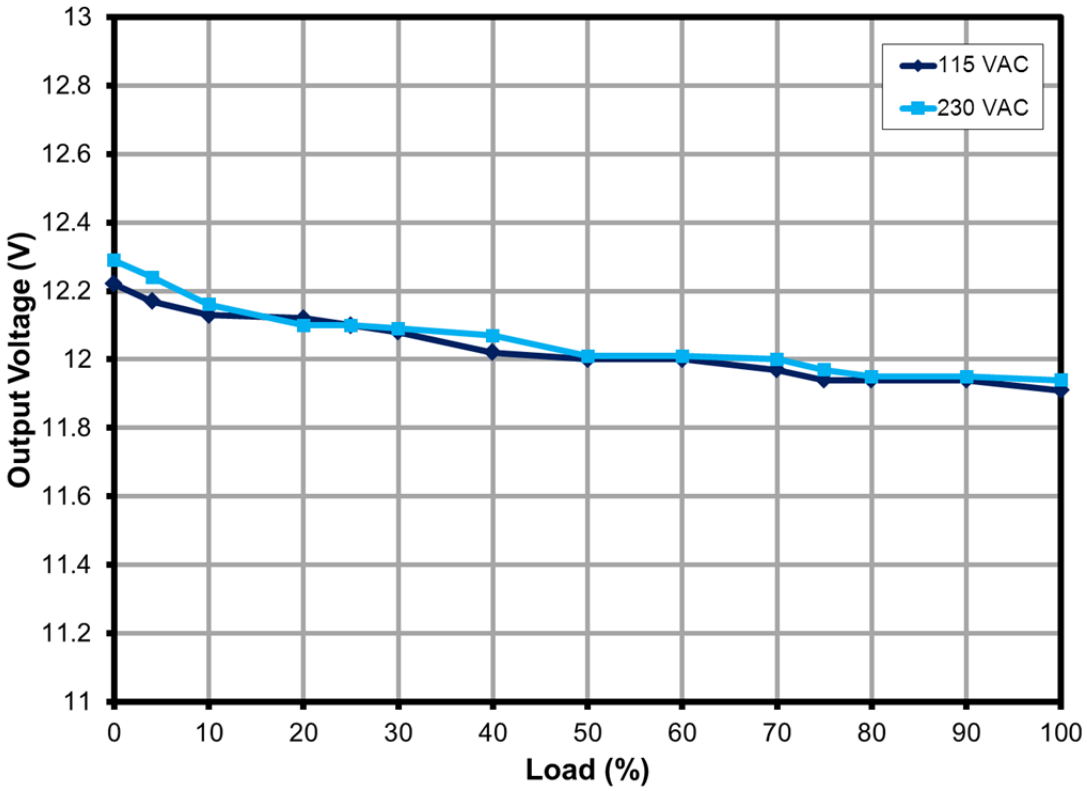

Figure 12 – Load Regulation, Room Temperature.

10.5 Power Limit

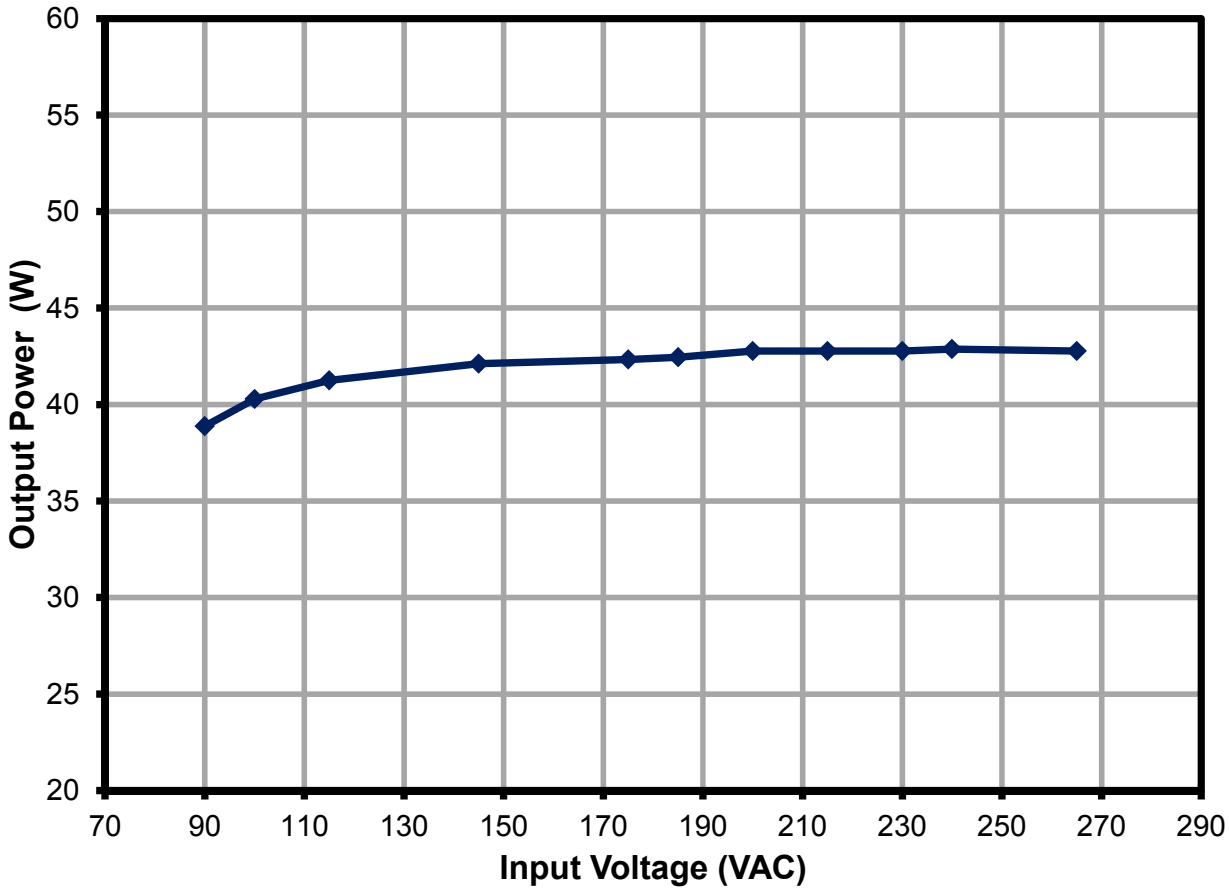

Figure 13 – Overload Power vs. Line Voltage.

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11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

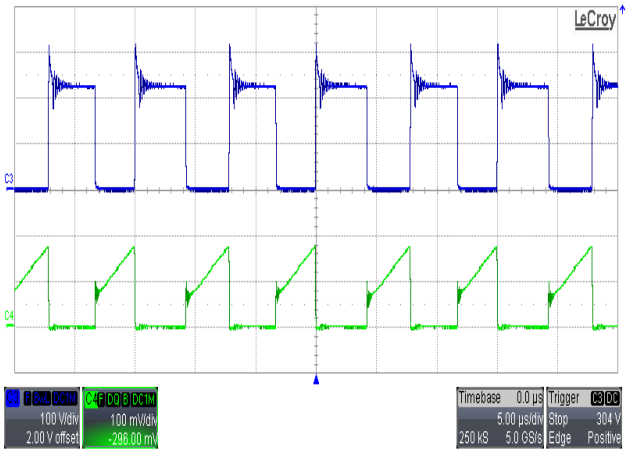

Figure 14 – 90 VAC, Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.5 A / div., 10 µs / div.

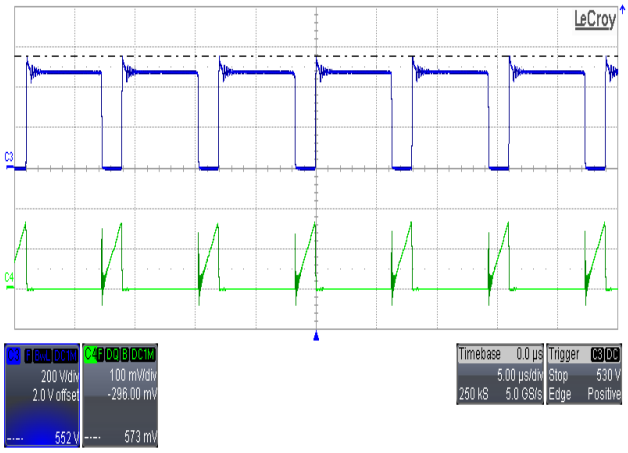

Figure 15 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A / div., 10 µs / div.

11.2 Drain Voltage and Current, Overload Power

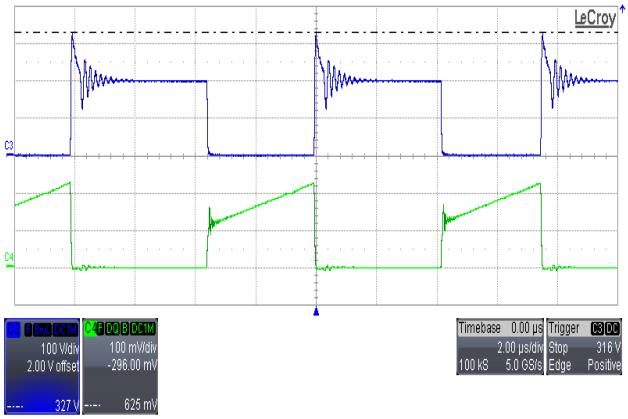

Figure 16 – 90 VAC, 38.8 W Overload Power.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.5 A / div., 10 µs / div.

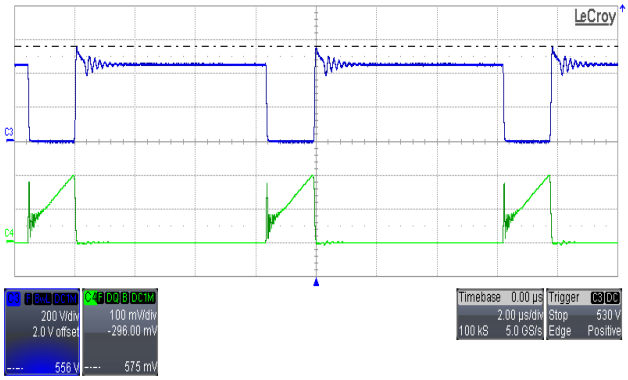

Figure 17 – 265 VAC, 42.78 W Overload Power.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A / div., 10 µs / div.

11.3 Voltage Stress, Overload Power

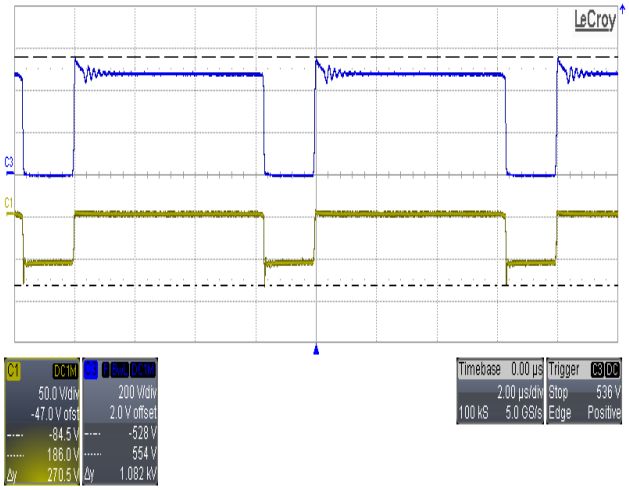

Figure 18 – 265 VAC, Overload Power.
Upper: V_{DRAIN}, 200 V / div.
Lower: PIV_{DIODE}, 50 V / div., 2.0 µs / div.

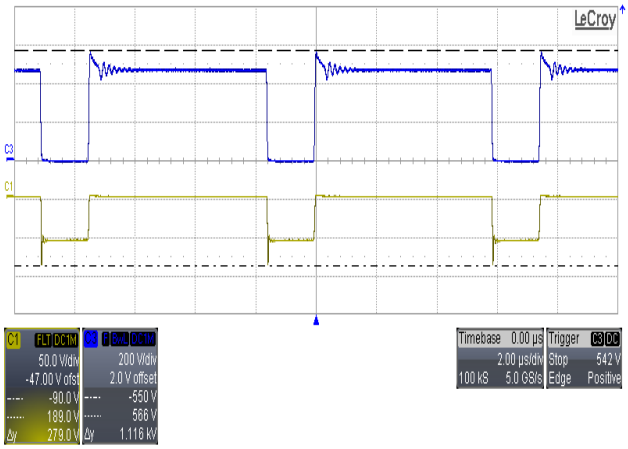

Figure 19 – 265 VAC, Overload Power.
Upper: V_{DRAIN}, 200 V / div.
Lower: PIV_{DIODE}, 50 V / div., 2.0 µs / div.

11.4 Drain Voltage and Current Start-up Profile

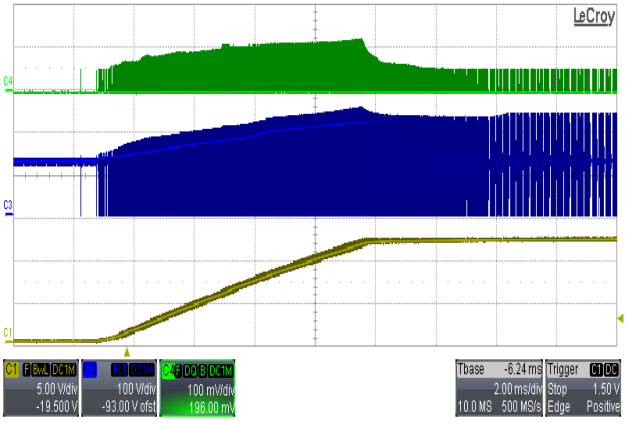

Figure 20 – 90 VAC, No-Load.
Upper: I_{DRAIN}, 0.5 A, 2 ms / div.
Middle: V_{DRAIN}, 100 V / div.
Lower: V_{OUT}, 5 V / div.

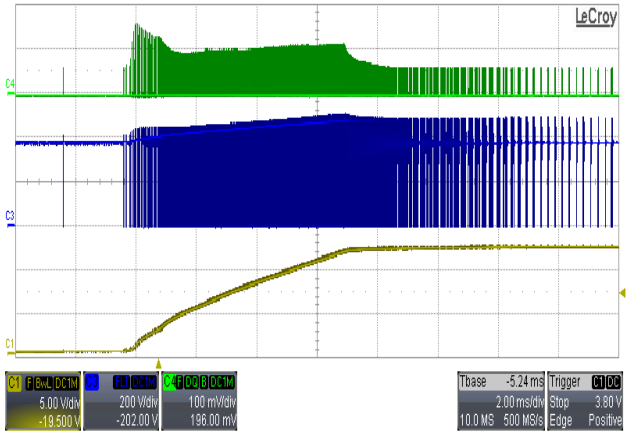

Figure 21 – 265 VAC, No-Load.
Upper: I_{DRAIN}, 0.5 A, 2 ms / div.
Middle: V_{DRAIN}, 200 V / div.
Lower: V_{OUT}, 5 V / div.

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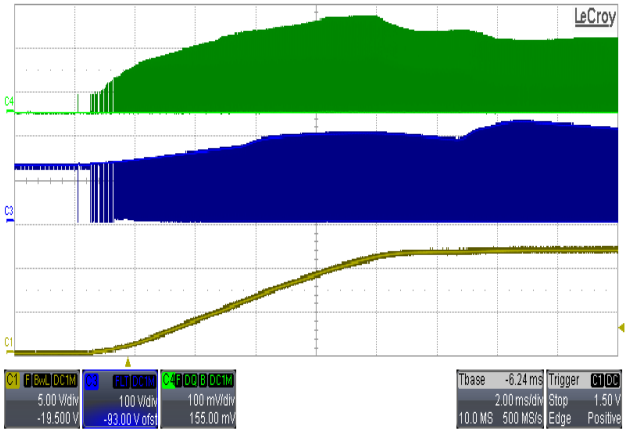

Figure 22 – 90 VAC, Full Load.
Upper: I_{DRAIN}, 0.5 A, 2 ms / div
Middle: V_{DRAIN}, 100 V / div.
Lower: V_{OUT}, 5 V / div.

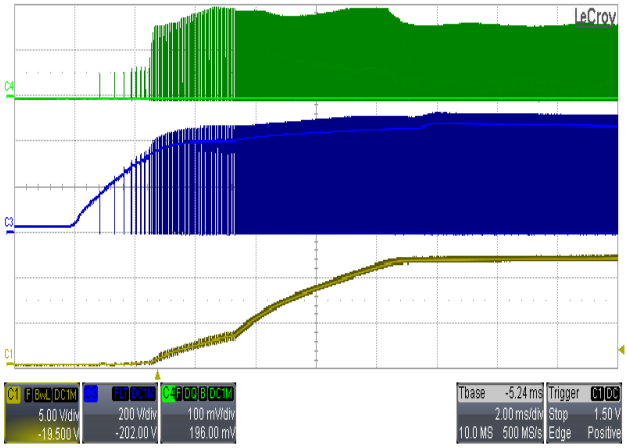

Figure 23 – 265 VAC, Full Load.
Upper: I_{DRAIN}, 0.5 A, 2 ms / div
Middle: V_{DRAIN}, 200 V / div.
Lower: V_{OUT}, 5 V / div.

11.5 Load Transient Response

In the figures shown below, the output was AC coupled to view the load transient response. The oscilloscope was triggered using the load current step as a trigger source.

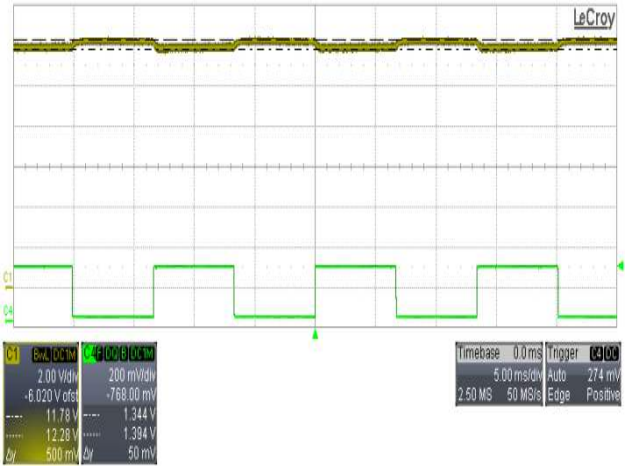

Figure 24 – Transient Response, 115 VAC, 5%<-->55% Step Load.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A / div., 5 ms / div.

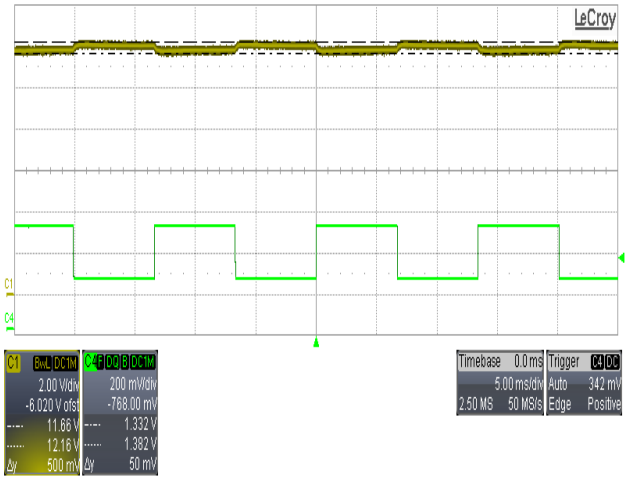

Figure 25 – Transient Response, 115 VAC, 50%<-->100% Step Load.
Upper: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 1 A / div., 5 ms / div.

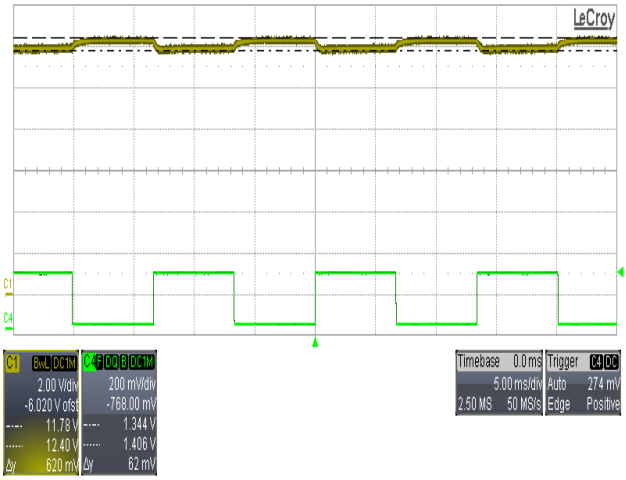

Figure 26 – Transient Response, 230 VAC, 5%<-->55% Step Load.
Upper: V_{OUT}, 2.0 V / div.
Lower: I_{OUT}, 1 A / div., 5 ms / div.

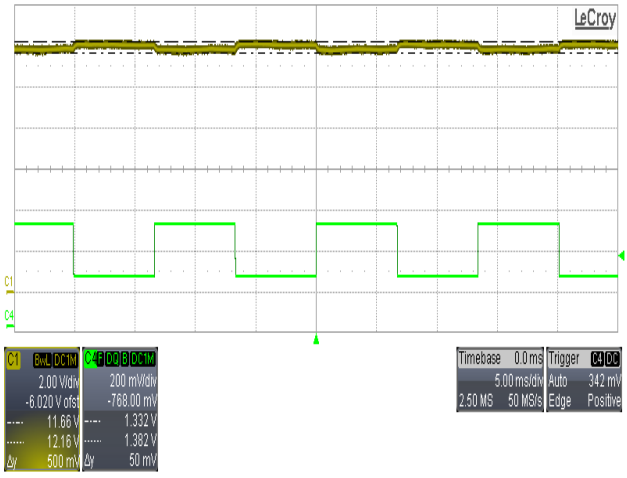

Figure 27 – Transient Response, 230 VAC, 50%<-->100% Step Load.
Upper: V_{OUT}, 2.0 V / div.
Lower: I_{OUT}, 1 A / div., 5 ms / div.

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11.6 Output Ripple and Noise Measurements

11.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the figures below.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 4.7 μF / 50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

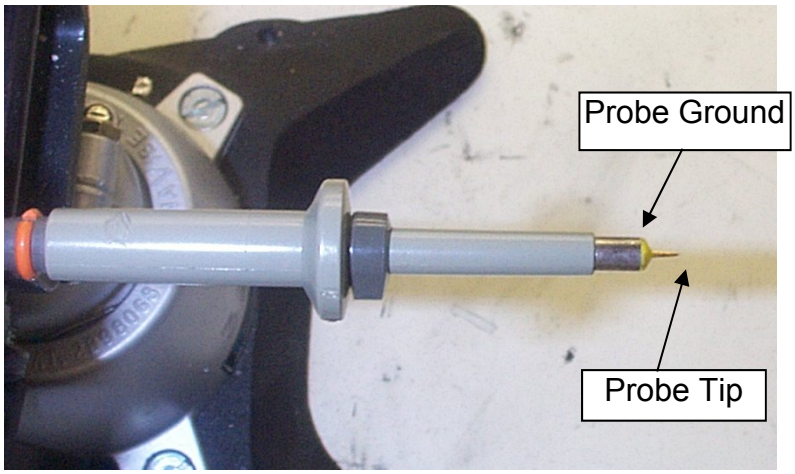

Figure 28 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

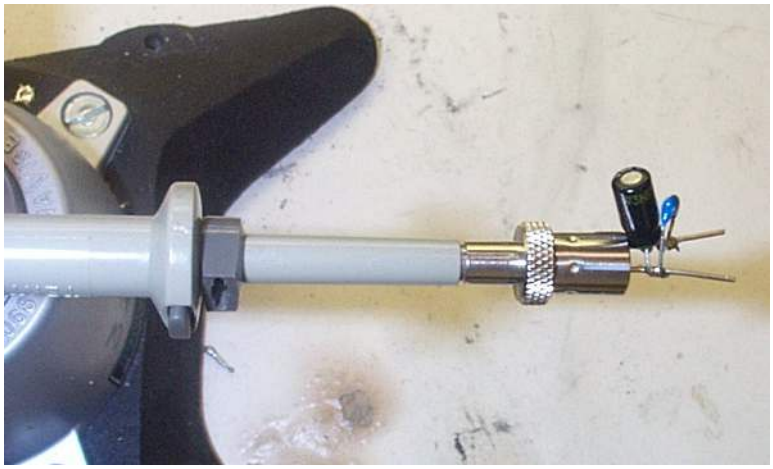

Figure 29 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter (Modified with Wires for Probe Ground for Ripple Measurement, and Two Parallel Decoupling Capacitors Added).

11.6.2 Ripple and Noise Measurement Results

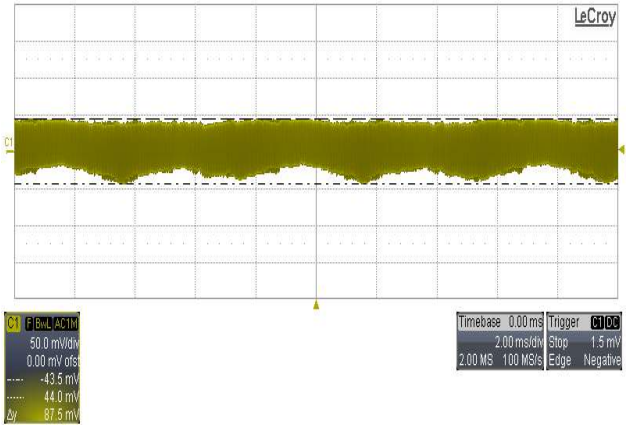

Figure 30 – Low Frequency Ripple, 115 VAC, Full Load.
V_{OUT}, 50 mV / div.

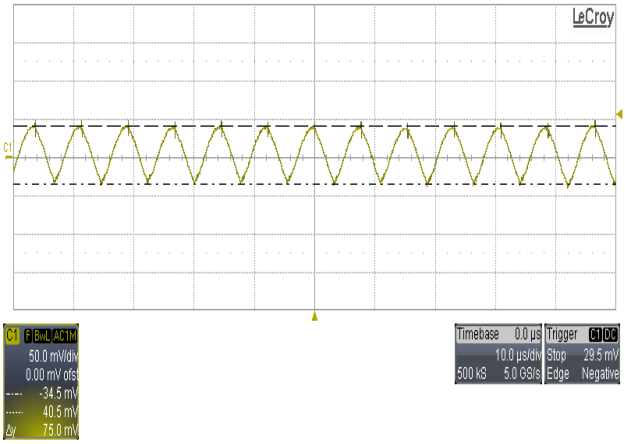

Figure 31 – Switching Noise, 115 VAC, Full Load.
V_{OUT}, 50 mV / div.

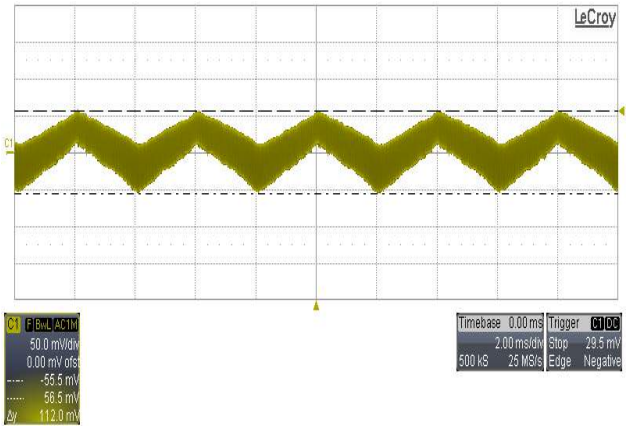

Figure 32 – Low Frequency Ripple, 230 VAC, Full Load.
V_{OUT}, 50 mV / div.

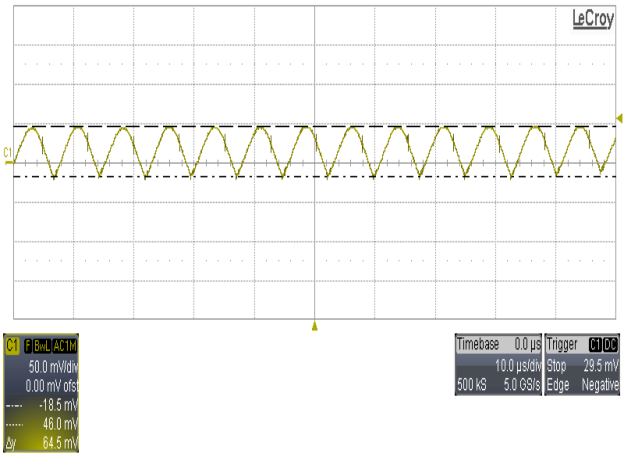

Figure 33 – Switching Noise, 230 VAC, Full Load.
V_{OUT}, 50 mV / div.

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12 Protection Feature

12.1 Auto-Restart under Short-Circuit Condition

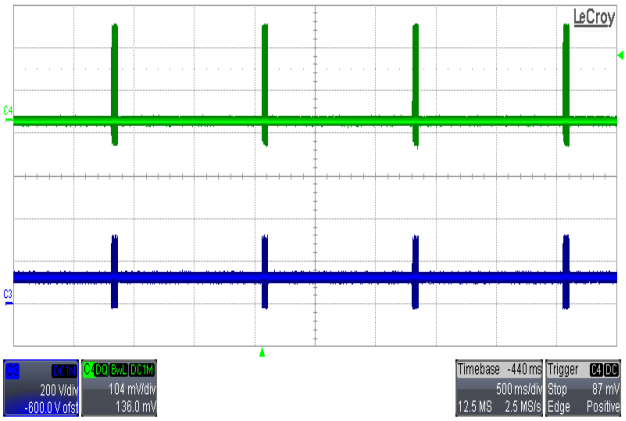

Figure 34 – Auto-restart Under Short-Circuit, 90 VAC.
Upper: I_{DRAIN}, 0.52 A / div., 500 ms / div.
Lower: V_{DRAIN}, 200 V / div.
Input Power = 1.38 W.

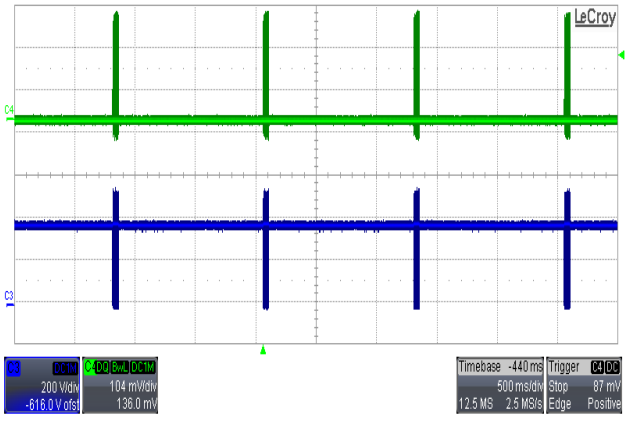

Figure 35 – Auto-restart Under Short-Circuit, 265 VAC.
Upper: I_{DRAIN}, 0.52 A / div., 500 ms / div.
Lower: V_{DRAIN}, 200 V / div.
Input Power = 1.41 W.

12.2 Latching Protection under Overvoltage (Open Loop Test)

OVP is initiated by inserting a 100 kΩ between BP and CP pin during normal operation.

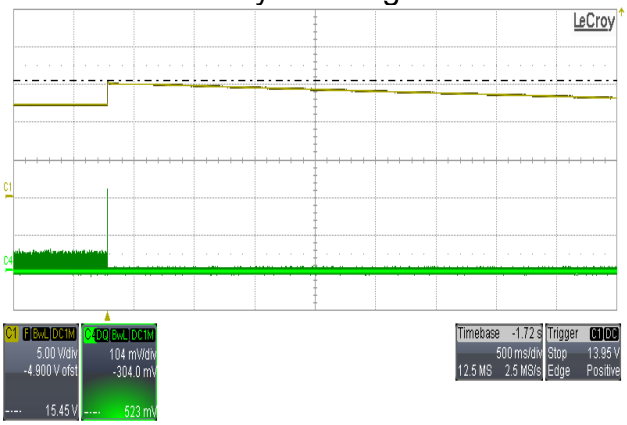

Figure 36 – OVP at 90 VAC, No-Load.
Upper: V_{OUT}, 5 V / div., 500 ms / div.
Lower: I_{DRAIN}, 0.52 A / div.
OVP Trip Point = 15.45 V.

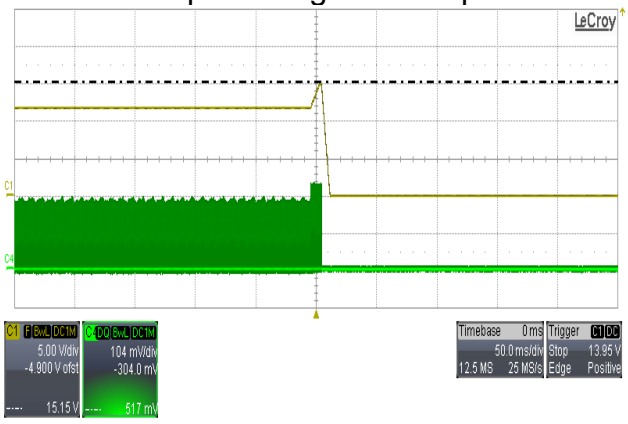

Figure 37 – OVP at 90 VAC, Full Load.
Upper: V_{OUT}, 5 V / div., 500 ms / div.
Lower: I_{DRAIN}, 0.52 A / div.
OVP Trip Point = 15.15 V.

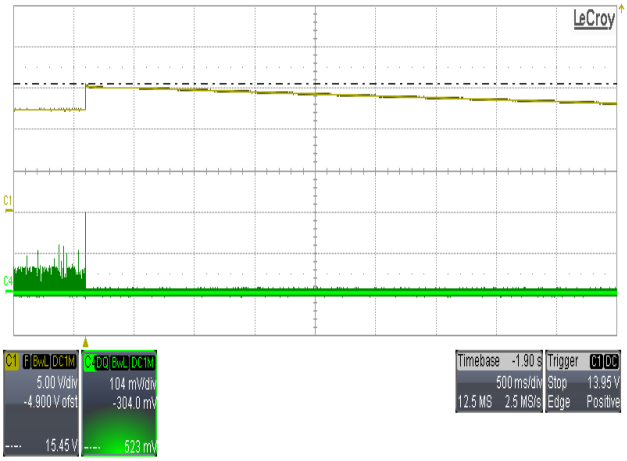

Figure 38 – OVP at 265 VAC, No-Load.
Upper: V_{OUT}, 5 V / div., 500 ms / div.
Lower: I_{DRAIN}, 0.52 A / div.
OVP Trip Point = 15.45 V.

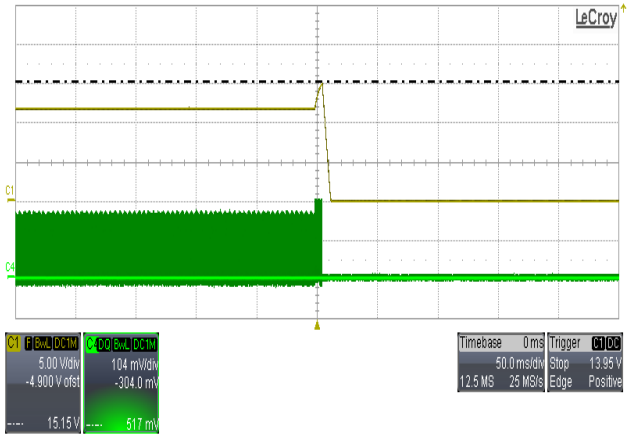

Figure 39 – OVP at 265 VAC, Full Load.
Upper: V_{OUT}, 5 V / div., 500 ms / div.
Lower: I_{DRAIN}, 0.52 A / div.
OVP Trip Point = 15.15 V.

12.3 Brown-in and Brown-out (Tested Using DC Input Source)

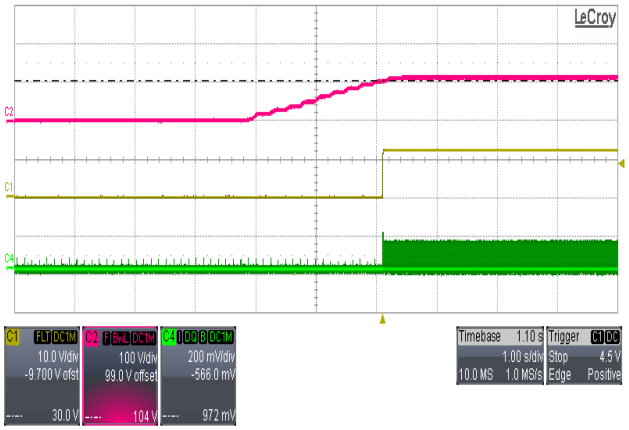

Figure 40 – Brown-in.
Upper: V_{IN}, 100 V / div., 1 s / div.
Middle: V_{OUT}, 10 V / div.
Lower: I_{DRAIN}, 1.0 A / div.

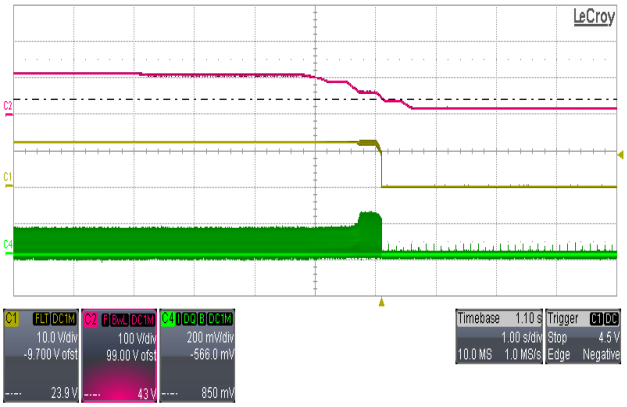

Figure 41 – Brown-out.
Upper: V_{IN}, 100 V / div., 1 s / div.
Middle: V_{OUT}, 10 V / div.
Lower: I_{DRAIN}, 1.0 A / div.

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12.4 Line Overvoltage Protection (Tested Using DC Input Source)

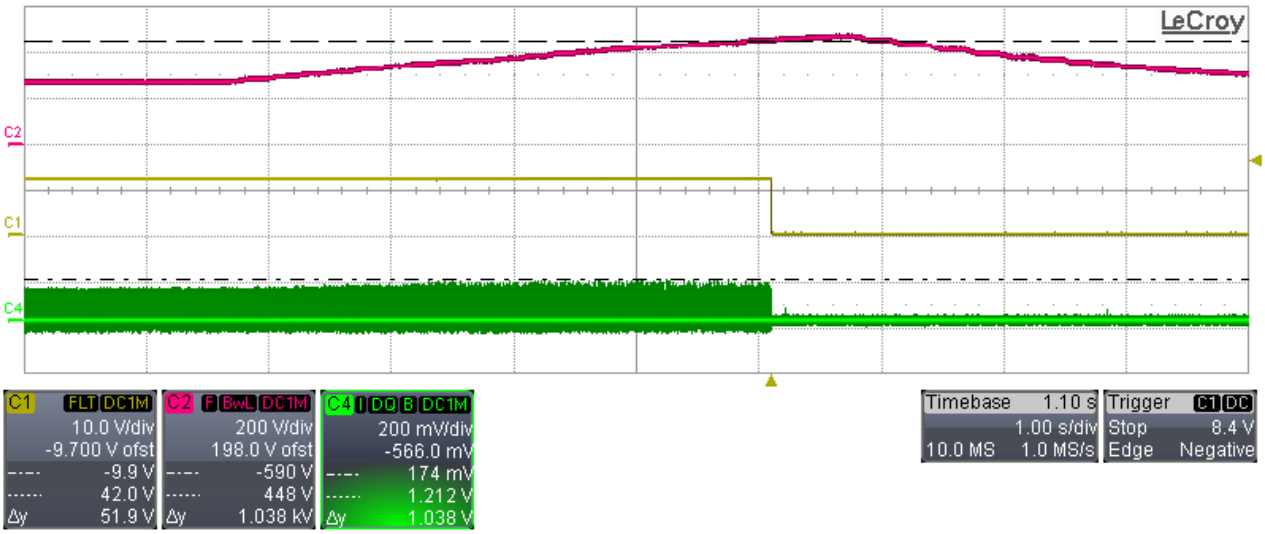


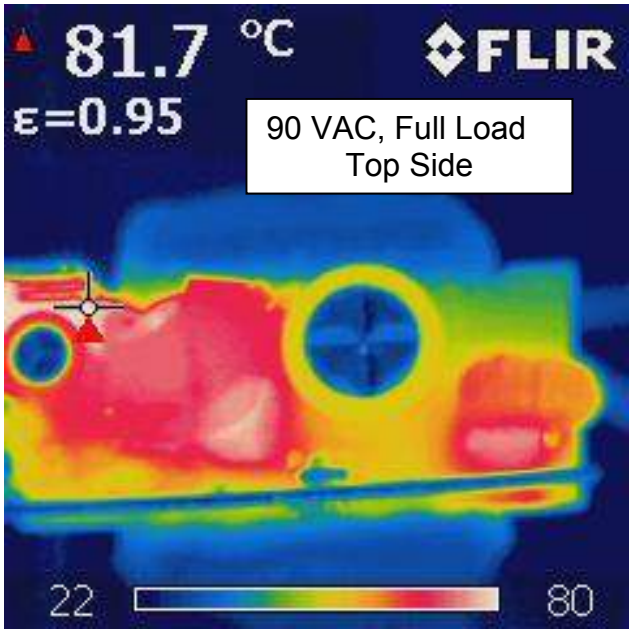
Figure 42 – Line Overvoltage Protection (Triggered at 448 V).
Upper: V_{IN}, 200 V / div., 1 s / div.
Middle: V_{OUT}, 10 V / div.
Lower: I_{DRAIN}, 1.0 A / div.

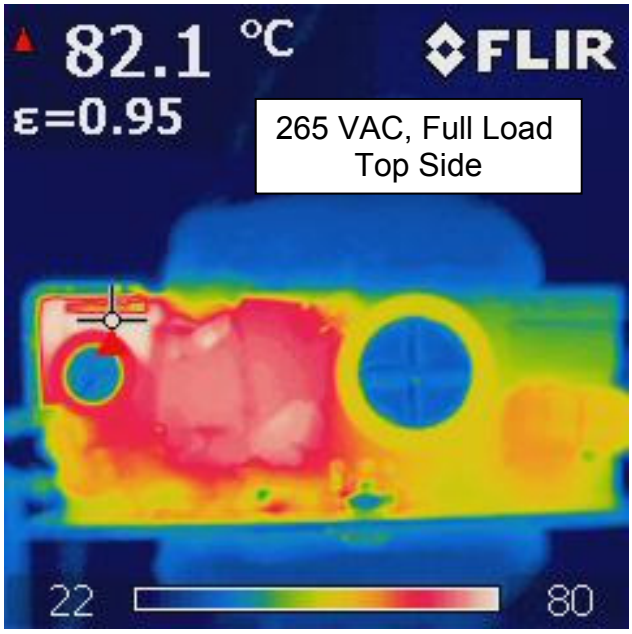
Note: Also programmed for latching under OTP conditions.

13 Thermal Performance ($T_{AMBIENT}$ = 25 °C)

Thermal performance was measured at full load operation, open frame at ambient temperature of 25 °C. The transformer winding temperature was taken on the outermost layer.

Item	Description	90 VAC Full Load	265 VAC Full Load
1	Output Diode	81.7	82.1
2	LNK6766E	68	65
3	Transformer	73.3	75
4	Input Capacitor	58	43
5	Output CMC	62	55
6	Input CMC	61	35
7	Bridge Diode	77	52
8	Zener Clamp	73	63





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14 AC Surge (Resistive Full Load at the Output)

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Results (Pass/Fail # Strikes)
D.M.		**(2Ω source)**		**10 Strikes Each Level**
+1000	230	L1 to L2	90	Pass
-1000	230	L1 to L2	270	Pass
C.M.		**(12Ω source)**		
+2000	230	L1, L2 to PE	90	Pass
-2000	230	L1, L2 to PE	270	Pass

15 ESD (Resistive Full Load at the Output)

Device	Discharge Type	Discharge Location	Voltage	# of Events (1/sec)	Remarks
LNK6766E	Contact	+ Output Terminal	+8 kV	10	PASS
			-8 kV	10	PASS
		- Output Terminal	+8 kV	10	PASS
			-8 kV	10	PASS
	Air	+ Output Terminal	+15 kV	10	PASS
			-15 kV	10	PASS
		- Output Terminal	+15 kV	10	PASS
			-15 kV	10	PASS

PASS = No output glitch or latch-off.

16 EMI Tests at Full Load

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load. Composite EN55022B / CISPR22B conducted limits are shown. All the tests show excellent EMI performance.

16.1 EMI Results

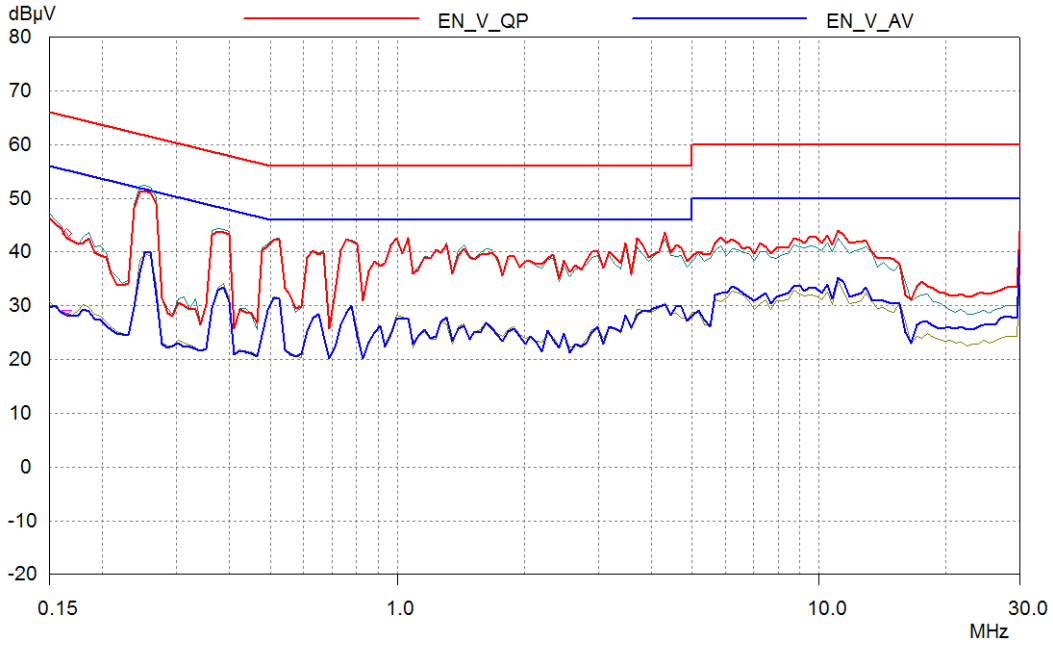

Figure 43 – Conducted EMI at 115 VAC 60 Hz, Full Load, and Output Return Connected to Ground.

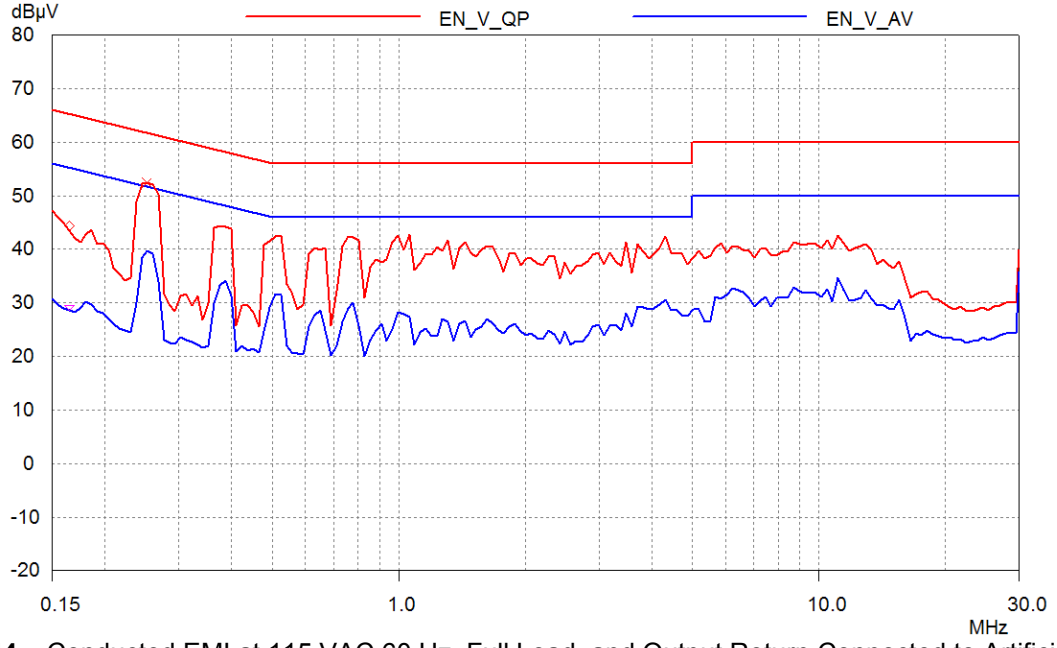

Figure 44 – Conducted EMI at 115 VAC 60 Hz, Full Load, and Output Return Connected to Artificial Hand.

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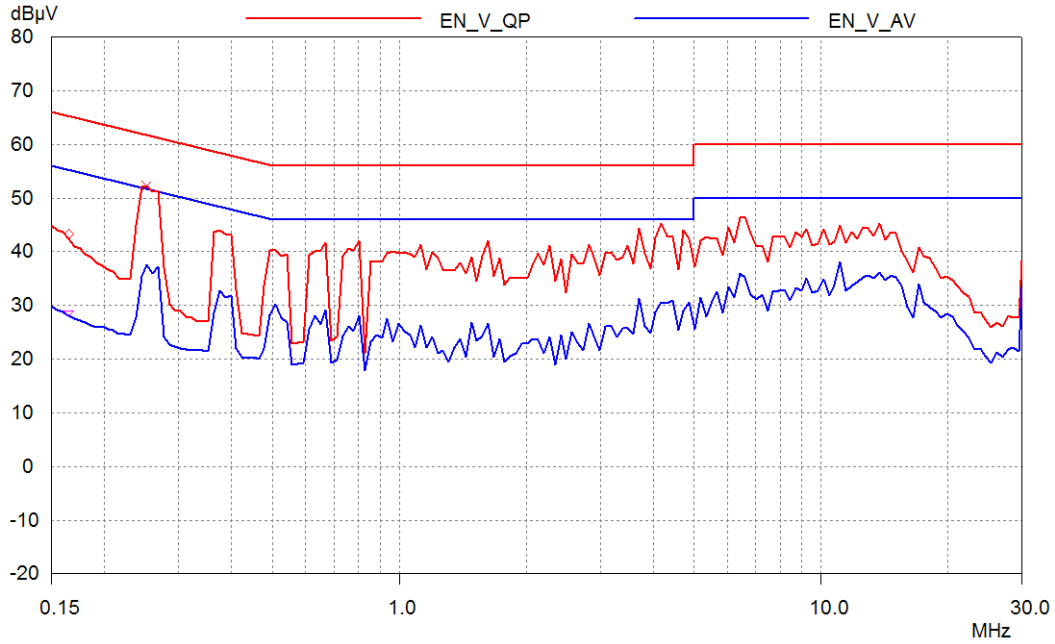

Figure 45 – Conducted EMI at 230 VAC 60 Hz, Full Load, and Output Return Connected to Ground.

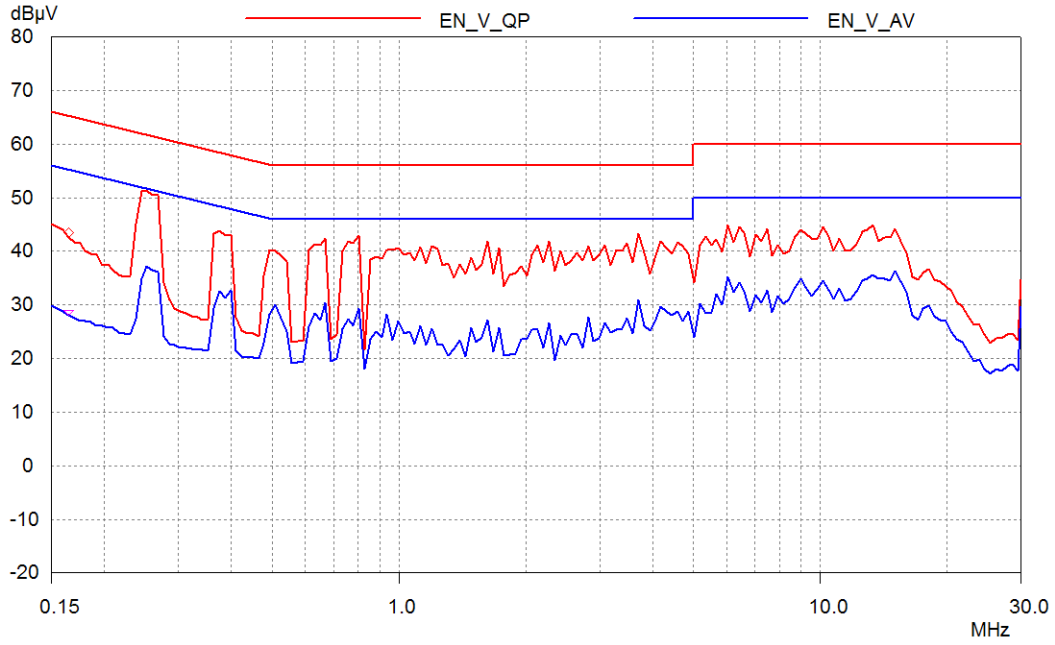

Figure 46 – Conducted EMI at 230 VAC 60 Hz, Full Load, and Output Return Connected to Artificial Hand.

17 Revision History

Date	Author	Revision	Description & changes	Reviewed
24-Jul-12	SS	1.0	Initial Release	Apps & Mktg
01-Aug-12	SS	1.1	Changed D8 to thru-hole. Improved heat sink for PI device and output diode. Changed BR2 and VR1 to SMD.	
14-Sep-12	KM	1.2	Updated schematic and format.	

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