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CY62156ESL MoBL[®] 8-Mbit (512 K × 16) Static RAM

Features

- High Speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra Low Standby Power
 Typical standby current: 2 μA
 Maximum standby current: 8 μA
- Ultra Low Active Power
 Typical active current: 1.8 mA at f = 1 MHz
- Easy Memory Expansion with CE₁, CE₂, and OE Features
- Automatic Power Down when Deselected
- CMOS for Optimum Speed and Power
- Available in Pb-free 48-ball very fine-pitch ball grid array (VFBGA) packages

Functional Description

The CY62156ESL is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life[™] (MoBL[®]) in portable

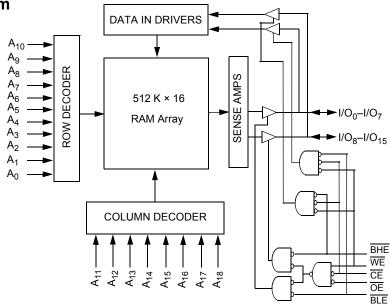
applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are <u>not</u> toggling. Place the device in standby mode when deselected (CE₁ HIGH or CE₂ LOW). The input or output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when the device is deselected (CE₁ HIGH or CE₂ LOW), the outputs are disabled (OE <u>HIGH</u>), Byte High Enable and Byte Low Enable are disabled (BHE, BLE <u>HIGH</u>), or a write operation is active (CE₁ LOW, CE₂ HIGH and WE LOW).

To write to the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 <u>HIGH</u>) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O₇) is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O₁₅) is written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.

Logic Block Diagram





CY62156ESL MoBL[®]

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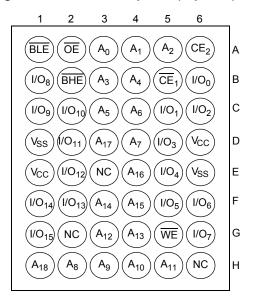
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Pin Configurations

Figure 1. 48-ball VFBGA pinout (Top View) ^[1]



Product Portfolio

					F	Power Di	ssipatio	n	
Product	Range	V _{CC} Range (V) ^[2]	Speed	Operating I _{CC} , (mA)		4)	Standby, I _{SB2}		
Froduct	Range		(ns)	f = 1MHz f = f _{max}		(μÅ)			
				Typ ^[3]	Max	Тур ^[3]	Max	Тур ^[3]	Max
CY62156ESL	Industrial	2.2 V to 3.6 V and 4.5 V to 5.5 V	45	1.8	3	18	25	2	8

Notes

NC pins are not connected on the die.
 Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.
 Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.



CY62156ESL MoBL[®]

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature65 °C to + 150°C
Ambient Temperature with Power Applied–55 °C to + 125 °C
Supply Voltage to Ground Potential0.5 V to 6.0 V
DC Voltage Applied to Outputs in High Z State ^[4, 5] –0.5 V to 6.0 V
in High Z State ^[4, 5] –0.5 V to 6.0 V
DC Input Voltage ^[4, 5] 0.5 V to 6.0 V

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage	
(MIL-STD-883, Method 3015)	>2,001V
Latch Up Current	>200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[6]
CY62156ESL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V, and 4.5 V to 5.5 V

Electrical Characteristics

Over the Operating Range

Deremeter	Description	Description Test Conditions			45 ns		Unit
Parameter	Description	Test Co			Typ ^[1]	Max	Unit
V _{OH}	Output HIGH Voltage	2.2 <u>≤</u> V _{CC} <u>≤</u> 2.7	I _{OH} = -0.1 mA	2.0	-	_	V
		2.7 <u><</u> V _{CC} <u><</u> 3.6	I _{OH} = -1.0 mA	2.4	-	_	1
		4.5 <u>≤</u> V _{CC} <u>≤</u> 5.5	I _{OH} = -1.0 mA	2.4	-	_	1
V _{OL}	Output LOW Voltage	2.2 <u>≤</u> V _{CC} <u>≤</u> 2.7	I _{OL} = 0.1 mA	-	-	0.4	V
		2.7 <u><</u> V _{CC} <u><</u> 3.6	I _{OL} = 2.1mA	_	-	0.4	1
		4.5 <u>≤</u> V _{CC} <u>≤</u> 5.5	I _{OL} = 2.1mA	_	-	0.4	1
V _{IH}	Input HIGH Voltage	2.2 <u>≤</u> V _{CC} <u>≤</u> 2.7	·	1.8	-	V _{CC} + 0.3	V
		2.7 <u><</u> V _{CC} <u><</u> 3.6		2.2	-	V _{CC} + 0.3	1
		4.5 <u>≤</u> V _{CC} <u>≤</u> 5.5		2.2	-	V _{CC} + 0.5	1
V _{IL}	Input LOW Voltage	2.2 <u>≤</u> V _{CC} <u>≤</u> 2.7		-0.3	-	0.6	V
		2.7 <u><</u> V _{CC} <u><</u> 3.6		-0.3	-	0.8	1
		4.5 <u><</u> V _{CC} <u><</u> 5.5		-0.5	-	0.8	
I _{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		-1	-	+1	μA
I _{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}, C$	Dutput Disabled	–1	-	+1	μA
I _{CC}	V _{CC} Operating Supply Current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$	_	18	25	mA
		f = 1 MHz	I _{OUT} = 0 mA, CMOS levels	-	1.8	3	
I _{SB1}	Automatic CE Power down Current – CMOS Inputs	$\label{eq:constraint} \begin{array}{ c c c } \hline \overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}, \ CE_2 \leq 0.2 \text{ V}, \\ \hline V_{IN} \geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \text{ V}, \\ \hline f = f_{max} \mbox{ (Address and Data Only)}, \\ \hline f = 0 \mbox{ (OE, BHE, BLE and WE)}, \\ \hline V_{CC} = V_{CC(max)} \end{array}$		-	2	8	μΑ
I _{SB2} ^[7]	Automatic CE Power down Current – CMOS Inputs	$ \overline{CE}_{1} \ge V_{CC} - 0.2 V \\ V_{IN} \ge V_{CC} - 0.2 V \\ f = 0, V_{CC} = V_{CC(n)} $	or $V_{IN} \le 0.2 V$,	-	2	8	μΑ

Notes

A. V_{IL}(min) = -2.0 V for pulse durations less than 20 ns.
 5. V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
 6. Full Device AC ope<u>ration</u> assumes a 100 μs ramp time from 0 to V_{CC}(min) and 200 μs wait time after V_{CC} stabilization.
 7. Only chip enables (CE₁ and CE₂) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.



Capacitance

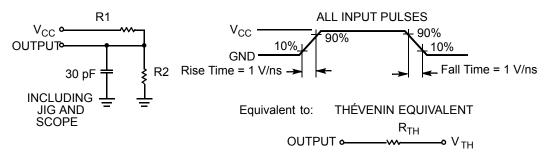
Parameter [8]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = V_{CC(typ)}$	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	48-ball BGA	Unit
- JA	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	72	°C/W
- 30	Thermal resistance (junction to case)		8.86	°C/W

AC Test Loads and Waveforms





Parameters	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R _{TH}	8000	645	639	Ω
V _{TH}	1.20	1.75	1.77	V



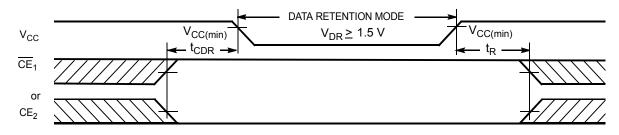
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[9]	Max	Unit
V _{DR}	V _{CC} for Data Retention		1.5	-	_	V
I _{CCDR} ^[10]			-	2	5	μΑ
t _{CDR} ^[11]	Chip Deselect to Data Retention Time		0	-	-	ns
t _R ^[12]	Operation Recovery Time		45	_	_	ns

Data Retention Waveform





Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25 \,^{\circ}C$. 10. Only chip enables (\overline{CE}_1 and \overline{CE}_2) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating. 11. Tested initially and after any design or process changes that may affect these parameters.

^{12.} Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} \geq 100 µs or stable at V_{CC(min)} \geq 100 µs.



Switching Characteristics

Over the Operating Range

Parameter [13]	Description	45	ns	11
Parameter [10]	Description	Min	Max	Unit
Read Cycle		·		
t _{RC}	Read Cycle Time	45	-	ns
t _{AA}	Address to Data Valid	-	45	ns
t _{OHA}	Data Hold from Address Change	10	-	ns
t _{ACE}	$\overline{\text{CE}}_1$ LOW and CE_2 HIGH to Data Valid	-	45	ns
t _{DOE}	OE LOW to Data Valid	-	22	ns
t _{LZOE}	OE LOW to Low Z ^[14]	5	-	ns
t _{HZOE}	OE HIGH to High Z ^[14, 15]	-	18	ns
t _{LZCE}	\overline{CE}_1 LOW and CE_2 HIGH to Low $Z^{[14]}$	10	-	ns
t _{HZCE}	CE ₁ HIGH and CE ₂ LOW to High Z ^[14, 15]	-	18	ns
t _{PU}	\overline{CE}_1 LOW and CE_2 HIGH to Power Up	0	-	ns
t _{PD}	\overline{CE}_1 HIGH and CE_2 LOW to Power Down	-	45	ns
t _{DBE}	BLE/BHE LOW to Data Valid	-	22	ns
t _{LZBE}	BLE/BHE LOW to Low Z ^[14]	5	-	ns
t _{HZBE}	BLE/BHE HIGH to High Z ^[14, 15]	-	18	ns
Write Cycle ^{[16,}	17]			
t _{WC}	Write Cycle Time	45	-	ns
t _{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to Write End	35	-	ns
t _{AW}	Address Setup to Write End	35	-	ns
t _{HA}	Address Hold from Write End	0	-	ns
t _{SA}	Address Setup to Write Start	0	-	ns
t _{PWE}	WE Pulse Width	35	-	ns
t _{BW}	BLE/BHE LOW to Write End	35	-	ns
t _{SD}	Data Setup to Write End	25	-	ns
t _{HD}	Data Hold from Write End	0	-	ns
t _{HZWE}	WE LOW to High Z ^[14, 15]	_	18	ns
t _{LZWE}	WE HIGH to Low Z ^[14]	10	_	ns

Notes

- 13. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of V_{CC(typ)}/2, input pulse levels of 0 to V_{CC(typ)}, and output loading of the specified 1_{OL}/1_{OH} as shown in the Figure 2 on page 5.
 14. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZDE}, and t_{HZWE} is less than t_{LZWE} for any device.
 15. t_{HZOE}, t_{HZDE}, t_{HZDE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
 16. The internal write time of the memory is defined by the overlap of WE, CE₁ = V_{IL}, BHE, BLE or both = V_{IL}, and CE₂ = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
 27. The internal write and and the subter to visit the total that the visit.
- 17. The minimum write cycle pulse width for Write Cycle No. 3 (WE controlled, OE LOW) should be equal to the sum of tsD and tHZWE.



Switching Waveforms

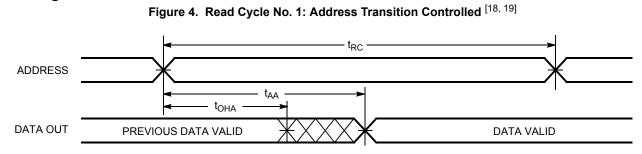
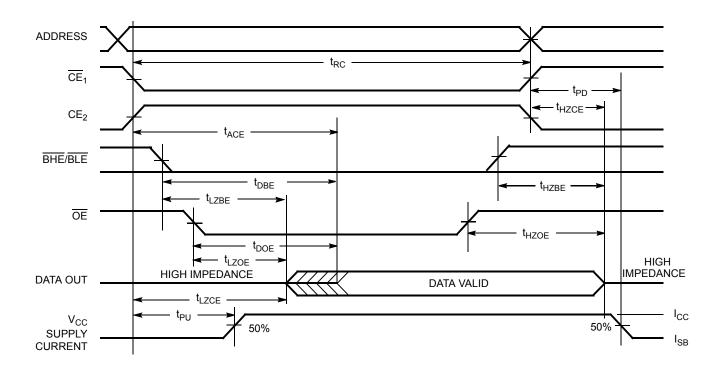


Figure 5. Read Cycle No. 2: OE Controlled ^[19, 20]

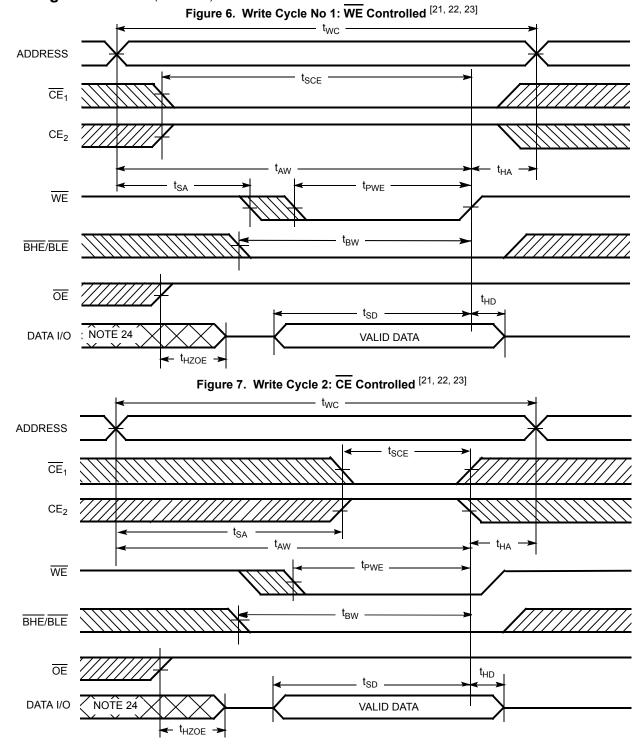


Notes

- 18. <u>The</u> device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} , and $CE_2 = V_{IH}$.
- 19. WE is HIGH for read cycle. 20. Address valid before or similar to \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.



Switching Waveforms (continued)



Notes

21. The internal write time of the memory is defined by the overlap of WE, $\overline{CE}_1 = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

22. Data I/O is high impedance if $\overline{OE} = V_{IH}$. 23. If \overline{CE}_1 goes HIGH and \overline{CE}_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state. 24. During this period, the I/Os are in output state. Do not apply input signals.



Switching Waveforms (continued)

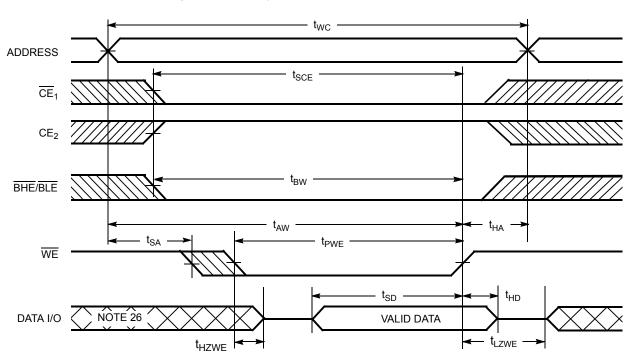
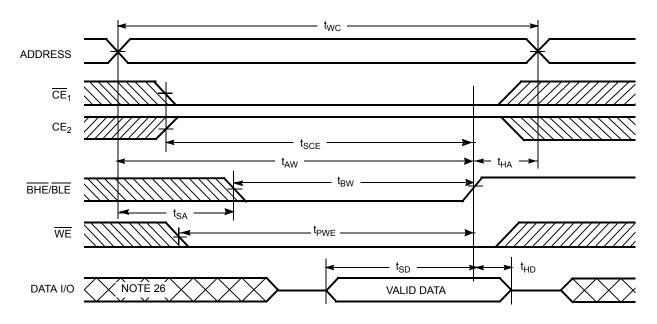


Figure 8. Write Cycle 3: $\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW [25, 27]

Figure 9. Write Cycle 4: BHE/BLE Controlled, OE LOW [25]



Notes

25. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

26. During this period, the I/Os are in output state. Do not apply input signals.

27. The minimum write cycle pulse width should be equal to the sum of tsp and tHzwE.





Truth Table

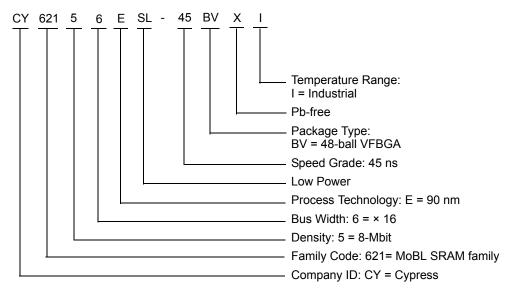
CE ₁	CE ₂	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
Н	Х	Х	Х	Х	Х	High Z	Deselect/Power Down	Standby (I _{SB})
Х	L	Х	Х	Х	Х	High Z	Deselect/Power Down	Standby (I _{SB})
L	Н	Х	Х	Н	Н	High Z	Output Disabled	Active (I _{CC})
L	Н	Н	L	L	L	Data Out (I/O ₀ –I/O ₁₅)	Read	Active (I _{CC})
L	Н	Н	L	Н	L	Data Out (I/O ₀ –I/O ₇); High Z (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})
L	Н	Н	L	L	Н	High Z (I/O ₀ –I/O ₇); Data Out (I/O ₈ –I/O ₁₅)	Read	Active (I _{CC})
L	Н	Н	Н	L	Н	High Z	Output Disabled	Active (I _{CC})
L	Н	Н	Н	Н	L	High Z	Output Disabled	Active (I _{CC})
L	Н	Н	Н	L	L	High Z	Output Disabled	Active (I _{CC})
L	Н	L	Х	L	L	Data In (I/O ₀ –I/O ₁₅)	Write	Active (I _{CC})
L	Н	L	Х	Н	L	Data In (I/O ₀ –I/O ₇); High Z (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})
L	Н	L	Х	L	Н	High Z (I/O ₀ –I/O ₇); Data In (I/O ₈ –I/O ₁₅)	Write	Active (I _{CC})



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62156ESL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial

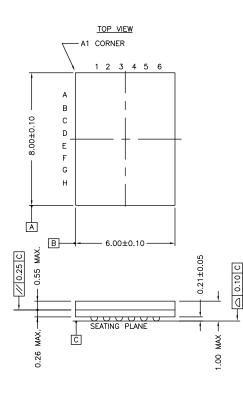
Ordering Code Definitions

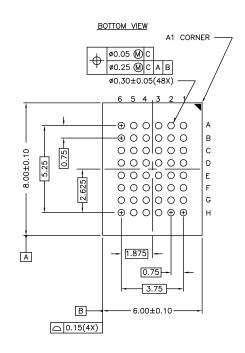




Package Diagrams

Figure 10. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150





NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H





Acronyms

Acronym	Description				
CE	Chip Enable				
CMOS	Complementary Metal Oxide Semiconductor				
I/O	Input/Output				
OE	Output Enable				
RAM	Random Access Memory				
SRAM	Static Random Access Memory				
VFBGA	Very Fine-Pitch Ball Grid Array				
WE	Write Enable				

Document Conventions

Units of Measure

Symbol	Unit of Measure		
°C	degree Celsius		
MHz	megahertz		
μA	microampere		
μs	microsecond		
mA	milliampere		
mm	millimeter		
ns	nanosecond		
Ω	ohm		
%	percent		
pF	picofarad		
V	volt		
W	watt		





Document History Page

Documen Documen	Document Title: CY62156ESL MoBL [®] , 8-Mbit (512 K × 16) Static RAM Document Number: 001-54995				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change	
**	2751673	VKN	08/13/09	New data sheet.	
*A	2899866	AJU	03/26/10	Removed inactive parts from Ordering Information. Updated Package Diagram.	
*В	3109032	AJU	12/13/2010	Obsolete document.	
*C	3903222	AJU	02/19/2013	Changed from Obsolete to Active. Removed all references of TSOP packages across the document and added 48-ball VFBGA package related information in the corresponding places. Updated Features. Updated Functional Description. Updated Logic Block Diagram. Updated Ordering Information (Updated part numbers) and added Ordering Code Definitions. Updated Package Diagrams: Removed spec 51-85087 and spec 51-85183. Added spec 51-85150. Added Acronyms and Units of Measure. Updated in new template.	
*D	3996550	MEMJ	05/13/2013	Changed status from Preliminary to Final.	
*E	4273754	VINI	02/06/2014	Updated in new template. Completing Sunset Review.	
*F	4571885	VINI	11/17/2014	Added related documentation hyperlink in page 1. Added Note 17 in Switching Characteristics. Added note reference 17 in the Switching Characteristics table. Added Note 27 in Switching Waveforms. Added note reference 27 in Figure 8.	



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