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CY62156ESL MoBL®

8-Mbit (512 K × 16) Static RAM

Features

- High Speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra Low Standby Power
  - Typical standby current: 2 μA
  - Maximum standby current: 8 μA
- Ultra Low Active Power
  - Typical active current: 1.8 mA at f = 1 MHz
- Easy Memory Expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ Features
- Automatic Power Down when Deselected
- CMOS for Optimum Speed and Power
- Available in Pb-free 48-ball very fine-pitch ball grid array (VFBGA) packages

Functional Description

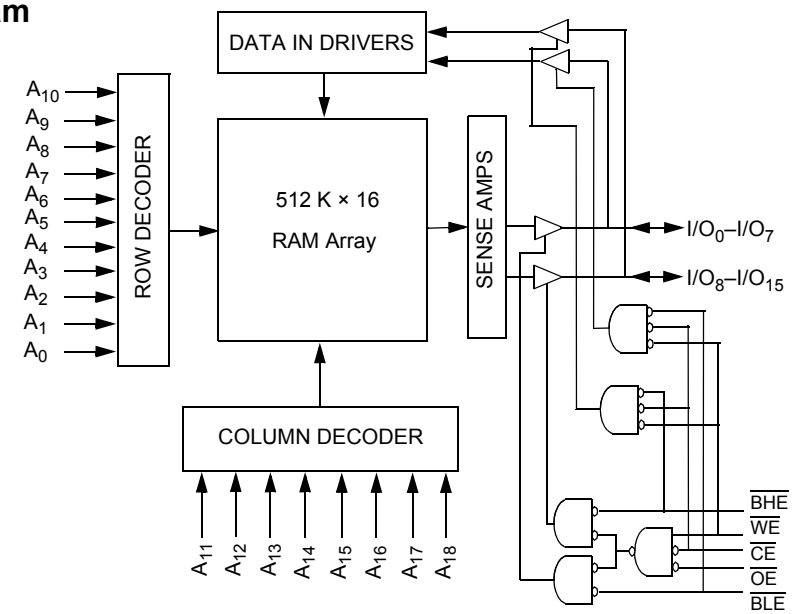
The CY62156ESL is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device in standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW). The input or output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation is active ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.

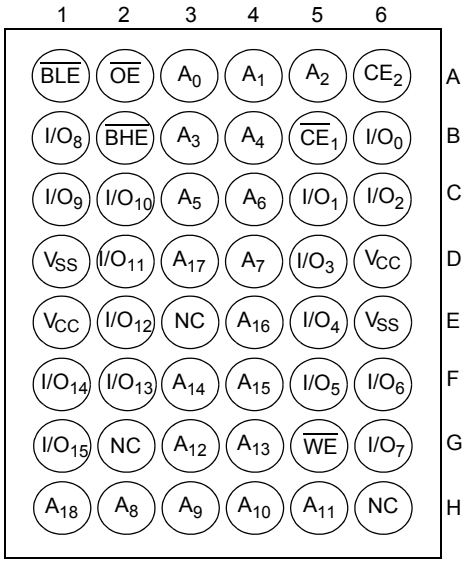
Logic Block Diagram



Contents

Pin Configurations

Figure 1. 48-ball VFBGA pinout (Top View) [1]



Product Portfolio

Product	Range	V_{CC} Range (V) [2]	Speed (ns)	Power Dissipation					
				Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
				f = 1MHz		f = f_{max}			
				Typ [3]	Max	Typ [3]	Max	Typ [3]	Max
CY62156ESL	Industrial	2.2 V to 3.6 V and 4.5 V to 5.5 V	45	1.8	3	18	25	2	8

Notes
1. NC pins are not connected on the die.
2. Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to + 150°C

Ambient Temperature with Power Applied ..... –55 °C to + 125 °C

Supply Voltage to Ground Potential .....–0.5 V to 6.0 V

DC Voltage Applied to Outputs in High Z State [4, 5] .....–0.5 V to 6.0 V

DC Input Voltage [4, 5] .....–0.5 V to 6.0 V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2,001V

Latch Up Current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[6]
CY62156ESL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V, and 4.5 V to 5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ [1]	Max	
V_{OH}	Output HIGH Voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0	–	–	V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4	–	–	
		$4.5 \le V_{CC} \le 5.5$	I_{OH} = –1.0 mA	2.4	–	–	
V_{OL}	Output LOW Voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA	–	–	0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OL} = 2.1mA	–	–	0.4	
		$4.5 \le V_{CC} \le 5.5$	I_{OL} = 2.1mA	–	–	0.4	
V_{IH}	Input HIGH Voltage	$2.2 \le V_{CC} \le 2.7$		1.8	–	V_{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2	–	V_{CC} + 0.3	
		$4.5 \le V_{CC} \le 5.5$		2.2	–	V_{CC} + 0.5	
V_{IL}	Input LOW Voltage	$2.2 \le V_{CC} \le 2.7$		–0.3	–	0.6	V
		$2.7 \le V_{CC} \le 3.6$		–0.3	–	0.8	
		$4.5 \le V_{CC} \le 5.5$		–0.5	–	0.8	
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		–1	–	+1	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled		–1	–	+1	µA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$, I_{OUT} = 0 mA, CMOS levels	–	18	25	mA
		f = 1 MHz		–	1.8	3	
I_{SB1}	Automatic CE Power down Current – CMOS Inputs	$\overline{CE_1} \ge V_{CC}$ – 0.2 V, $CE_2 \le$ 0.2 V, $V_{IN} \ge V_{CC}$ – 0.2 V or $V_{IN} \le$ 0.2 V, f = f_{max} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), $V_{CC} = V_{CC(max)}$		–	2	8	µA
I_{SB2} [7]	Automatic CE Power down Current – CMOS Inputs	$\overline{CE_1} \ge V_{CC}$ – 0.2 V or $CE_2 \le$ 0.2 V, $V_{IN} \ge V_{CC}$ – 0.2 V or $V_{IN} \le$ 0.2 V, f = 0, $V_{CC} = V_{CC(max)}$		–	2	8	µA

Notes

4. V_{IL}(min) = –2.0 V for pulse durations less than 20 ns.
5. V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
6. Full Device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
7. Only chip enables ($\overline{CE_1}$ and CE_2) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

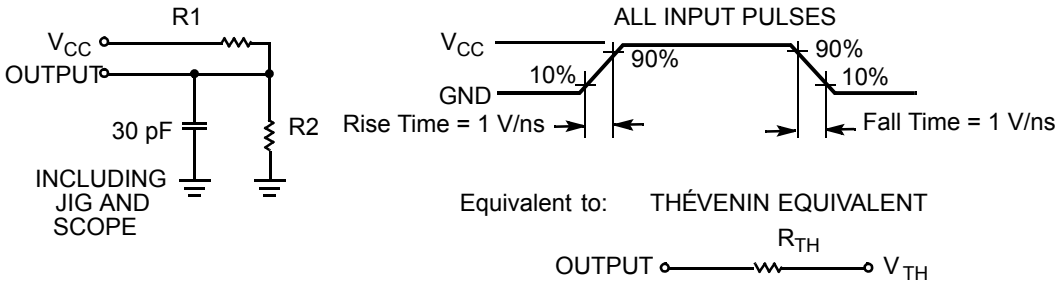
Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	48-ball BGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	72	°C/W
Θ_{JC}	Thermal resistance (junction to case)		8.86	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R_{TH}	8000	645	639	Ω
V_{TH}	1.20	1.75	1.77	V

Note
8. Tested initially and after any design or process changes that may affect these parameters.

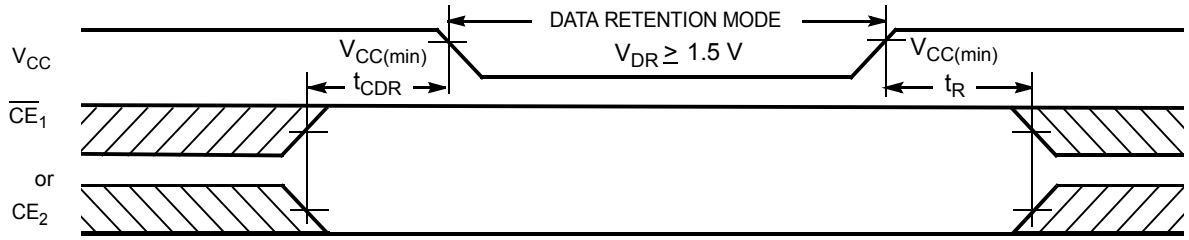
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for Data Retention		1.5	–	–	V
I_{CCDR} [10]	Data Retention Current	$\overline{CE_1} \geq V_{CC} - 0.2$ V, $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $V_{CC} = 1.5$ V	–	2	5	µA
t_{CDR} [11]	Chip Deselect to Data Retention Time		0	–	–	ns
t_R [12]	Operation Recovery Time		45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
10. Only chip enables ($\overline{CE_1}$ and CE_2) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [13]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	45	–	ns
t_{AA}	Address to Data Valid	–	45	ns
t_{OHA}	Data Hold from Address Change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[14]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[14, 15]	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[14]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[14, 15]	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power Up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power Down	–	45	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid	–	22	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z[14]	5	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to High Z[14, 15]	–	18	ns
Write Cycle[16, 17]				
t_{WC}	Write Cycle Time	45	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	35	–	ns
t_{AW}	Address Setup to Write End	35	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Setup to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	35	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	35	–	ns
t_{SD}	Data Setup to Write End	25	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[14, 15]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[14]	10	–	ns

Notes

13. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 2 on page 5.
14. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
15. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
16. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
17. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1: Address Transition Controlled [18, 19]

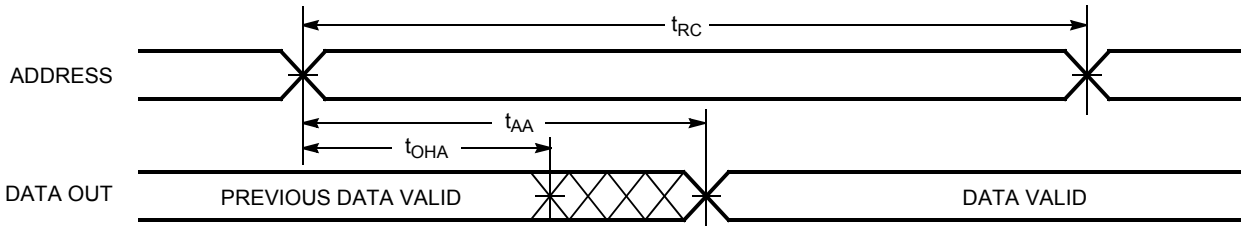
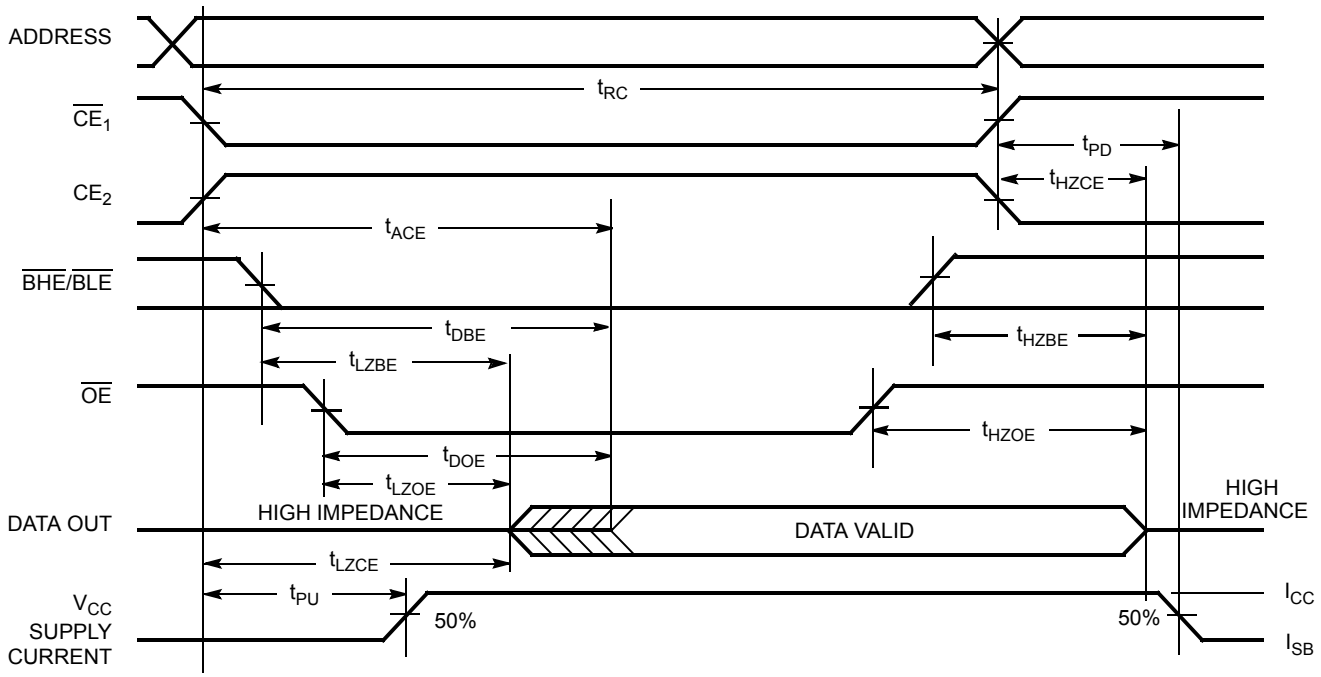


Figure 5. Read Cycle No. 2: $\overline{OE}$ Controlled [19, 20]



Notes
18. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}, and CE_2 = V_{IH}.
19. $\overline{WE}$ is HIGH for read cycle.
20. Address valid before or similar to $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle No 1: $\overline{WE}$ Controlled [21, 22, 23]

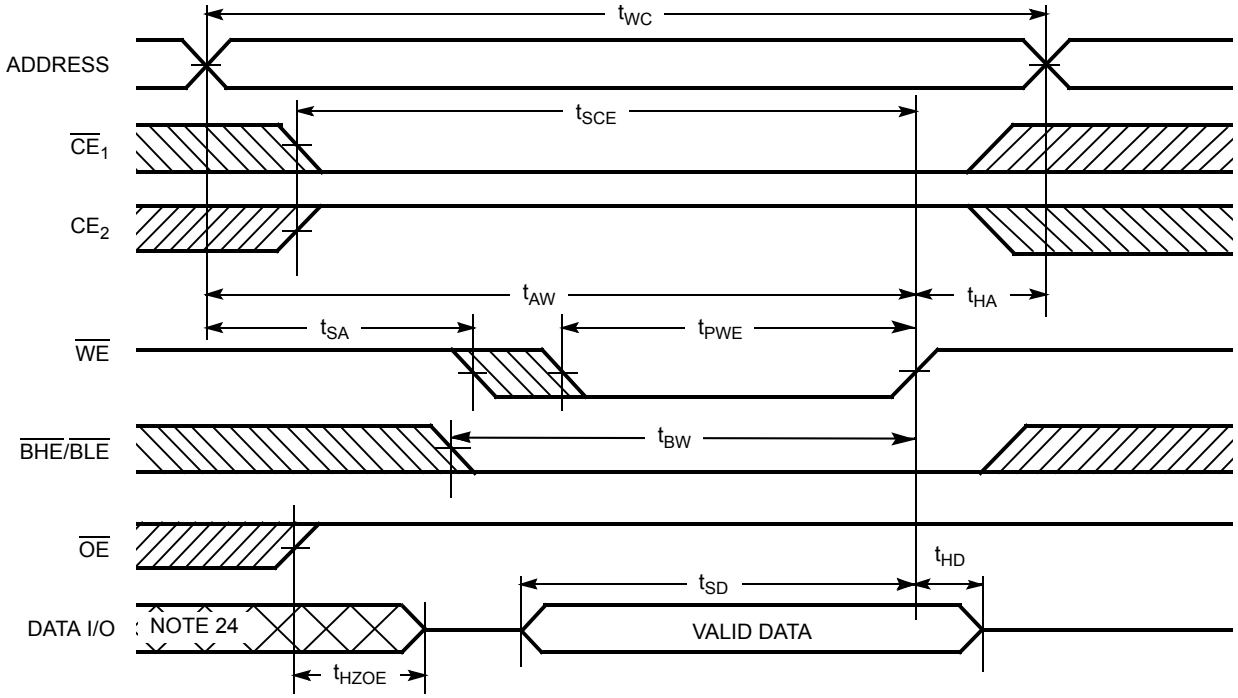
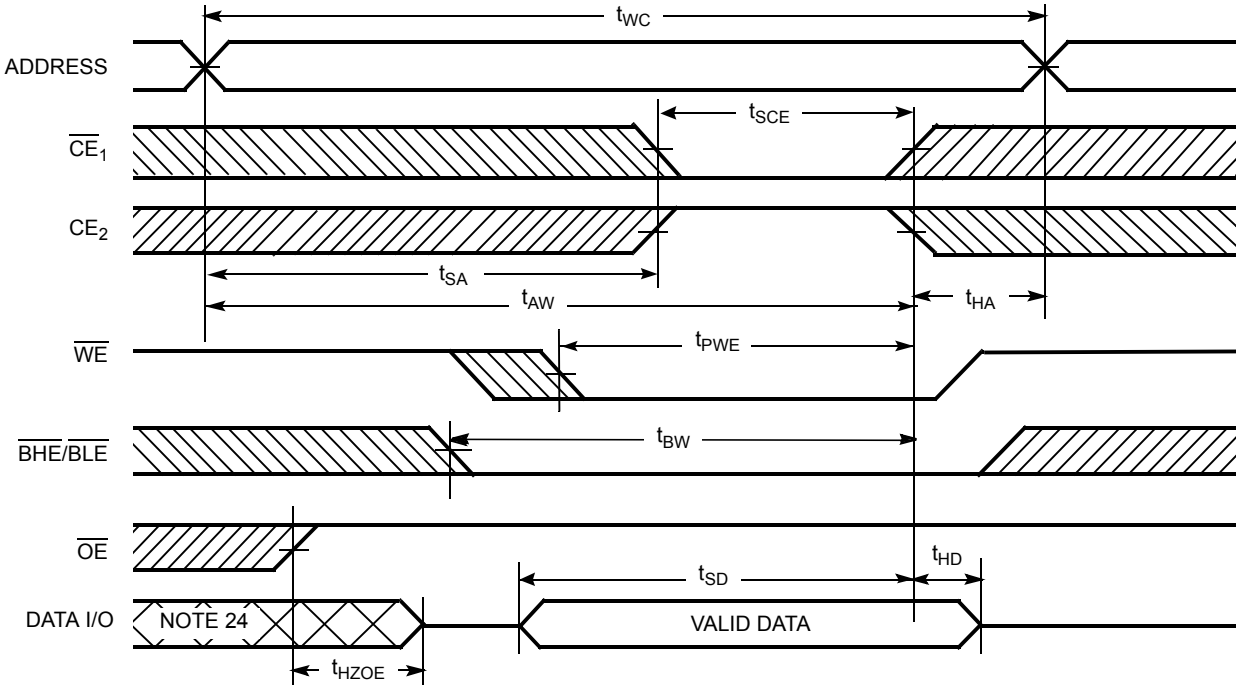


Figure 7. Write Cycle 2: $\overline{CE}$ Controlled [21, 22, 23]



Notes

21. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
22. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
23. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
24. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle 3: $\overline{WE}$ controlled, $\overline{OE}$ LOW [25, 27]

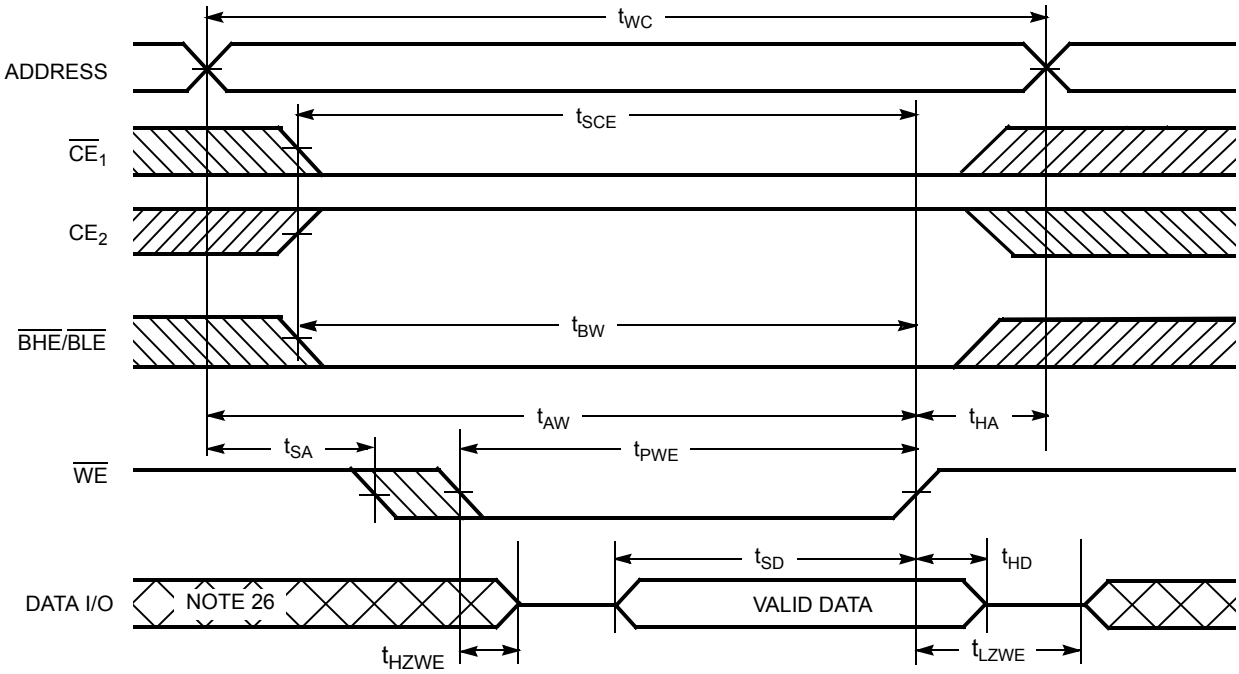
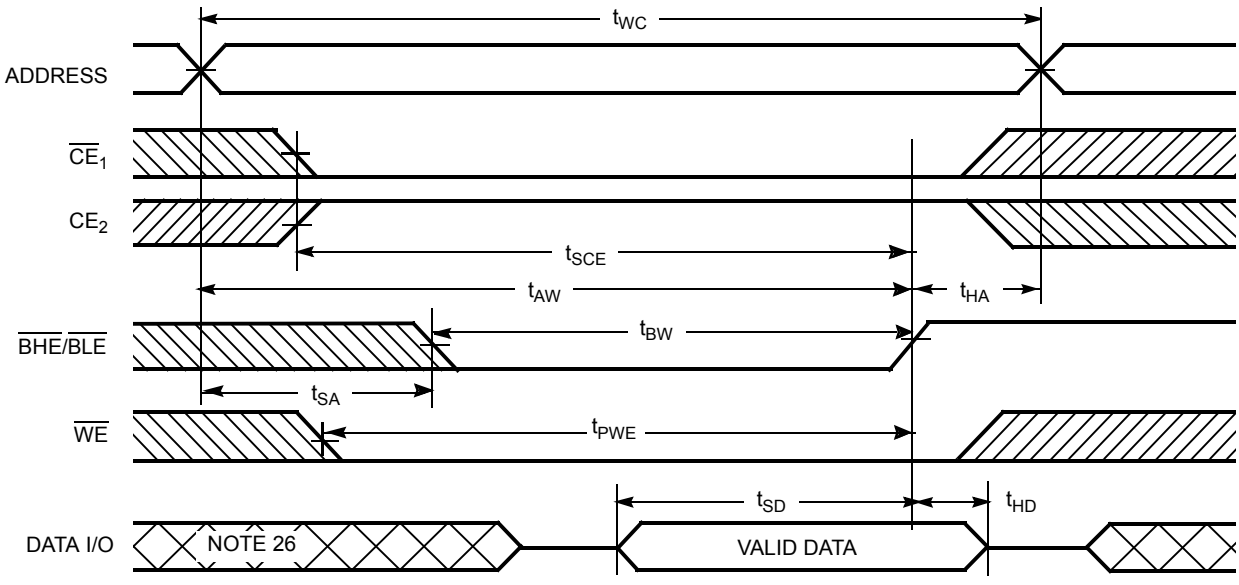


Figure 9. Write Cycle 4: $\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW [25]



Notes
25. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
26. During this period, the I/Os are in output state. Do not apply input signals.
27. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.

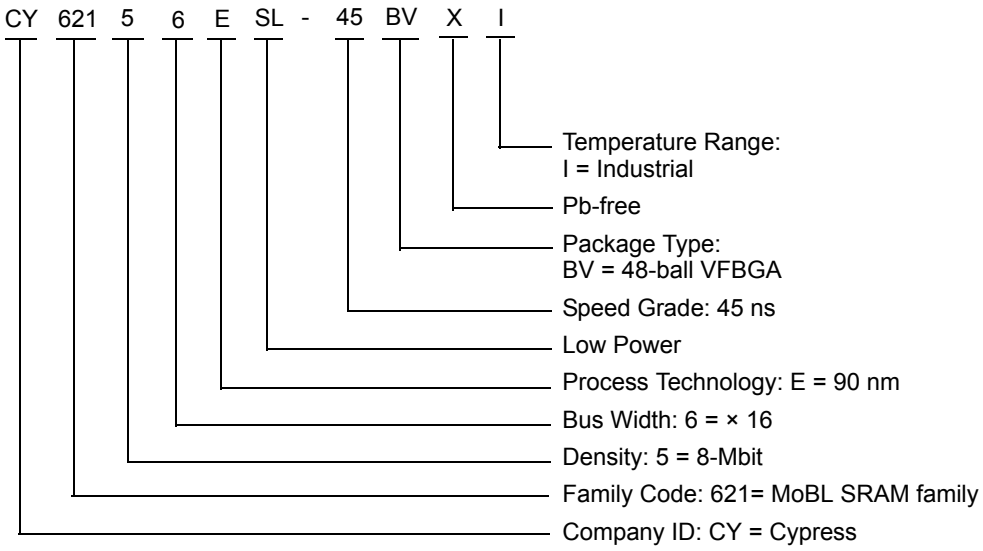
Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
L	H	X	X	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

Ordering Information

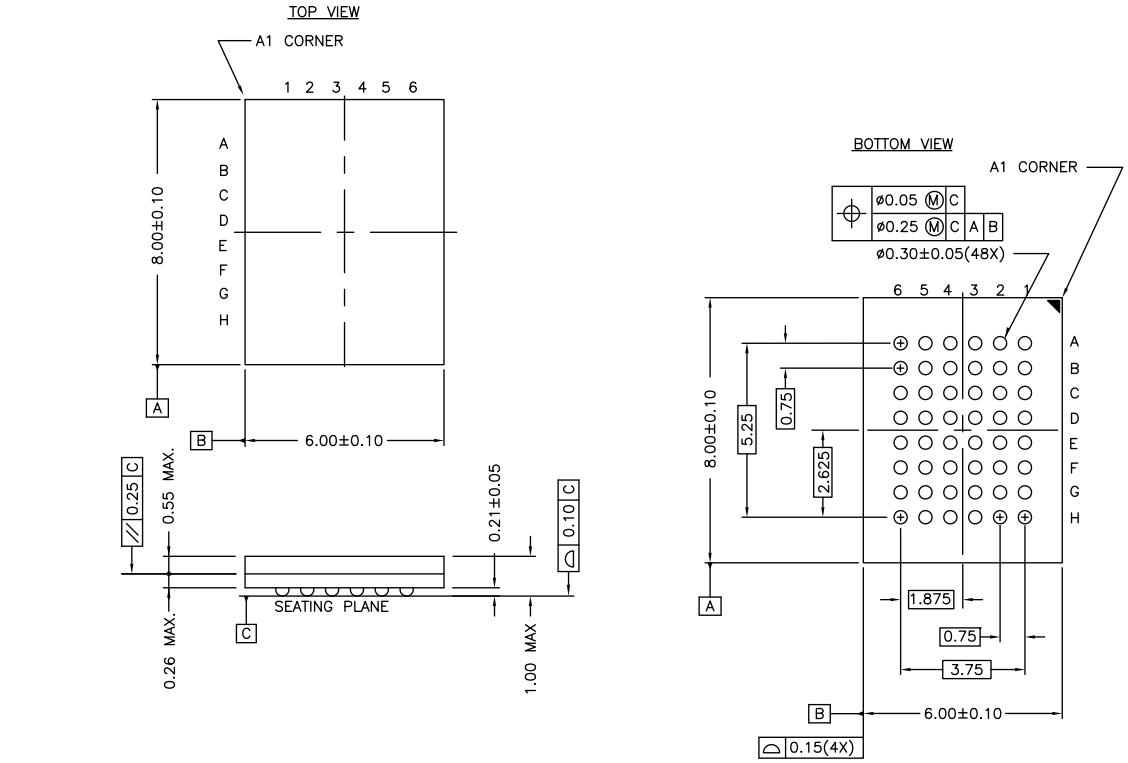
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62156ESL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial

Ordering Code Definitions



Package Diagrams

Figure 10. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
RAM	Random Access Memory
SRAM	Static Random Access Memory
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62156ESL MoBL®, 8-Mbit (512 K × 16) Static RAM Document Number: 001-54995				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2751673	VKN	08/13/09	New data sheet.
*A	2899866	AJU	03/26/10	Removed inactive parts from Ordering Information. Updated Package Diagram.
*B	3109032	AJU	12/13/2010	Obsolete document.
*C	3903222	AJU	02/19/2013	Changed from Obsolete to Active. Removed all references of TSOP packages across the document and added 48-ball VFBGA package related information in the corresponding places. Updated Features. Updated Functional Description. Updated Logic Block Diagram. Updated Ordering Information (Updated part numbers) and added Ordering Code Definitions. Updated Package Diagrams: Removed spec 51-85087 and spec 51-85183. Added spec 51-85150. Added Acronyms and Units of Measure. Updated in new template.
*D	3996550	MEMJ	05/13/2013	Changed status from Preliminary to Final.
*E	4273754	VINI	02/06/2014	Updated in new template. Completing Sunset Review.
*F	4571885	VINI	11/17/2014	Added related documentation hyperlink in page 1. Added Note 17 in Switching Characteristics. Added note reference 17 in the Switching Characteristics table. Added Note 27 in Switching Waveforms. Added note reference 27 in Figure 8.

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