National Semiconductor

PRELIMINARY
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DP8520A/DP8521A/DP8522A microCMOS Programmable 256k/1M/4M Video RAM Controller/Drivers

General Description

The DP8520A/21A/22A video RAM controllers provide a low cost, single chip interface between video RAM and all 8-, 16- and 32-bit systems. The DP8520A/21A/22A generate all the required access control signal timing for VRAMs. An on-chip refresh request clock is used to automatically refresh the VRAM array. Refreshes and accesses are arbitrated on chip. If necessary, a $\overline{WAIT}$ or $\overline{DTACK}$ output inserts wait states into system access cycles, including burst mode accesses. $\overline{RAS}$ low time during refreshes and $\overline{RAS}$ precharge time after refreshes and back to back accesses are guaranteed through the insertion of wait states. Separate on-chip precharge counters for each $\overline{RAS}$ output can be used for memory interleaving to avoid delayed back to back accesses because of precharge. An additional feature of the DP8522A is two access ports to simplify dual accessing. Arbitration among these ports and refresh is done on chip.

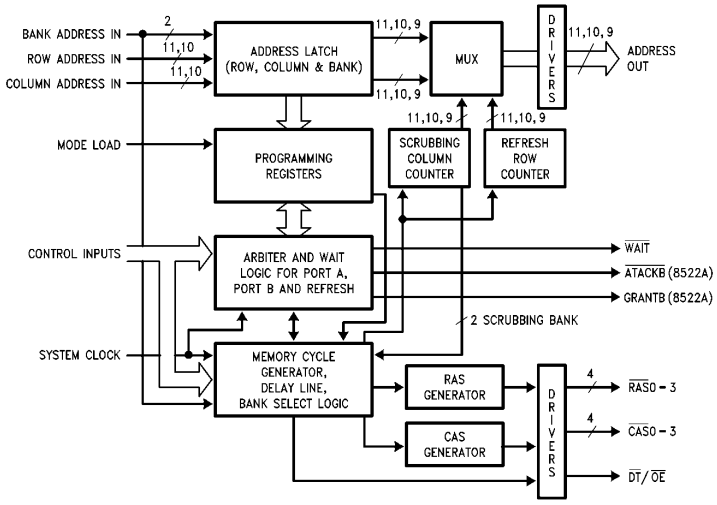
Features

- On chip high precision delay line to guarantee critical VRAM access timing parameters
- microCMOS process for low power
- High capacitance drivers for $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and VRAM address on chip
- On chip support for nibble, page and static column VRAMs
- Byte enable signals on chip allow byte writing in a word size up to 16 bits with no external logic
- Selection of controller speeds: 20 MHz and 25 MHz
- On board Port A/Port B (DP8522A only)/refresh arbitration logic
- Direct interface to all major microprocessors (application notes available)
- 4 $\overline{RAS}$ and 4 $\overline{CAS}$ drivers (the $\overline{RAS}$ and $\overline{CAS}$ configuration is programmable)

Control	# of Pins (PLCC)	# of Address Outputs	Largest VRAM Possible	Direct Drive Memory Capacity	Access Ports Available
DP8520A	68	9	256 kbit	4 Mbytes	Single Access Port
DP8521A	68	10	1 Mbit	16 Mbytes	Single Access Port
DP8522A	84	11	4 Mbit	64 Mbytes	Dual Access Ports (A and B)

Block Diagram

DP8520A/21A/22A VRAM Controller



TL/F/9338–5

FIGURE 1

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1.0 Introduction

The DP8520A/21A/22A are CMOS Video RAM controllers that incorporate many advanced features including the capabilities of address latches, refresh counter, refresh clock, row, column and refresh address multiplexor, delay line, refresh/access/VRAM transfer cycle arbitration logic and high capacitive drivers. The programmable system interface allows any manufacturer's microprocessor or bus to directly interface via the DP8520A/21A/22A to VRAM arrays up to 64 Mbytes in size.

After power up, the DP8520A/21A/22A must first be programmed before accessing the VRAM. The chip is programmed through the address bus.

There are two methods of programming the chip. The first method, mode load only, is accomplished by asserting the signal mode load, $\overline{ML}$. A valid programming selection is presented on the row, column, bank and $\overline{ECAS}$ inputs, then $\overline{ML}$ is negated. When $\overline{ML}$ is negated, the chip is programmed with the valid programming bits on the address bus.

The second method, chip selected access, is accomplished by asserting $\overline{ML}$ and performing a chip selected access. When $\overline{CS}$ and $\overline{AREQ}$ are asserted for the access, the chip is programmed. During this programming access, the programming bits affecting the wait logic become effective immediately, allowing the access to terminate. After the access, $\overline{ML}$ is negated and the rest of the programming bits take effect.

Once the DP8520A/21A/22A has been programmed, a 60 ms initialization period is entered. During this time, the DP8520A/21A/22A controllers perform refreshes to the VRAM array so further VRAM warm up cycles are unnecessary.

The DP8520A/21A/22A can now be used to access the VRAM. There are two modes of accessing with the controller. The two modes are Mode 0, which initiates $\overline{RAS}$ synchronously, and Mode 1, which initiates $\overline{RAS}$ asynchronously.

To access the VRAM using Mode 0, the signal ALE is asserted along with $\overline{CS}$ to ensure a valid VRAM access. ALE asserting sets an internal latch and only needs to be pulsed and not held throughout the entire access. On the next rising clock edge, after the latch is set, $\overline{RAS}$ will be asserted for that access. The DP8520A/21A/22A will place the row address on the VRAM address bus, guarantee the programmed value of row address hold time of the VRAM, place the column address on the VRAM address bus, guarantee the programmed value of column address setup time and assert $\overline{CAS}$. $\overline{AREQ}$ can be asserted anytime after the clock edge which starts the access $\overline{RAS}$. $\overline{RAS}$ and $\overline{CAS}$ will extend until $\overline{AREQ}$ is negated.

The other access mode, Mode 1, is asynchronous to the clock. When $\overline{ADS}$ is asserted, $\overline{RAS}$ is asserted. The DP8520A/21A/22A will place the row address on the VRAM address bus, guarantee the programmed value of row address hold time, place the column address on the VRAM address bus, guarantee the programmed value of column address setup time and assert $\overline{CAS}$. $\overline{AREQ}$ can be tied to $\overline{ADS}$ or can be asserted after $\overline{ADS}$ is asserted. $\overline{AREQ}$ negated will terminate the access.

The DP8520A/21A/22A also provides full support for VRAM transfer cycles. To begin the cycle, the input $\overline{AVSRLRQ}$, Advanced Video Shift Register Load Request, is asserted and must precede the input $\overline{VSRL}$, Video Shift Register Load, asserting by enough CLK periods to guarantee any access in progress or pending refresh can finish. $\overline{VSRL}$ asserting causes $\overline{DT}/\overline{OE}$ to transition low immediately. Both $\overline{VSRL}$ and $\overline{DT}/\overline{OE}$ assert before $\overline{RAS}$ and $\overline{CAS}$ assert for the transfer. The cycle is ended by $\overline{DT}/\overline{OE}$ negating. This is caused by either $\overline{VSRL}$ negating or by four rising edges of CLK from $\overline{VSRL}$ asserting, whichever comes first.

The DP8520A/21A/22A have greatly expanded refresh capabilities compared to other VRAM controllers. There are three modes of refreshing available. These modes are internal automatic refreshing, externally controlled/burst refreshing, and refresh request/acknowledge refreshing. Any of these modes can be used together or separately to achieve the desired results. In any combination of these modes, the programming of $\overline{ECAS}0$ determines the use of the $\overline{RFIP}$ ($\overline{RFRQ}$) pin. $\overline{ECAS}0$ asserted during programming causes this pin to function as $\overline{RFIP}$ which will assert just prior to a refresh cycle and will negate when the refresh is completed. $\overline{ECAS}0$ negated during programming causes this pin to function as $\overline{RFRQ}$ which indicates an internal refresh request when asserted.

When using internal automatic refreshing, the DP8520A/21A/22A will generate an internal refresh request from the refresh request clock. The DP8520A/21A/22A will arbitrate between the refresh requests and accesses. Assuming an access is not currently in progress, the DP8520A/21A/22A will grant a refresh, assert $\overline{RFIP}$ if programmed, and on the next positive clock edge, refreshing will begin. If an access had been in progress, the refresh will begin after the access has terminated.

To use externally controlled/burst refresh, the user disables the internal refresh request by asserting the input $\overline{DISRFRSH}$. A refresh can now be externally requested by asserting the input $\overline{RFSH}$. The DP8520A/21A/22A will arbitrate between the external refresh request and accesses. Assuming an access is not currently in progress, the DP8520A/21A/22A will grant a refresh, assert $\overline{RFIP}$ if programmed, and on the next positive clock edge, refreshing will begin. If an access had been in progress, the refresh would take place after the access has terminated.

With refresh request/acknowledge mode, the DP8520A/21A/22A broadcasts the internal refresh request to the system through the $\overline{RFRQ}$ output pin. External circuitry can determine when to refresh the VRAM through the $\overline{RFSH}$ input.

The controllers have three types of refreshing available: conventional, staggered and error scrubbing. Any refresh control mode can be used with any type of refresh. In a conventional refresh, all of the $\overline{RAS}$ outputs will be asserted and negated at once. In a staggered refresh, the $\overline{RAS}$ outputs will be asserted one positive clock edge apart. Error scrubbing is the same as conventional refresh except that a $\overline{CAS}$ will be asserted during a refresh allowing the system to run that data through an EDAC chip and write it back to memory, if a single bit error has occurred. The refreshes can be extended with the EXTEND REFRESH input, EXTNDRF.

The DP8520A/21A/22A have wait support available as $\overline{DTACK}$ or $\overline{WAIT}$. Both are programmable. $\overline{DTACK}$, Data Transfer ACKnowledge, is useful for processors whose wait signal is active high. $\overline{WAIT}$ is useful for processors whose

1.0 Introduction (Continued)

wait signal is active low. The user can choose either at programming. These signals are used by the on-chip arbitor to insert wait states to guarantee the arbitration between accesses and refreshes or precharge. Both signals are independent of the access mode chosen.

$\overline{\text{DTACK}}$ will assert a programmed number of clock edges from the event that starts the access $\overline{\text{RAS}}$. $\overline{\text{DTACK}}$ will be negated, when the access is terminated, by $\overline{\text{AREQ}}$ being negated. $\overline{\text{DTACK}}$ can also be programmed to toggle with the $\overline{\text{ECAS}}$ inputs during burst/page mode accesses.

$\overline{\text{WAIT}}$ is asserted during the start of the access (ALE and $\overline{\text{CS}}$, or $\overline{\text{ADS}}$ and $\overline{\text{CS}}$) and will negate a number of clock edges from the event that starts the access $\overline{\text{RAS}}$. After $\overline{\text{WAIT}}$ is negated, it will stay negated until the next access. $\overline{\text{WAIT}}$ can also be programmed to toggle with $\overline{\text{ECAS}}$ inputs during a burst/page mode access.

Both signals can be dynamically delayed further through the $\overline{\text{WAITIN}}$ signal to the DP8520A/21A/22A.

The DP8520A/21A/22A have address latches, used to latch the bank, row and column address inputs. Once the address is latched, a column increment feature can be used to increment the column address. The address latches can also be programmed to be fall through.

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ drivers can be configured to drive a one, two or four bank memory array up to 32 bits in width. The two $\overline{\text{ECAS}}$ signals can then be used to select one pair of $\overline{\text{CAS}}$ drivers for byte writing with no external logic for systems with a word length of up to 16 bits.

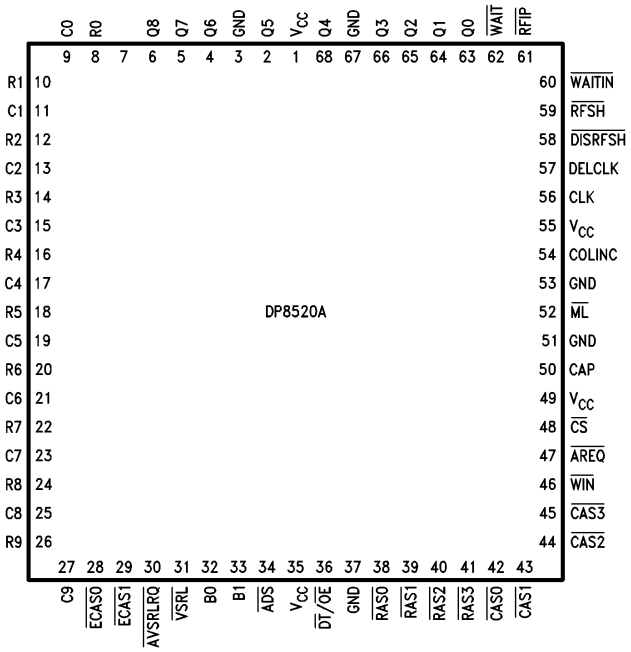
When configuring the DP8520A/21A/22A for more than one bank, memory interleaving can be used. By tying the low order address bits to the bank select lines, B0 and B1, sequential back to back accesses will not be delayed since the DP8520A/21A/22A have separate precharge counters per bank. The DP8520A/21A/22A are capable of performing address pipelining. In address pipelining, the DP8520A/21A/22A guarantee the column address hold time and switch the internal multiplexor to place the row address on the address bus. At this time, another memory access to another bank can be initiated.

The DP8522A has all the features previously mentioned. Unlike the DP8520A/21A, the DP8522A has a second port to allow a second CPU to access the memory array. This port, Port B, has two control signals to allow a CPU to access the VRAM array. These signals are access request for Port B, $\overline{\text{AREQB}}$, and Advanced Transfer ACKnowledge for Port B, $\overline{\text{ATACKB}}$. Two other signals are used by both Port A and Port B for dual accessing purposes. The signals are lock, $\overline{\text{LOCK}}$ and grant Port B, GRANTB. All arbitration for the two ports and refresh is done on-chip by the DP8522A through the insertion of wait states. Since the DP8522A has only one input address bus, the address lines have to be multiplexed externally. The signal GRANTB can be used for this purpose since it is asserted when Port B has access to the VRAM array and negated when Port A has access to the VRAM array. Once a port has access to the array, the other port can be ''locked out'' by asserting the input $\overline{\text{LOCK}}$. $\overline{\text{AREQB}}$, when asserted, is used by Port B to request an access. $\overline{\text{ATACKB}}$, when asserted, signifies that access $\overline{\text{RAS}}$ has been asserted for the requested Port B access. By using $\overline{\text{ATACKB}}$, the user can generate an appropriate $\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$ like signal for the Port B CPU.

The following explains the terminology used in this data sheet. The terms negated and asserted are used. Asserted refers to a ''true'' signal. Thus, ''$\overline{\text{ECAS}}$0 asserted'' means the $\overline{\text{ECAS}}$0 input is at a logic 0. The term ''COLINC asserted'' means the COLINC input is at a logic 1. The term negated refers to a ''false'' signal. Thus, ''$\overline{\text{ECAS}}$0 negated'' means the $\overline{\text{ECAS}}$0 input is at a logic 1. The term ''COLINC negated'' means the input COLINC is at a logic 0. The table shown below clarifies this terminology.

Signal	Action	Logic Level
Active High	Asserted	High
Active High	Negated	Low
Active Low	Asserted	Low
Active Low	Negated	High

Connection Diagrams



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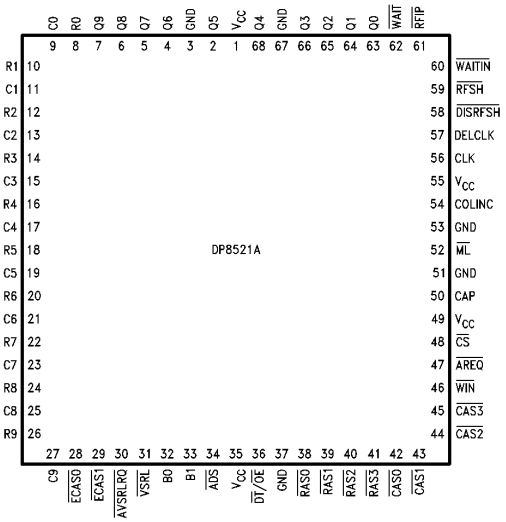
Top View

FIGURE 2

Order Number DP8520AV-20 or DP8520AV-25
See NS Package Number V68A

Connection Diagrams (Continued)



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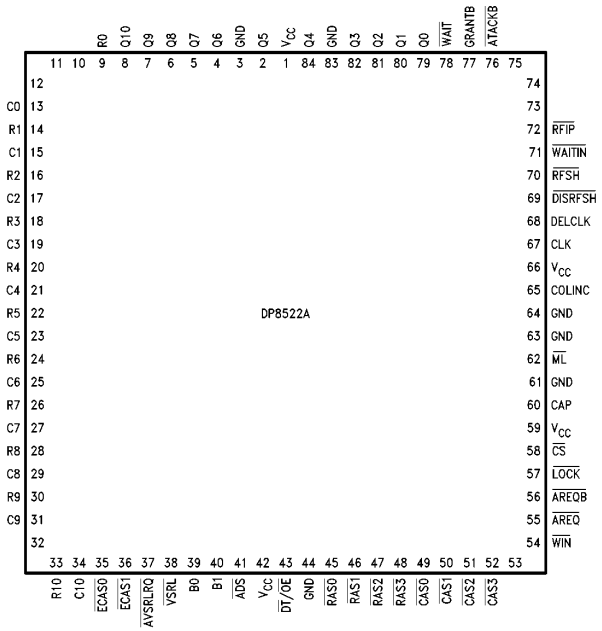
Top View

FIGURE 3

Order Number DP8521AV-20 or DP8521AV-25
See NS Package Number V68A



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Top View

FIGURE 4

Order Number DP8522AV-20 or DP8522AV-25
See NS Package Number V84A

2.0 Signal Descriptions

Pin Name	Device (If not applicable to all)	Input/ Output	Description
2.1 ADDRESS, R/W AND PROGRAMMING SIGNALS			
R0–10 R0–9	DP8522A DP8520A/21A	I I	**ROW ADDRESS:** These inputs are used to specify the row address during an access or refresh to the VRAM or for a VRAM transfer cycle. They are also used to program the chip when $\overline{ML}$ is asserted (except R10).
C0–10 C0–9	DP8522A DP8520A/21A	I I	**COLUMN ADDRESS:** These inputs are used to specify the column address during an access to the VRAM or for a VRAM transfer cycle. They are also used to program the chip when $\overline{ML}$ is asserted (except C10).
B0, B1		I	**BANK SELECT:** Depending on programming, these inputs are used to select a group of $\overline{RAS}$ and $\overline{CAS}$ outputs to assert during an access. They are also used to program the chip when $\overline{ML}$ is asserted.
$\overline{ECAS}$0–1		I	**ENABLE $\overline{CAS}$:** These inputs are used to enable a single or group of $\overline{CAS}$ outputs when asserted. In combination with the B0, B1 and the programming bits, these inputs select which $\overline{CAS}$ output or $\overline{CAS}$ outputs will assert during an access. $\overline{ECAS}$0 must be asserted for either $\overline{CAS}$0 or $\overline{CAS}$1 to assert during an access. $\overline{ECAS}$1 must be asserted for either $\overline{CAS}$2 or $\overline{CAS}$3 to assert during an access. The $\overline{ECAS}$ signals can also be used to toggle a group of $\overline{CAS}$ outputs for page/nibble mode accesses. They also can be used for byte write operations. If $\overline{ECAS}$0 is negated during programming, continuing to assert the $\overline{ECAS}$0 while negating $\overline{AREQ}$ or $\overline{AREQB}$ during an access, will cause the $\overline{CAS}$ outputs to be extended while the $\overline{RAS}$ outputs are negated (the $\overline{ECAS}$n inputs have no effect during scrubbing refreshes).
$\overline{WIN}$		I	**WRITE ENABLE IN:** This input is used to signify a write operation to the VRAM. This input asserted will also cause $\overline{CAS}$ to delay to the next positive clock edge if address bit C9 is asserted during programming.
COLINC (EXTNDRF)		I I	**COLUMN INCREMENT:** When the address latches are used, and a refresh is not in progress, this input functions as COLINC. Asserting this signal causes the column address to be incremented by one. When a refresh is in progress, this signal, when asserted, is used to extend the refresh cycle by any number of periods of CLK until it is negated.
$\overline{ML}$		I	**MODE LOAD:** This input signal, when low, enables the internal programming register that stores the programming information.
2.2 VRAM CONTROL SIGNALS			
Q0–10 Q0–9 Q0–8	DP8522A DP8521A DP8521A	O O O	**VRAM ADDRESS:** These outputs are the multiplexed output of the R0–9, 10 and C0–9, 10 and form the VRAM address bus. These outputs contain the refresh address whenever a refresh is in progress. They contain high capacitive drivers with 20Ω series damping resistors.
$\overline{RAS}$0–3		O	**ROW ADDRESS STROBES:** These outputs are asserted to latch the row address contained on the outputs Q0–8, 9, 10 into the VRAM. When a refresh is in progress, the $\overline{RAS}$ outputs are used to latch the refresh row address contained on the Q0–8, 9, 10 outputs in the VRAM. These outputs contain high capacitive drivers with 20Ω series damping resistors.
$\overline{CAS}$0–3		O	**COLUMN ADDRESS STROBES:** These outputs are asserted to latch the column address contained on the outputs Q0–8, 9, 10 into the VRAM. These outputs have high capacitive drivers with 20Ω series damping resistors.
$\overline{DT}/\overline{OE}$		O	**DATA TRANSFER/OUTPUT ENABLE:** This output transitions low before $\overline{RAS}$ goes low and transitions high before $\overline{RAS}$ goes high during a video RAM shift register load operation (see $\overline{VSRL}$ pin description). During normal write accesses this output is held high, and for read accesses this output is asserted after $\overline{CAS}$ is asserted, and is negated after $\overline{CAS}$ negates.

2.0 Signal Descriptions (Continued)

Pin Name	Device (If not applicable to all)	Input/ Output	Description
2.3 REFRESH SIGNALS			
$\overline{\text{RFIP}}$($\overline{\text{RFRQ}}$)		O	**REFRESH IN PROGRESS** or **REFRESH REQUEST:** When $\overline{\text{ECAS}}$0 is asserted during programming, this output functions as $\overline{\text{RFIP}}$, and is asserted prior to a refresh cycle and is negated when all the $\overline{\text{RAS}}$ outputs are negated for that refresh. When $\overline{\text{ECAS}}$0 is negated during programming, this output functions as $\overline{\text{RFRQ}}$. When asserted, this pin specifies that 13 μs or 15 μs have passed. If $\overline{\text{DISRFSH}}$ is negated, the DP8520A/21A/22A will perform an internal refresh as soon as possible. If $\overline{\text{DISRFRSH}}$ is asserted, $\overline{\text{RFRQ}}$ can be used to externally request a refresh through the input $\overline{\text{RFSH}}$. This output has a high capacitive driver and a 20Ω series damping resistor.
$\overline{\text{RFSH}}$		I	**REFRESH:** This input asserted with $\overline{\text{DISRFRSH}}$ already asserted will request a refresh. If this input is continually asserted, the DP8520A/21A/22A will perform refresh cycles in a burst refresh fashion until the input is negated. If $\overline{\text{RFSH}}$ is asserted with $\overline{\text{DISRFSH}}$ negated, the internal refresh address counter is cleared (useful for burst refreshes).
$\overline{\text{DISRFSH}}$		I	**DISABLE REFRESH:** This input is used to disable internal refreshes and must be asserted when using $\overline{\text{RFSH}}$ for externally requested refreshes.
2.4 PORT A ACCESS			
$\overline{\text{ADS}}$ (ALE)		I I	**ADDRESS STROBE** or **ADDRESS LATCH ENABLE:** Depending on programming, this input can function as $\overline{\text{ADS}}$ or ALE. In mode 0, the input functions as ALE and when asserted along with $\overline{\text{CS}}$ causes an internal latch to be set. Once this latch is set an access will start from the positive clock edge of CLK as soon as possible. In Mode 1, the input functions as $\overline{\text{ADS}}$ and when asserted along with $\overline{\text{CS}}$, causes the access $\overline{\text{RAS}}$ to assert if no other event is taking place. If an event is taking place, $\overline{\text{RAS}}$ will be asserted from the positive edge of CLK as soon as possible. In both cases, the low going edge of this signal latches the bank, row and column address if programmed to do so.
$\overline{\text{CS}}$		I	**CHIP SELECT:** This input signal must be asserted to enable a Port A access.
$\overline{\text{AREQ}}$		I	**ACCESS REQUEST:** This input signal in Mode 0 must be asserted some time after the first positive clock edge after ALE has been asserted. When this signal is negated, $\overline{\text{RAS}}$ is negated for the access. In Mode 1, this signal must be asserted before $\overline{\text{ADS}}$ can be negated. When this signal is negated, $\overline{\text{RAS}}$ is negated for the access.
$\overline{\text{WAIT}}$ ($\overline{\text{DTACK}}$)		O O	**WAIT** or **DTACK:** This output can be programmed to insert wait states into a CPU access cycle. With R7 negated during programming, the output will function as a $\overline{\text{WAIT}}$ type output. In this case, the output will be active low to signal a wait condition. With R7 asserted during programming, the output will function as $\overline{\text{DTACK}}$. In this case, the output will be negated to signify a wait condition and will be asserted to signify the access has taken place. Each of these signals can be delayed by a number of positive clock edges or negative clock levels of CLK to increase the microprocessor's access cycle through the insertion of wait states.
$\overline{\text{WAITIN}}$		I	**WAIT INCREASE:** This input can be used to dynamically increase the number of positive clock edges of CLK until $\overline{\text{DTACK}}$ will be asserted or $\overline{\text{WAIT}}$ will be negated during a VRAM access.
2.5 PORT B ACCESS SIGNALS			
$\overline{\text{AREQB}}$	DP8522A only	I	**PORT B ACCESS REQUEST:** This input asserted will latch the row, column and bank address if programmed, and requests an access to take place for Port B. If the access can take place, $\overline{\text{RAS}}$ will assert immediately. If the access has to be delayed, $\overline{\text{RAS}}$ will assert as soon as possible from a positive edge of CLK.
$\overline{\text{ATACKB}}$	DP8522A only	O	**ADVANCED TRANSFER ACKNOWLEDGE PORT B:** This output is asserted when the access $\overline{\text{RAS}}$ is asserted for a Port B access. This signal can be used to generate the appropriate $\overline{\text{DTACK}}$ or $\overline{\text{WAIT}}$ type signal for Port B's CPU or bus.

2.0 Signal Descriptions (Continued)

Pin Name	Device (If not applicable to all)	Input/ Output	Description
2.6 COMMON DUAL PORT SIGNALS			
GRANTB	DP8522A only	O	**GRANT B:** This output indicates which port is currently granted access to the VRAM array. When GRANTB is asserted, Port B has access to the array. When GRANTB is negated, Port A has access to the VRAM array. This signal is used to multiplex the signals R0–8, 9, 10; C0–8, 9, 10; B0–1; $\overline{WIN}$; $\overline{LOCK}$ and $\overline{ECAS}$0–1 to the DP8522A when using dual accessing.
$\overline{LOCK}$	DP8522A only	I	**LOCK:** This input can be used by the currently granted port to ''lock out'' the other port from the VRAM array by inserting wait states into the locked out port's access cycle until $\overline{LOCK}$ is negated.
2.7 VRAM TRANSFER CYCLE SIGNALS			
$\overline{AVSRLRQ}$		I	**ADVANCED VIDEO SHIFT REGISTER LOAD REQUEST:** This must precede the $\overline{VSRL}$ input going low by the amount of time necessary to guarantee that any currently executing access and pending refresh can finish. This input disables Port B and refresh requests until four CLK periods after $\overline{VSRL}$ has transitioned low. This input may be held low until the video RAM transfer cycle is completed or may be momentarily pulsed low.
$\overline{VSRL}$		I	**VIDEO SHIFT REGISTER LOAD:** This input causes the $\overline{DT}/\overline{OE}$ output to transition low immediately. Therefore, when executing a video RAM shift register load, $\overline{VSRL}$ transitions low before $\overline{RAS}$ goes low. The $\overline{DT}/\overline{OE}$ output will transition high from $\overline{VSRL}$ going high or four CLK periods (rising clock edges) from $\overline{VSRL}$ going low, whichever occurs first. $\overline{VSRL}$ low also disables the $\overline{WIN}$ input from affecting the $\overline{DT}/\overline{OE}$ logic, until the video shift register load access is over.
2.8 POWER SIGNALS AND CAPACITOR INPUT			
V_{CC}		I	**POWER:** Supply Voltage.
GND		I	**GROUND:** Supply Voltage Reference.
CAP		I	**CAPACITOR:** This input is used by the internal PLL for stabilization. The value of the ceramic capacitor should be 0.1 μF and should be connected between this input and ground.
2.9 CLOCK INPUTS There are two clock inputs to the DP8520A/21A/22A, CLK and DELCLK. These two clocks may both be tied to the same clock input, or they may be two separate clocks, running at different frequencies, asynchronous to each other.			
CLK		I	**SYSTEM CLOCK:** This input may be in the range of 0 Hz up to 25 MHz. This input is generally a constant frequency but it may be controlled externally to change frequencies or perhaps be stopped for some arbitrary period of time. This input provides the clock to the internal state machine that arbitrates between accesses and refreshes. This clock's positive edges and negative levels are used to extend the $\overline{WAIT}$ ($\overline{DTACK}$) signals. Ths clock is also used as the reference for the $\overline{RAS}$ precharge time and $\overline{RAS}$ low time during refresh. All Port A and Port B accesses are assumed to be synchronous to the system clock CLK.
DELCLK		I	**DELAY LINE CLOCK:** The clock input DELCLK, may be in the range of 6 MHz to 20 MHz and should be a multiple of 2 (i.e., 6, 8, 10, 12, 14, 16, 18, 20 MHz) to have the DP8520A/21A/22A switching characteristics hold. If DELCLK is not one of the above frequencies the accuracy of the internal delay line will suffer. This is because the phase locked loop that generates the delay line assumes an input clock frequency of a multiple of 2 MHz. For example, if the DELCLK input is at 7 MHz and we choose a divide by 3 (program bits C0–2) this will produce 2.333 MHz which is 16.667% off of 2 MHz. Therefore, the DP8520A/21A/22A delay line would produce delays that are shorter (faster delays) than what is intended. If divide by 4 was chosen the delay line would be longer (slower delays) than intended (1.75 MHz instead of 2 MHz). (See Section 10 for more information.) This clock is also divided to create the internal refresh clock.

3.0 Port A Access Modes

The DP8520A/21A/22A have two general purpose access modes. With one of these modes, any microprocessor can be interfaced to VRAM. A Port A access to VRAM is initiated by two input signals: $\overline{ADS}$ (ALE) and $\overline{CS}$. The access is always terminated by one signal: $\overline{AREQ}$. These input signals should be synchronous to the input clock, CLK. One of these access modes is selected at programming through the B1 input signal. In both modes, once an access has been requested by $\overline{CS}$ and $\overline{ADS}$ (ALE), the DP8522A will guarantee the following:

The DP8520A/21A/22A will have the row address valid to the VRAMs' address bus, Q0–8, 9, 10 given that the row address setup time to the DP8520A/21A/22A was met;

The DP8520A/21A/22A will bring the appropriate $\overline{RAS}$ or $\overline{RAS}$s low;

The DP8520A/21A/22A will guarantee the minimum row address hold time, before switching the internal multiplexor to place the column address on the VRAM address bus, Q0–8, 9, 10;

The DP8520A/21A/22A will guarantee the minimum column address setup time before asserting the appropriate $\overline{CAS}$ or $\overline{CAS}$s;

The DP8520A/21A/22A will hold the column address valid the minimum specified column address hold time in address pipelining mode and will hold the column address valid the remainder of the access in non-pipelining mode.

The chip includes a $\overline{WIN}$ pin to signify a write operation to the DP8520A/21A/22A. When asserted, $\overline{WIN}$ will cause $\overline{CAS}$ to delay to the next positive clock edge if address bit C9 is asserted during programming. When negated, $\overline{WIN}$ will cause the $\overline{DT}/\overline{OE}$ output to follow the $\overline{CAS}$ outputs for a read access, if $\overline{ECAS0}$ is negated during programming. $\overline{WE}$, write enable, must be externally gated from the processor to the VRAM as there is no output pin from the $\overline{WIN}$ input pin available on chip.

3.1 ACCESS MODE 0

Access Mode 0, shown in *Figure 5a,* is selected by negating the input B1 during programming. This access mode allows accesses to VRAM to always be initiated from the positive edge of the system input clock, CLK. To initiate a Mode 0 access, ALE is pulsed high and $\overline{CS}$ is asserted. Pulsing ALE high and asserting $\overline{CS}$, sets an internal latch which requests an access. If the precharge time from the last access or VRAM refresh had been met and a refresh of VRAM, a Port B access, or a VRAM transfer cycle was not in progress, the $\overline{RAS}$ or group of $\overline{RAS}$s would be initiated from the first positive edge of CLK. If a VRAM refresh is in progress or precharge time is required, the controller will wait until these events have taken place and assert $\overline{RAS}$ on the next positive edge of CLK.

Sometime after the first positive edge of CLK after ALE and $\overline{CS}$ have been asserted, the input $\overline{AREQ}$ must be asserted. In single port applications, once $\overline{AREQ}$ has been asserted, $\overline{CS}$ can be negated. Once $\overline{AREQ}$ is negated, $\overline{RAS}$ and $\overline{DTACK}$, if programmed, will be negated. If $\overline{ECAS0}$ is asserted during programming, $\overline{CAS}$ will be negated with $\overline{AREQ}$. If $\overline{ECAS0}$ was negated during programming, a single $\overline{CAS}$ or group of $\overline{CAS}$s will continue to be asserted after $\overline{RAS}$ has been negated given that the appropriate $\overline{ECAS}$s inputs were asserted as shown in *Figure 5b*. This allows the VRAM to have data present on the data out bus while gaining $\overline{RAS}$ precharge time. ALE can stay asserted several periods of CLK. However, ALE must be negated before or during the period of CLK in which $\overline{AREQ}$ is negated.

When performing address pipelining, the ALE input cannot be asserted to start another access until $\overline{AREQ}$ has been asserted for at least one clock period of CLK for the present access.

3.2 ACCESS MODE 1

Access Mode 1, shown in *Figure 6a*, is selected by asserting the input B1 during programming. This mode allows accesses, which are not delayed by precharge, Port B access, VRAM transfer cycle or refresh, to start immediately from the access request input, $\overline{ADS}$. To initiate a Mode 1 access, $\overline{CS}$ is asserted followed by $\overline{ADS}$ asserted. If the programmed precharge time from the last access or VRAM refresh had been met and a refresh of the VRAM, a Port B access to the VRAM, or a VRAM transfer cycle was not in progress, the $\overline{RAS}$ or group of $\overline{RAS}$s selected by programming and the bank select inputs would be asserted from $\overline{ADS}$ being asserted. If a VRAM refresh, a Port B access, or a VRAM transfer cycle is in progress or precharge time is required, the controller will wait until these events have taken place and assert $\overline{RAS}$ or the group of $\overline{RAS}$s from the next positive edge of CLK.

When $\overline{ADS}$ is asserted or sometime after, $\overline{AREQ}$ must be asserted. At this time, $\overline{ADS}$ can be negated and $\overline{AREQ}$ will continue the access. Once $\overline{AREQ}$ is negated, $\overline{RAS}$ and $\overline{DTACK}$, if programmed, will be negated. If $\overline{ECAS0}$ was asserted during programming, $\overline{CAS}$ will be negated with $\overline{AREQ}$. If $\overline{ECAS0}$ was negated during programming, a single $\overline{CAS}$ or group of $\overline{CAS}$s will continue to be asserted after $\overline{RAS}$ has been negated given that the appropriate $\overline{ECAS}$ inputs were asserted as shown in *Figure 6b*. This allows a VRAM to have data present on the data out bus while gaining $\overline{RAS}$ precharge time. $\overline{ADS}$ can continue to be asserted after $\overline{AREQ}$ has been asserted and negated, however a new access would not be started until $\overline{ADS}$ is negated and asserted again. $\overline{ADS}$ and $\overline{AREQ}$ can be tied together in applications not using address pipelining.

If address pipelining is programmed, it is possible for $\overline{ADS}$ to be negated after $\overline{AREQ}$ is asserted. Once $\overline{AREQ}$ is asserted, $\overline{ADS}$ can be asserted again to initiate a new access.

3.0 Port A Access Modes (Continued)

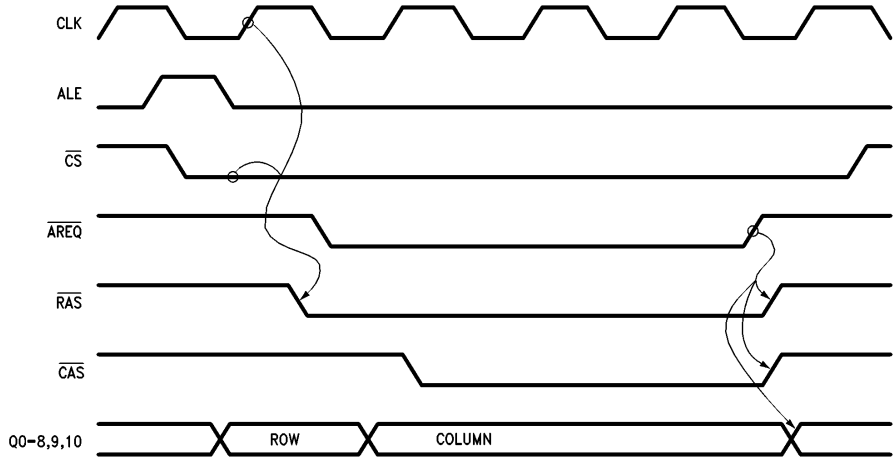

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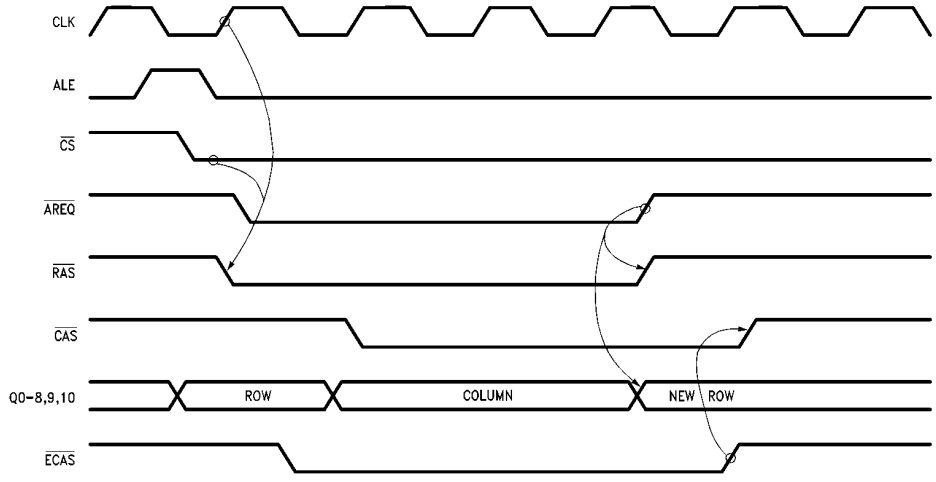
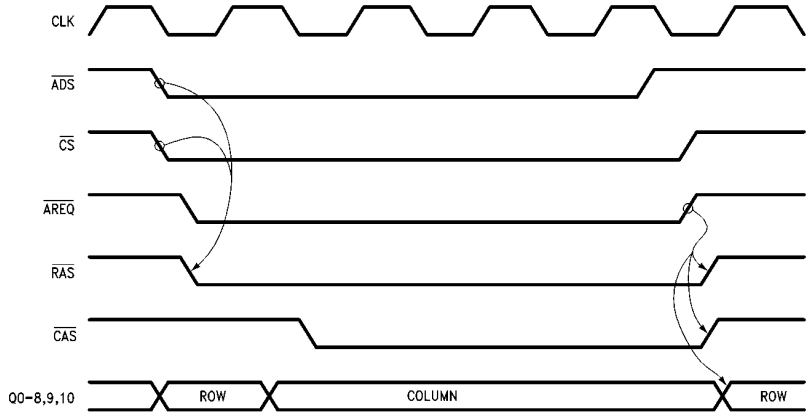
FIGURE 5a. Access Mode 0



TL/F/9338–7

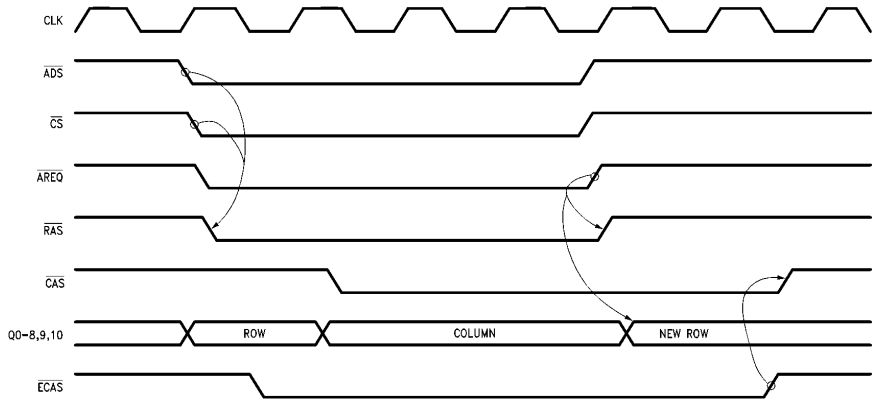
FIGURE 5b. Access Mode 0 Extending $\overline{CAS}$

3.0 Port A Access Modes (Continued)



TL/F/9338–8

FIGURE 6a. Access Mode 1



TL/F/9338–9

FIGURE 6b. Access Mode 1 Extending $\overline{CAS}$

4.0 Refresh Options

The DP8520A/21A/22A support a wide variety of refresh control mode options including automatic internally controlled refresh, externally controlled/burst refresh, refresh request/acknowledge and any combination of the above. With each of the control modes above, different types of refreshes can be performed. These different types include all $\overline{RAS}$ refresh, staggered refresh and error scrubbing during all $\overline{RAS}$ refresh.

There are three inputs, EXTNDRF, $\overline{RFSH}$ and $\overline{DISRFSH}$, and one output, $\overline{RFIP}$ ($\overline{RFRQ}$), associated with refresh. There are also ten programming bits; R0–1, R9, C0–6 and $\overline{ECAS}$0 used to program the various types of refreshing.

The two inputs, $\overline{RFSH}$ and $\overline{DISRFSH}$, are used in the externally controlled/burst refresh mode and the refresh request/acknowledge mode. The output $\overline{RFRQ}$ is used in the refresh request/acknowledge mode. The input EXTNDRF is used in all refresh modes and the output $\overline{RFIP}$ is used in all refresh modes except the refresh request/acknowledge mode. Asserting the input EXTNDRF, extends the refresh cycle single or multiple integral clock periods of CLK. The output $\overline{RFIP}$ is asserted one period of CLK before the first refresh $\overline{RAS}$ is asserted. If an access is currently in progress, $\overline{RFIP}$ will be asserted up to one period of CLK before the first refresh $\overline{RAS}$, once $\overline{AREQ}$ or $\overline{AREQB}$ is negated for the access (see *Figure 7a*).

The DP8520A/21A/22A will increment the refresh address counter automatically, independent of the refresh mode used. The refresh address counter will be incremented once all the refresh $\overline{RAS}$s have been negated.

In every combination of refresh control mode and refresh type, the DP8520A/21A/22A is programmed to keep $\overline{RAS}$ asserted a number of CLK periods. The values of $\overline{RAS}$ low time during refresh are programmed with the programming bits R0 and R1.

4.1 REFRESH CONTROL MODES

There are three different modes of refresh control. Any of these modes can be used in combination or singularly to produce the desired refresh results. The three different modes of control are: automatic internal refresh, external/burst refresh and refresh request/acknowledge.

4.1.1 Automatic Internal Refresh

The DP8520A/21A/22A have an internal refresh clock. The period of the refresh clock is generated from the programming bits C0–3. Every period of the refresh clock, an internal refresh request is generated. As long as a VRAM access is not currently in progress and precharge time has been met, the internal refresh request will generate an automatic internal refresh. If a VRAM access is in progress, the DP8520A/21A/22A on-chip arbitration logic will wait until the access is finished before performing the refresh. The refresh/access arbitration logic can insert a refresh cycle between two address pipelined accesses. However, the refresh arbitration logic can not interrupt an access cycle to perform a refresh. To enable automatic internally controlled refreshes, the input $\overline{DISRFSH}$ must be negated.

4.1.2 Externally Controlled/Burst Refresh

To use externally controlled/burst refresh, the user must disable the automatic internally controlled refreshes by asserting the input $\overline{DISRFSH}$. The user is responsible for generating the refresh request by asserting the input $\overline{RFSH}$. Pulsing $\overline{RFSH}$ low, sets an internal latch, that is used to produce the internal refresh request. The refresh cycle will take place on the next positive edge of CLK as shown in *Figure 7b*. If an access to VRAM is in progress or precharge time for the last access has not been met, the refresh will be delayed. Since pulsing $\overline{RFSH}$ low sets a latch, the user does not have to keep $\overline{RFSH}$ low until the refresh starts. When the last refresh $\overline{RAS}$ negates, the internal refresh request latch is cleared.

By keeping $\overline{RFSH}$ asserted past the positive edge of CLK which ends the refresh cycle as shown in *Figure 8*, the user will perform another refresh cycle. Using this technique, the user can perform a burst refresh consisting of any number of refresh cycles. Each refresh cycle during a burst refresh will meet the refresh $\overline{RAS}$ low time and the $\overline{RAS}$ precharge time (programming bits R0–1).

If the user desires to burst refresh the entire VRAM (all row addresses) he could generate an end of count signal (burst refresh finished) by looking at one of the DP8520A/21A/22A high address outputs (Q7, Q8, Q9 or Q10) and the $\overline{RFIP}$ output. The Qn outputs function as a decode of how many row addresses have been refreshed (Q7 = 128 refreshes, Q8 = 256 refreshes, Q9 = 512 refreshes, Q10 = 1024 refreshes).

4.1.3 Refresh Request/Acknowledge

The DP8520A/21A/22A can be programmed to output internal refresh requests. When the user programs $\overline{ECAS}$0 negated during programming, the $\overline{RFIP}$ output functions as $\overline{RFRQ}$. $\overline{RFRQ}$ will be asserted from a positive edge of CLK as shown in *Figure 9a.* Once $\overline{RFRQ}$ is asserted, it will stay asserted until the $\overline{RFSH}$ is pulsed low with $\overline{DISRFSH}$ asserted. This will cause an externally requested/burst refresh to take place. If $\overline{DISRFSH}$ is negated, an automatic internal refresh will take place as shown in *Figure 9b*.

$\overline{RFRQ}$ will go high and then assert if additional periods of the internal refresh clock have expired and neither an externally controlled refresh nor an automatically controlled internal refresh have taken place as shown in *Figure 9c*. If a time critical event, or long access like page/static column mode access can not be interrupted, $\overline{RFRQ}$ pulsing high can be used to increment a counter. The counter can be used to perform a burst refresh of the number of refreshes missed (through the $\overline{RFSH}$ input).

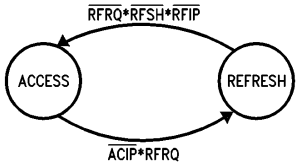
4.2 REFRESH CYCLE TYPES

Three different types of refresh cycles are available for use. The three different types are mutually exclusive and can be used with any of the three modes of refresh control. The three different refresh cycle types are: all $\overline{RAS}$ refresh, staggered $\overline{RAS}$ refresh and error scrubbing during all $\overline{RAS}$ refresh. In all refresh cycle types, the $\overline{RAS}$ precharge time is guaranteed: between the previous access $\overline{RAS}$ ending and the refresh $\overline{RAS}$0 starting; between refresh $\overline{RAS}$3 ending and access $\overline{RAS}$ beginning; between burst refresh $\overline{RAS}$s.

4.2.1 Conventional $\overline{RAS}$ Refresh

A conventional refresh cycle causes $\overline{RAS}$0–3 to all assert from the first positive edge of CLK after $\overline{RFIP}$ is asserted as shown in *Figure 10*. $\overline{RAS}$0–3 will stay asserted until the number of positive edges of CLK programmed have passed. On the last positive edge, $\overline{RAS}$0–3, and $\overline{RFIP}$ will be negated. This type of refresh cycle is programmed by negating address bit R9 during programming.

4.0 Refresh Options (Continued)



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Explanation of Terms

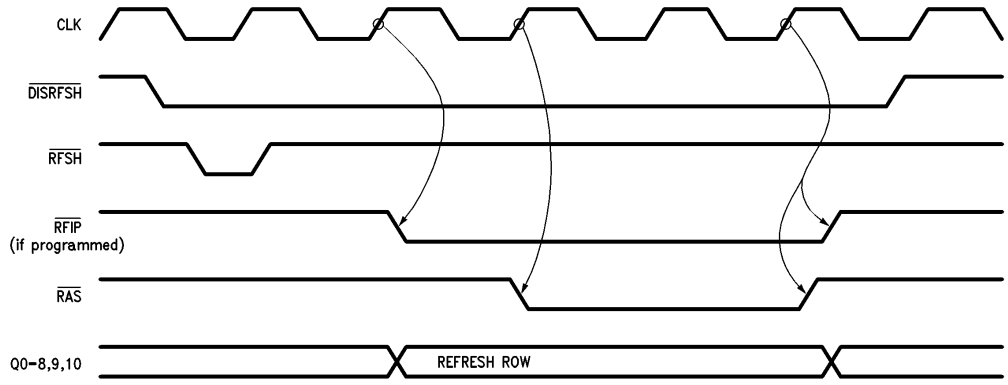
RFRQ = ReFresh ReQuest internal to the DP8520A/21A/22A. RFRQ has the ability to hold off a pending access.

RFSH = Externally requested ReFreSH

RFIP = ReFresh In Progress

ACIP = Port A or Port B (DP8522A only) ACcess In Progress. This means that either RAS is low for an access or is in the process of transitioning low for an access.

FIGURE 7a. DP8520A/21A/22A Access/Refresh Arbitration State Program



TL/F/9338–11

FIGURE 7b. Single External Refresh (2 Periods of RAS Low during Refresh Programmed)

4.0 Refresh Options (Continued)

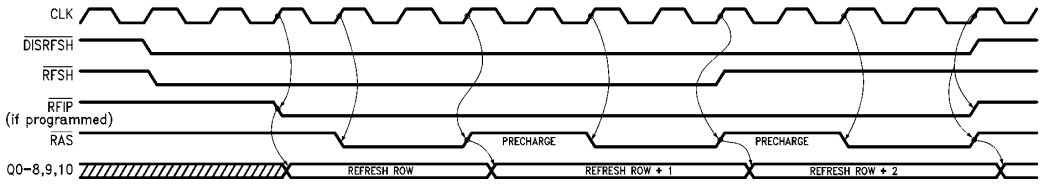


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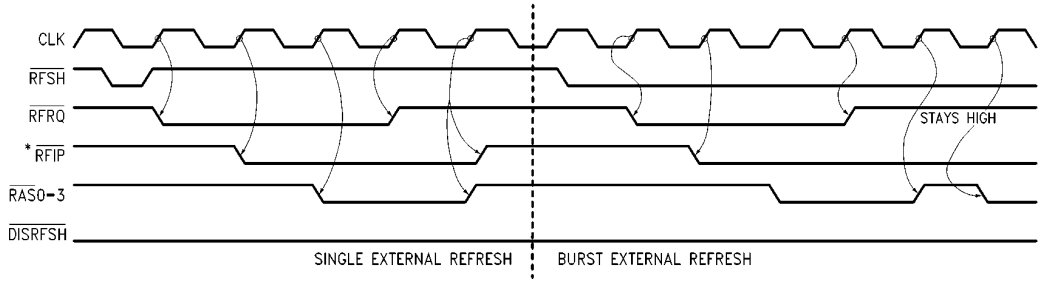
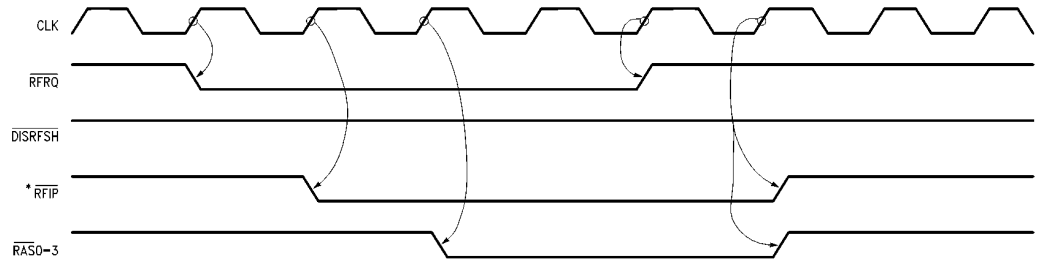
FIGURE 8. External Burst Refresh (2 Periods of $\overline{RAS}$ Precharge, 2 Periods of Refresh $\overline{RAS}$ Low during Refresh Programmed)



TL/F/9338–13

FIGURE 9a. Externally Controlled Single and Burst Refresh with Refresh Request ($\overline{RFRQ}$) Output (2 Periods of $\overline{RAS}$ Low during Refresh Programmed)



TL/F/9338–14

FIGURE 9b. Automatic Internal Refresh with Refresh Request (3T of $\overline{RAS}$ low during refresh programmed)

*In *Figures 9a* and *9b*, where the DP8520A/21A/22A operate in the refresh request/acknowledge mode, the $\overline{RFIP}$ output pin functions as $\overline{RFRQ}$. An $\overline{RFIP}$ timing waveform is included in the figure solely for the purpose of simplifying the diagrams.

4.0 Refresh Options (Continued)

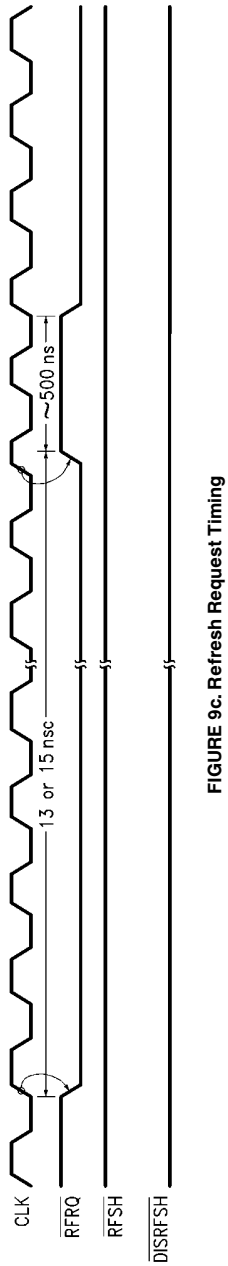


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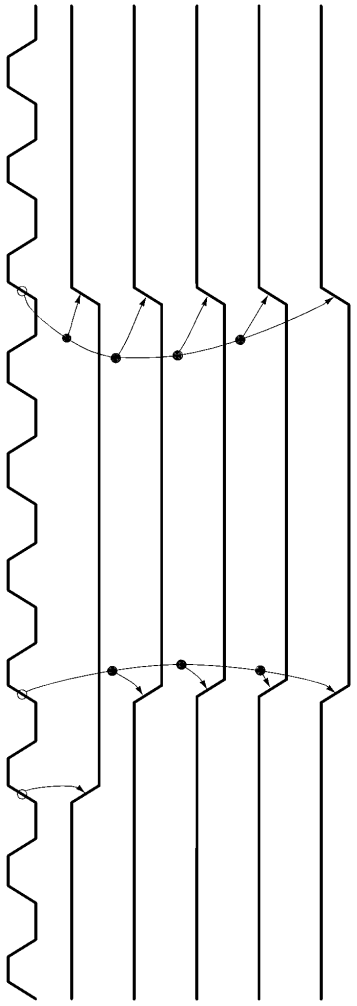
FIGURE 9c. Refresh Request Timing



TL/F/9338–16

FIGURE 10. Conventional $\overline{RAS}$ Refresh

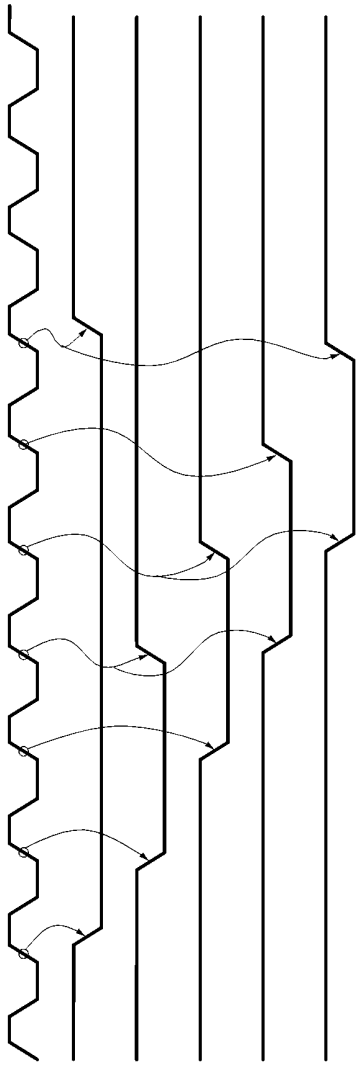


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FIGURE 11. Staggered $\overline{RAS}$ Refresh

4.0 Refresh Options (Continued)

4.2.2 Staggered $\overline{RAS}$ Refresh

A staggered refresh staggers each $\overline{RAS}$ or group of $\overline{RAS}$s by a positive edge of CLK as shown in *Figure 11*. The number of $\overline{RAS}$s, which will be asserted on each positive edge of CLK, is determined by the $\overline{RAS}$, $\overline{CAS}$ configuration mode programming bits C4–C6. If single $\overline{RAS}$ outputs are selected during programming, then each $\overline{RAS}$ will assert on successive positive edges of CLK. If two $\overline{RAS}$ outputs are selected during programming then $\overline{RAS}$0 and $\overline{RAS}$1 will assert on the first positive edge of CLK after $\overline{RFIP}$ is asserted. $\overline{RAS}$2 and $\overline{RAS}$3 will assert on the second positive edge of CLK after $\overline{RFIP}$ is asserted. If all $\overline{RAS}$ outputs were selected during programming, all $\overline{RAS}$ outputs would assert on the first positive edge of CLK after $\overline{RFIP}$ is asserted. Each $\overline{RAS}$ or group of $\overline{RAS}$s will meet the programmed $\overline{RAS}$ low time and then negate.

4.2.3 Error Scrubbing during Refresh

The DP8520A/21A/22A support error scrubbing during all $\overline{RAS}$ VRAM refreshes. Error scrubbing during refresh is selected through bits C4–C6 with bit R9 negated during programming. Error scrubbing can not be used with staggered refresh (see Section 9.0). Error scrubbing during refresh allows a $\overline{CAS}$ or group of $\overline{CAS}$s to assert during the all $\overline{RAS}$ refresh as shown in *Figure 12*. This allows data to be read from the VRAM array and passed through an Error Detection And Correction Chip, EDAC. It is important to note that while an error scrubbing during refresh access is being peformed, it is the system designer's responsibility to properly control the $\overline{WE}$ input of the VRAM. $\overline{WE}$ should be high during the initial access of the VRAM, which could be accomplished by gating $\overline{RFIP}$, if programmed, with the processor access circuitry that creates $\overline{WE}$. If the EDAC determines that the data contains a single bit error and corrects that error, the refresh cycle can be extended with the input extend refresh, EXTNDRF, and a read-modify-write operation can be performed, and the corrected data can be written back to the VRAM by bringing $\overline{WE}$ low. The DP8522A has a 24-bit internal refresh address counter that contains the 11 row, 11 column and 2 bank addresses. The DP8520A/21A have a 22-bit internal refresh address counter that contains the 10 row, 10 column and 2 bank addresses. These counters are configured as bank, column, row with the row address as the least significant bits. The bank counter bits are then used with the programming selection to determine which $\overline{CAS}$ or group of $\overline{CAS}$s will assert during a refresh.

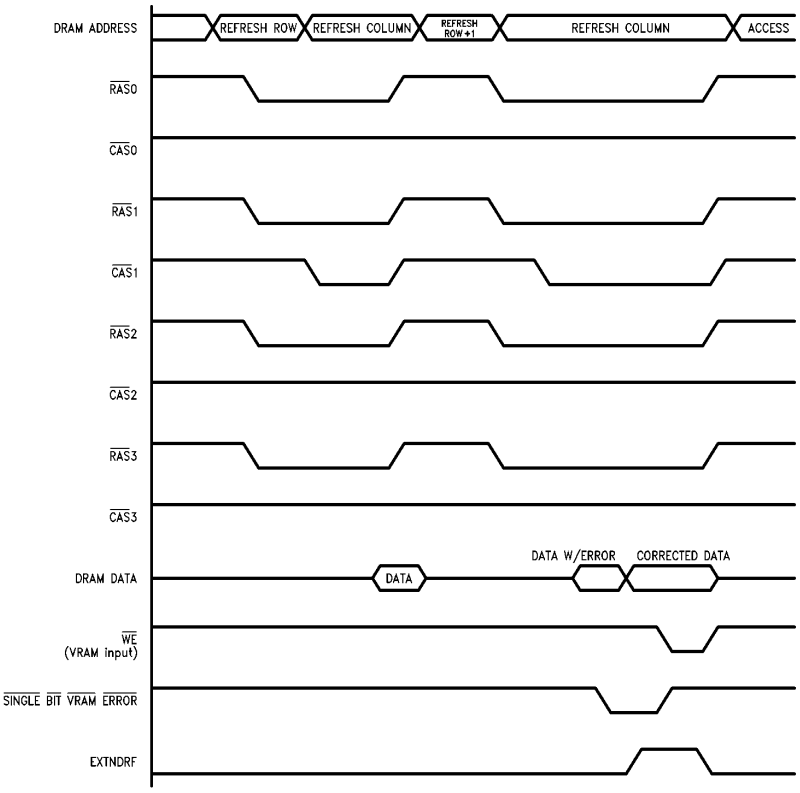

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FIGURE 12. Error Scrubbing during Refresh

4.0 Refresh Options (Continued)

4.3 EXTENDING REFRESH

The programmed number of periods of CLK that refresh $\overline{\text{RAS}}$s are asserted can be extended by one or multiple periods of CLK. Only the all $\overline{\text{RAS}}$ (with or without error scrubbing) type of refresh can be extended. To extend a refresh cycle, the input extend refresh, EXTNDRF, must be asserted before the positive edge of CLK that would have negated all the $\overline{\text{RAS}}$ outputs during the refresh cycle and after the positive edge of CLK which starts all $\overline{\text{RAS}}$ outputs during the refresh as shown in *Figure 13*. This will extend the refresh to the next positive edge of CLK and EXTNDRF will be sampled again. The refresh cycle will continue until EXTNDRF is sampled low on a positive edge of CLK.

4.4 CLEARING THE REFRESH ADDRESS COUNTER

The refresh address counter can be cleared by asserting $\overline{\text{RFSH}}$ while $\overline{\text{DISRFSH}}$ is negated as shown in *Figure 14a*. This can be used prior to a burst refresh of the entire memory array. By asserting $\overline{\text{RFSH}}$ one period of CLK before $\overline{\text{DISRFSH}}$ is asserted and then keeping both inputs asserted, the DP8520A/21A/22A will clear the refresh address counter and then perform refresh cycles separated by the programmed value of precharge as shown in *Figure 14b*. An end-of-count signal can be generated from the Q VRAM address outputs of the DP8520A/21A/22A and used to negate $\overline{\text{RFSH}}$.

4.5 CLEARING THE REFRESH REQUEST CLOCK

The refresh request clock can be cleared by negating $\overline{\text{DISRFSH}}$ and asserting $\overline{\text{RFSH}}$ for 500 ns, one period of the internal 2 MHz clock as shown in *Figure 15*. By clearing the refresh request clock, the user is guaranteed that an internal refresh request will not be generated for approximately 15 μs, one refresh clock period, from the time $\overline{\text{RFSH}}$ is negated. This action will also clear the refresh address counter.

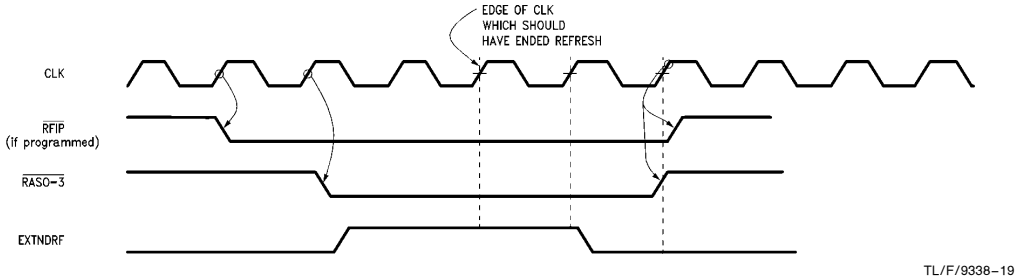

FIGURE 13. Extending Refresh with the Extend Refresh (EXTNDRF) Input

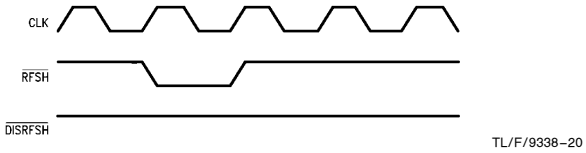

FIGURE 14a. Clearing the Refresh Address Counter

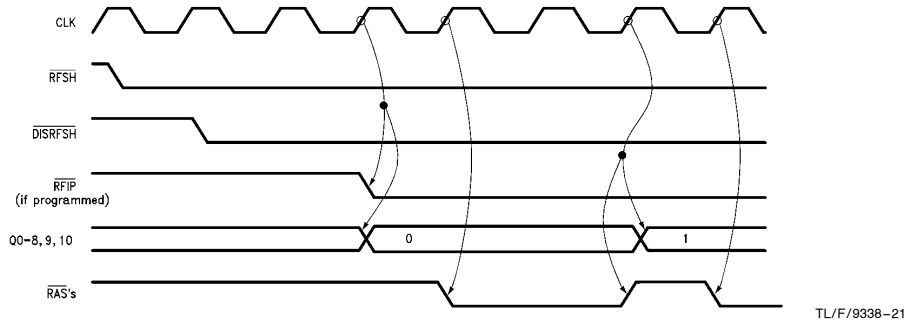

FIGURE 14b. Clearing the Refresh Counter during Burst

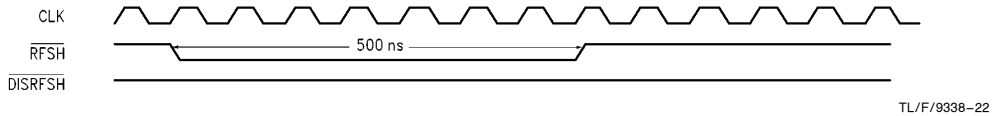

FIGURE 15. Clearing the Refresh Request Clock Counter

5.0 Port A Wait State Support

Wait states allow a CPU's access cycle to be increased by one or multiple CPU clock periods. The wait or ready input is named differently by CPU manufacturers. However, any CPU's wait or ready input is compatible with either the $\overline{WAIT}$ or $\overline{DTACK}$ output of the DP8520A/21A/22A. The user determines whether to program $\overline{WAIT}$ or $\overline{DTACK}$ (R7) and which value to select for $\overline{WAIT}$ or $\overline{DTACK}$ (R2, R3) depending upon the CPU used and where the CPU samples its wait input during an access cycle.

The decision to terminate the CPU access cycle is directly affected by the speed of the VRAMs used. The system designer must ensure that the data from the VRAMs will be present for the CPU to sample or that the data has been written to the VRAM before allowing the CPU access cycle to terminate.

The insertion of wait states also allows a CPU's access cycle to be extended until the VRAM access has taken place. The DP8520A/21A/22A insert wait states into CPU access cycles due to; guaranteeing precharge time, refresh currently in progress, user programmed wait states, the $\overline{WAITIN}$ signal being asserted and GRANTB not being valid (DP8522A only). If one of these events is taking place and the CPU starts an access, the DP8520A/21A/22A will insert wait states into the access cycle, thereby increasing the length of the CPU's access. Once the event has been completed, the DP8520A/21A/22A will allow the access to take place and stop inserting wait states.

There are six programming bits, R2–R7; an input, $\overline{WAITIN}$; and an output that functions as $\overline{WAIT}$ or $\overline{DTACK}$.

5.1 WAIT TYPE OUTPUT

With the R7 address bit negated during programming, the user selects the $\overline{WAIT}$ output. As long as $\overline{WAIT}$ is sampled asserted by the CPU, wait states (extra clock periods) are inserted into the current access cycle as shown in *Figure 16*. Once $\overline{WAIT}$ is sampled negated, the access cycle is completed by the CPU. $\overline{WAIT}$ is asserted at the beginning of a chip selected access and is programmed to negate a number of positive edges and/or negative levels of CLK from the event that starts the access. $\overline{WAIT}$ can also be programmed to function in page/burst mode applications. Once $\overline{WAIT}$ is negated during an access, and the $\overline{ECAS}$ inputs are negated with $\overline{AREQ}$ asserted, $\overline{WAIT}$ can be programmed to toggle, following the $\overline{ECAS}$ inputs. Once $\overline{AREQ}$ is negated, ending the access, $\overline{WAIT}$ will stay negated until the next chip selected access. For more details about $\overline{WAIT}$ Type Output, see Application Note AN-773.

5.2 $\overline{DTACK}$ TYPE OUTPUT

With the R7 address bit asserted during programming, the user selects the $\overline{DTACK}$ type output. As long as $\overline{DTACK}$ is sampled negated by the CPU, wait states are inserted into the current access cycle as shown in *Figure 17.* Once $\overline{DTACK}$ is sampled asserted, the access cycle is completed by the CPU. $\overline{DTACK}$, which is normally negated, is programmed to assert a number of positive edges and/or negative levels from the event that starts $\overline{RAS}$ for the access. $\overline{DTACK}$ can also be programmed to function during page/burst mode accesses. Once $\overline{DTACK}$ is asserted and the $\overline{ECAS}$ inputs are negated with $\overline{AREQ}$ asserted, $\overline{DTACK}$ can be programmed to negate and assert from the $\overline{ECAS}$ inputs toggling to perform a page/burst mode operation. Once $\overline{AREQ}$ is negated, ending the access, $\overline{DTACK}$ will be negated and stays negated until the next chip selected access. For more details about $\overline{DTACK}$ Type Output, see Application Note AN-773.

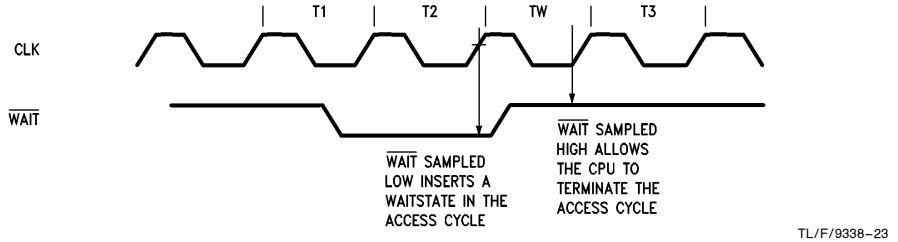

FIGURE 16. $\overline{WAIT}$ Type Output

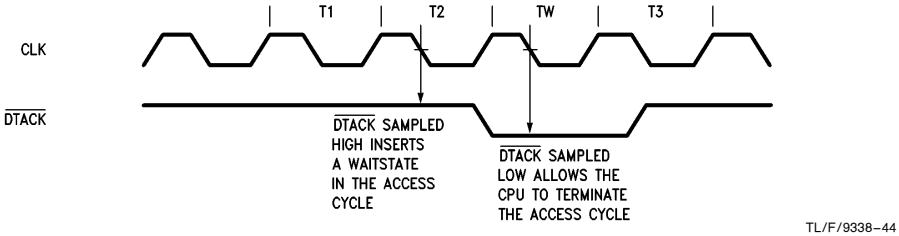

FIGURE 17. $\overline{DTACK}$ Type Output

5.0 Port A Wait State Support (Continued)

5.3 WAIT STATE SUPPORT FOR VIDEO RAM SHIFT REGISTER LOAD OPERATIONS FOR PORT A

If using the DP8520A/21A/22A in a system using video VRAMs, the CPU that controls loading the Video RAM shift register must be connected to Port A. The input $\overline{\text{AVSRLRQ}}$ asserts, signaling an advanced request for a Video RAM shift register load operation. Sometime later, the input $\overline{\text{VSRL}}$ asserts, signifying that the transfer cycle has started, and this action causes the $\overline{\text{DT}}/\overline{\text{OE}}$ output to transfer low. $\overline{\text{VSRL}}$ asserting also asserts $\overline{\text{WAIT}}$ (keeps $\overline{\text{DTACK}}$ negated) and will then insert wait states into the transfer cycle. The transfer cycle is completed from either $\overline{\text{VSRL}}$ negating or four clocks from $\overline{\text{VSRL}}$ asserting. The first event of these two to take place causes $\overline{\text{WAIT}}$ to negate ($\overline{\text{DTACK}}$ to assert) immediately or one half system clock period later, depending on how the user had programmed $\overline{\text{WAIT}}$ to end ($\overline{\text{DTACK}}$ to start) during a non-burst type of access. The wait logic is intimately connected to the DP8520A/21A/22A graphics functions and the $\overline{\text{WAIT}}$ output functions the same as the $\overline{\text{DT}}/\overline{\text{OE}}$ output (see *Figure 18*).

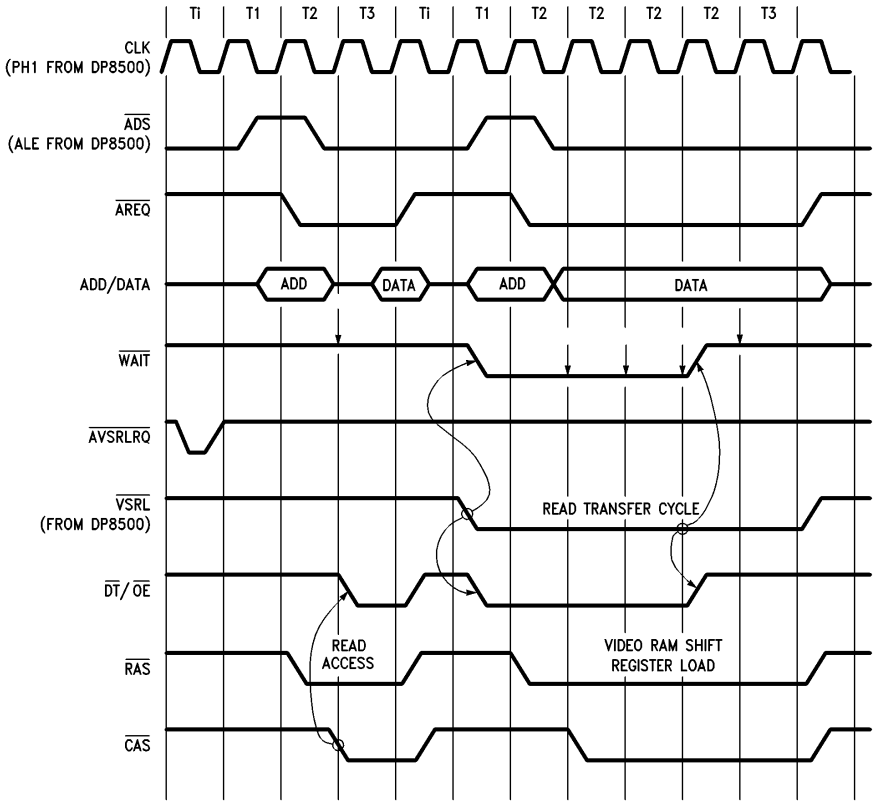

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FIGURE 18. Wait State Timing during a VRAM Transfer Cycle ($\overline{\text{WAIT}}$ Programmed as OT, $\overline{\text{WAIT}}$ Sampled at the "T3" Rising Clock Edge)

5.0 Port A Wait State Support (Continued)

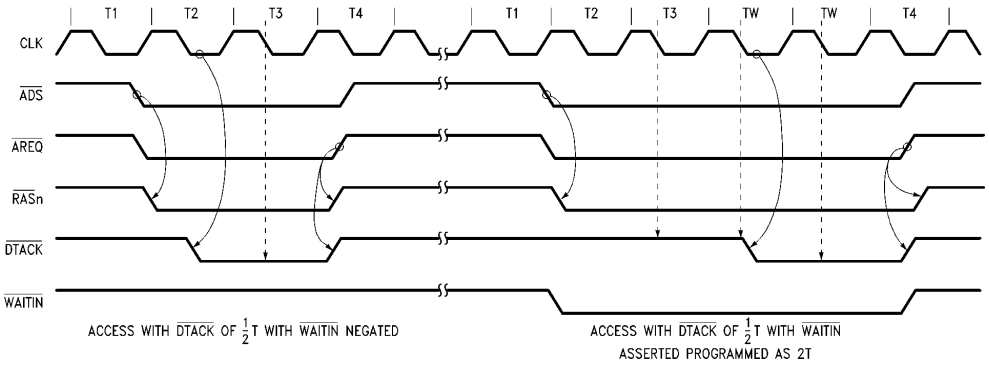
5.4 DYNAMICALLY INCREASING THE NUMBER OF WAIT STATES

The user can increase the number of positive edges of CLK before $\overline{\text{DTACK}}$ is asserted or $\overline{\text{WAIT}}$ is negated. With the input $\overline{\text{WAITIN}}$ asserted, the user can delay $\overline{\text{DTACK}}$ asserting or $\overline{\text{WAIT}}$ negating either one or two more positive edges of CLK. The number of edges is programmed through address bit R6. If the user is increasing the number of positive edges in a delay that contains a negative level, the positive edges will be met before the negative level. For example if the user programmed $\overline{\text{DTACK}}$ of ½T, asserting $\overline{\text{WAITIN}}$, programmed as 2T, would increase the number of positive edges resulting in $\overline{\text{DTACK}}$ of 2½T as shown in *Figure 19*. Similarly, $\overline{\text{WAITIN}}$ can increase the number of positive edges in a page/burst access. $\overline{\text{WAITIN}}$ can be permanently asserted in systems requiring an increased number of wait states. $\overline{\text{WAITIN}}$ can also be asserted and negated, depending on the type of access. As an example, a user could invert the $\overline{\text{WRITE}}$ line from the CPU and connect the output to $\overline{\text{WAITIN}}$. This could be used to perform write accesses with 1 wait state and read accesses with 2 wait states as shown in *Figure 20*.

5.5 GUARANTEEING $\overline{\text{RAS}}$ LOW TIME AND $\overline{\text{RAS}}$ PRECHARGE TIME

The DP8520A/21A/22A will guarantee $\overline{\text{RAS}}$ precharge time between accesses; between refreshes; and between access and refreshes. The programming bits R0 and R1 are used to program combinations of $\overline{\text{RAS}}$ precharge time and $\overline{\text{RAS}}$ low time referenced by positive edges of CLK. $\overline{\text{RAS}}$ low time is programmed for refreshes only. During an access, the system designer guarantees the time $\overline{\text{RAS}}$ is asserted through the DP8520A/21A/22A wait logic. Since inserting wait states into an access increases the length of the CPU signals which are used to create $\overline{\text{ADS}}$ or ALE and $\overline{\text{AREQ}}$, the time that $\overline{\text{RAS}}$ is asserted can be guaranteed.

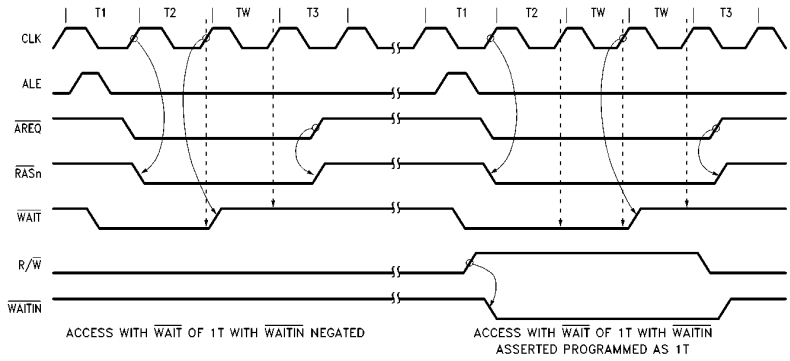
Precharge time is also guaranteed by the DP8520A/21A/22A. Each $\overline{\text{RAS}}$ output has a separate positive edge of CLK counter. $\overline{\text{AREQ}}$ is negated setup to a positive edge of CLK to terminate the access. That positive edge is 1T. The next positive edge is 2T. $\overline{\text{RAS}}$ will not be asserted until the programmed number of positive edges of CLK have passed as shown in *Figure 21*. Once the programmed precharge time has been met, $\overline{\text{RAS}}$ will be asserted from the positive edge of CLK. However, since there is a precharge counter per $\overline{\text{RAS}}$, an access using another $\overline{\text{RAS}}$ will not be delayed. Precharge time before a refresh is always referenced from the access $\overline{\text{RAS}}$ negating before $\overline{\text{RAS}}$0 for the refresh asserting. After a refresh, precharge time is referenced from $\overline{\text{RAS}}$3 negating, for the refresh, to the access $\overline{\text{RAS}}$ asserting.



TL/F/9338–75

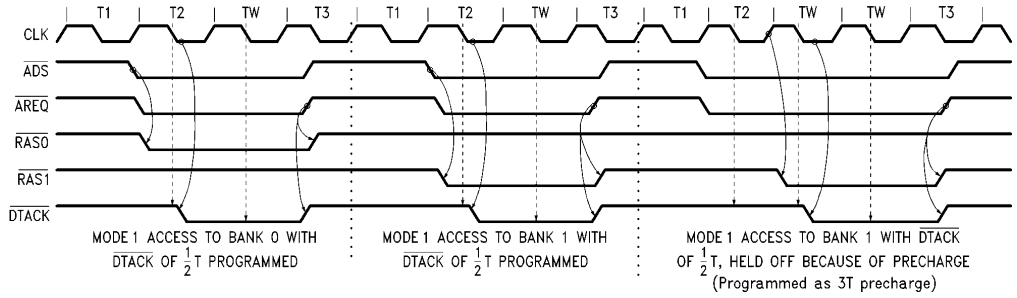
FIGURE 19. $\overline{\text{WAITIN}}$ Example ($\overline{\text{DTACK}}$ is Sampled at the "T3" Falling Clock Edge)

5.0 Port A Wait State Support (Continued)



TL/F/9338–76

FIGURE 20. WAITIN Example (WAIT is Sampled at the End of "T2")



TL/F/9338–77

FIGURE 21. Guaranteeing RAS Precharge (DTACK is Sampled at the "T2" Falling Clock Edge)

6.0 DP8520A/21A/22A Video RAM Support

The DP8520A/21A/22A provides full support for all access modes of video RAMs through the addition of three pins ($\overline{AVSRLRQ}$, $\overline{VSRL}$, and $\overline{DT}/\overline{OE}$) to the standard DP8420A/21A/22A. The access modes of video RAMs can be split up into two groups; video RAM transfer cycles (read with the serial port in active or in standby mode, write, and pseudo write transfer cycles), and non-transfer cycles. The DP8520A/21A/22A support of video RAMs allows the full capabilities of the National Semiconductor Advanced Graphics chip set (DP8500 Series) to be realized. See *Figures 22, 23,* and *58a.*

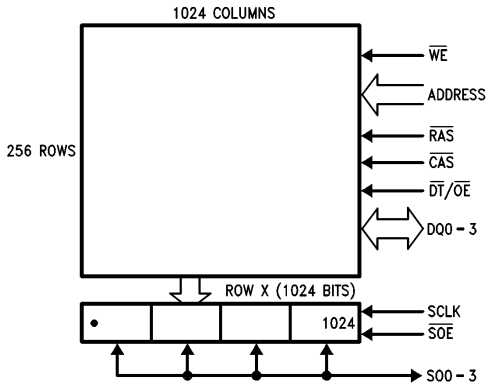


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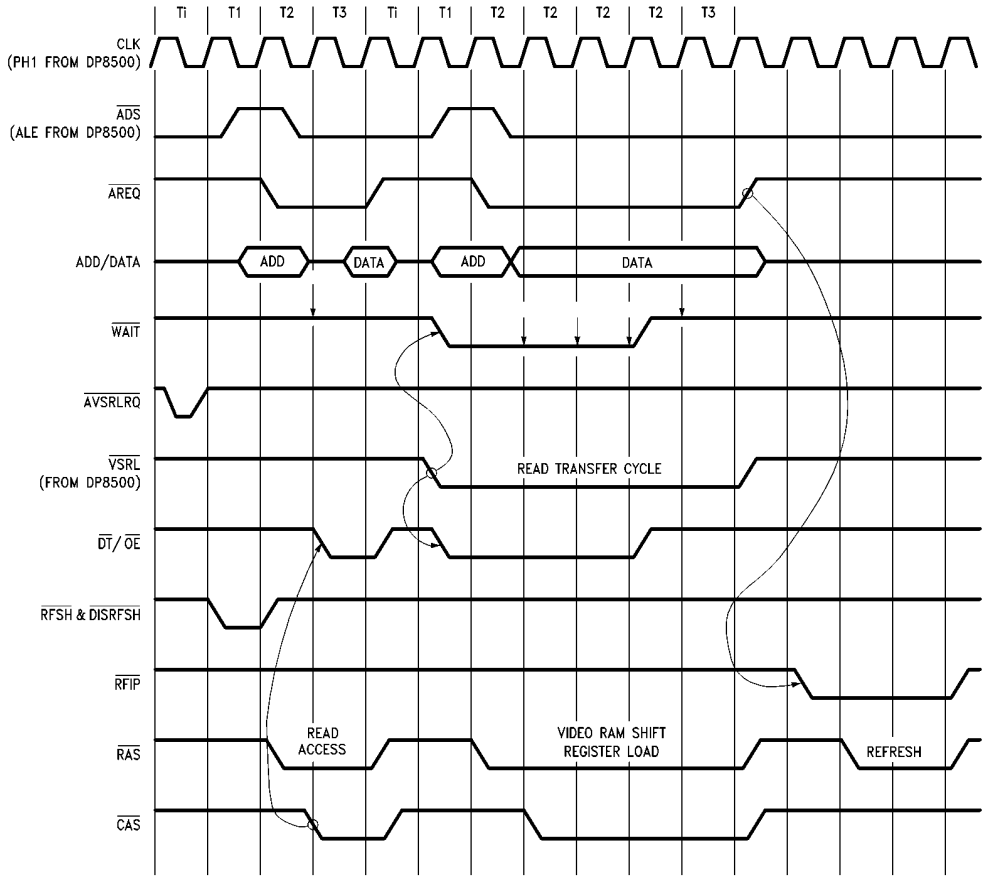
FIGURE 22. The Video RAM (A Dual Ported Memory) Ideal solution for graphics frame buffer. Screen refresh can occur at the same time as random access to the frame buffer for screen update and manipulation.



TL/F/9338–56

FIGURE 23. The DP8500 Raster Graphics Processor Interfaced to the DP8520A/21A/22A Video RAM Controller

6.0 DP8520A/21A/22A Video RAM Support (Continued)

6.1 SUPPORT FOR VRAM TRANSFER CYCLES (TO THE SERIAL PORT OF THE VRAM)

The DP8520A/21A/22A supports VRAM transfer cycles with the serial port in the active or standby mode. Active or standby refers to whether data is or is not currently being shifted in or out of the VRAM serial port (i.e., whether the shift clock (SCLK) is currently active). The DP8520A/21A/22A support for data transfer cycles with the serial port in the active mode includes the ability to support transfer cycles with the serial port in the standby mode. Hereafter, the term VRAM transfer cycle means VRAM transfer cycle with the serial port in the active mode.

In order to support VRAM transfer cycles, the DP8520A/21A/22A must be able to guarantee timing with respect to its input CLK (which must be synchronous to VRAM shift clock), $\overline{RAS}$, $\overline{CAS}$, and $\overline{DT}/\overline{OE}$. *Figure 23* shows the timing of a graphics memory system where the DP8520A/21A/22A is being used with the National Semiconductor DP8500 Raster Graphics Processor (RGP). If the DP8520A/21A/22A is being used in a graphics frame buffer application, it has the ability to support a VRAM transfer cycle during active video time (ex. mid scan line). This is one of the very attractive features supported by the National Semiconductor Advanced Graphics chip set. Most of the commercial graphics controller chip sets available will only support VRAM transfer cycles during blanking periods (while the VRAM is in standby mode).

The DP8520A/21A/22A supports VRAM transfer cycles during active video time by being able to guarantee an exact instant during which the transfer of VRAM data to the VRAM shift register will occur. This exact instant can be guaranteed through the $\overline{AVSRLRQ}$ and $\overline{VSRL}$ inputs.

The input $\overline{AVSRLRQ}$ disables any further internally or externally requested refreshes or Port B access requests from being executed. The $\overline{AVSRLRQ}$ input does this by making the VRAM controller arbitration logic think that a Port A access is in progress from the point where the $\overline{AVSRLRQ}$ input asserts until the VRAM shift register load operation is completed. *Figure 23* shows the case of an externally requested refresh being disabled, because of a previous $\overline{AVSRLRQ}$, until the VRAM shift register load has been completed.

The $\overline{VSRL}$ input causes the $\overline{DT}/\overline{OE}$ output to assert immediately, regardless of what else may be happening in the DP8520A/21A/22A. Therefore, it is the system designer's responsibility to guarantee that all pending accesses have been completed by the time the $\overline{VSRL}$ input asserts. The system designer can guarantee this by issuing $\overline{AVSRLRQ}$ far enough in advance to guarantee that all pending accesses have been completed by the time $\overline{VSRL}$ asserts.

The $\overline{AVSRLRQ}$ input does not override the $\overline{LOCK}$ input (see Section 12.0) for dual port systems, and as a result, the designer must also guarantee that Port A can be accessed by assuring that GRANTB and $\overline{LOCK}$ are both not asserted when $\overline{AVSRLRQ}$ is asserted.

Generally, the $\overline{VSRL}$ is the status of the upcoming access cycle (of the graphics processor). Therefore, this input precedes the inputs $\overline{ADS}$ and $\overline{AREQ}$ that execute the VRAM shift register load transfer cycle. This sequence of events guarantees the correct relationship of $\overline{DT}/\overline{OE}$, $\overline{RAS}$ and $\overline{CAS}$ ($\overline{DT}$ preceding $\overline{RAS}$ and $\overline{CAS}$ when asserting and negating). The wait logic is also intimately connected to the graphics functions on the DP8520A/21A/22A. The $\overline{DT}/\overline{OE}$ (and $\overline{WAIT}/\overline{DTACK}$) relationship to $\overline{VSRL}$ during a VRAM transfer cycle depends upon how the DP8520A/21A/22A was programmed with respect to the $\overline{ECAS0}$ input. If $\overline{ECAS0}$ was negated during programming, the $\overline{DT}/\overline{OE}$ output will follow the $\overline{VSRL}$ input. If $\overline{ECAS0}$ was asserted during programming, the $\overline{DT}/\overline{OE}$ output will follow $\overline{VSRL}$ asserting. $\overline{DT}/\overline{OE}$ will then negate either when $\overline{VSRL}$ negates or from the fourth rising clock edge after $\overline{VSRL}$ asserted, whichever event takes place first. This allows $\overline{DT}$ to negate before $\overline{RAS}$ and $\overline{CAS}$ negate, thus guaranteeing the correct timing relationship during the transfer cycle (see *Figure 23*). The $\overline{WE}$ input of the VRAM determines whether the access is a read or write transfer cycle (see *Figures 24* and *25* respectively).

6.0 DP8520A/21A/22A Video RAM Support (Continued)

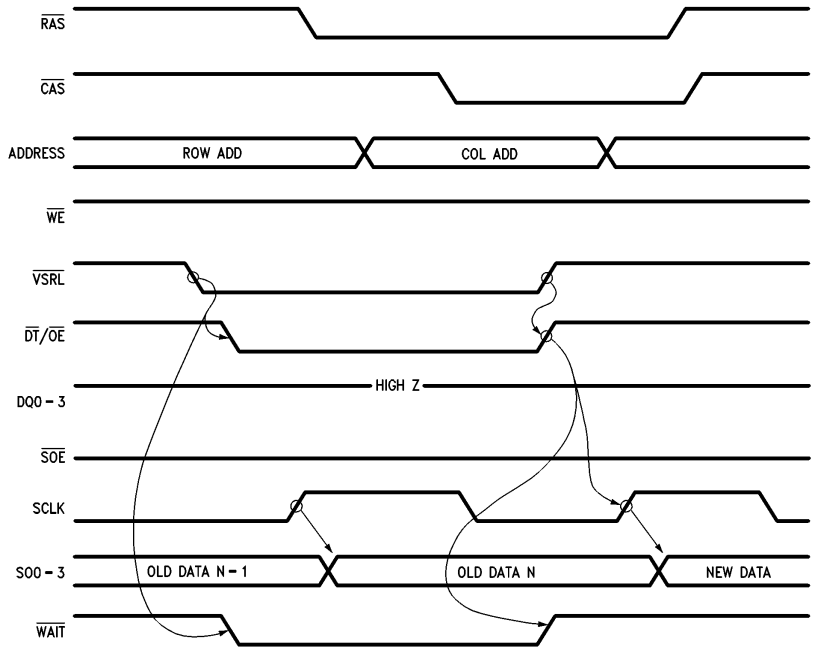


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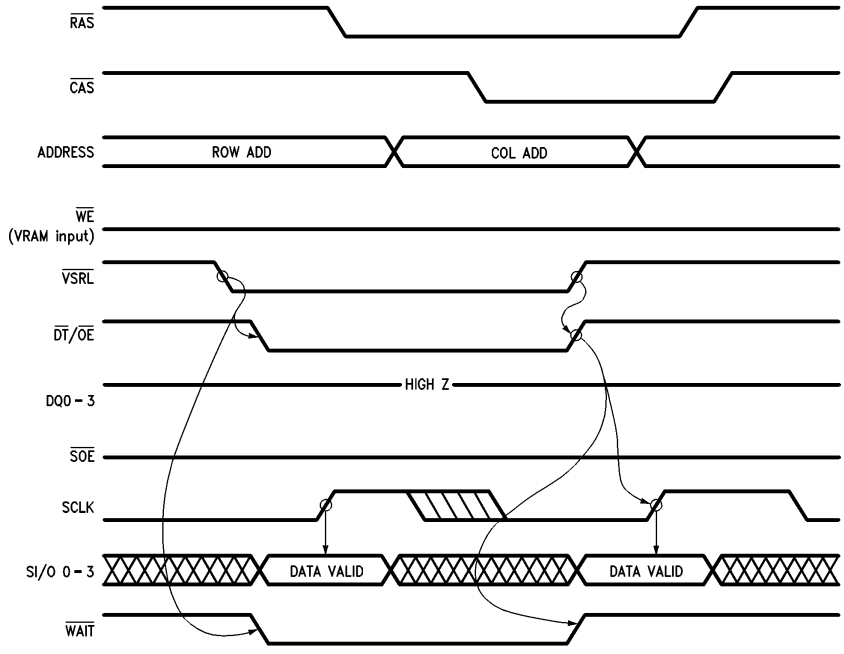
FIGURE 24. Video RAM Timing READ Transfer Cycle, B Port Active (Transfer VRAM Row Data into Shift Register)

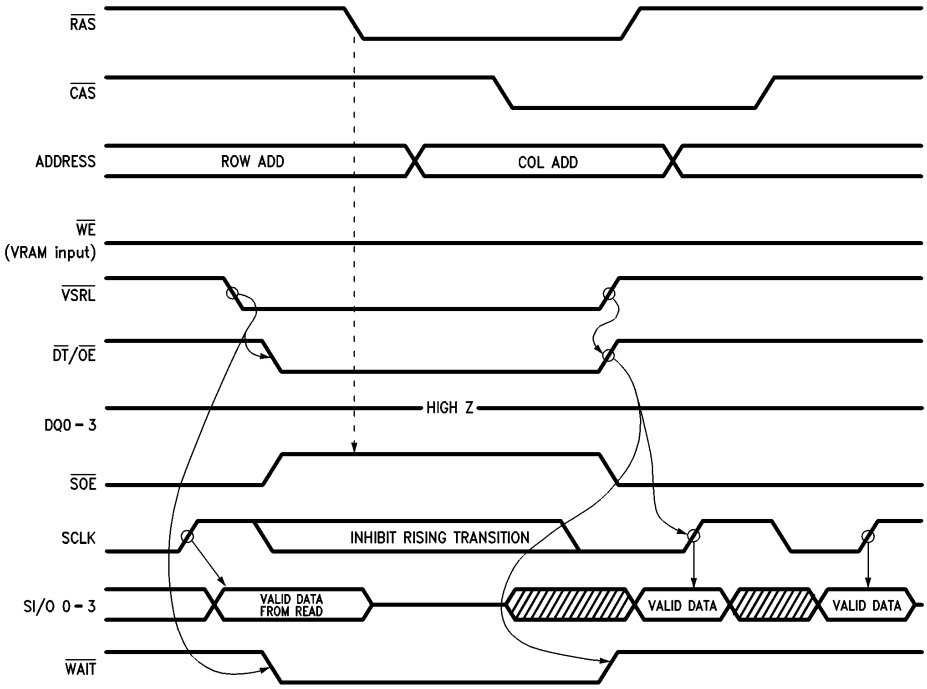


TL/F/9338–55

FIGURE 25. Video RAM Timing WRITE Transfer Cycle, B Port Active (Transfer Shift Register Data into VRAM Row)

6.0 DP8520A/21A/22A Video RAM Support (Continued)

During a transfer cycle ($\overline{VSRL}$ asserted during the access) $\overline{WIN}$ is disabled from affecting the $\overline{DT}/\overline{OE}$ logic until the transfer cycle is completed as shown by $\overline{CAS}$ negating. During a transfer cycle, the $\overline{SOE}$ (Serial Output Enable) input to the VRAM is asserted and is used as an output control for a read transfer cycle and is used as a write enable control during a write transfer cycle. When $\overline{SOE}$ is negated, serial access is disabled, and a transfer cycle cannot take place. $\overline{SOE}$ asserted during a read enables the serial input/output bus SI/O (0–3) while the VRAM data bus (DQ0–3) is put into a high impedance state, thus allowing the transfer cycle to take place from the serial port. In addition to both read and write transfer cycles, the DP8520A/21A/22A also supports pseudo write transfer cycles (see *Figure 26*). A pseudo write transfer cycle must be performed after a read transfer cycle if the subsequent operation is a write transfer cycle. The DP8520A/21A/22A VRAM controller is operated as if it is doing a write transfer cycle, but since the $\overline{SOE}$ input to the VRAM is negated (disabling the serial port), a transfer doesn't take place. The purpose of this pseudo write transfer cycle is to switch the SI/O (0–3) lines of the VRAM's serial port from output mode to input mode.



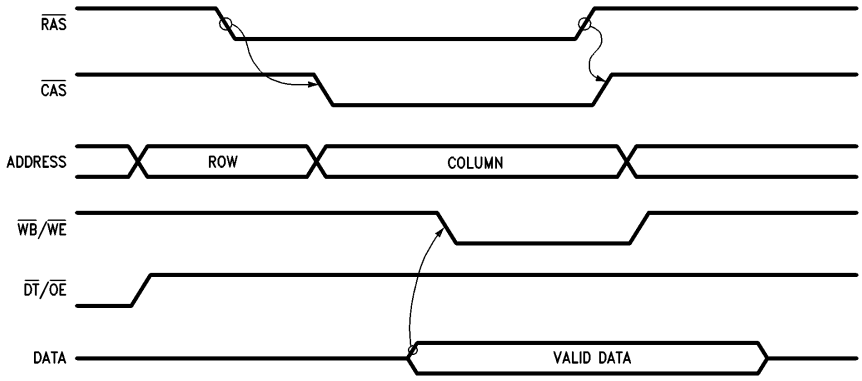
TL/F/9338–79

FIGURE 26. Video RAM Timing Pseudo WRITE Transfer Cycle, B Port Active (Transfer Shift Register Data into VRAM Row)

6.0 DP8520A/21A/22A Video RAM Support (Continued)

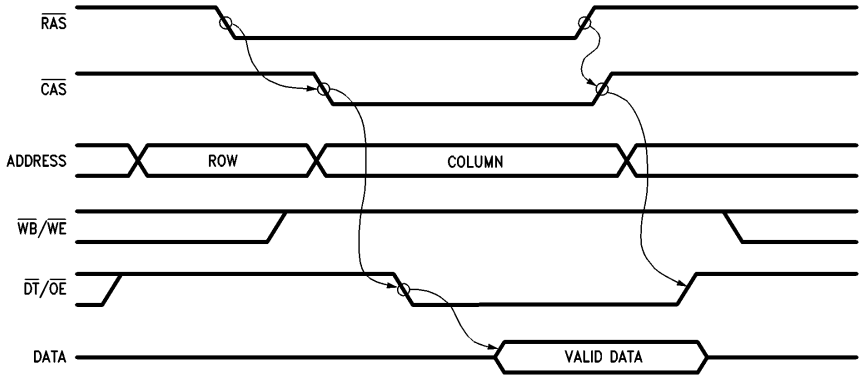
6.2 SUPPORT FOR VRAM ACCESS CYCLES THROUGH PORT A USING THE DP8520A/21A/22A

With the DP8520A/21A/22A, the output $\overline{DT}/\overline{OE}$ will remain negated during write accesses (see *Figure 27*), but during read accesses it will assert after $\overline{CAS}$n asserts. $\overline{DT}/\overline{OE}$ will be negated for a read access once $\overline{CAS}$n is negated (see *Figure 28*), causing the VRAM outputs to be enabled. If $\overline{CAS}$n toggles during a page mode read access, then the $\overline{DT}/\overline{OE}$ logic will also toggle following the $\overline{CAS}$n input.



TL/F/9338–54

FIGURE 27. Video RAM Random Access Write Cycle



TL/F/9338–53

FIGURE 28. Video RAM Random Access Read Cycle

7.0 Additional Access Support Features

To support the different modes of accessing, the DP8520A/21A/22A have multiple access features. These features allow the user to take advantage of CPU or VRAM functions. These additional features include: address latches and column increment for page/burst mode support; address pipelining to allow a new access to start to a different bank of VRAM after $\overline{CAS}$ has been asserted and the column address hold time has been met; and delay $\overline{CAS}$, to allow the user with a multiplexed bus to ensure valid data is present before $\overline{CAS}$ is asserted.

7.1 ADDRESS LATCHES AND COLUMN INCREMENT

The address latches can be programmed, through programming bit B0, to either latch the address or remain permanently in fall-through mode. If the address latches are used to latch the address, the rising edge of ALE in Mode 0 places the latches in fall-through. Once ALE is negated, the address present on the row, column and bank inputs is latched. In Mode 1, the address latches are in fall-through mode until $\overline{ADS}$ is asserted. $\overline{ADS}$ asserted latches the address.

Once the address is latched, the column address can be incremented with the input COLINC. With COLINC asserted, the column address is incremented. If COLINC is asserted with all of the bits of the column address asserted, the column address will return to zero. COLINC can be used for sequential accesses of static column VRAMs. COLINC can also be used with the $\overline{ECAS}$ inputs to support sequential accesses to page mode VRAMs as shown in *Figure 29.* COLINC should only be asserted when a refresh is not in progress as indicated by $\overline{RFIP}$, if programmed, being negated during an access since this input functions as an extend refresh when a refresh is in progress.

The address latches function differently with the DP8522A. The DP8522A will latch the address of the currently granted port. If Port A is currently granted, the address will be latched as described in Section 7.1. If Port A is not granted, and requests an access, the address will be latched on the first or second positive edge of CLK after GRANTB has been negated depending on the programming bits R0, R1. For Port B, if GRANTB is asserted, the address will be latched with $\overline{AREQB}$ asserted. If GRANTB is negated, the address will latch on the first or second positive edge of CLK after GRANTB is asserted depending on the programming bits R0, R1.

7.2 ADDRESS PIPELINING

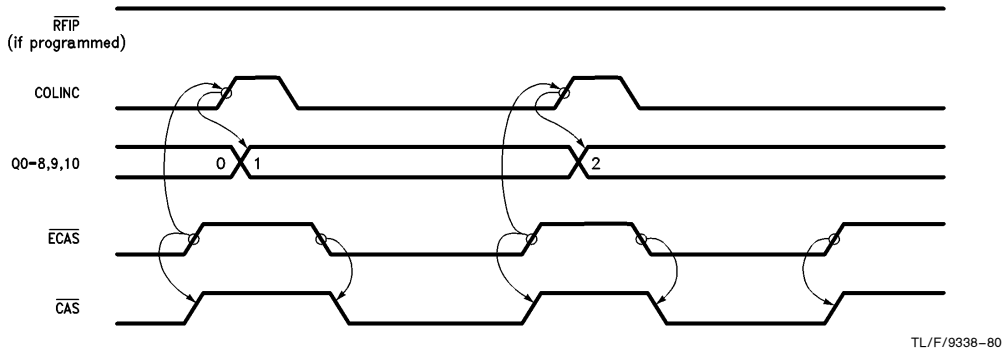
Address pipelining is the overlapping of accesses to different banks of VRAM. If the majority of successive accesses are to a different bank, the accesses can be overlapped. Because of this overlapping, the cycle time of the VRAM accesses are greatly reduced. The DP8520A/21A/22A can be programmed to allow a new row address to be placed on the VRAM address bus after the column address hold time has been met. At this time, a new access can be initiated with $\overline{ADS}$ or ALE, depending on the access mode, while $\overline{AREQ}$ is used to sustain the current access. The DP8522A supports address pipelining for Port A only. This mode can not be used with page, static column or nibble modes of operations because the VRAM column address is switched back to the row address after $\overline{CAS}$ is asserted. This mode is programmed through address bit R8 (see *Figures 30* and *31*).

During address pipelining in Mode 0, shown in *Figure 32*, ALE cannot be pulsed high to start another access until $\overline{AREQ}$ has been asserted for the previous access for at least one period of CLK. $\overline{DTACK}$, if programmed, will be negated once $\overline{AREQ}$ is negated. $\overline{WAIT}$, if programmed to insert wait states, will be asserted once ALE and $\overline{CS}$ are asserted.

In Mode 1, shown in *Figure 33,* $\overline{ADS}$ can be negated once $\overline{AREQ}$ is asserted. After meeting the minimum negated pulse width for $\overline{ADS}$, $\overline{ADS}$ can again be asserted to start a new access. $\overline{DTACK}$, if programmed, will be negated once $\overline{AREQ}$ is negated. $\overline{WAIT}$, if programmed, will be asserted once $\overline{ADS}$ is asserted.

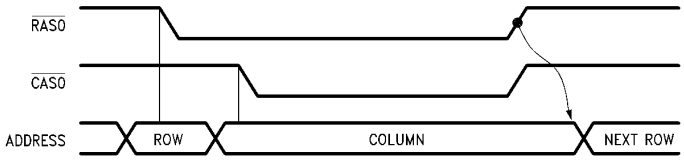
In either mode with either type of wait programmed, the DP8520A/21A/22A will still delay the access for precharge if sequential accesses are to the same bank or if a refresh takes place.

7.0 Additional Access Support Features (Continued)



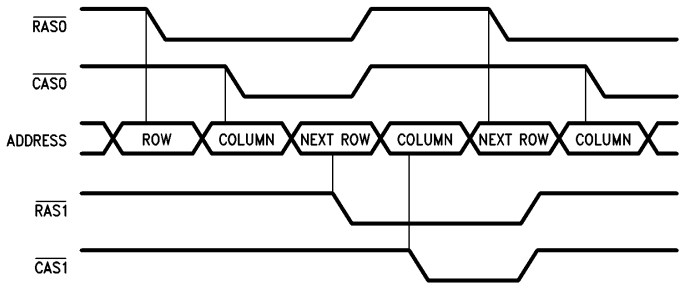
TL/F/9338–80

FIGURE 29. Column Increment



TL/F/9338–81

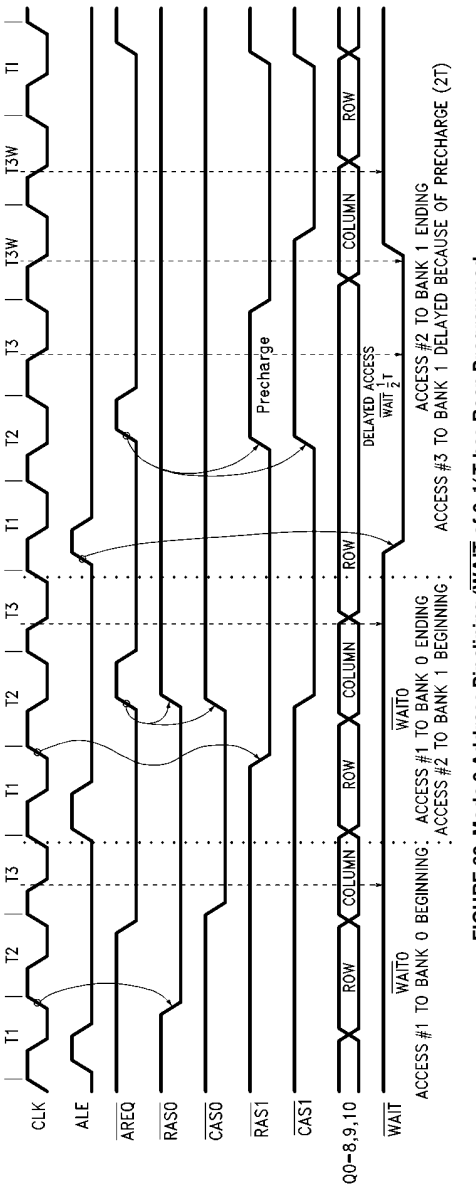
FIGURE 30. Non-Address Pipelined Mode



TL/F/9338–82

FIGURE 31. Address Pipelined Mode

7.0 Additional Access Support Features



TL/F/9338–83

FIGURE 32. Mode 0 Address Pipelining ($\overline{WAIT}$ of 0, ½T has Been Programmed. $\overline{WAIT}$ is Sampled at the "T3" Falling Clock Edge)

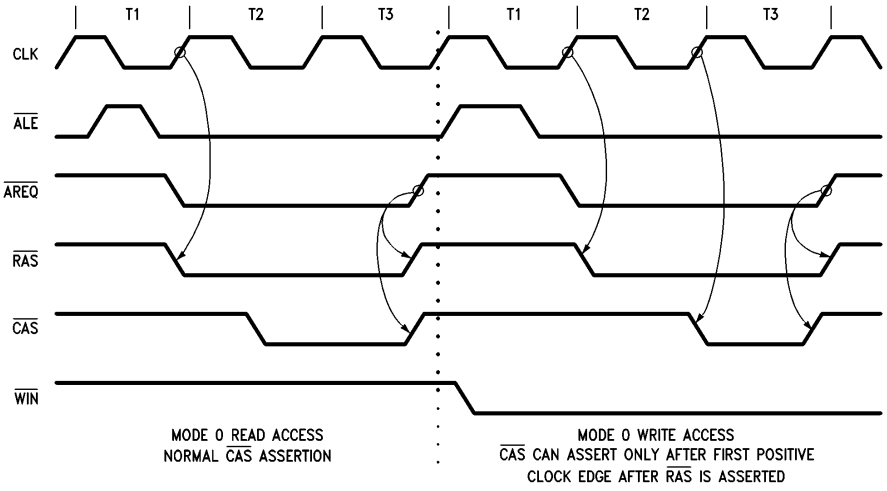
TL/F/9338–84

FIGURE 33. Mode 1 Address Pipelining ($\overline{DTACK}$ 1½T Programmed, $\overline{DTACK}$ is Sampled at the "T3" Falling Clock Edge)

7.0 Additional Access Support Features

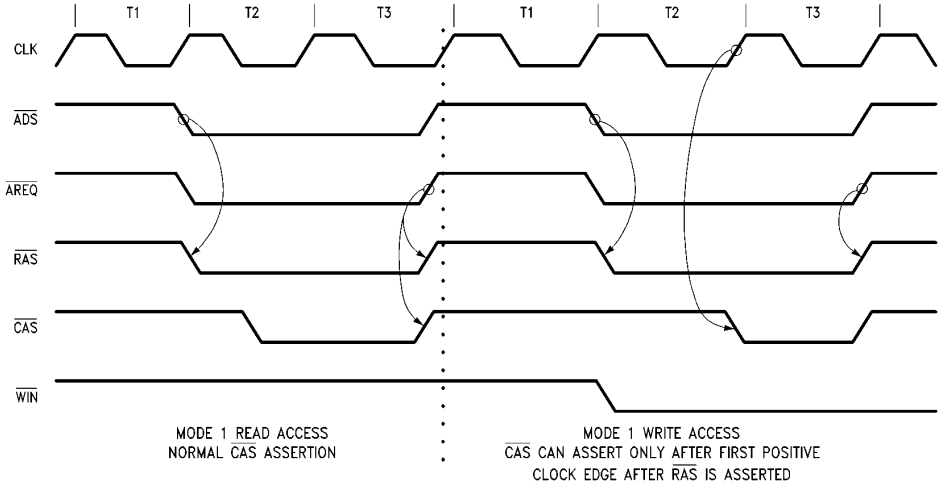
7.3 DELAY $\overline{CAS}$ DURING WRITE ACCESSES

Address bit C9 asserted during programming will cause $\overline{CAS}$ to be delayed until the first positive edge of CLK after $\overline{RAS}$ is asserted when the input $\overline{WIN}$ is asserted. Delaying $\overline{CAS}$ during write accesses ensures that the data to be written to VRAM will be setup to $\overline{CAS}$ asserting as shown in *Figures 34* and *35*. If the possibility exists that data still may not be present after the first positive edge of CLK, $\overline{CAS}$ can be delayed further with the $\overline{ECAS}$ inputs. If address bit C9 is negated during programming, read and write accesses will be treated the same (with regard to $\overline{CAS}$).



TL/F/9338–85

FIGURE 34. Mode 0 Delay $\overline{CAS}$



TL/F/9338–86

FIGURE 35. Mode 1 Delay $\overline{CAS}$

8.0 $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Configuration Modes

The DP8520A/21A/22A allow the user to configure the VRAM array to contain one, two or four banks of VRAM. Depending on the functions used, certain considerations must be used when determining how to set up the VRAM array. Programming address bits C4, C5 and C6 along with bank selects, B0–1, and $\overline{\text{CAS}}$ enables, $\overline{\text{ECAS}}$0–1, determine which $\overline{\text{RAS}}$ or group of $\overline{\text{RAS}}$s and which $\overline{\text{CAS}}$ or group of $\overline{\text{CAS}}$s will be asserted during an access. Different memory schemes are described. The DP8520A/21A/22A is specified driving a heavy load of 72 VRAMs, representing four banks of VRAM with 16-bit words and 2 parity bits. The DP8520A/21A/22A can drive more than 72 VRAMs, but the AC timing must be increased. Since the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ outputs are configurable, all $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ outputs should be used for the maximum amount of drive.

8.1 BYTE WRITING

By selecting a configuration in which all $\overline{\text{CAS}}$ outputs are selected during an access, each $\overline{\text{ECAS}}$ input enables a pair of $\overline{\text{CAS}}$ outputs to select a byte in a word size of up to 16 bits. In this case, the $\overline{\text{RAS}}$ outputs are used to select which of up to 4 banks is to be used as shown in *Figures 36* and *37.* The user can also configure the VRAM array into an 8 bank system as shown in *Figure 38.* This setup can be used along with byte writing for an 8-bit system if the $\overline{\text{LOW BYTE}}$ and $\overline{\text{HIGH BYTE}}$ are connected to $\overline{\text{ECAS}}$0 and $\overline{\text{ECAS}}$1 respectively. The user can connect upper address bits to $\overline{\text{ECAS}}$0,1 for use in an 8 bank–16-bit system, but cannot use byte writing in this case.

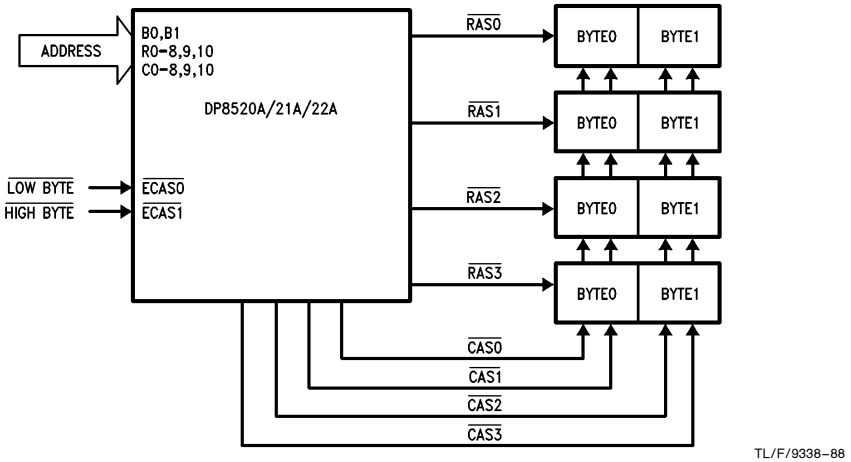


FIGURE 36. VRAM Array Setup for 16-Bit System (C6, C5, C4 = 1, 1, 0 during Programming)

8.0 $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Configuration Modes (Continued)

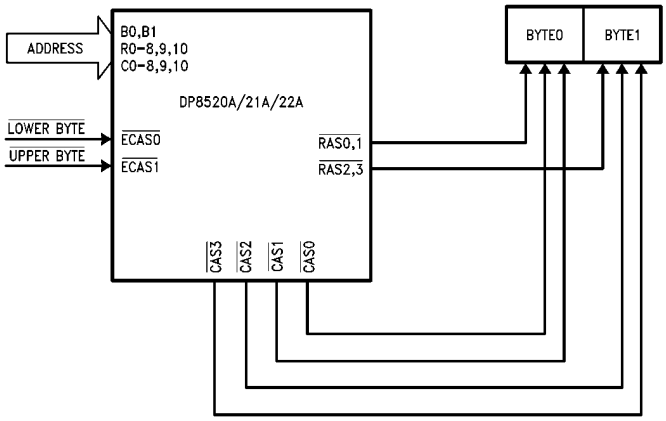


FIGURE 37. VRAM Array Setup for 16-Bit, 1 Bank System (C6, C5, C4 = 0, 0, 0 Allowing Error Scrubbing or C6, C5, C4 = 0, 1, 1 No Error Scrubbing during Programming)

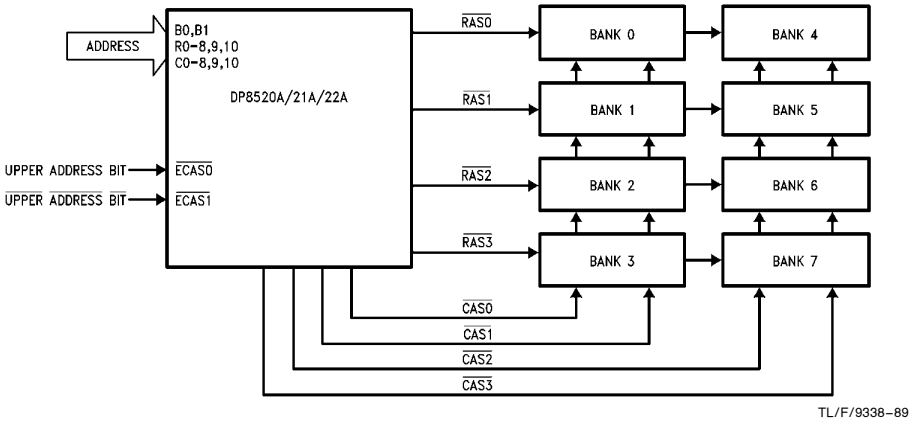


FIGURE 38. 8 Bank VRAM Array (C6, C5, C4 = 1, 1, 0 during Programming)

8.0 $\overline{RAS}$ and $\overline{CAS}$ Configuration Modes (Continued)

8.2 MEMORY INTERLEAVING

Memory interleaving allows the cycle time of VRAMs to be reduced by having sequential accesses to different memory banks. Since the DP8520A/21A/22A have separate precharge counters per bank, sequential accesses will not be delayed if the accessed banks use different $\overline{RAS}$ outputs. To ensure different $\overline{RAS}$ outputs will be used, a mode is selected where either one or two $\overline{RAS}$ outputs will be asserted during an access. The bank select or selects, B0 and B1, are then tied to the least significant address bits, causing a different group of $\overline{RAS}$s to assert during each sequential access as shown in *Figure 39.* In this figure there should be at least one clock period of all $\overline{RAS}$'s negated between different $\overline{RAS}$'s being asserted to avoid the condition of a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

8.3 ADDRESS PIPELINING

Address pipelining allows several access $\overline{RAS}$s to be asserted at once. Because $\overline{RAS}$s can overlap, each bank requires either a mode where one $\overline{RAS}$ and one $\overline{CAS}$ are used per bank as shown in *Figure 40* or where two $\overline{RAS}$s and two $\overline{CAS}$s are used per bank as shown in *Figure 41.* In order to perform byte writing while using address pipelining, external gating on the $\overline{CAS}$ outputs must be used. If the array is not layed out this way, a $\overline{CAS}$ to a bank can be low before $\overline{RAS}$, which will cause a refresh of the VRAM, not an access. To take full advantage of address pipelining, memory interleaving is used. To memory interleave, the least significant address bits should be tied to the bank select inputs to ensure that all ''back to back'' sequential accesses are not delayed, since different memory banks are accessed.

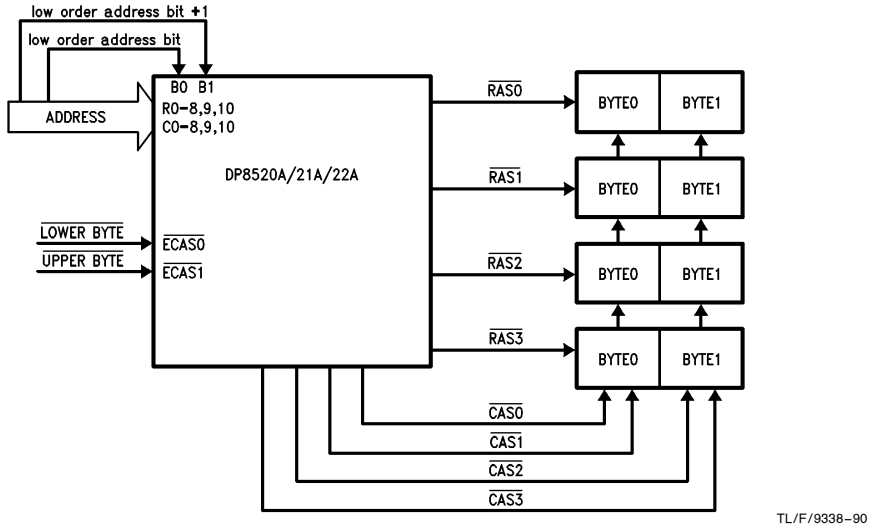


FIGURE 39. Memory Interleaving with Byte Writing Capability (C6, C5, C4 = 1, 1, 0 during Programming)

8.0 $\overline{RAS}$ and $\overline{CAS}$ Configuration Modes (Continued)

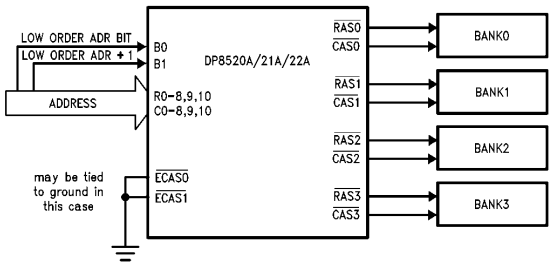


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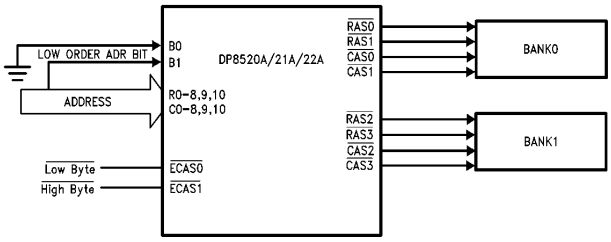
FIGURE 40. VRAM Array Setup for 4 Banks Using Address Pipelining (C6, C5, C4 = 1, 1, 1 or C6, C5, C4 = 0, 1, 0 (Also Allowing Error Scrubbing) during Programming)

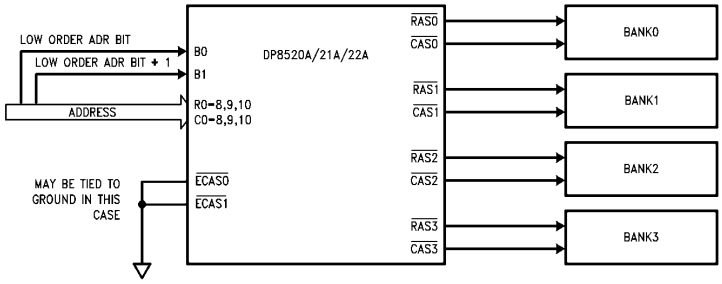


TL/F/9338–92

FIGURE 41. VRAM Array Setup for Address Pipelining with 2 Banks (C6, C5, C4 = 1, 0, 1 or C6, C5, C4 = 0, 0, 1 (Also Allowing Error Scrubbing) during Programming)

8.4 ERROR SCRUBBING

In error scrubbing during refresh, the user selects one, two or four $\overline{RAS}$ and $\overline{CAS}$ outputs per bank. When performing error detection and correction, memory is always accessed as words. Since the $\overline{CAS}$ signals are not used to select individual bytes, their corresponding $\overline{ECAS}$ inputs can be tied low as shown in *Figures 42* and *43*.



TL/F/9338–93

FIGURE 42. VRAM Array Setup for 4 Banks Using Error Scrubbing (C6, C5, C4 = 0, 1, 0 during Programming)

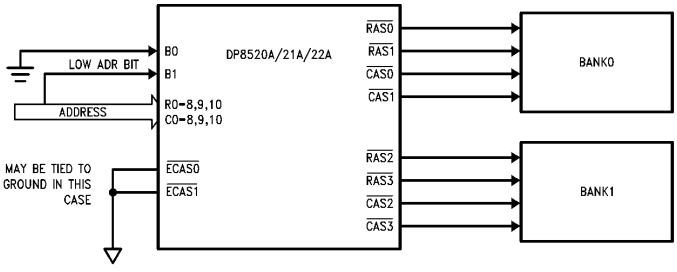


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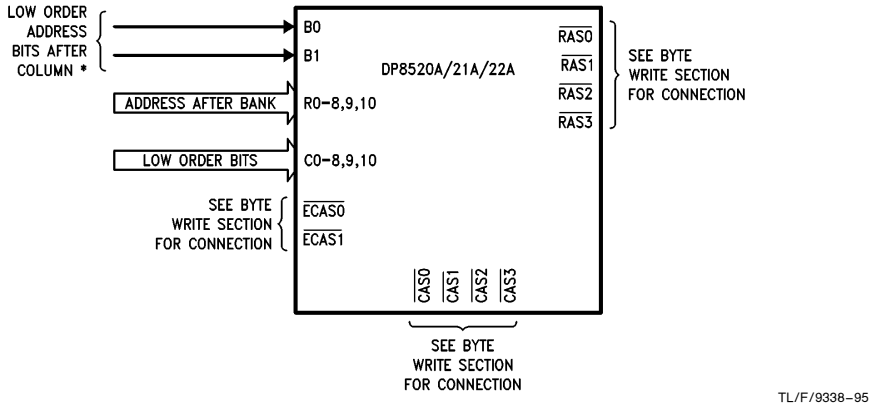
FIGURE 43. VRAM Array Setup for Error Scrubbing with 2 Banks (C6, C5, C4 = 0, 0, 1 during Programming)

8.0 $\overline{RAS}$ and $\overline{CAS}$ Configuration Modes (Continued)

8.5 PAGE/BURST MODE

In a static column, page or burst mode system, the least significant bits must be tied to the column address in order to ensure that the page/burst accesses are to sequential memory addresses, as shown in *Figure 44*. In a nibble mode system, the two least significant address bits (A2, A3) must be tied to the highest row and column address inputs (depends on VRAM size) to ensure that the toggling bits of nibble mode VRAMs are to sequential memory addresses. The $\overline{ECAS}$ inputs may then be toggled with the DP8520A/21A/22A's address latches in fall-through mode, while $\overline{AREQ}$ is asserted. The $\overline{ECAS}$ inputs can also be used to select individual bytes. When using nibble mode VRAMS, the third and fourth address bits can be tied to the bank select inputs to perform memory interleaving. In page or static column modes, the two address bits after the page size can be tied to the bank select inputs to select a new bank if the page size is exceeded.



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*See table below for row, column & bank address bit map. A0,A1 are used for byte addressing in this example.

Addresses	Nibble Mode*	Page Mode/Static Column Mode Page Size			
		256 Bits/Page	512 Bits/Page	1024 Bits/Page	2048 Bits/Page
Column Address	R9, C9 = A2, A3 C0–8 = X	C0–7 = A2–9 C8–10 = X	C0–8 = A2–10 C9,10 = X	C0–9 = A2–11 C10 = X	C0–10 = A2–12
Row Address	X	X	X	X	X
B0 B1	A4 A5	A10 A11	A11 A12	A12 A13	A13 A14

*Assuming 1 M-bit Vrams are being used.

Assume that the least significant address bits are used for byte addressing. Given a 32-bit system A0,A1 would be used for byte addressing.

X = DON'T CARE, the user can do as he pleases.

FIGURE 44. Page, Static Column, Nibble Mode System

9.0 Programming and Resetting

The DP8520A/21A/22A must be programmed by one of two possible programming sequences before it can be used. After power up, the DP8520A/21A/22A must be externally reset (see External Reset) before programming. After programming, the DP8520A/21A/22A enters a 60 ms initialization period. During this initialization period, the DP8520A/21A/22A performs refreshes about every 15 μs; this makes further VRAM warmup cycles unnecessary. The chip can be programmed as many times as the user wishes. After the first programming, the 60 ms initialization period will not be entered into unless the chip is reset. Refreshes occur during the 60 ms initialization period. If $\overline{\text{ECAS}}$0 was asserted during programming, the $\overline{\text{RFIP}}$ ($\overline{\text{RFRQ}}$) pin will act as $\overline{\text{RFIP}}$ and will be asserted throughout the initialization period, otherwise the pin will act like $\overline{\text{RFRQ}}$ and toggle every 13 μs−15 μs in conjunction with internal refresh requests. If the user attempts an access during the initialization period, wait states will be inserted into the access cycle until the initialization period is complete and $\overline{\text{RAS}}$ precharge time has been met. The actual initialization time period is given by the following formula:

T = 4096*(Clock Divisor Select)
*(Refresh Clock Fine Tune)
/(DELCK Frequency)

9.1 MODE LOAD ONLY PROGRAMMING

MODE LOAD, $\overline{\text{ML}}$, asserted enables an internal 23-bit programmable register. To use this method, the user asserts $\overline{\text{ML}}$, enabling the internal programming register. After $\overline{\text{ML}}$ is asserted, a valid programming selection is placed on the address bus (and $\overline{\text{ECAS}}$0), then $\overline{\text{ML}}$ is negated. When $\overline{\text{ML}}$ is negated, the value on the address bus (and $\overline{\text{ECAS}}$0) is latched into the internal programming register and the DP8520A/21A/22A is programmed, as shown in *Figure 45.* After $\overline{\text{ML}}$ is negated, the DP8520A/21A/22A will enter the 60 ms initialization period only if this is the first programming after power up or reset.

Using this method, a set of transceivers on the address bus can be put at TRI-STATE® by the system reset signal. A combination of pull-up and pull-down resistors can be used on the address inputs of the DP8520A/21A/22A to select the programming values, as shown in *Flgure 46*.

9.2 CHIP SELECTED ACCESS PROGRAMMING

The chip can also be programmed by asserting $\overline{\text{ML}}$ and performing a chip selected access. $\overline{\text{ADS}}$ (or ALE) is disabled internally until after programming. To program the chip using this method, $\overline{\text{ML}}$ is asserted. After $\overline{\text{ML}}$ is asserted, $\overline{\text{CS}}$ is asserted and a valid programming selection is placed on the address bus. When $\overline{\text{AREQ}}$ is asserted, the chip is programmed with the programming selection on the address bus. After $\overline{\text{AREQ}}$ is negated, $\overline{\text{ML}}$ can be negated as shown in *Figure 47*.

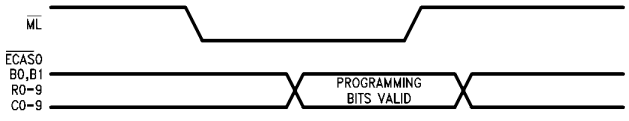
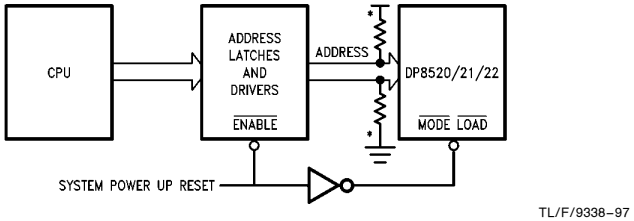


FIGURE 45. Mode Load Only Programming



*Pull-Up or Pull-Down Resistors on Each Address Input

FIGURE 46. Programming during System Reset

9.0 Programming and Resetting (Continued)

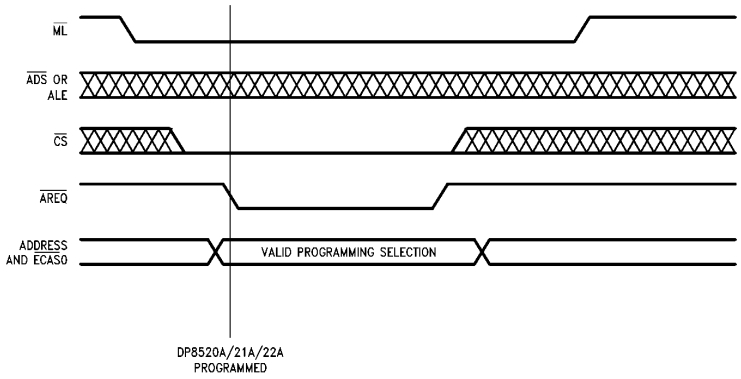


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FIGURE 47. $\overline{CS}$ Access Programming

Using this method, various programming schemes can be used. For example if extra upper address bits are available, an unused high order address bit can be tied to the signal $\overline{ML}$. Using this method, one need only write to a page of memory, thus asserting the high order bit and in turn programming the chip as shown in *Figure 48*.

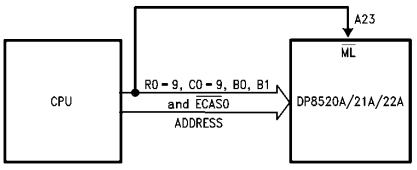

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FIGURE 48. Programming the DP8520A/21A/22A through the Address Bus Only

An I/O port can also be used to assert $\overline{ML}$. After $\overline{ML}$ is asserted, a chip selected access can be performed to program the chip. After the chip selected access, $\overline{ML}$ can be negated through the I/O port as shown in *Figure 49*.

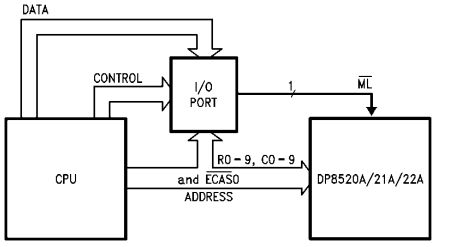

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FIGURE 49. Programming the DP8520A/21A/22A through the Address Bus and an I/O Port

Another simple way the chip can be programmed is the first write after system reset. This method requires only a flip-flop and an OR gate as shown in *Figure 50.* At reset, the flip-flop is preset, which pulls the $\overline{Q}$ output low. Since $\overline{WR}$ is negated, $\overline{ML}$ is not enabled. The first write access is used to program the chip. When $\overline{WR}$ is asserted, $\overline{ML}$ is asserted. $\overline{WR}$ negated clocks the flip-flop, negates $\overline{ML}$, and programs the DP8520A/21A/22A with the address and $\overline{ECAS0}$ available at that time. $\overline{CS}$ does not need to be asserted using this method.

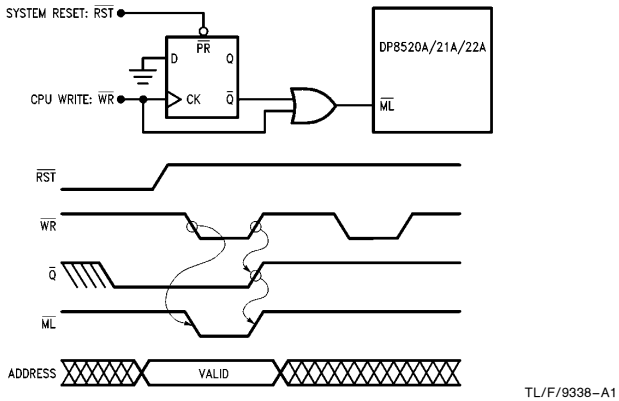

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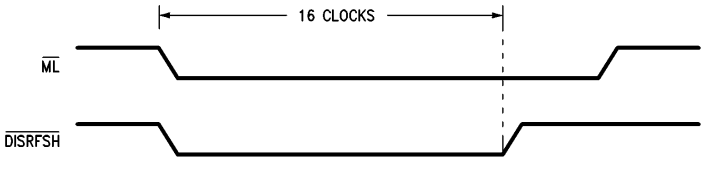
FIGURE 50. Programming the DP8520A/21A/22A on the First CPU Write after Power Up

9.0 Programming and Resetting (Continued)

9.3 EXTERNAL RESET

At power up, if the internal power up reset worked, all internal latches and flip-flops are cleared. The power up state is entered by asserting $\overline{ML}$ and $\overline{DISRFSH}$ for 16 positive edges of CLK. After 16 clocks if the user negates $\overline{DISRFSH}$ before negating $\overline{ML}$ as shown in *Figure 51,* $\overline{ML}$ negated will program the chip. If $\overline{ML}$ is negated before or at the same time as $\overline{DISRFSH}$ as shown in *Figure 52,* the chip will not be programmed. After the chip is programmed, the 60 ms initialization period will be entered into if this is the first programming after power up or reset. The user must perform an external reset before programming the DP8520A/21A/22A.



TL/F/9338–A2

FIGURE 51. Chip Reset and Programmed

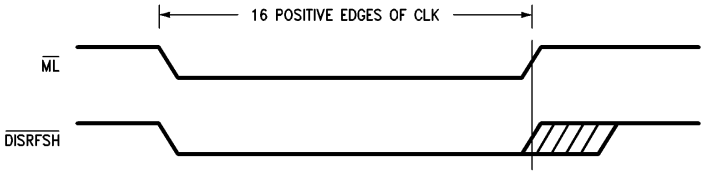


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FIGURE 52. Chip Reset but Not Programmed

9.0 Programming and Resetting (Continued)

9.4 PROGRAMMING BIT DEFINITIONS

Symbol	Description
$\overline{ECAS}$0	**Extend $\overline{CAS}$/Refresh Request Select**
0	The $\overline{CAS}$n outputs will be negated with the $\overline{RAS}$n outputs when $\overline{AREQ}$ (or $\overline{AREQB}$, DP8522A only) is negated. The $\overline{RFIP}$ pin will function as refresh in progress. During a video shift register load operation, the $\overline{DT}/\overline{OE}$ output will be negated by either the 4th rising clock edge after the input $\overline{VSRL}$ asserts, or by the $\overline{VSRL}$ input negating, whichever occurs first, when this mode is programmed.
1	The $\overline{CAS}$n outputs will be negated, during an access (Port A (or Port B, DP8522A only)) when their corresponding $\overline{ECAS}$n inputs are negated. This feature allows the $\overline{CAS}$ outputs to be extended beyond the $\overline{RAS}$ outputs negating. Scrubbing refreshes are NOT affected. During scrubbing refreshes the $\overline{CAS}$ outputs will negate along with the $\overline{RAS}$ outputs regardless of the state of the $\overline{ECAS}$ inputs. The $\overline{RFIP}$ output will function as ReFresh ReQuest ($\overline{RFRQ}$) when this mode is programmed. The $\overline{DT}/\overline{OE}$ output will be negated by the input $\overline{VSRL}$ negating when this mode is programmed.
B1	**Access Mode Select**
0	**ACCESS MODE 0:** ALE pulsing high sets an internal latch. On the next positive edge of CLK, the access ($\overline{RAS}$) will start. $\overline{AREQ}$ will terminate the access.
1	**ACCESS MODE 1:** $\overline{ADS}$ asserted starts the access ($\overline{RAS}$) immediately. $\overline{AREQ}$ will terminate the access.
B0	**Address Latch Mode**
0	$\overline{ADS}$ or ALE asserted for Port A or $\overline{AREQB}$ asserted for Port B with the appropriate GRANT latch the input row, column and bank address.
1	The row, column and bank latches are fall through.
C9	**Delay $\overline{CAS}$ during WRITE Accesses**
0	$\overline{CAS}$ is treated the same for both READ and WRITE accesses.
1	During WRITE accesses, $\overline{CAS}$ will be asserted by the event that occurs last: $\overline{CAS}$ asserted by the internal delay line or $\overline{CAS}$ asserted on the positive edge of CLK after $\overline{RAS}$ is asserted.
C8	**Row Address Hold Time**
0	Row Address Hold Time = 25 ns minimum
1	Row Address Hold Time = 15 ns minimum
C7	**Column Address Setup Time**
0	Column Address Setup Time = 10 ns minimum
1	Column Address Setup Time = 0 ns minimum
C6, C5, C4	**$\overline{RAS}$ and $\overline{CAS}$ Configuration Modes/Error Scrubbing during Refresh**
0, 0, 0	$\overline{RAS}$0–3 and $\overline{CAS}$0–3 are all selected during an access. For a particular $\overline{CAS}$ to be asserted, its corresponding $\overline{ECAS}$ input must be asserted. B0 and B1 are not used during an access. Error scrubbing during refresh.
0, 0, 1	$\overline{RAS}$ and $\overline{CAS}$ pairs are selected during an access by B1. For a particular $\overline{CAS}$ to be asserted, its corresponding $\overline{ECAS}$ input must be asserted. B1 = 0 during an access selects $\overline{RAS}$0–1 and $\overline{CAS}$0–1. B1 = 1 during an access selects $\overline{RAS}$2–3 and $\overline{CAS}$2–3. B0 is not used during an Access. Error scrubbing during refresh.
0, 1, 0	RAS and CAS singles are selected during an access by B0–1. For a particular $\overline{CAS}$ to be asserted, its corresponding $\overline{ECAS}$ input must be asserted. B1 = 0, B0 = 0 during an access selects $\overline{RAS}$0 and $\overline{CAS}$0. B1 = 0, B0 = 1 during an access selects $\overline{RAS}$1 and $\overline{CAS}$1. B1 = 1, B0 = 0 during an access selects $\overline{RAS}$2 and $\overline{CAS}$2. B1 = 1, B0 = 1 during an access selects $\overline{RAS}$3 and $\overline{CAS}$3. Error scrubbing during refresh.
0, 1, 1	$\overline{RAS}$0–3 and $\overline{CAS}$0–3 are all selected during an access. For a particular $\overline{CAS}$ to be asserted, its corresponding $\overline{ECAS}$ input must be asserted. B1, B0 are not used during an access. No error scrubbing. ($\overline{RAS}$ only refreshing)

9.0 Programming and Resetting (Continued)

9.4 PROGRAMMING BIT DEFINITIONS (Continued)

Symbol	Description
C6, C5, C4	**$\overline{RAS}$ and $\overline{CAS}$ Configuration Modes** (Continued)
1, 0, 0	$\overline{RAS}$ pairs are selected by B1. $\overline{CAS}$0–3 are all selected. For a particular $\overline{CAS}$ to be asserted, its corresponding $\overline{ECAS}$ input must be asserted. B1 = 0 during an access selects $\overline{RAS}$0–1 and $\overline{CAS}$0–3. B1 = 1 during an access selects $\overline{RAS}$2–3 and $\overline{CAS}$0–3. B0 is not used during an access. No error scrubbing.
1, 0, 1	$\overline{RAS}$ and $\overline{CAS}$ pairs are selected by B1. For a particular $\overline{CAS}$ to be asserted, its corresponding $\overline{ECAS}$ input must be asserted. B1 = 0 during an access selects $\overline{RAS}$0–1 and $\overline{CAS}$0–1. B1 = 1 during an access selects $\overline{RAS}$2–3 and $\overline{CAS}$2–3. B0 is not used during an access. No error scrubbing.
1, 1, 0	$\overline{RAS}$ singles are selected by B0–1. $\overline{CAS}$0–3 are all selected. For a particular $\overline{CAS}$ to be asserted, its corresponding $\overline{ECAS}$ input must be asserted. B1 = 0, B0 = 0 during an access selects $\overline{RAS}$0 and $\overline{CAS}$0–3. B1 = 0, B0 = 1 during an access selects $\overline{RAS}$1 and $\overline{CAS}$0–3. B1 = 1, B0 = 0 during an access selects $\overline{RAS}$2 and $\overline{CAS}$0–3. B1 = 1, B0 = 1 during an access selects $\overline{RAS}$3 and $\overline{CAS}$0–3. No error scrubbing.
1, 1, 1	$\overline{RAS}$ and $\overline{CAS}$ singles are selected by B0, 1. For a particular $\overline{CAS}$ to be asserted, its corresponding $\overline{ECAS}$ input must be asserted. B1 = 0, B0 = 0 during an access selects $\overline{RAS}$0 and $\overline{CAS}$0. B1 = 0, B0 = 1 during an access selects $\overline{RAS}$1 and $\overline{CAS}$1. B1 = 1, B0 = 0 during an access selects $\overline{RAS}$2 and $\overline{CAS}$2. B1 = 1, B0 = 1 during an access selects $\overline{RAS}$3 and $\overline{CAS}$3. No error scrubbing.
C3	**Refresh Clock Fine Tune Divisor**
0	Divide delay line/refresh clock further by 30 (If DELCLK/Refresh Clock Clock Divisor = 2 MHz = 15 μs refresh period).
1	Divide delay line/refresh clock further by 26 (If DELCLK/Refresh Clock Clock Divisor = 2 MHz = 13 μs refresh period).
C2, C1, C0	**Delay Line/Refresh Clock Divisor Select**
0, 0, 0	Divide DELCLK by 10 to get as close to 2 MHz as possible.
0, 0, 1	Divide DELCLK by 9 to get as close to 2 MHz as possible.
0, 1, 0	Divide DELCLK by 8 to get as close to 2 MHz as possible.
0, 1, 1	Divide DELCLK by 7 to get as close to 2 MHz as possible.
1, 0, 0	Divide DELCLK by 6 to get as close to 2 MHz as possible.
1, 0, 1	Divide DELCLK by 5 to get as close to 2 MHz as possible.
1, 1, 0	Divide DELCLK by 4 to get as close to 2 MHz as possible.
1, 1, 1	Divide DELCLK by 3 to get as close to 2 MHz as possible.
R9	**Refresh Mode Select**
0	$\overline{RAS}$0–3 will all assert and negate at the same time during a refresh.
1	Staggered Refresh. $\overline{RAS}$ outputs during refresh are separated by one positive clock edge. Depending on the configuration mode chosen, either one or two $\overline{RAS}$s will be asserted.
R8	**Address Pipelining Select**
0	Address pipelining is selected. The VRAM controller will switch the VRAM column address back to the row address after guaranteeing the column address hold time.
1	Non-address pipelining is selected. The VRAM controller will hold the column address on the VRAM address bus until the access $\overline{RAS}$s are negated.

9.0 Programming and Resetting (Continued)

9.4 PROGRAMMING BIT DEFINITIONS (Continued)

Symbol	Description
R7	**$\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$ Select**
0	$\overline{\text{WAIT}}$ type output is selected.
1	$\overline{\text{DTACK}}$ (Data Transfer ACKnowledge) type output is selected.
R6	**Add Wait States to the Current Access if $\overline{\text{WAITIN}}$ is Low**
0	$\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$ will be delayed by one additional positive edge of CLK.
1	$\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$ will be delayed by two additional positive edges of CLK.
R5, R4	**$\overline{\text{WAIT}}$/$\overline{\text{DTACK}}$ during Burst (See Section 5.1.2 or 5.2.2)**
0, 0	NO WAIT STATES; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will remain negated during burst portion of access. If R7 = 1 programming, $\overline{\text{DTACK}}$ will remain asserted during burst portion of access.
0, 1	1T; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will assert when the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted. $\overline{\text{WAIT}}$ will negate from the positive edge of CLK after the $\overline{\text{ECAS}}$s have been asserted. If R7 = 1 during programming, $\overline{\text{DTACK}}$ will negate when the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted. $\overline{\text{DTACK}}$ will assert from the positive edge of CLK after the $\overline{\text{ECAS}}$s have been asserted.
1, 0	½T; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will assert when the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted. $\overline{\text{WAIT}}$ will negate on the negative level of CLK after the $\overline{\text{ECAS}}$s have been asserted. If R7 = 1 during programming, $\overline{\text{DTACK}}$ will negate when the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted. $\overline{\text{DTACK}}$ will assert from the negative level of CLK after the $\overline{\text{ECAS}}$s have been asserted.
1, 1	0T; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will assert when the $\overline{\text{ECAS}}$ inputs are negated. $\overline{\text{WAIT}}$ will negate when the $\overline{\text{ECAS}}$ inputs are asserted. If R7 = 1 during programming, $\overline{\text{DTACK}}$ will negate when the $\overline{\text{ECAS}}$ inputs are negated. $\overline{\text{DTACK}}$ will assert when the $\overline{\text{ECAS}}$ inputs are asserted.
R3, R2	**$\overline{\text{WAIT}}$/$\overline{\text{DTACK}}$ Delay Times (See Section 5.1.1 or 5.2.1)**
0, 0	NO WAIT STATES; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will remain high during non-delayed accesses. $\overline{\text{WAIT}}$ will negate when $\overline{\text{RAS}}$ is negated during delayed accesses. NO WAIT STATES; If R7 = 1 during programming, $\overline{\text{DTACK}}$ will be asserted when $\overline{\text{RAS}}$ is asserted.
0, 1	½T; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will negate on the negative level of CLK, after the access $\overline{\text{RAS}}$. 1T; If R7 = 1 during programming, $\overline{\text{DTACK}}$ will be asserted on the positive edge of CLK after the access $\overline{\text{RAS}}$.
1, 0	NO WAIT STATES, ½T; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will remain high during non-delayed accesses. $\overline{\text{WAIT}}$ will negate on the negative level of CLK, after the access $\overline{\text{RAS}}$, during delayed accesses. ½T; If R7 = 1 during programming, $\overline{\text{DTACK}}$ will be asserted on the negative level of CLK after the access $\overline{\text{RAS}}$.
1, 1	1T; If R7 = 0 during programming, $\overline{\text{WAIT}}$ will negate on the positive edge of CLK after the access $\overline{\text{RAS}}$. 1½T; If R7 = 1 during programming, $\overline{\text{DTACK}}$ will be asserted on the negative level of CLK after the positive edge of CLK after the access $\overline{\text{RAS}}$.
R1, R0	**$\overline{\text{RAS}}$ Low and $\overline{\text{RAS}}$ Precharge Time**
0, 0	$\overline{\text{RAS}}$ asserted during refresh = 2 positive edges of CLK. $\overline{\text{RAS}}$ precharge time = 1 positive edge of CLK. $\overline{\text{RAS}}$ will start from the first positive edge of CLK after GRANTB transitions (DP8522A).
0, 1	$\overline{\text{RAS}}$ asserted during refresh = 3 positive edges of CLK. $\overline{\text{RAS}}$ precharge time = 2 positive edges of CLK. $\overline{\text{RAS}}$ will start from the second positive edge of CLK after GRANTB transitions (DP8522A).
1, 0	$\overline{\text{RAS}}$ asserted during refresh = 2 positive edges of CLK. $\overline{\text{RAS}}$ precharge time = 2 positive edges of CLK. $\overline{\text{RAS}}$ will start from the first positive edge of CLK after GRANTB transitions (DP8522A).
1, 1	$\overline{\text{RAS}}$ asserted during refresh = 4 positive edges of CLK. $\overline{\text{RAS}}$ precharge time = 3 positive edges of CLK. $\overline{\text{RAS}}$ will start from the second positive edge of CLK after GRANTB transitions (DP8522A).

Note 1: The configuration modes allow $\overline{\text{RAS}}$s and $\overline{\text{CAS}}$s to be grouped such that each $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ will drive one-fourth of the total VRAM array whether the array is organized as 1, 2, or 4 banks.

Note 2: In order for a $\overline{\text{CAS}}$ output to go low during an access, it must be both selected and enabled. $\overline{\text{ECAS}}$0–1 are used to enable the $\overline{\text{CAS}}$ outputs ($\overline{\text{ECAS}}$0 enables $\overline{\text{CAS}}$0,1; $\overline{\text{ECAS}}$1 enables $\overline{\text{CAS}}$2,3). Selection is determined by the configuration mode and B1, B0.

10.0 Test Mode

Staggered refresh in combination with the error scrubbing mode places the DP8520A/21A/22A in test mode. In this mode, the 24-bit refresh counter is divided into a 13-bit and 11-bit counter. During refreshes both counters are incremented to reduce test time.

11.0 VRAM Critical Timing Parameters

The two critical timing parameters, shown in *Figure 53*, that must be met when controlling the access timing to a VRAM are the row address hold time, tRAH, and the column address setup time, tASC. Since the DP8520A/21A/22A contain a precise internal delay line, the values of these parameters can be selected at programming time. These values will also increase and decrease if DELCLK varies from 2 MHz.

11.1 PROGRAMMABLE VALUES OF tRAH AND tASC

The DP8520A/21A/22A allow the values of tRAH and tASC to be selected at programming time. For each parameter, two choices can be selected. tRAH, the row address hold time, is measured from $\overline{RAS}$ asserted to the row address starting to change to the column address. The two choices for tRAH are 15 ns and 25 ns, programmable through address bit C8.

tASC, the column address setup time, is measured from the column address valid to $\overline{CAS}$ asserted. The two choices for tASC are 0 ns and 10 ns, programmable through address bit C7.

11.2 CALCULATION OF tRAH AND tASC

There are two clock inputs to the DP8520A/21A/22A. These two clocks, DELCLK and CLK can either be tied together to the same clock or be tied to different clocks running asynchronously at different frequencies.

The clock input, DELCLK, controls the internal delay line and refresh request clock. DELCLK should be a multiple of 2 MHz. If DELCLK is not a multiple of 2 MHz, tRAH and tASC will change. The new values of tRAH and tASC can be calculated by the following formulas:

If tRAH was programmed to equal 15 ns then tRAH = 30*(((DELCLK Divisor)* 2 MHz/(DELCLK Frequency))−1) + 15 ns.

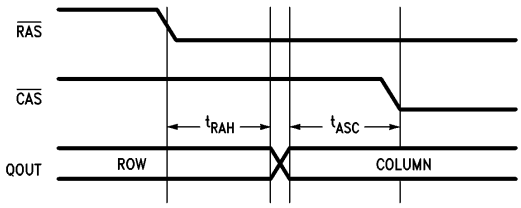
If tRAH was programmed to equal 25 ns then tRAH = 30*(((DELCLK Divisor)* 2 MHz/(DELCLK Frequency))−1) + 25 ns.

If tASC was programmed to equal 0 ns then tASC = 15* ((DELCLK Divisor)* 2 MHz/(DELCLK Frequency)) − 15 ns.

If tASC was programmed to equal 10 ns then tASC = 25* ((DELCLK Divisor)* 2 MHz/(DELCLK Frequency)) − 15 ns.

Since the values of tRAH and tASC are increased or decreased, the time to $\overline{CAS}$ asserted will also increase or decrease. These parameters can be adjusted by the following formula:

Delay to $\overline{CAS}$ = Actual Spec. + Actual tRAH − Programmed tRAH + Actual tASC − Programmed tASC.



TL/F/9338–A4

FIGURE 53. tRAH and tASC

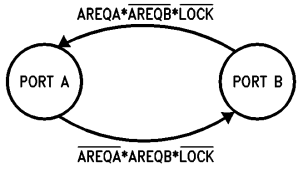
12.0 Dual Accessing Functions (DP8522A)

The DP8522A has all the functions previously described. In addition to those features, the DP8522A also has the capabilities to arbitrate among refresh, Port A and a second port, Port B. This allows two CPUs to access a common VRAM array. VRAM refresh has the highest priority followed by the currently granted port. The ungranted port has the lowest priority. The last granted port will continue to stay granted even after the access has terminated, until an access request is received from the ungranted port (see *Figure 54a*). The dual access configuration assumes that both Port A and Port B are synchronous to the system clock. If they are not synchronous to the system clock they should be externally synchronized (Ex. By running the access requests through several Flip-Flops, see *Figure 58a*).

12.1 PORT B ACCESS MODES (DP8522A)

Port B accesses are initiated from a single input, $\overline{\text{AREQB}}$. When $\overline{\text{AREQB}}$ is asserted, an access request is generated. If GRANTB is asserted and a refresh is not taking place or precharge time is not required, $\overline{\text{RAS}}$ will be asserted when $\overline{\text{AREQB}}$ is asserted. Once $\overline{\text{AREQB}}$ is asserted, it must stay asserted until the access is over. $\overline{\text{AREQB}}$ negated, negates $\overline{\text{RAS}}$ as shown in *Figure 54b.* Note that if $\overline{\text{ECAS}}0 = 1$ during programming the $\overline{\text{CAS}}$ outputs may be held asserted (beyond $\overline{\text{RAS}}$n negating) by continuing to assert the appropriate $\overline{\text{ECAS}}$ input (the same as Port A accesses). If Port B is not granted, the access will begin on the first or second positive edge of CLK after GRANTB is asserted (See R0, R1 programming bit definitions) as shown in *Figure 54c*, assuming that Port A is not accessing the VRAM ($\overline{\text{CS}}$, $\overline{\text{ADS}}$/ALE and $\overline{\text{AREQ}}$) and $\overline{\text{RAS}}$ precharge for the particular bank has completed. It is important to note that for GRANTB to transition to Port B, Port A must **not** be requesting an access at a rising clock edge (or locked) and Port B must be requesting an access at that rising clock edge. Port A can request an access through $\overline{\text{CS}}$ and $\overline{\text{ADS}}$/ALE or $\overline{\text{CS}}$ and $\overline{\text{AREQ}}$. Therefore during an interleaved access where $\overline{\text{CS}}$ and $\overline{\text{ADS}}$/ALE become asserted before $\overline{\text{AREQ}}$ from the previous access is negated, Port A will retain GRANTB = 0 whether $\overline{\text{AREQB}}$ is asserted or not.

Since there is no chip select for Port B, $\overline{\text{AREQB}}$ must incorporate this signal. This mode of accessing is similar to Mode 1 accessing for Port A.



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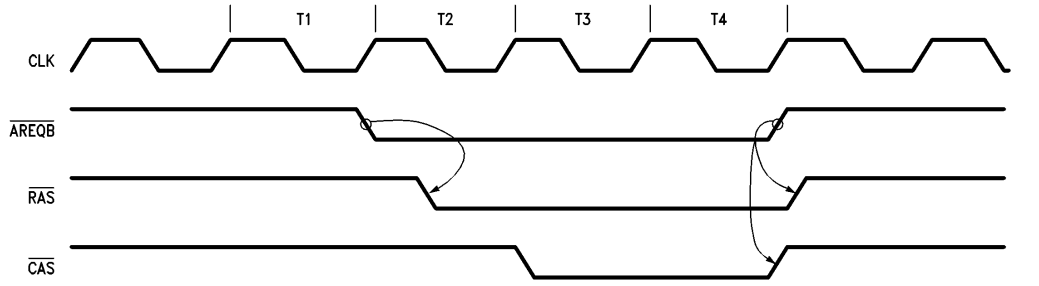
Explanation of Terms

AREQA = Chip Selected access request from Port A

AREQB = Chip Selected access request from Port B

LOCK = Externally controlled LOCKing of the Port that is currently GRANTed.

FIGURE 54a. DP8522A PORT A/PORT B ARBITRATION STATE DIAGRAM. This arbitration may take place during the "ACCESS" or "REFRESH" state (see *Figure 7a*).



TL/F/9338–A6

FIGURE 54b. Access Request for Port B

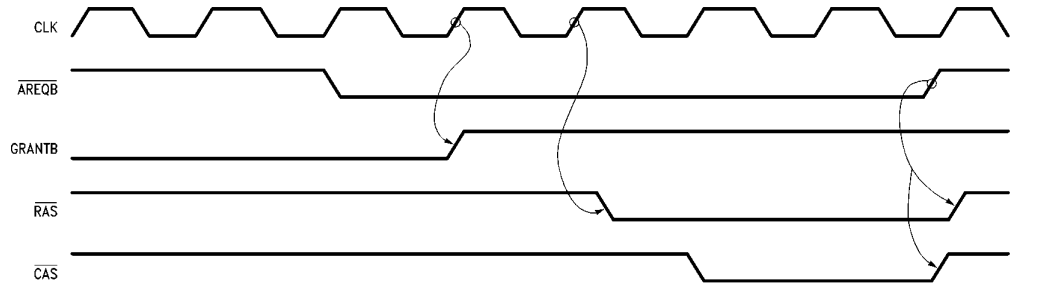


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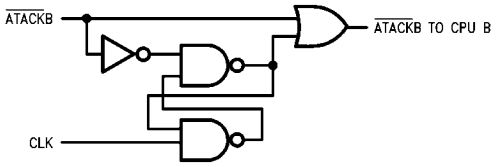
FIGURE 54c. Delayed Port B Access

12.0 Dual Accessing Functions (DP8522A) (Continued)

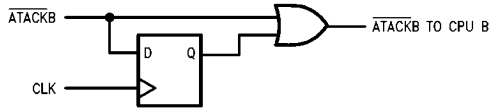
12.2 PORT B WAIT STATE SUPPORT (DP8522A)

Advanced transfer acknowledge for Port B, $\overline{\text{ATACKB}}$, is used for wait state support for Port B. This output will be asserted when $\overline{\text{RAS}}$ for the Port B access is asserted, as shown in *Figures 55* and *56*. Once asserted, this output will stay asserted until $\overline{\text{AREQB}}$ is negated. With external logic, $\overline{\text{ATACKB}}$ can be made to interface to any CPU's wait input as shown in *Figure 57*.



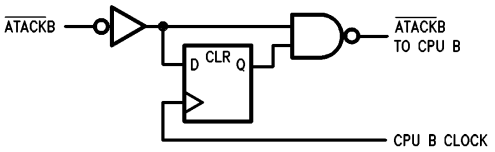
TL/F/9338–A8

A) Extend $\overline{\text{ATACK}}$ to ½T (½ Clock) after $\overline{\text{RAS}}$ goes low.



TL/F/9338–A9

B) Extend $\overline{\text{ATACK}}$ to 1T after $\overline{\text{RAS}}$ goes low.



TL/F/9338–B0

C) Synchronize $\overline{\text{ATACKB}}$ to CPU B Clock. This is useful if CPU B runs asynchronous to the DP8522.

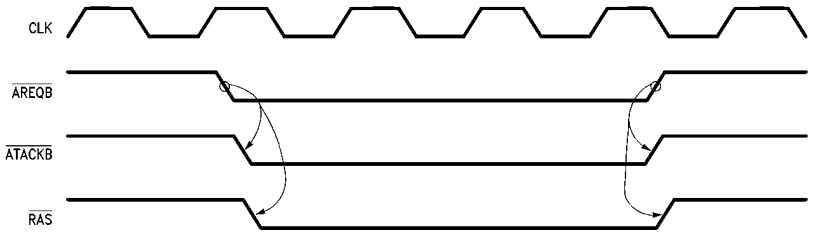
FIGURE 57. Modifying Wait Logic for Port B

12.3 COMMON PORT A AND PORT B DUAL PORT FUNCTIONS

An input, $\overline{\text{LOCK}}$, and an output, GRANTB, add additional functionality to the dual port arbitration logic. $\overline{\text{LOCK}}$ allows Port A or Port B to lock out the other port from the VRAM. When a Port is locked out of the VRAM, wait states will be inserted into its access cycle until it is allowed to access memory. GRANTB is used to multiplex the input control signals and addresses to the DP8522A.

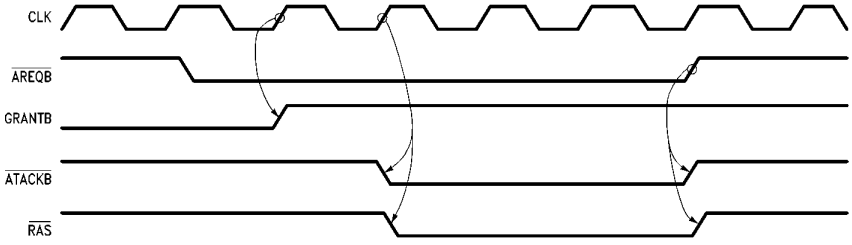
12.3.1 GRANTB Output

The output GRANTB determines which port has current access to the VRAM array. GRANTB asserted signifies Port B has access. GRANTB negated signifies Port A has access to the VRAM array.



TL/F/9338–B1

FIGURE 55. Non-Delayed Port B Access



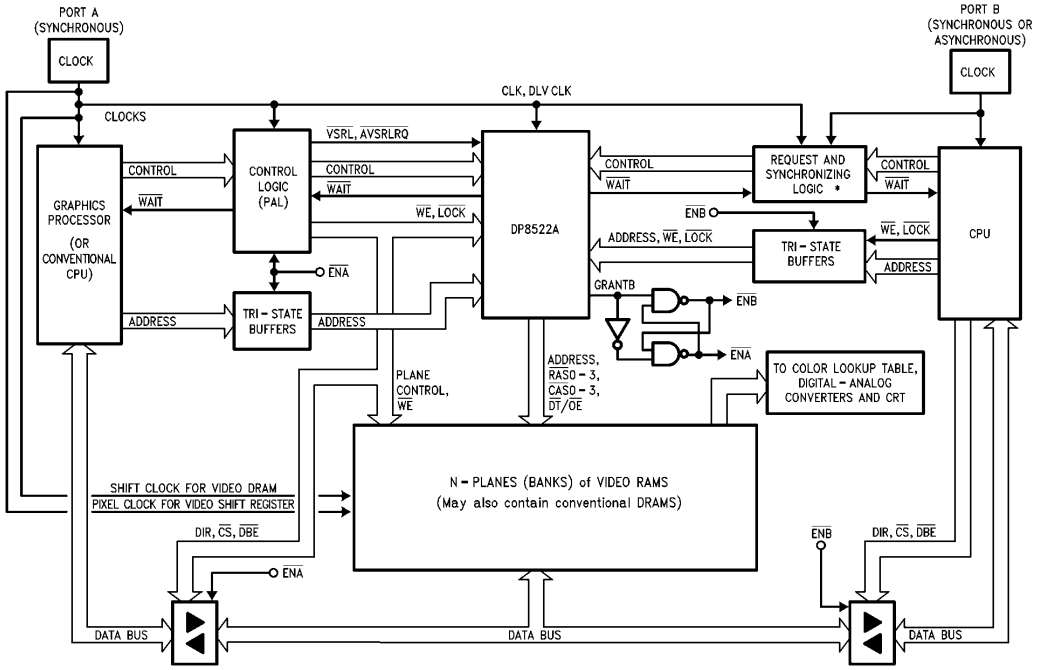
TL/F/9338–B2

FIGURE 56. Delayed Port B Access

12.0 Dual Accessing Functions (DP8522A) (Continued)

Since the DP8522A has only one set of address inputs, the signal is used, with the addition of buffers, to allow the currently granted port's addresses to reach the DP8522A. The signals which need to be bufferred are R0–10, C0–10, B0–1, $\overline{ECAS}$0–1, and $\overline{LOCK}$. All other inputs are not common and do not have to be buffered as shown in *Figure 58a*. If a Port, which is not currently granted, tries to access the VRAM array, the GRANTB output will transition from a rising clock edge from $\overline{AREQ}$ or $\overline{AREQB}$ negating and will preceed the $\overline{RAS}$ for the access by one or two clock periods. GRANTB will then stay in this state until the other port requests an access and the currently granted port is not accessing the VRAM as shown in *Figure 58b*.

Dual Accessing Using the DP8522A

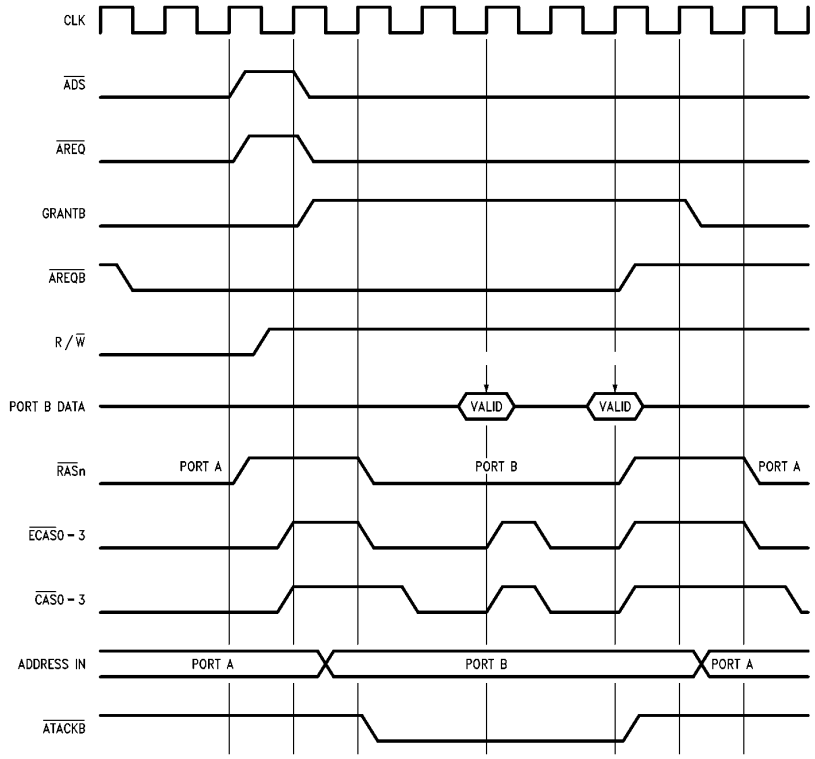


TL/F/9338–1

*If Port B is synchronous the Request Synchronizing logic will not be required.

FIGURE 58a. Dual Accessing Using the DP8522A to interface a CPU and a Graphics Processor to a Video RAM System

12.0 Dual Accessing Functions (DP8522A) (Continued)



TL/F/9338–B3

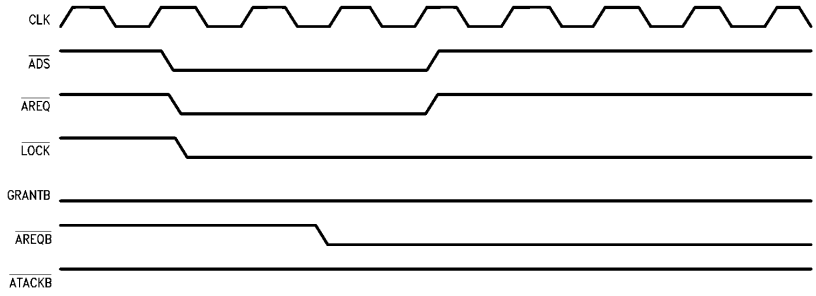
FIGURE 58b. Wait States during a Port B Access

12.3.2 LOCK Input

When the LOCK input is asserted, the currently granted port can ''lock out'' the other port through the insertion of wait states to that port's access cycle. LOCK does not disable refreshes, it only keeps GRANTB in the same state even if the other port requests an access, as shown in *Figure 59*. LOCK can be used by either port. The user must guarantee that LOCK is not asserted with Port B granted when AVSRLRQ is asserted to request a VRAM transfer cycle.

12.4 DUAL PORTING AND VRAM TRANSFER CYCLES

The input AVSRLRQ disables any further internally or externally requested refreshes or Port B access requests from being executed. The AVSRLRQ input does this by making the VRAM controller arbitration logic think that a Port A access is in progress from the point where the AVSRLRQ input goes low until the VRAM shift register load operation is completed.



TL/F/9338–B4

FIGURE 59. LOCK Function

13.0 Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature under Bias . . . . . 0°C to +70°C

Storage Temperature . . . . . −65°C to +150°C

All Input or Output Voltage with Respect to GND . . . . . −0.5V to +7V

Power Dissipation @ 20 MHz 0.5W

14.0 DC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage	Tested with a Limited Functional Pattern	2.0		$V_{CC} + 0.5$	V
V_{IL}	Logical 0 Input Voltage	Tested with a Limited Functional Pattern	−0.5		0.8	V
V_{OH1}	Q and $\overline{WE}$ Outputs	$I_{OH} = -10$ mA	$V_{CC} - 1.0$			V
V_{OL1}	Q and $\overline{WE}$ Outputs	$I_{OL} = 10$ mA			0.5	V
V_{OH2}	All Outputs except Qs, $\overline{WE}$	$I_{OH} = -3$ mA	$V_{CC} - 1.0$			V
V_{OL2}	All Outputs except Qs, $\overline{WE}$	$I_{OL} = 3$ mA			0.5	V
I_{IN}	Input Leakage Current	$V_{IN} = V_{CC}$ or GND	−10		10	μA
$I_{IL\ ML}$	$\overline{ML}$ Input Current (Low)	V_{IN} = GND			200	μA
I_{CC1}	Standby Current	CLK at 8 MHz ($V_{IN} = V_{CC}$ or GND)		6	15	mA
I_{CC1}	Standby Current	CLK at 20 MHz ($V_{IN} = V_{CC}$ or GND)		8	17	mA
I_{CC1}	Standby Current	CLK at 25 MHz ($V_{IN} = V_{CC}$ or GND)		10	20	mA
I_{CC2}	Supply Current	CLK at 8 MHz (Inputs Active) ($I_{LOAD} = 0$) ($V_{IN} = V_{CC}$ or GND)		20	40	mA
I_{CC2}	Supply Current	CLK at 20 MHz (Inputs Active) ($I_{LOAD} = 0$) ($V_{IN} = V_{CC}$ or GND)		40	75	mA
I_{CC2}	Supply Current	CLK at 25 MHz (Inputs Active) ($I_{LOAD} = 0$) ($V_{IN} = V_{CC}$ or GND)		50	95	mA
C_{IN}*	Input Capacitance	f_{IN} at 1 MHz			10	pF

*Note: C_{IN} is not 100% tested.

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A

The AC timing parameters are grouped into sectional numbers as shown below. These numbers also refer to the timing diagrams.

1–38 Common parameters to all modes of operation

50–56 Difference parameters used to calculate;
$\overline{RAS}$ low time,
$\overline{RAS}$ precharge time,
$\overline{CAS}$ high time and
$\overline{CAS}$ low time

100–121 Common dual access parameters used for Port B accesses and inputs and outputs used only in dual accessing

200–212 Refresh parameters

300–315 Mode 0 access parameters used in both single and dual access applications

400–416 Mode 1 access parameters used in both single and dual access applications

450–455 Special Mode 1 access parameters which supersede the 400–416 parameters when dual accessing

500–506 Programming parameters

600–605 Graphics parameters for VRAM transfer cycles

Unless otherwise stated $V_{CC} = 5.0V \pm 10\%$, $0 < T_A < 70°C$, the output load capacitance is typical for 4 banks of 18 VRAMs per bank, including trace capacitance (see Note 2).

Two different loads are specified:

C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9, and 10; or

C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9, and 10.

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)

Number	Symbol	Common Parameter Description	8520A/21A/22A-25			
			C_L		C_H	
			Min	Max	Min	Max
1	fCLK	CLK Frequency	0	25	0	25
2	tCLKP	CLK Period	40		40	
3, 4	tCLKPW	CLK Pulse Width	12		12	
5	fDCLK	DELCLK Frequency	5	20	5	20
6	tDCLKP	DELCLK Period	50	200	50	200
7, 8	tDCLKPW	DELCLK Pulse Width	12		12	
9a	tPRASCAS0	$\overline{RAS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 0 ns)	30		30	
9b	tPRASCAS1	$\overline{RAS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 10 ns)	40		40	
9c	tPRASCAS2	($\overline{RAS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 0 ns)	40		40	
9d	tPRASCAS3	($\overline{RAS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 10 ns)	50		50	
10a	tRAH	Row Address Hold Time (tRAH = 15)	15		15	
10b	tRAH	Row Address Hold Time (tRAH = 25)	25		25	
11a	tASC	Column Address Setup Time (tASC = 0)	0		0	
11b	tASC	Column Address Setup Time (tASC = 10)	10		10	
12	tPCKRAS	CLK High to $\overline{RAS}$ Asserted following Precharge		22		26
13	tPARQRAS	$\overline{AREQ}$ Negated to $\overline{RAS}$ Negated		31		35
14	tPENCL	$\overline{ECAS}$0–1 Asserted to $\overline{CAS}$ Asserted		20		27
15	tPENCH	$\overline{ECAS}$0–1 Negated to $\overline{CAS}$ Negated		20		27
16	tPARQCAS	$\overline{AREQ}$ Negated to $\overline{CAS}$ Negated		47		54
17	tPCLKWH	CLK to $\overline{WAIT}$ Negated		31		31
18	tPCLKDL0	CLK to $\overline{DTACK}$ Asserted (Programmed as $\overline{DTACK}$ of 1/2, 1, 1½ or if $\overline{WAITIN}$ is Asserted)		28		28
19	tPEWL	$\overline{ECAS}$ Negated to $\overline{WAIT}$ Asserted during a Burst Access		36		36
20	tSECK	$\overline{ECAS}$ Asserted Setup to CLK High to Recognize the Rising Edge of CLK during a Burst Access	19		19	

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)

Unless otherwise stated $V_{CC} = 5.0V \pm 10\%$, $0°C < T_A < 70°C$, the output load capacitance is typical for 4 banks of 18 VRAMs per bank, including trace capacitance (see Note 2).

Two different loads are specified:
$C_L = 50$ pF loads on all outputs except
$C_L = 150$ pF loads on Q0–8, 9 and 10; or
$C_H = 50$ pF loads on all outputs except
$C_H = 125$ pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
$C_H = 380$ pF loads on Q0–8, 9 and 10.

Number	Symbol	Common Parameter Description	8520A/21A/22A-25			
			C_L		C_H	
			Min	Max	Min	Max
21	tPEDL	$\overline{ECAS}$ Asserted to $\overline{DTACK}$ Asserted during a Burst Access (Programmed as $\overline{DTACK}$0)		38		38
22	tPEDH	$\overline{ECAS}$ Negated to $\overline{DTACK}$ Negated during a Burst Access		38		38
23	tSWCK	$\overline{WAITIN}$ Asserted Setup to CLK	5		5	
26	tPAQ	Row, Column Address Valid to Q0–8, 9, 10 Valid		26		35
27	tPCINCQ	COLINC Asserted to Q0–8, 9, 10 Incremented		30		39
28	tSCINEN	COLINC Asserted Setup to $\overline{ECAS}$ Asserted to Ensure tASC = 0 ns	17		19	
29a	tSARQCK1	$\overline{AREQ}$ Negated Setup to CLK High with 1 Period of Precharge	37		37	
29b	tSARQCK2	$\overline{AREQ}$ Negated Setup to CLK High with >1 Period of Precharge Programmed	15		15	
30	tPAREQDH	$\overline{AREQ}$ Negated to $\overline{DTACK}$ Negated		27		27
31	tPCKCAS	CLK High to $\overline{CAS}$ Asserted when Delayed by $\overline{WIN}$		25		32
32	tSCADEN	Column Address Setup to $\overline{ECAS}$ Asserted to Guarantee tASC = 0	14		16	
33	tWCINC	COLINC Pulse Width	20		20	
34a	tPCKCL0	CLK High to $\overline{CAS}$ Asserted following Precharge (tRAH = 15 ns, tASC = 0 ns)		72		79
34b	tPCKCL1	CLK High to $\overline{CAS}$ Asserted following Precharge (tRAH = 25 ns, tASC = 0 ns)		82		89
34c	tPCKCL2	CLK High to $\overline{CAS}$ Asserted following Precharge (tRAH = 25 ns, tASC = 0 ns)		82		89
34d	tPCKCL3	CLK High to $\overline{CAS}$ Asserted following Precharge (tRAH = 25 ns, tASC = 10 ns)		92		99
35	tCAH	Column Address Hold Time (Interleave Mode Only)	32		32	
36	tPCQR	$\overline{CAS}$ Asserted to Row Address Valid (Interleave Mode Only)		90		90
37	tPCASDTH	$\overline{CAS}$ Asserted to $\overline{DT}/\overline{OE}$ Asserted for a VRAM Read Access		14		24
38	tPCASDTL	$\overline{CAS}$ Negated to $\overline{DT}/\overline{OE}$ Negated for a VRAM Read Access		14		24

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 VRAMs per bank, including trace capacitance (see Note 2).

Two different loads are specified:
C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9 and 10; or
C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9 and 10.

Number	Symbol	Difference Parameter Description	8520A/21A/22A-25			
			C_L		C_H	
			Min	Max	Min	Max
50	tD1	($\overline{AREQ}$ or $\overline{AREQB}$ Negated to $\overline{RAS}$ Negated) Minus (CLK High to $\overline{RAS}$ Asserted)		14		14
51	tD2	(CLK High to Refresh $\overline{RAS}$ Negated) Minus (CLK High to $\overline{RAS}$ Asserted)		11		11
52	tD3a	($\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted (Mode 1)) Minus ($\overline{AREQ}$ Negated to $\overline{RAS}$ Negated)		4		4
53	tD3b	(CLK High to $\overline{RAS}$ Asserted (Mode 0)) Minus ($\overline{AREQ}$ Negated to $\overline{RAS}$ Negated)		4		4
54	tD4	($\overline{ECAS}$ Asserted to $\overline{CAS}$ Asserted) Minus ($\overline{ECAS}$ Negated to $\overline{CAS}$ Negated)	−7	7	−7	7
55	tD5	(CLK to Refresh $\overline{RAS}$ Asserted) Minus (CLK to Refresh $\overline{RAS}$ Negated)		6		6
56	tD6	($\overline{AREQ}$ Negated to $\overline{RAS}$ Negated) Minus ($\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted ((Mode 1))		10		10

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 VRAMs per bank, including trace capacitance (see Note 2).

Two different loads are specified:
C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9 and 10; or
C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9 and 10.

Number	Symbol	Common Dual Access Parameter Description	8520A/21A/22A-25			
			C_L		C_H	
			Min	Max	Min	Max
100	tHCKARQB	$\overline{AREQB}$ Negated Held from CLK High	3		3	
101	tSARQBCK	$\overline{AREQB}$ Asserted Setup to CLK High	7		7	
102	tPAQBRASL	$\overline{AREQB}$ Asserted to $\overline{RAS}$ Asserted		37		41
103	tPAQBRASH	$\overline{AREQB}$ Negated to $\overline{RAS}$ Negated		32		36
105	tPCKRASG	CLK High to $\overline{RAS}$ Asserted for Pending Port B Access		44		48
106	tPAQBATKBL	$\overline{AREQB}$ Asserted to $\overline{ATACKB}$ Asserted		45		45
107	tPCKATKB	CLK High to $\overline{ATACKB}$ Asserted for Pending Access		51		51
108	tPCKGH	CLK High to GRANTB Asserted		32		32
109	tPCKGL	CLK High to GRANTB Negated		29		29
110	tSADDCKG	Row Address Setup to CLK High That Asserts $\overline{RAS}$ following a GRANTB Change to Ensure tASR = 0 ns for Port B	11		16	
111	tSLOCKCK	$\overline{LOCK}$ Asserted Setup to CLK Low to Lock Current Port	5		5	
112	tPAQATKBH	$\overline{AREQ}$ Negated to $\overline{ATACKB}$ Negated		21		21
113	tPAQBCASH	$\overline{AREQB}$ Negated to $\overline{CAS}$ Negated		47		54
114	tSADAQB	Address Valid Setup to $\overline{AREQB}$ Asserted	7		12	
116	tHCKARQG	$\overline{AREQ}$ Negated Held from CLK High	5		5	
117	tWAQB	$\overline{AREQB}$ High Pulse Width to Guarantee tASR = 0 ns	26		31	
118a	tPAQBCAS0	$\overline{AREQB}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 0 ns)		87		94
118b	tPAQBCAS1	$\overline{AREQB}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 10 ns)		97		104
118c	tPAQBCAS2	$\overline{AREQB}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 0 ns)		97		104
118d	tPAQBCAS3	$\overline{AREQB}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 10 ns)		107		114
120a	tPCKCASG0	CLK High to $\overline{CAS}$ Asserted for Pending Port B Access (tRAH = 15 ns, tASC = 0 ns)		96		103
120b	tPCKCASG1	CLK High to $\overline{CAS}$ Asserted for Pending Port B Access (tRAH = 15 ns, tASC = 0 ns)		106		113
120c	tPCKCASG2	CLK High to $\overline{CAS}$ Asserted for Pending Port B Access (tRAH = 25 ns, tASC = 0 ns)		106		113
120d	tPCKCASG3	CLK High to $\overline{CAS}$ Asserted for Pending Port B Access (tRAH = 25 ns, tASC = 10 ns)		116		123
121	tSBADDCKG	Bank Address Valid Setup to CLK High That Starts $\overline{RAS}$ for Pending Port B Access	10		10	

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 VRAMs per bank, including trace capacitance (see Note 2).

Two different loads are specified:
C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9 and 10; or
C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9 and 10.

Number	Symbol	Refresh Parameter Description	8520A/21A/22A-25			
			C_L		C_H	
			Min	Max	Min	Max
200	tSRFCK	$\overline{RFSH}$ Asserted Setup to CLK High	22		22	
201	tSDRFCK	$\overline{DISRFSH}$ Asserted Setup to CLK High	22		22	
202	tSXRFCK	EXTENDRF Setup to CLK High	12		12	
204	tPCKRFL	CLK High to $\overline{RFIP}$ Asserted		31		31
205	tPARQRF	$\overline{AREQ}$ Negated to $\overline{RFIP}$ Asserted		50		50
206	tPCKRFH	CLK High to $\overline{RFIP}$ Negated		51		51
207	tPCKRFRASH	CLK High to Refresh $\overline{RAS}$ Negated		29		33
208	tPCKRFRASL	CLK High to Refresh $\overline{RAS}$ Asserted		23		27
209a	tPCKCL0	CLK High to $\overline{CAS}$ Asserted during Error Scrubbing (tRAH = 15 ns, tASC = 0 ns)		73		80
209b	tPCKCL1	CLK High to $\overline{CAS}$ Asserted during Error Scrubbing (tRAH = 15 ns, tASC = 10 ns)		83		90
209c	tPCKCL2	CLK High to $\overline{CAS}$ Asserted during Error Scrubbing (tRAH = 25 ns, tASC = 0 ns)		83		90
209d	tPCKCL3	CLK High to $\overline{CAS}$ Asserted during Error Scrubbing (tRAH = 25 ns, tASC = 10 ns)		93		100
210	tWRFSH	$\overline{RFSH}$ Pulse Width	15		15	
211	tPCKRQL	CLK High to $\overline{RFRQ}$ Asserted		40		40
212	tPCKRQH	CLK High to $\overline{RFRQ}$ Negated		40		40

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)

Unless otherwise stated $V_{CC} = 5.0V \pm 10\%$, $0°C < T_A < 70°C$, the output load capacitance is typical for 4 banks of 18 VRAMs per bank, including trace capacitance (see Note 2).

Two different loads are specified:
$C_L = 50$ pF loads on all outputs except
$C_L = 150$ pF loads on Q0–8, 9 and 10; or
$C_H = 50$ pF loads on all outputs except
$C_H = 125$ pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
$C_H = 380$ pF loads on Q0–8, 9 and 10.

Number	Symbol	Mode 0 Access Parameter Description	8520A/21A/22A-25			
			C_L		C_H	
			Min	Max	Min	Max
300	tSCSCK	$\overline{CS}$ Asserted to CLK High	13		13	
301a	tSALECKNL	ALE Asserted Setup to CLK High Not Using On-Chip Latches or if Using On-Chip Latches and B0, B1, Are Constant, Only 1 Bank	15		15	
301b	tSALECKL	ALE Asserted Setup to CLK High, if Using On-Chip Latches if B0, B1 Can Change, More Than One Bank	29		29	
302	tWALE	ALE Pulse Width	13		13	
303	tSBADDCK	Bank Address Valid Setup to CLK High	18		18	
304	tSADDCK	Row, Column Valid Setup to CLK High to Guarantee tASR = 0 ns	11		16	
305	tHASRCB	Row, Column, Bank Address Held from ALE Negated (Using On-Chip Latches)	8		8	
306	tSRCBAS	Row, Column, Bank Address Setup to ALE Negated (Using On-Chip Latches)	2		2	
307	tPCKRL	CLK High to $\overline{RAS}$ Asserted		22		26
308a	tPCKCL0	CLK High to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 0 ns)		72		79
308b	tPCKCL1	CLK High to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 10 ns)		82		89
308c	tPCKCL2	CLK High to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 0 ns)		82		89
308d	tPCKCL3	CLK High to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 10 ns)		92		99
309	tHCKALE	ALE Negated Hold from CLK High	0		0	
310	tSWINCK	$\overline{WIN}$ Asserted Setup to CLK High to Guarantee $\overline{CAS}$ is Delayed	−16		−16	
311	tPCSWL	$\overline{CS}$ Asserted to $\overline{WAIT}$ Asserted		22		22
312	tPCSWH	$\overline{CS}$ Negated to $\overline{WAIT}$ Negated		25		25
313	tPCLKDL1	CLK High to $\overline{DTACK}$ Asserted (Programmed as $\overline{DTACK0}$)		32		32
314	tPALEWL	ALE Asserted to $\overline{WAIT}$ Asserted ($\overline{CS}$ is Already Asserted)		29		29
315		$\overline{AREQ}$ Negated to CLK High That Starts Access $\overline{RAS}$ to Guarantee tASR = 0 ns (Non-Interleaved Mode Only)	34		39	

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 VRAMs per bank, including trace capacitance (see Note 2).

Two different loads are specified:
C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9 and 10; or
C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9 and 10.

Number	Symbol	Mode 1 Access Parameter Description	8520A/21A/22A-25			
			C_L		C_H	
			Min	Max	Min	Max
400a	tSADSCK1	$\overline{ADS}$ Asserted Setup to CLK High	13		13	
400b	tSADSCKW	$\overline{ADS}$ Asserted Setup to CLK (to Guarantee Correct $\overline{WAIT}$ or $\overline{DTACK}$ Output; Doesn't Apply for $\overline{DTACK}$0)	25		25	
401	tSCSADS	$\overline{CS}$ Setup to $\overline{ADS}$ Asserted	5		5	
402	tPADSRL	$\overline{ADS}$ Asserted to $\overline{RAS}$ Asserted		25		29
403a	tPADSCL0	$\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 0 ns)		75		82
403b	tPADSCL1	$\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 15 ns, tASC = 10 ns)		85		92
403c	tPADSCL2	$\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 10 ns)		85		92
403d	tPADSCL3	$\overline{ADS}$ Asserted to $\overline{CAS}$ Asserted (tRAH = 25 ns, tASC = 10 ns)		95		102
404	tSADDADS	Row Address Valid Setup to $\overline{ADS}$ Asserted to Guarantee tASR = 0 ns	9		14	
405	tHCKADS	$\overline{ADS}$ Negated Held from CLK High	0		0	
406	tSWADS	$\overline{WAITIN}$ Asserted Setup to $\overline{ADS}$ Asserted to Guarantee $\overline{DTACK}$0 Is Delayed	0		0	
407	tSBADAS	Bank Address Setup to $\overline{ADS}$ Asserted	11		11	
408	tHASRCB	Row, Column, Bank Address Held from $\overline{ADS}$ Asserted (Using On-Chip Latches)	10		10	
409	tSRCBAS	Row, Column, Bank Address Setup to $\overline{ADS}$ Asserted (Using On-Chip Latches)	2		2	
410	tWADSH	$\overline{ADS}$ Negated Pulse Width	12		17	
411	tPADSD	$\overline{ADS}$ Asserted to $\overline{DTACK}$ Asserted (Programmed as $\overline{DTACK}$0)		35		35
412	tSWINADS	$\overline{WIN}$ Asserted Setup to $\overline{ADS}$ Asserted (to Guarantee $\overline{CAS}$ Delayed during Writes Accesses)	−10		−10	
413	tPADSWL0	$\overline{ADS}$ Asserted to $\overline{WAIT}$ Asserted (Programmed as $\overline{WAIT}$0, Delayed Access)		29		29
414	tPADSWL1	$\overline{ADS}$ Asserted to $\overline{WAIT}$ Asserted (Programmed $\overline{WAIT}$ 1/2 or 1)		29		29
415	tPCLKDL1	CLK High to $\overline{DTACK}$ Asserted (Programmed as $\overline{DTACK}$0, Delayed Access)		32		32
416		$\overline{AREQ}$ Negated to $\overline{ADS}$ Asserted to Guarantee tASR = 0 ns (Non Interleaved Mode Only)	31		36	

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)

Unless otherwise stated V_{CC} = 5.0V ±10%, 0°C < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 VRAMs per bank, including trace capacitance (see Note 2).

Two different loads are specified:
C_L = 50 pF loads on all outputs except
C_L = 150 pF loads on Q0–8, 9 and 10; or
C_H = 50 pF loads on all outputs except
C_H = 125 pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
C_H = 380 pF loads on Q0–8, 9 and 10.

Number	Symbol	Mode 1 Dual Access Parameter Description	8520A/21A/22A-25			
			C_L		C_H	
			Min	Max	Min	Max
450	tSADDCKG	Row Address Setup to CLK High That Asserts $\overline{RAS}$ following a GRANTB Port Change to Ensure tASR = 0 ns	11		16	
451	tPCKRASG	CLK High to $\overline{RAS}$ Asserted for Pending Access		38		42
452	tPCLKDL2	CLK to $\overline{DTACK}$ Asserted for Delayed Accesses (Programmed as $\overline{DTACK}$0)		43		43
453a	tPCKCASG0	CLK High to $\overline{CAS}$ Asserted for Pending Access (tRAH = 15 ns, tASC = 0 ns)		86		93
453b	tPCKCASG1	CLK High to $\overline{CAS}$ Asserted for Pending Access (tRAH = 15 ns, tASC = 10 ns)		96		103
453c	tPCKCASG2	CLK High to $\overline{CAS}$ Asserted for Pending Access (tRAH = 25 ns, tASC = 0 ns)		96		103
453d	tPCKCASG3	CLK High to $\overline{CAS}$ Asserted for Pending Access (tRAH = 25 ns, tASC = 10 ns)		106		113
454	tSBADDCKG	Bank Address Valid Setp to CLK High That Asserts $\overline{RAS}$ for Pending Access	4		4	
455	tSADSCK0	$\overline{ADS}$ Asserted Setup to CLK High	11		11	

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)

Unless otherwise stated $V_{CC} = 5.0V \pm 10\%$, $0°C < T_A < 70°C$, the output load capacitance is typical for 4 banks of 18 VRAMs per bank, including trace capacitance (see Note 2).

Two different loads are specified:
$C_L = 50$ pF loads on all outputs except
$C_L = 150$ pF loads on Q0–8, 9 and 10; or
$C_H = 50$ pF loads on all outputs except
$C_H = 125$ pF loads on $\overline{RAS}$0–3 and $\overline{CAS}$0–3 and
$C_H = 380$ pF loads on Q0–8, 9 and 10.

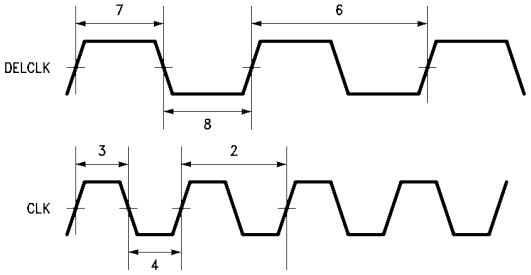
Number	Symbol	Programing Parameter Description	8520A/21A/22A-25			
			C_L		C_H	
			Min	Max	Min	Max
500	tHMLADD	Mode Address Held from $\overline{ML}$ Negated	7		7	
501	tSADDML	Mode Address Setup to $\overline{ML}$ Negated	6		6	
502	tWML	$\overline{ML}$ Pulse Width	15		15	
503	tSADAQML	Mode Address Setup to $\overline{AREQ}$ Asserted	0		0	
504	tHADAQML	Mode Address Held from $\overline{AREQ}$ Asserted	38		38	
505	tSCSARQ	$\overline{CS}$ Asserted Setup to $\overline{AREQ}$ Asserted	6		6	
506	tSMLARQ	$\overline{ML}$ Asserted Setup to $\overline{AREQ}$ Asserted	10		10	
600	tSCKVSRL	$\overline{VSRL}$ Low Setup to CLK Rising Edge to guarantee counting $\overline{VSRL}$ as being Low (used to determine when to end Graphics Shift load access)	7		7	
601	tHVSRLCK	$\overline{VSRL}$ Low from CLK High (to guarantee $\overline{VSRL}$ is not counted as being Low until the next rising clock edge)	3		3	
602	tSCKAVSRL	$\overline{AVSRLRQ}$ Low before CLK Rising Edge to guarantee locking the VRAM to only Port A accesses	12		12	
603	tPVSRLDTL	$\overline{VSRL}$ Low to $\overline{DT}/\overline{OE}$ Low during Graphics Shift Register Load access		23		33
604	tPVSRLDTH	$\overline{VSRL}$ Negated to $\overline{DT}/\overline{OE}$ Negated		22		32
605	tPCKDTL	CLK to $\overline{DT}/\overline{OE}$ Negated		27		37

Note 1: ''Absolute Maximum Ratings'' are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of ''Electrical Characteristics'' provides conditions for actual device operation.

Note 2: Input pulse 0V to 3V; tR = tF = 2.5 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.4V for High and 0.8V for Low.

Note 3: AC Production testing is done at 50 pF.

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)



TL/F/9338–B5

FIGURE 60. Clock, DELCLK Timing

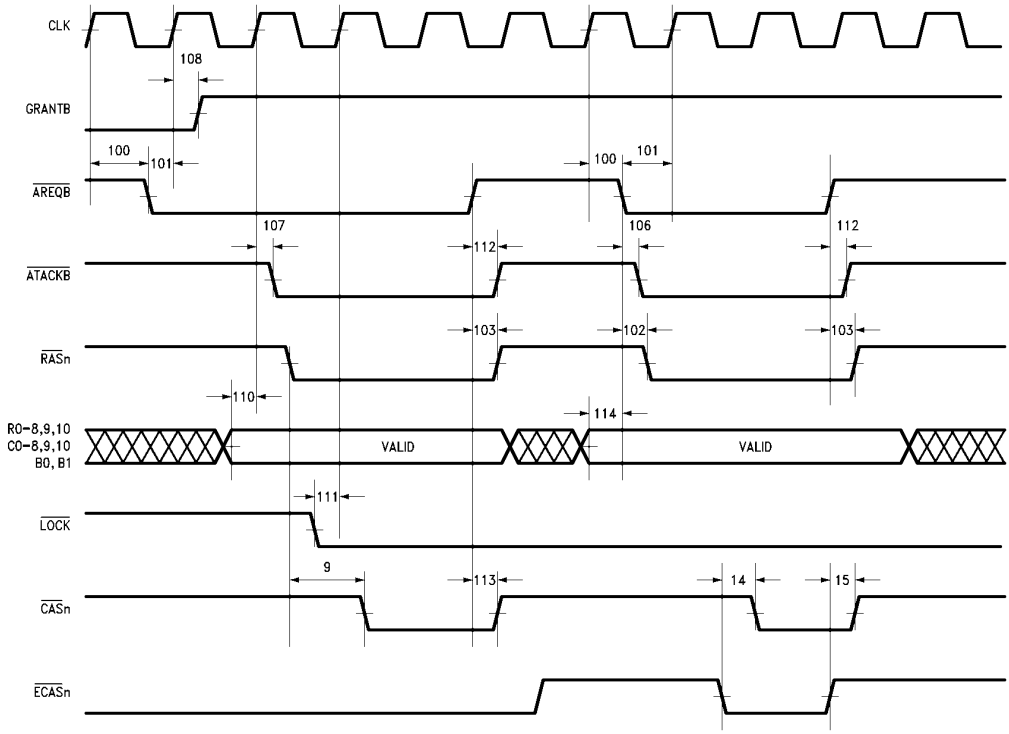


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FIGURE 61. 100: Dual Access Port B

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)

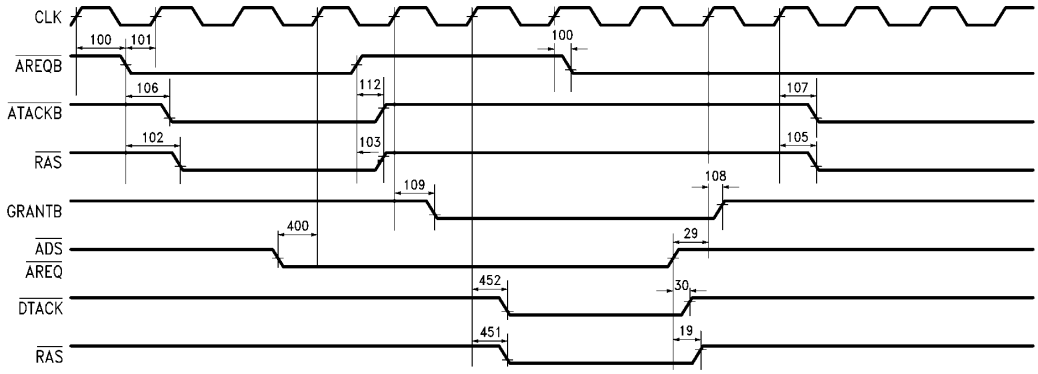

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FIGURE 62. 100: Port A and Port B Dual Access

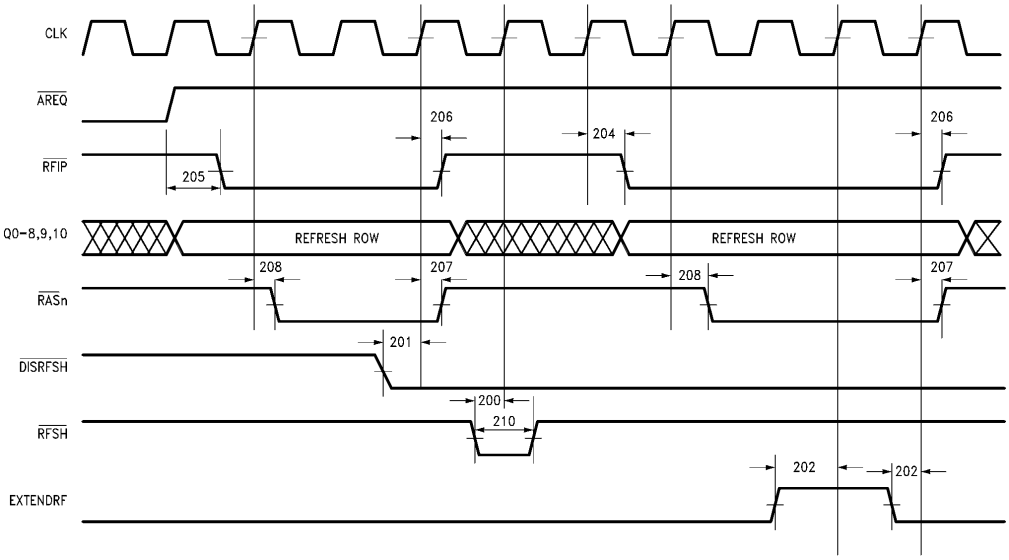

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FIGURE 63. 200: Refresh Timing

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)

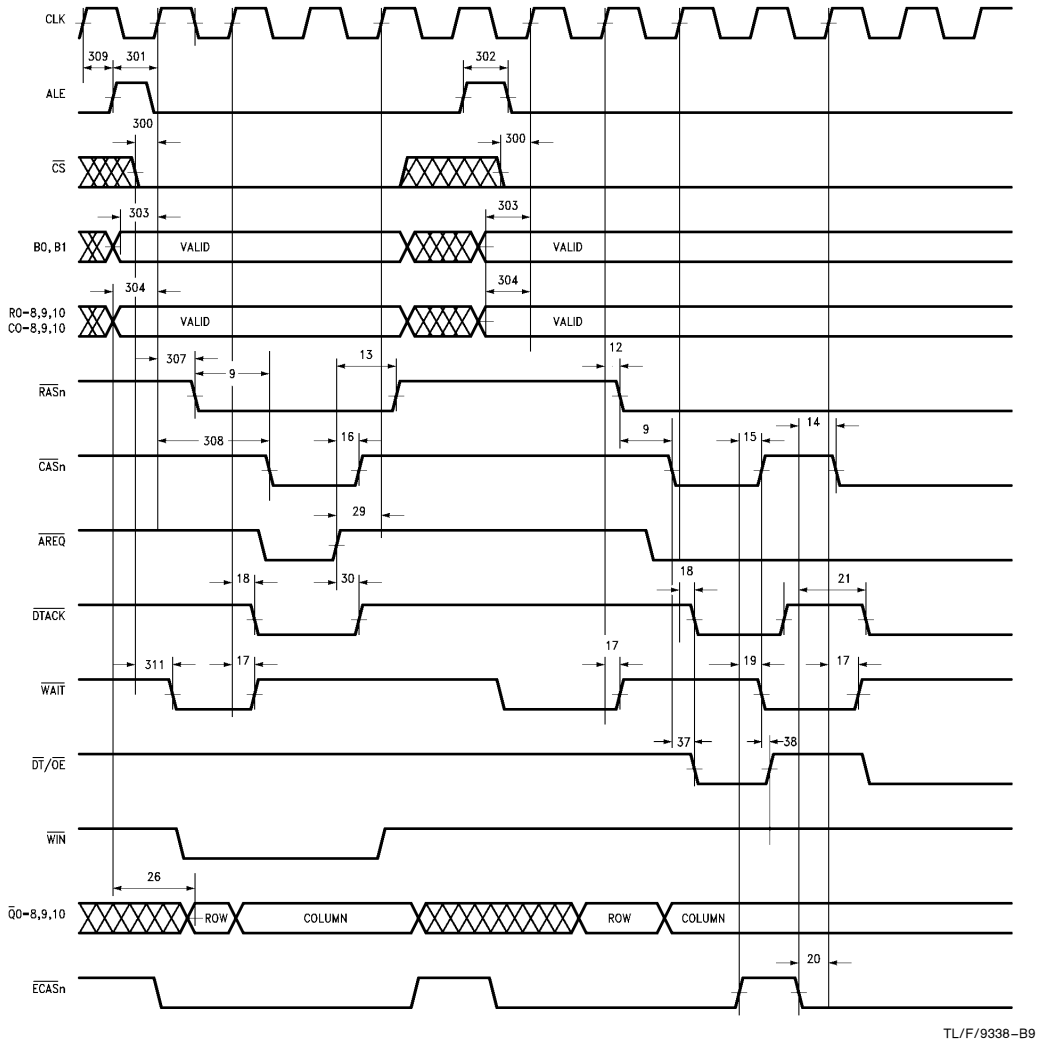
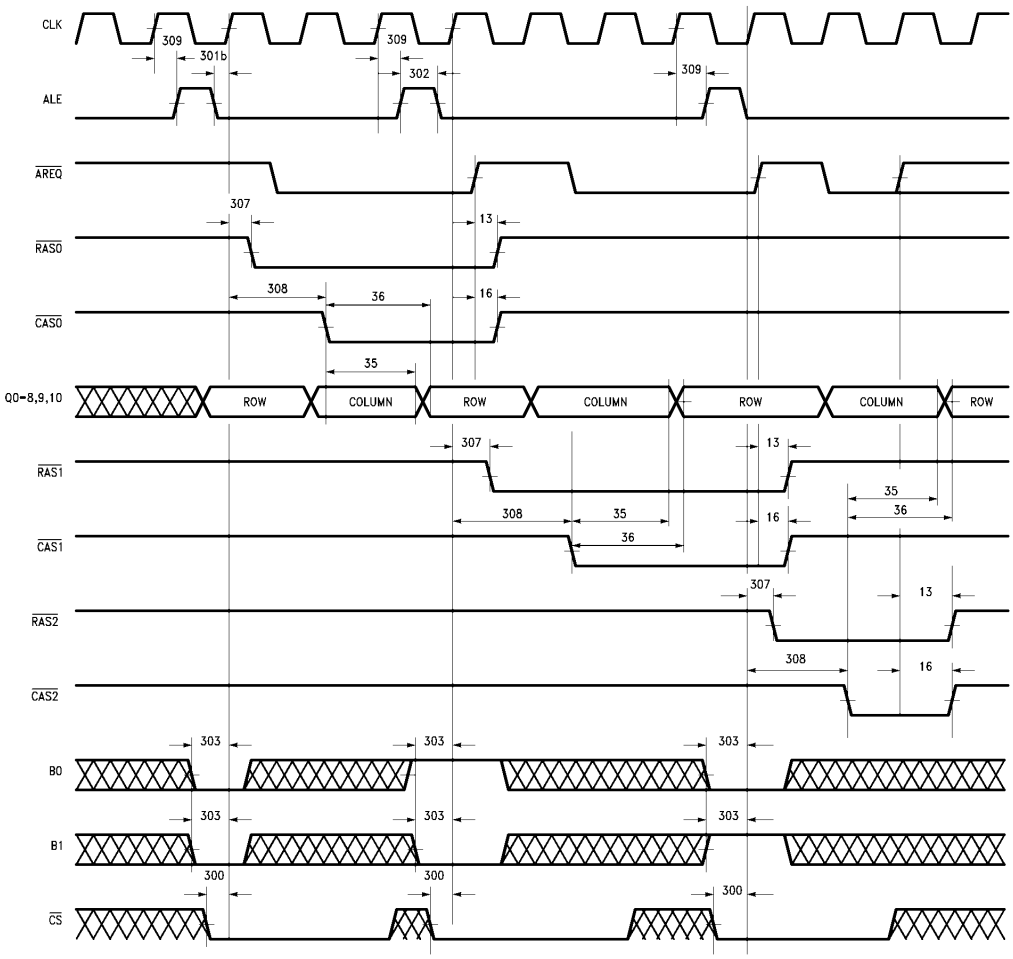


FIGURE 64. 300: Mode 0 Timing

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)



TL/F/9338–C0

(Programmed as C4 = 1, C5 = 1, C6 = 1)

FIGURE 65. 300: Mode 0 Interleaving

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)

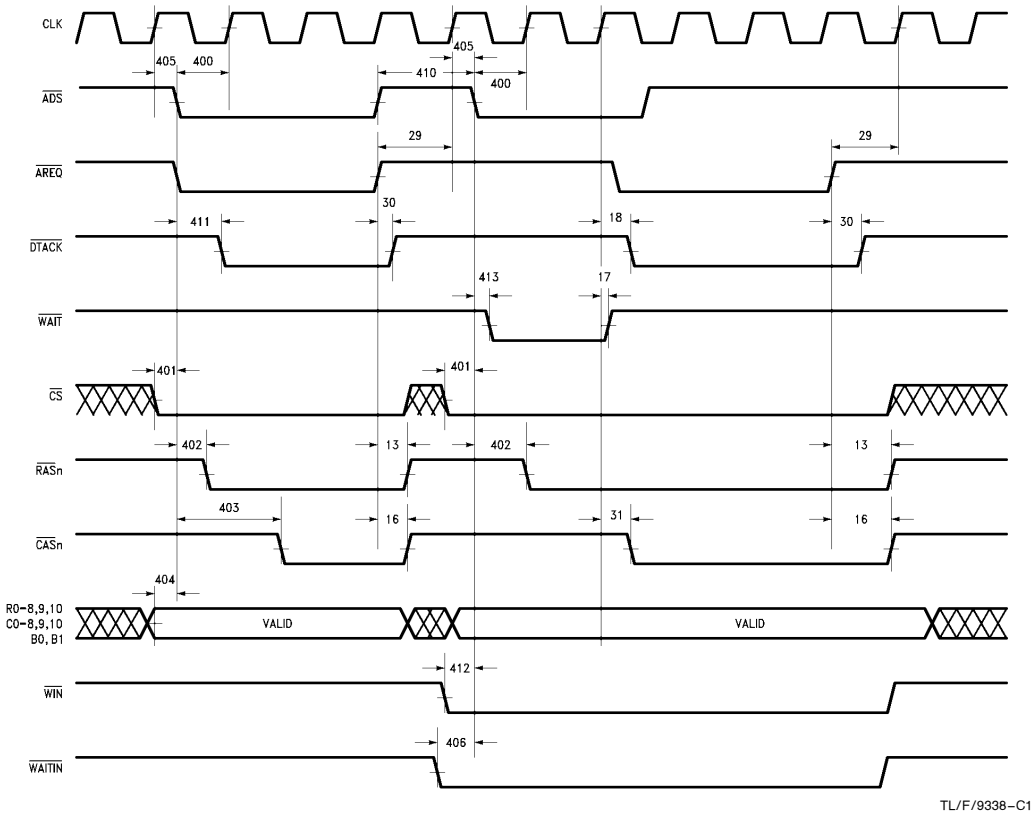


FIGURE 66. 400: Mode 1 Timing

15.0 AC Timing Parameters: DP8520A/DP8521A/DP8522A (Continued)

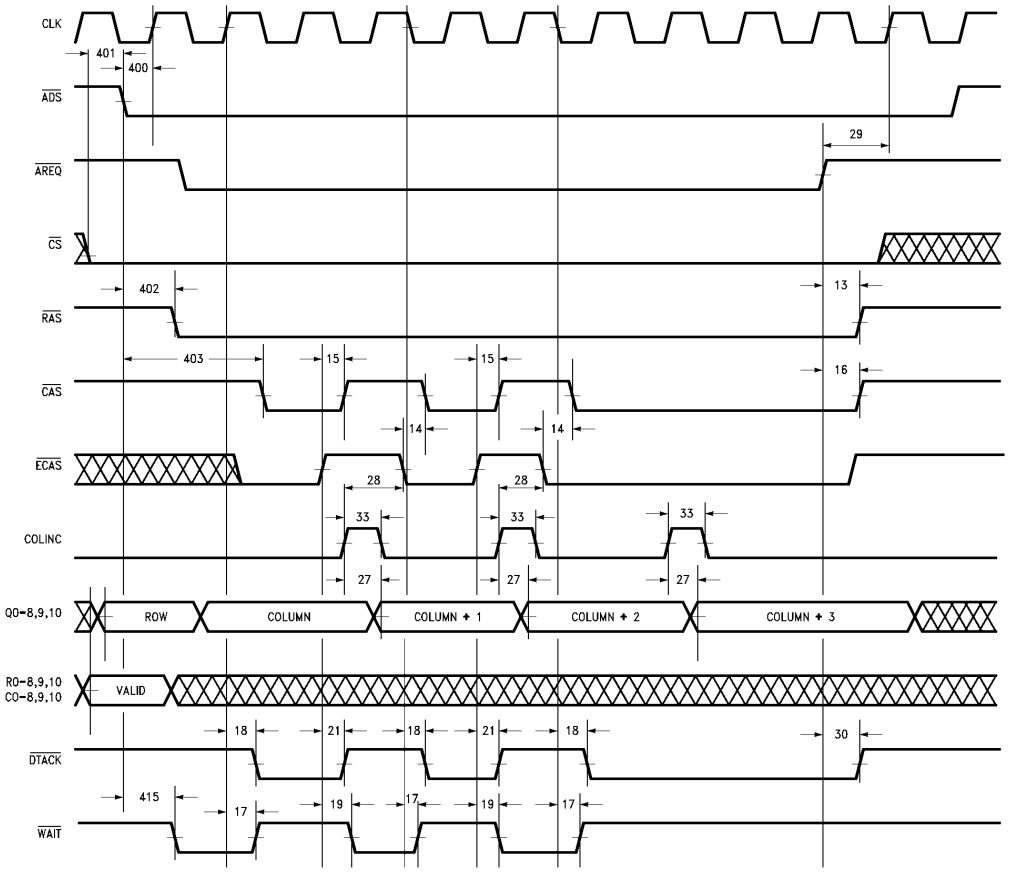


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FIGURE 67. 400: COLINC Page/Static Column Access Timing

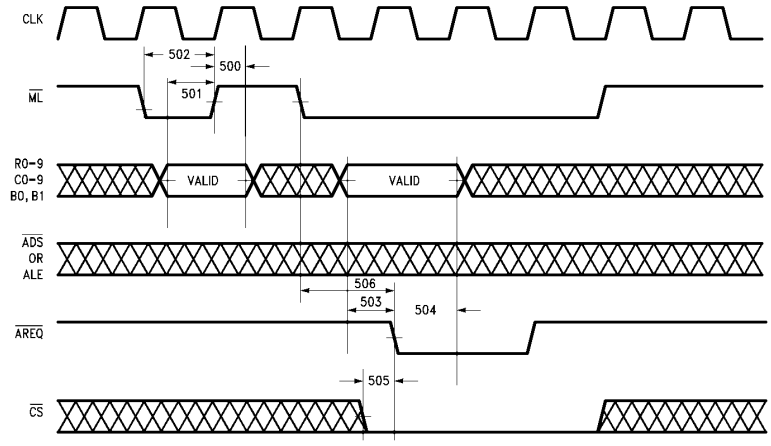

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FIGURE 68. 500: Programming

15.0 AC Timing Parameters: DP8520A/21A/22A (Continued)

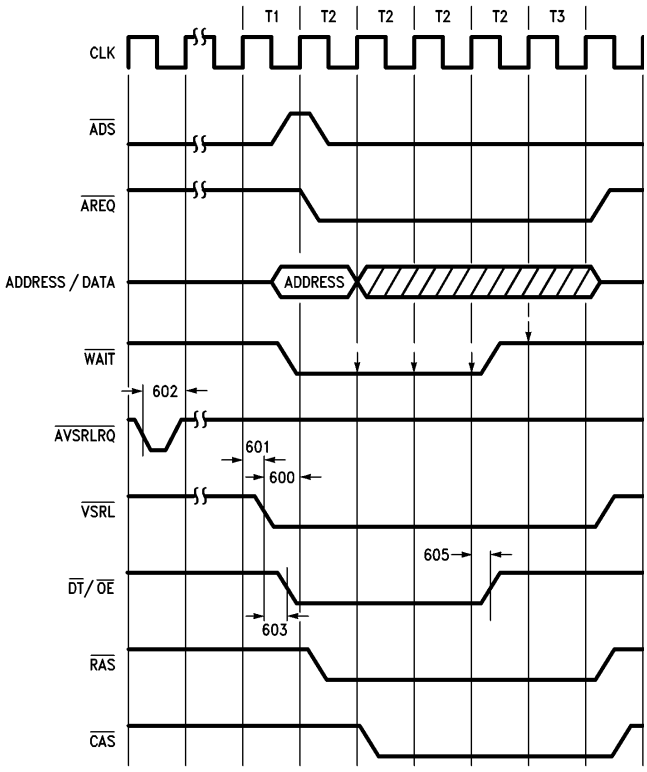

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FIGURE 69. Graphics Timing Diagram

16.0 Functional Differences between the DP8520A/21A/22A and the DP8520/21/22

1. Extending the Column Address Strobe ($\overline{CAS}$)

$\overline{CAS}$ can be extended indefinitely after $\overline{AREQ}$ transitions high in non-interleaved mode only, providing that the user program the DP8520A/21A/22A with the $\overline{ECAS}$0 (negated) during programming. To extend $\overline{CAS}$, the user continues to assert any or multiple $\overline{ECAS}$s after negating $\overline{AREQ}$. Extending $\overline{CAS}$ with $\overline{RAS}$ negated can be used to gain $\overline{RAS}$ precharge time. By negating $\overline{AREQ}$, $\overline{RAS}$ will be negated. The user can then continue to assert a one or both of the $\overline{ECAS}$s, which will keep $\overline{CAS}$ asserted. By keeping $\overline{CAS}$ asserted with $\overline{RAS}$ negated, the VRAM will keep the data valid until $\overline{CAS}$ is negated. Even though $\overline{CAS}$ will be extended, $\overline{DTACK}$ output will always end from $\overline{AREQ}$ negated.

2. Extending $\overline{DT}/\overline{OE}$ Functionality

The $\overline{DT}/\overline{OE}$ output will follow the $\overline{CAS}$ output during a VRAM read access, and will remain negated during a VRAM write access. For the DP8520/21/22, the $\overline{DT}/\overline{OE}$ output remained negated for all VRAM access cycles. This will allow the VRAM to drive the data bus. There are 2 options for the function of the $\overline{DT}/\overline{OE}$ output during a video shift register load operation. With $\overline{ECAS}$0 negated during programming, the $\overline{DT}/\overline{OE}$ output will follow the $\overline{VSRL}$ input during video shift register load operations. With the $\overline{ECAS}$0 asserted during programming, $\overline{VSRL}$ will assert $\overline{DT}/\overline{OE}$. $\overline{VSRL}$ negated before four rising clock edges will cause $\overline{DT}/\overline{OE}$ to be negated. $\overline{VSRL}$ asserted more than four rising clock edges will cause $\overline{DT}/\overline{OE}$ to be negated from the fourth rising clock edge.

3. Dual Accessing

$\overline{RAS}$ will be asserted either one or two clock periods after GRANTB has been asserted. The amount of $\overline{RAS}$ low and high time, programmed by bits R0 and R1, determines the number of clock periods after GRANTB changes before $\overline{RAS}$ will start. This is shown in the table below.

R0, R1	$\overline{RAS}$ Precharge Time	$\overline{RAS}$ Asserted During Refresh	$\overline{RAS}$ Asserted from GRANTB Change
0, 0	1T	2T	1 Rising Clock Edge
0, 1	2T	2T	1 Rising Clock Edge
1, 0	2T	3T	2 Rising Clock Edges
1, 1	3T	4T	2 Rising Clock Edges

4. Refresh Clock Counter

The refresh clock counter will count and assert $\overline{RFRQ}$ externally when it is time to do a refresh. This will occur even when internal refreshes are disabled. This allows the user to run the chip in a request/acknowledge mode for refreshing. $\overline{ECAS}$0 is used to program the $\overline{RFIP}$ output to act as either refresh request ($\overline{RFRQ}$) or $\overline{RFIP}$. $\overline{ECAS}$0 asserted during programming causes the $\overline{RFIP}$ output to function as $\overline{RFIP}$. $\overline{ECAS}$0 negated during programming causes the $\overline{RFIP}$ output to function as $\overline{RFRQ}$.

5. Clearing the Refresh Clock

The refresh clock counter is cleared by negating $\overline{DISRFSH}$ and asserting $\overline{RFSH}$ for at least 500 ns.

17.0 DP8520A/21A/22A User Hints

1. All inputs to the DP8520A/21A/22A should be tied high, low or the output of some other device.
   Note: One signal is active high. COLINC (EXTNDRF) should be tied low to disable.
2. Each ground on the DP8520A/21A/22A must be decoupled to the closest on-chip supply (V_{CC}) with 0.1 μF ceramic capacitor. This is necessary because these grounds are kept separate inside the DP8520A/21A/22A. The decoupling capacitors should be placed as close as possible with short leads to the ground and supply pins of the DP8520A/21A/22A.
3. The output called "CAP" should have a 0.1 μF capacitor to ground.
4. The DP8520A/21A/22A has 20Ω series damping resistors built into the output drivers of $\overline{RAS}$, $\overline{CAS}$, address and $\overline{DT}/\overline{OE}$. Space should be provided for external damping resistors on the printed circuit board (or wire-wrap board) because they may be needed. The value of these damping resistors (if needed) will vary depending upon the output, the capacitance of the load, and the characteristics of the trace as well as the routing of the trace. The value of the damping resistor also may vary between the wire-wrap board and the printed circuit board. To determine the value of the series damping resistor it is recommended to use an oscilloscope and look at the furthest VRAM from the DP8520A/21A/22A. The undershoot of $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and the addresses should be kept to less than 0.5V below ground by varying the value of the damping resistor. The damping resistors should be placed as close as possible with short leads to the driver outputs of the DP8520A/21A/22A.
5. The circuit board must have a good V_{CC} and ground plane connection. If the board is wire-wrapped, the V_{CC} and ground pins of the DP8520A/21A/22A, the VRAM associated logic and buffer circuitry must be soldered to the V_{CC} and ground planes.
6. The traces from the DP8520A/21A/22A to the VRAM should be as short as possible.
7. $\overline{ECAS}$0 should be held low during programming if the user wishes that the DP8520A/21A/22A be compatible with a DP8520/21/22 design.

18.0 Description of a DP8522A/ DP8500 System Interface

Several simple block and timing diagrams are inserted to help the user design a system interface between the DP8520A/21A/22A VRAM controller and the Raster Graphics Processor DP8500 (as shown in *Figure 70*). For accessing the VRAM, the DP8520A/21A/22A uses the RGP's PHI 2 clock as an input clock and it runs in Mode 1 (asynchronous mode). This allows the user to guarantee row, column and bank address set up times to a rising clock edge (as shown in timing calculations provided). This system design uses a PAL® to interface the access request logic and the wait logic between the DP8522A and the RGP. External logic is also needed for plane control.

18.0 Description of a DP8522A/DP8500 System Interface (Continued)

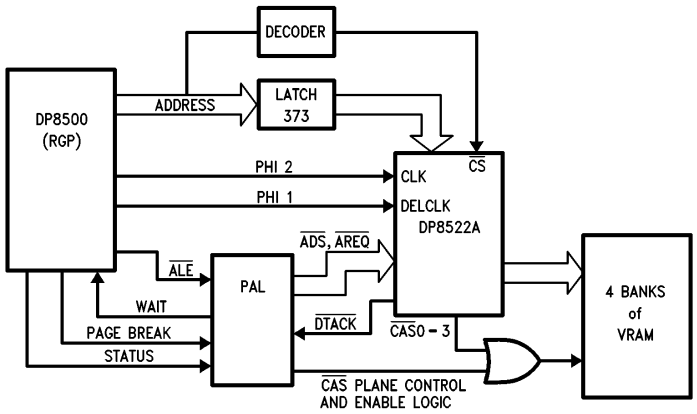

FIGURE 70. DP8422A/DP8500 (RGP) Interface Block Diagram

The main idea of the block diagram in *Figure 73* is to cause the video DRAM shift register load operation to happen correctly. Once the DP8500 (RGP) issues the Display Refresh REQuest signal ($\overline{DRREQ}$) the system knows that the video shift register load operation should occur at a certain defined time later. In the block diagram this time is controlled by the counter device. This counter determines when $\overline{VSRL}$ transitions high, thereby causing the video shift register load operation.

In the upper part of the block diagram is the "$\overline{REFRESH}$" output that is used as the "$\overline{VSRL}$" input of the DP8522A and is also used to create "$\overline{REFRESH\ NOT\ DONE}$". To creat the "$\overline{REFRESH}$" output a NAND latch is used. This latch is set when a screen refresh is in progress, shown by the RGP outputs ALE, B0, and B1 all being high. If the status of the RGP is anything other than screen refresh the latch is reset. The latch is also reset during a screen refresh when the load shift register counter times out. This counter determines when the "$\overline{VSRL}$" input of the DP8522A transitions high, causing the video DRAMs to load a row of data into their shift registers.

The "$\overline{REFRESH}$" signal along with the load shift register counter output "$\overline{NOT\ DONE}$" are used to create the "$\overline{REFRESH\ NOT\ DONE}$" signal. This output is used for two purposes. One of which is to hold the "$\overline{WAIT}$" output low, thereby inserting WAIT states into the RGP video shift register load access. The other purpose is to hold "$\overline{DT/OE}$" low until "$\overline{VSRL}$" transitions high.

Important setup timing parameters which must be met for a DP8500(RGP)–DP8522A system (assuming RGP is running at 20 MHz (T_{CP} = 50 ns)).

1. **Address Setup to $\overline{ADS}$ Asserted**

   = 1 T_{CP} − #t_{ALV} + Derating the DP8500 Spec for Light Load − t_{PF373} + Min PAL Delay to Produce $\overline{ADS}$ & $\overline{AREQ}$

   = 50 ns − 38 ns + 5 ns − 8 ns + 2 ns

   = 11 ns

   (Using Light Load Timing Specs, the DP8520A/21A/22A Needs)

   9 ns Setup for Row Address to $\overline{ADS}$ Asserted

   11 ns Setup for Bank Address to $\overline{ADS}$ Asserted

2. **$\overline{ADS}$ Setup to Clock Rising Edge**

   = 1 T_{CP} − #t_{ALEV} − Max PAL Delay

   = 50 ns − 26 ns − 10 ns

   = 14 ns

   (DP8520A/21A/22A Needs 7 ns)

3. **$\overline{WAIT}$ Negated Setup to Clock**

   = 1 T_{CP} − $18 − Max PAL Delay

   = 50 ns − 28 ns − 10 ns

   = 12 ns

   (The DP8500 Needs 5 ns Setup Time)

Note 1: "$" symbol refers to a DP8520A/21A/22A timing parameter.

Note 2: "#" symbol refers to a DP8500 timing parameter.

Note 3: ALE asserted by the RGP (DP8500) should use the system PAL to assert $\overline{WAIT}$ in order to guarantee proper setup time. $\overline{DTACK}$ low should then be used to negate the $\overline{WAIT}$ signal through PAL equations.

18.0 Description of a DP8522A/DP8500 System Interface (Continued)

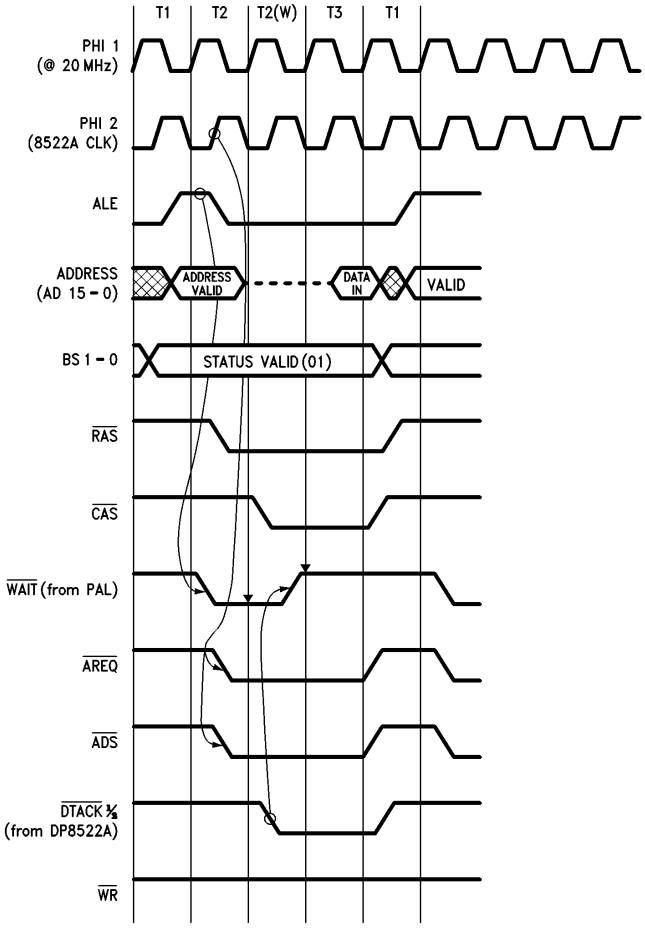

FIGURE 71. DP8522A/DP8500 (RGP)
Instruction Read Cycle Timing

18.0 Description of a DP8522A/DP8500 System Interface (Continued)

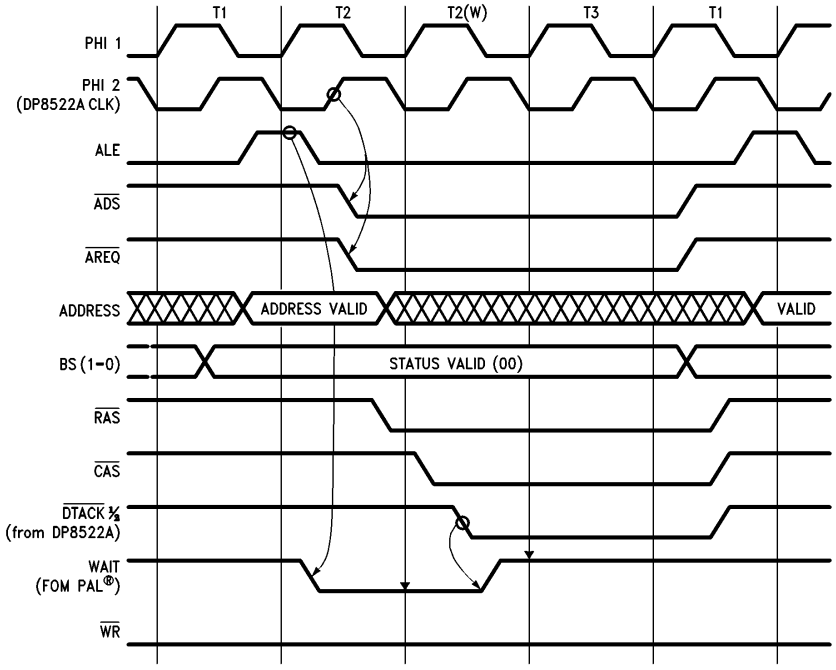

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FIGURE 72. DP8500 (20 MHz)/DP8522A Write Operand Cycle Timing

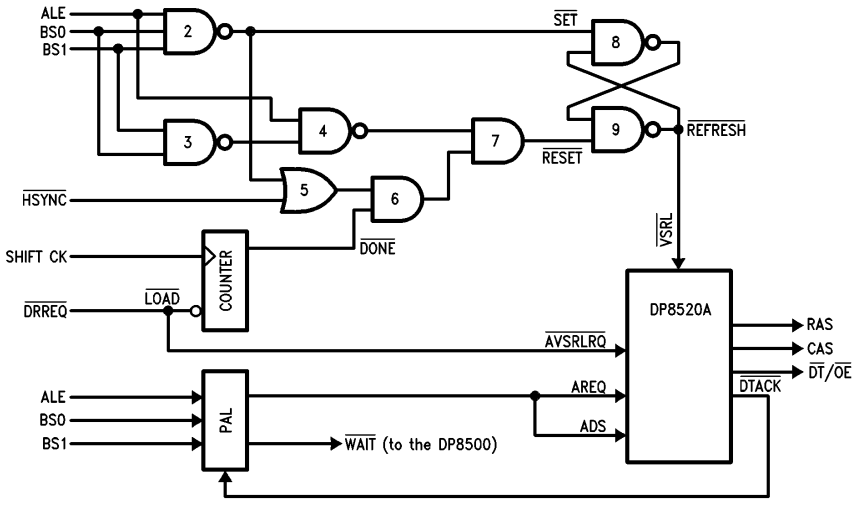

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FIGURE 73. Mid-Scan Line Load Application Example

18.0 Description of a DP8522A/DP8500 System Interface (Continued)

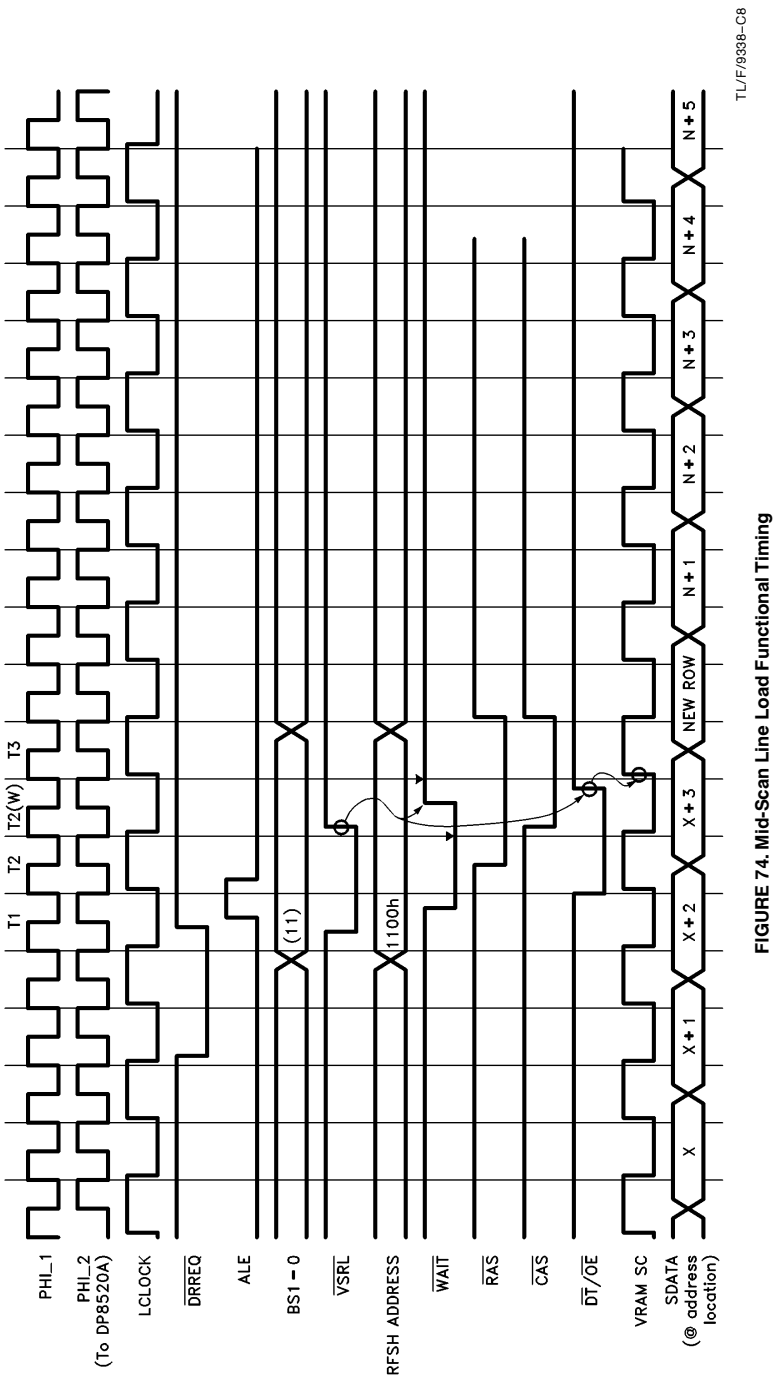
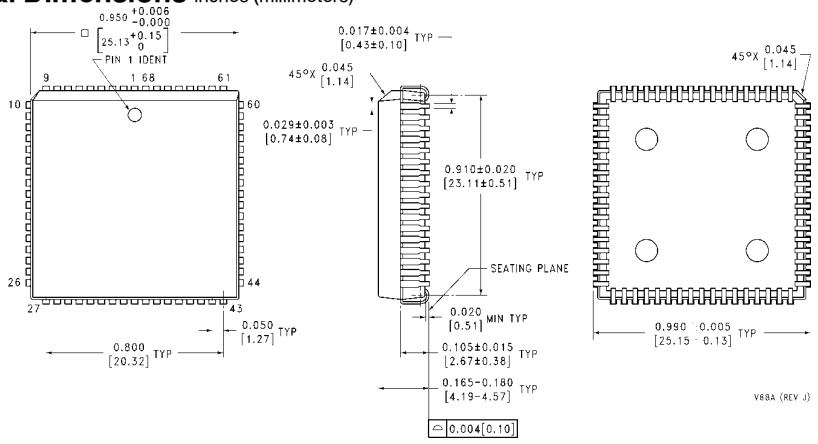
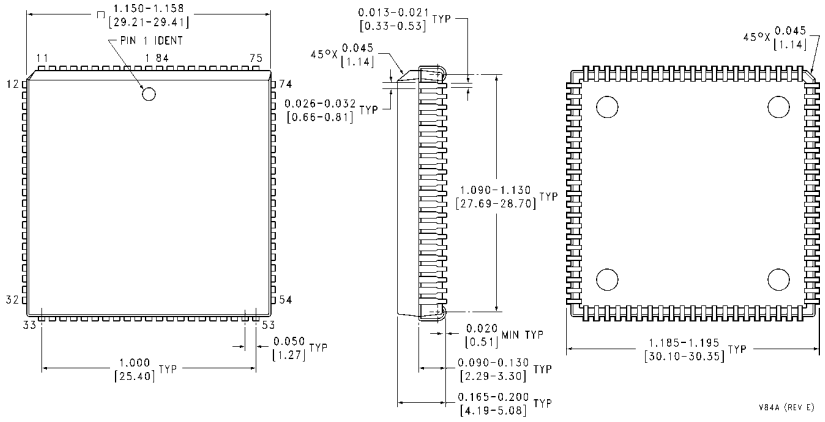


FIGURE 74. Mid-Scan Line Load Functional Timing

Physical Dimensions inches (millimeters)



Plastic Chip Carrier (V)
Order Number DP8520AV-20, DP8520AV-25, DP8521AV-20 or DP8521AV-25
NS Package Number V68A



Plastic Chip Carrier (V)
Order Number DP8522AV-20 or DP8522AV-25
NS Package Number V84A

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