10-Bit, 105 MSPS, 3 V, Dual ADC

Enhanced Product

AD9218-EP

FEATURES

Dual, 10-bit, 105 MSPS ADC
Low power: 275 mW at 105 MSPS per channel
On-chip reference and track-and-hold
300 MHz analog bandwidth for each channel
SNR = 54 dB at 51 MHz, encode = 105 MSPS
1 V p-p analog input range for each channel
3.0 V single-supply operation (2.7 V to 3.6 V)
Power-down mode for single-channel operation
Twos complement or offset binary output mode
Output data alignment mode
−75 dBc crosstalk between channels

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)
Extended industrial temperature range: −55°C to +105°C
Controlled manufacturing baseline
1 assembly/test site
1 fabrication site
Product change notification
Qualification data available on request

APPLICATIONS

Radar
Avionics
Unmanned systems
Military communications
Missiles and munitions

GENERAL DESCRIPTION

The AD9218-EP is a dual, 10-bit, monolithic sampling analog-to-digital converter (ADC) with on-chip track-and-hold circuits. The product is low cost, low power, and is small and easy to use. The AD9218-EP operates at a 105 MSPS conversion rate with dynamic performance over its full operating range. Each channel can be operated independently.

The ADC requires only a single 3.0 V (2.7 V to 3.6 V) power supply and a clock for full operation. No external reference or driver components are required for many applications. The digital outputs are transistor-to-transistor logic (TTL)/complementary metal-oxide semiconductor (CMOS) compatible, and a separate output power supply pin supports interfacing with 3.3 V or 2.5 V logic.

The clock input is TTL/CMOS compatible and the 10-bit digital outputs can be operated from a 3.0 V (2.5 V to 3.6 V) supply. User-selectable options offer a combination of power-down modes, digital data formats, and digital data timing schemes. In power-down mode, the digital outputs are driven to a high impedance state.

The AD9218-EP is fabricated on an advanced CMOS process and is available in a 48-lead, 7 mm × 7 mm, low profile quad flat package (LQFP), and is specified over the extended industrial temperature range of −55°C to +105°C.

Additional application and technical information can be found in the AD9218 data sheet.

FUNCTIONAL BLOCK DIAGRAM

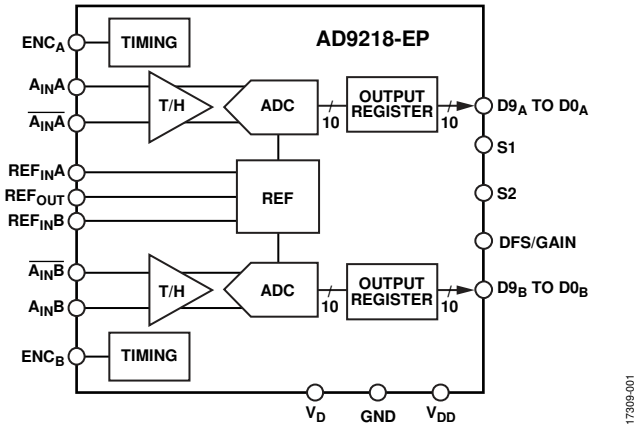

Figure 1.

Rev. 0 **Document Feedback**

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REVISION HISTORY

12/2018—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

V_{DD} = 3.0 V, V_D = 3.0 V; external reference, unless otherwise noted.

Table 1.

Parameter	Temperature	Test Level	Min	Typ	Max	Unit
RESOLUTION				10		Bits
ACCURACY						
No Missing Codes[1]	Full	VI		Guaranteed, not tested		
Offset Error[2]	25°C	I	−18	+2	+18	LSB
Gain Error[2]	25°C	I	−2	+3.5	+8	% FS
Differential Nonlinearity (DNL)	25°C	I	−1	±0.8	+1.7	LSB
	Full	VI		±0.9		LSB
Integral Nonlinearity (INL)	25°C	I	−2.7	±2	+2.7	LSB
	Full	VI		±2.3		LSB
TEMPERATURE DRIFT						
Offset Error	Full	V		4		ppm/°C
Gain Error[2]	Full	V		100		ppm/°C
Reference	Full	V		40		ppm/°C
REFERENCE						
Internal Reference Voltage (REF_{OUT})	25°C	I	1.18	1.24	1.28	V
Input Resistance ($REF_{IN}A$, $REF_{IN}B$)	Full	VI	9	11	13	kΩ
ANALOG INPUTS						
Differential Input Voltage Range (A_{INX}, $\overline{A_{INX}}$)[3]	Full	V		1		V
Common-Mode Voltage[3]	Full	V		V_D/3		V
Input Resistance	Full	VI	7	10	16	kΩ
Input Capacitance	25°C	V		3		pF
POWER SUPPLY						
V_D	Full	IV	2.7	3	3.6	V
V_{DD}	Full	IV	2.5	3	3.6	V
Supply Currents						
IV_D (V_D = 3.0 V)[4]	Full	VI		183	188	mA
IV_{DD} (V_{DD} = 3.0 V)[4]	25°C	V		17		mA
Power Dissipation DC[5]	Full	VI		550	565	mW
IV_D Power-Down Current[6]	Full	VI		22		mA
Power Supply Rejection Ratio	25°C	I		±1		mV/V

[1] No missing codes at room temperature guaranteed.
[2] Gain error and gain temperature coefficients are based on the ADC only (with a fixed 1.25 V external reference) in 1 V p-p range.
[3] (A_{INX} – $\overline{A_{INX}}$) = ±0.5 V in 1 V range (full-scale). The analog inputs self-bias to V_D/3. This common-mode voltage can be overdriven externally by a low impedance source by ±300 mV (differential drive, gain = 1).
[4] AC power dissipation measured with rated encode and a 10 MHz analog input at 0.5 dBFS, C_{LOAD} = 5 pF.
[5] DC power dissipation measured with rated encode and a dc analog input (outputs static, IV_{DD} = 0).
[6] In power-down state, IV_{DD} = ±10 µA typical.

DIGITAL SPECIFICATIONS

V_{DD} = 3.0 V, V_D = 3.0 V; external reference, unless otherwise noted.

Table 2.

Parameter	Temperature	Test Level	Min	Typ	Max	Unit
DIGITAL INPUTS						
Encode Input Common Mode	Full	V		V_D/2		V
Encode 1 Voltage	Full	VI	2			V
Encode 0 Voltage	Full	VI			0.8	V
Encode Input Resistance	Full	VI	1.75	2.0	2.4	kΩ
Logic 1 Voltage—S1, S2, DFS	Full	VI	2			V
Logic 0 Voltage—S1, S2, DFS	Full	VI			0.8	V
Logic 1 Current—S1	Full	VI	–50	±0	50	µA
Logic 0 Current—S1	Full	VI	–400	–230	–50	µA
Logic 1 Current—S2	Full	VI	50	230	400	µA
Logic 0 Current—S2	Full	VI	–50	±0	50	µA
Logic 1 Current—DFS	Full	VI	30	100	200	µA
Logic 0 Current—DFS	Full	VI	–400	–230	–50	µA
Input Capacitance—S1, S2, Encode Inputs	25°C	V		2		pF
Input Capacitance DFS	25°C	V		4.5		pF
DIGITAL OUTPUTS						
Logic 1 Voltage	Full	VI	2.45			V
Logic 0 Voltage	Full	VI			0.05	V
Output Coding				Twos complement or offset binary		

AC SPECIFICATIONS

V_{DD} = 3.0 V, V_D = 3.0 V; external reference, unless otherwise noted.

Table 3.

Parameter	Temperature	Test Level	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE[1]						
Signal-to-Noise Ratio (SNR)						
(Without Harmonics)						
f_{IN} = 10 MHz	25°C	I	53	55		dB
f_{IN} = Nyquist[2]	25°C	I	52	54		dB
Signal-to-Noise and Distortion (SINAD)						
(With Harmonics)						
f_{IN} = 10 MHz	25°C	I	52	53		dB
f_{IN} = Nyquist[2]	25°C	I	51	53		dB
Effective Number of Bits						
f_{IN} = 10 MHz	25°C	I	8.4	8.6		Bits
f_{IN} = Nyquist[2]	25°C	I	8.3	8.6		Bits
Second Harmonic Distortion						
f_{IN} = 10 MHz	25°C	I	−60	−68		dBc
f_{IN} = Nyquist[2]	25°C	I	−57	−66		dBc
Third Harmonic Distortion						
f_{IN} = 10 MHz	25°C	I	−57	−63		dBc
f_{IN} = Nyquist[2]	25°C	I	−57	−69		dBc
Spurious Free Dynamic Range (SFDR)						
f_{IN} = 10 MHz	25°C	I	−57	−62		dBc
f_{IN} = Nyquist[2]	25°C	I	−57	−63		dBc
Two-Tone Intermodulation Distortion (IMD)						
f_{IN1} = 30 MHz, f_{IN2} = 31 MHz at −7 dBFS	25°C	V		−67		dBc
Analog Bandwidth, Full Power	25°C	V		300		MHz
Crosstalk	25°C	V		−75		dBc

[1] AC specifications based on an analog input voltage of −0.5 dBFS at 10.0 MHz, unless otherwise noted. AC specifications are tested in 1 V p-p range and driven differentially.
[2] Tested close to Nyquist: 51 MHz.

SWITCHING SPECIFICATIONS

V_{DD} = 3.0 V, V_D = 3.0 V; external reference, unless otherwise noted.

Table 4.

Parameter	Temperature	Test Level	Min	Typ	Max	Unit
ENCODE INPUT PARAMETERS						
Maximum Encode Rate	Full	VI	105			MSPS
Minimum Encode Rate	Full	IV			20	MSPS
Encode Pulse Width High (t_{EH})	Full	IV	3.8			ns
Encode Pulse Width Low (t_{EL})	Full	IV	3.8			ns
Aperture Delay (t_A)	25°C	V		2		ns
Aperture Uncertainty (Jitter)	25°C	V		3		ps rms
DIGITAL OUTPUT PARAMETERS						
Output Valid Time (t_V)[1]	Full	VI	2.5			ns
Output Propagation Delay (t_{PD})[1]	Full	VI		4.5	6	ns
Output Rise Time (t_R)	25°C	V		1.0		ns
Output Fall Time (t_F)	25°C	V		1.2		ns
Out-of-Range Recovery Time	25°C	V		5		ns
Transient Response Time	25°C	V		5		ns
Recovery Time from Power-Down	25°C	V		10		Cycles
Pipeline Delay	Full	IV		5		Cycles

[1] t_V and t_{PD} are measured from the 1.5 level of the ENC_x input to the 50%/50% levels of the digital outputs swing. The digital output load during test must not exceed an ac load of 5 pF or a dc current of ±40 µA. Rise and fall times are measured from 10% to 90%.

TIMING DIAGRAMS

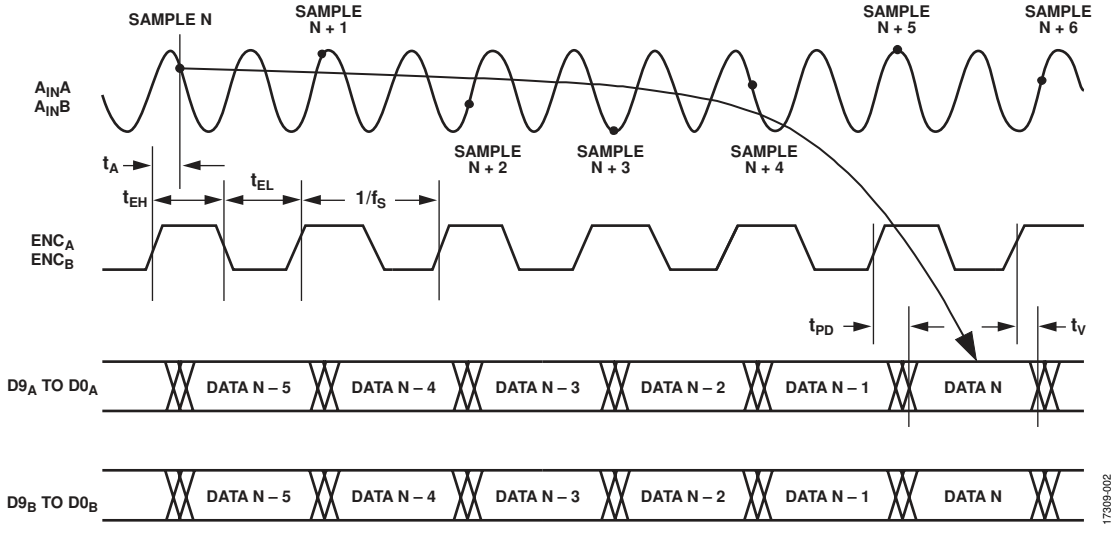


Figure 2. Normal Operation, Same Clock (S1 = 1, S2 = 0) Channel Timing

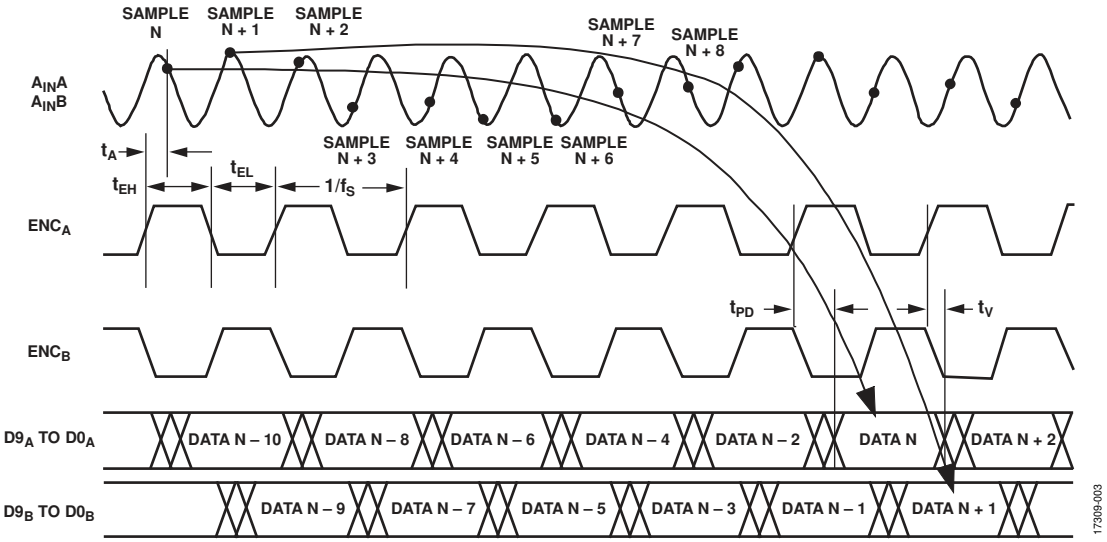


Figure 3. Normal Operation with Two Clock Sources (S1 = 1, S2 = 0) Channel Timing

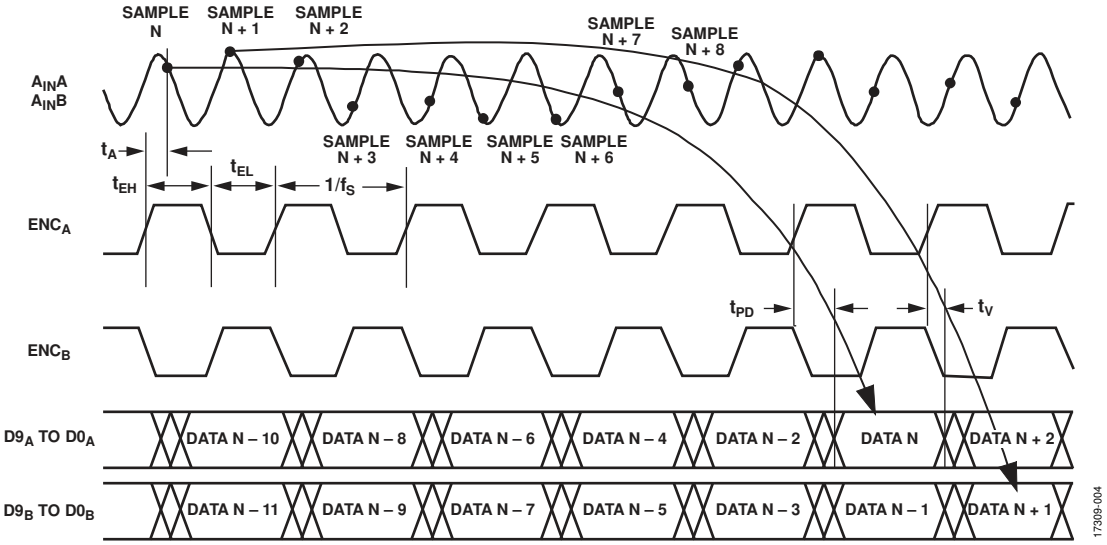


Figure 4. Data Align with Two Clock Sources (S1 = 1, S2 = 1) Channel Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_D, V_{DD}	4 V
Analog Inputs	−0.5 V to V_D + 0.5 V
Digital Inputs	−0.5 V to V_{DD} + 0.5 V
REF_{IN} Inputs	−0.5 V to V_D + 0.5 V
Digital Output Current	20 mA
Operating Temperature Range	−55°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Operating	115°C
Case Temperature	150°C
Operating	105°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

EXPLANATION OF TEST LEVELS

Test Level	Description
I	100% production tested.
II	100% production tested at 25°C and sample tested at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C; guaranteed by design and characterization testing for extended industrial temperature range.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
ST-48[1]	73	12	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board. See JEDEC JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

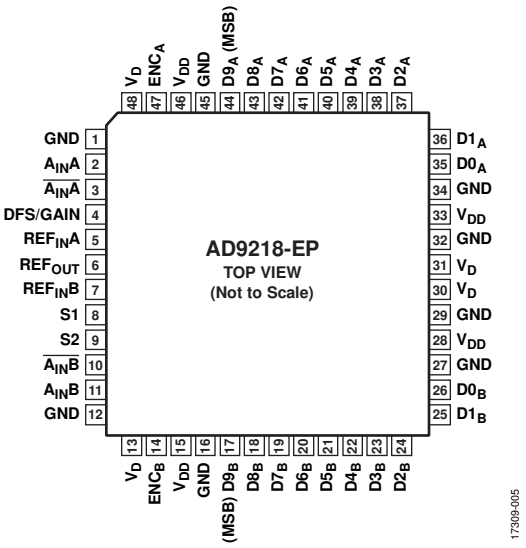


Figure 5. Pin Configuration

Table 7. Pin Function Descriptions

Pin Number	Mnemonic	Description
1, 12, 16, 27, 29, 32, 34, 45	GND	Ground.
2	$A_{IN}A$	Analog Input for Channel A.
3	$\overline{A_{IN}A}$	Analog Input for Channel A (Complementary).
4	DFS/GAIN	Data Format Select and Analog Input Gain Mode. Low = offset binary output available, 1 V p-p supported; high = twos complement output available, 1 V p-p supported.
5	$REF_{IN}A$	Reference Voltage Input for Channel A.
6	REF_{OUT}	Internal Reference Voltage.
7	$REF_{IN}B$	Reference Voltage Input for Channel B.
8	S1	User Select 1.
9	S2	User Select 2.
10	$\overline{A_{IN}B}$	Analog Input for Channel B (Complementary).
11	$A_{IN}B$	Analog Input for Channel B.
13, 30, 31, 48	V_D	Analog Supply.
14	ENC_B	Encode B. Clock input for Channel B.
15, 28, 33, 46	V_{DD}	Digital Supply.
17 to 26	$D9_B$ to $D0_B$	Digital Output for Channel B ($D9_B$ = MSB).
35 to 44	$D0_A$ to $D9_A$	Digital Output for Channel A ($D9_A$ = MSB).
47	ENC_A	Encode A. Clock input for Channel A.

TYPICAL PERFORMANCE CHARACTERISTICS

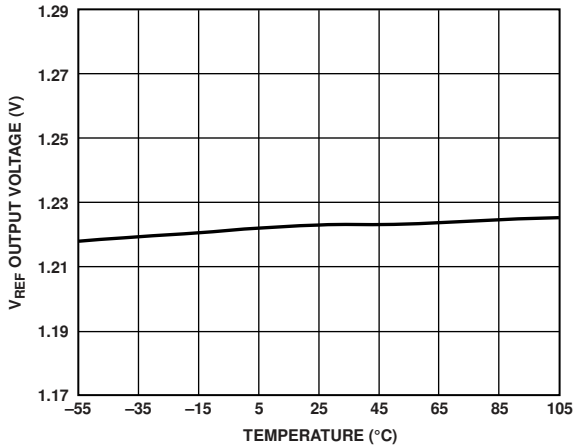


Figure 6. V_{REF} Output Voltage vs. Temperature (I_{LOAD} = 300 µA)

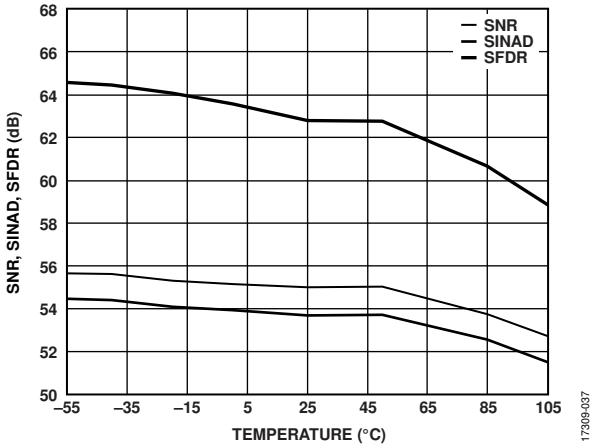


Figure 8. SNR, SINAD, SFDR vs. Temperature, A_{IN} = 10 MHz, 1 V p-p

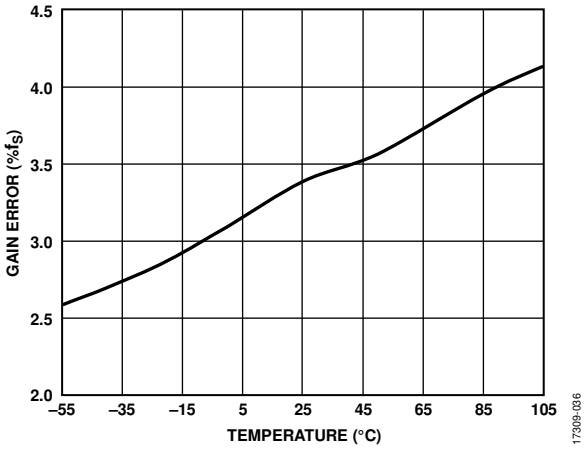
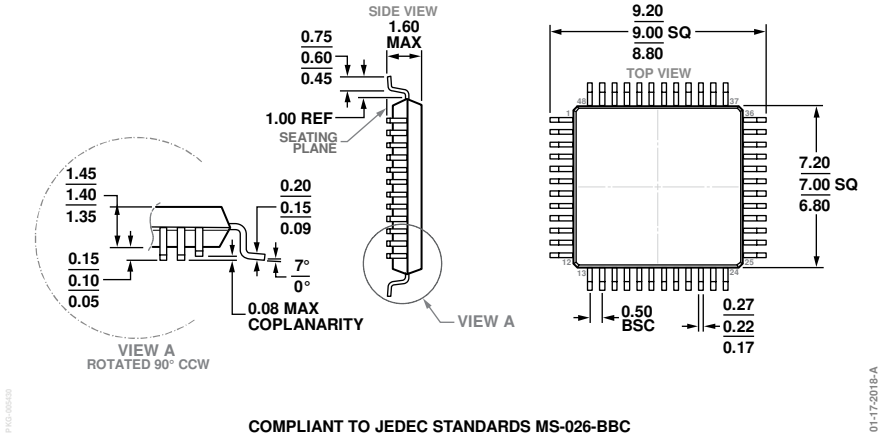


Figure 7. Gain Error vs. Temperature, A_{IN} = 10 MHz, 1 V p-p

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 9. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9218SSTZ-105-EP	−55°C to +105°C	48-Lead Low Profile Quad Flat Pack [LQFP]	ST-48
AD9218SSTZ-105EPRL	−55°C to +105°C	48-Lead Low Profile Quad Flat Pack [LQFP]	ST-48

[1] Z = RoHS Compliant Part.