# **4-Bit Bus Switch**

The ON Semiconductor 74FST3126 is a quad, high performance switch. The device is CMOS TTL compatible when operating between 4 and 5.5 Volts. The device exhibits extremely low  $R_{\rm ON}$  and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

The device consists of four independent 1-bit switches with separate Output/Enable (OE) pins. Port A is connected to Port B when OE is high. If OE is low, the switch is high Z.

## **Features**

- $R_{ON} < 4 \Omega$  Typical
- Less Than 0.25 ns-Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- Pin-For-Pin Compatible With QS3126, FST3126, CBT3126
- All Popular Packages: QSOP-16, TSSOP-14, SOIC-14
- All Devices in Package TSSOP are Inherently Pb-Free\*

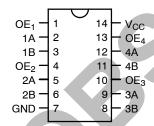


Figure 1. Pin Assignment for SOIC and TSSOP

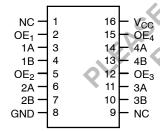
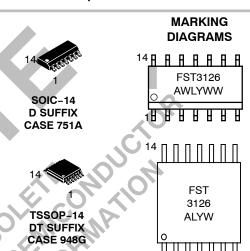


Figure 2. Pin Assignment for QSOP



# ON Semiconductor®

http://onsemi.com





QSOP-16 QS SUFFIX CASE 492

16	<u> </u>
	S3126 ALYW
	0
1	

Α	=	Assembly
Location		
L, WL	=	Wafer Lot
Υ	=	Year
W. WW	=	Work

# PIN NAMES Week

Pin	Description		
OE <sub>1</sub> , OE <sub>2</sub> , OE <sub>3</sub> , OE <sub>4</sub>	Bus Switch Enables		
1A, 2A, 3A, 4A	Bus A		
1B, 2B, 3B, 4B	Bus B		
NC	Not Connected		

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

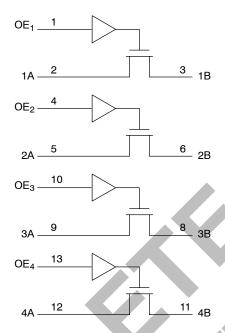


Figure 3. Logic Diagram

# TRUTH TABLE

Inputs	Outputs
OE	A, B
L L	S 05 11
Н	A = B

# **ORDERING INFORMATION**

Device Order Number	Package	Shipping <sup>†</sup>
74FST3126D	SOIC-14	55 Units / Rail
74FST3126DR2	SOIC-14	2500 Units / Tape & Reel
74FST3126DT	TSSOP* (Pb-Free)	96 Units / Rail
74FST3126DTR2	TSSOP* (Pb-Free)	2500 Units / Tape & Reel
74FST3126QS	QSOP-16	96 Units / Rail
74FST3126QSR	QSOP-16	2500 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
\*This package is inherently Pb-Free.

#### **MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
VI	DC Input Voltage	-0.5 to +7.0	V
Vo	DC Output Voltage	-0.5 to +7.0	V
I <sub>IK</sub>	DC Input Diode Current $V_{I} < GND$	-50	mA
lok	DC Output Diode Current V <sub>O</sub> < GND	-50	mA
Io	DC Output Sink Current	128	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	±100	mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±100	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C
$\theta_{\sf JA}$	Thermal Resistance (Note 1)  SOIC TSSOP QSOP	125 170 200	°C/W
MSL	Moisture Sensitivity	Level 1	
F <sub>R</sub>	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3)	>2000 >200	V
I <sub>Latchup</sub>	Latchup Performance Above V <sub>CC</sub> and Below GND at 85°C (Note 4)	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- newice reliability.

  1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.

  2. Tested to EIA/JESD22-A114-A.

  3. Tested to EIA/JESD22-A115-A.

  4. Tested to EIA/JESD78.

  RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage Operating, Data Retention Only	4.0	5.5	V
VI	Input Voltage (Note 5)	0	5.5	V
Vo	Output Voltage (HIGH or LOW State)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Free-Air Temperature	-40	+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate Switch Control Input Switch I/O	0 0	5 DC	ns/V

<sup>5.</sup> Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

## DC ELECTRICAL CHARACTERISTICS

			V <sub>cc</sub>	T <sub>A</sub> = -	40°C to	+85°C	
Symbol	Parameter	Conditions	(V)	Min	Тур*	Max	Unit
V <sub>IK</sub>	Clamp Diode Resistance	$I_{IN} = -18mA$	4.5			-1.2	V
V <sub>IH</sub>	High-Level Input Voltage		4.0 to 5.5	2.0			V
V <sub>IL</sub>	Low-Level Input Voltage		4.0 to 5.5			0.8	V
lį	Input Leakage Current	$0\leqV_{IN}\leq5.5V$	5.5			±1.0	μΑ
I <sub>OZ</sub>	OFF-STATE Leakage Current	$0 \le A, B \le V_{CC}$	5.5			±1.0	μΑ
R <sub>ON</sub>	Switch On Resistance (Note 6)	$V_{IN} = 0 \text{ V}, I_{IN} = 64 \text{ mA}$	4.5		4	7	Ω
		$V_{IN} = 0 \text{ V}, I_{IN} = 30 \text{ mA}$	4.5		4	7	
		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA	4.5		8	15	
		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA	4.0		11	20	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> = 0	5.5			3	μΑ
$\Delta I_{CC}$	Increase In I <sub>CC</sub> per Input	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5			2.5	mA

# **AC ELECTRICAL CHARACTERISTICS**

					Limit			
				V . U	$_{A} = -40^{\circ}C$	to +85°C		
			-62	V <sub>CC</sub> = 4.5	5 to 5.5 V	V <sub>CC</sub> =	4.0 V	
Symbol	Parameter	Conditions	Figures	Min	Max	Min	Max	Unit
t <sub>PHL</sub> , t <sub>PLH</sub>	Prop Delay Bus to Bus (Note 7)	V <sub>I</sub> = OPEN	4 and 5	RIF	0.25		0.25	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time	V <sub>I</sub> = 7 V for t <sub>PZL</sub> V <sub>I</sub> = OPEN for t <sub>PZH</sub>	4 and 5	1.0	4.5		5.0	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	V <sub>I</sub> = 7 V for t <sub>PLZ</sub> V <sub>I</sub> = OPEN for t <sub>PHZ</sub>	4 and 5	1.5	5.7		6.2	ns

<sup>7.</sup> This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

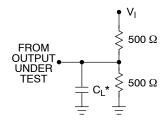
# **CAPACITANCE** (Note 8)

Symbol	Parameter	Conditions	Тур	Max	Unit
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> = 5.0 V	3		pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>CC</sub> = 5.0 V, OE = 0 V	5		pF

<sup>8.</sup>  $T_A = +25^{\circ}C$ , f = 1 MHz, Capacitance is characterized but not tested.

<sup>\*</sup>Typical values are at V<sub>CC</sub> = 5.0 V and T<sub>A</sub> = 25°C.
6. Measured by the voltage drop between A and B pins at the indicated current through the switch.

# **AC Loading and Waveforms**



#### NOTES:

- 1. Input driven by 50  $\Omega$  source terminated in 50  $\Omega.$
- 2. CL includes load and stray capacitance.

Figure 4. AC Test Circuit

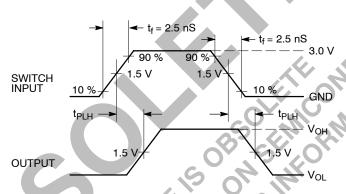


Figure 5. Propagation Delays

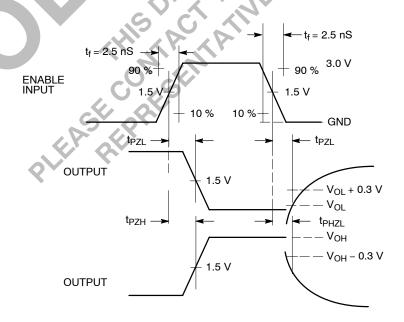
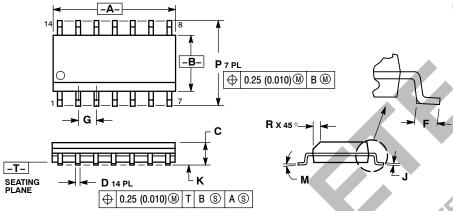


Figure 6. Enable/Disable Delays

 $<sup>*</sup>C_L = 50 pF$ 

#### PACKAGE DIMENSIONS

# SOIC-14 **D SUFFIX** CASE 751A-03 **ISSUE G**



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- ANGIT 14-5W, 1962.

  2. CONTROLLING DIMENSION: MILLIMETER.

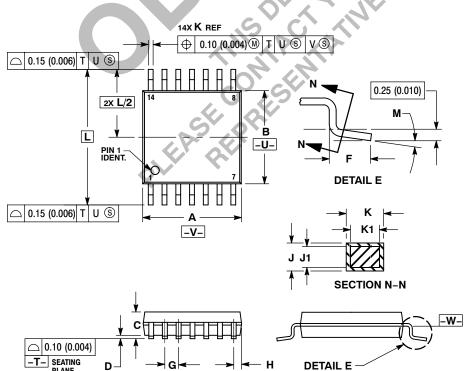
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- PER SIDE.
- PEH SIDE.

  5. DIMENSION D DOES NOT INCLUDE
  DAMBAR PROTRUSION. ALLOWABLE
  DAMBAR PROTRUSION SHALL BE 0.127
  (0.005) TOTAL IN EXCESS OF THE D
  DIMENSION AT MAXIMUM MATERIAL
  CANDITION. CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 0	7°	0 °	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019





# NOTES:

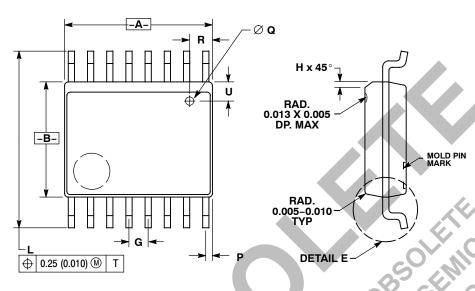
- DIMENSIONING AND TOLERANCING PER ANSI
  - Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE
- PEH SIDE.

  DIMENSION K DOES NOT INCLUDE DAMBAR
  PROTRUSION. ALLOWABLE DAMBAR
  PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN
  EXCESS OF THE K DIMENSION AT MAXIMUM
  MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES		
DIM	MIN	MAX	MIN	MAX		
Α	4.90	5.10	0.193	0.200		
В	4.30	4.50	0.169	0.177		
С		1.20		0.047		
D	0.05	0.15	0.002	0.006		
F	0.50	0.75	0.020	0.030		
G	0.65	BSC	0.026	BSC		
Н	0.50	0.60	0.020	0.024		
J	0.09	0.20	0.004	0.008		
J1	0.09	0.16	0.004	0.006		
K	0.19	0.30	0.007	0.012		
K1	0.19	0.25	0.007	0.010		
L	6.40	6.40 BSC		0.252 BSC		
M	0°	8°	0°	8°		

#### PACKAGE DIMENSIONS

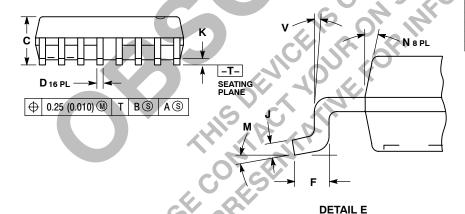
# QSOP-16 QS SUFFIX CASE 492-01 ISSUE O



#### NOTES

- DIMENSIONING AND TOLERANCING PER ANSI
   VALUE AND TOLERANCING PER ANSI
   VALU
  - Y14.5M, 1982.
    CONTROLLING DIMENSION: INCH.
- 3. THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
- PLASTIC DIMENSIONS DOES NOT INCLUDE
   MOLD FLASH OR PROTRUSIONS, MOLD FLASH
   OR PROTRUSIONS SHALL NOT EXCEED 6 MILS
   PER SIDE.
- 5. BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

	INCHES		MILLIMETERS	
DIM	MAX	MIN	MAX	MIN
Α	0.189	0.196	4.80	4.98
В	0.150	0.157	3.81	3.99
u	0.061	0.068	1.55	1.73
۴	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025 BSC		0.64 BSC	
H	0.008	0.018	0.20	0.46
5	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
M	0°	8°	0 °	8°
N	0°	7°	0°	7°
P	0.007	0.011	0.18	0.28
Q	0.020 DIA		0.51 DIA	
R	0.025	0.035	0.64	0.89
U	0.025	0.035	0.64	0.89
٧	0 °	8°	0°	8 °



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